VLSI

Interconnects

VLSI Interconnects

- Used to connect components on a VLSI chip
- Used to connect chips on a multichip module
- Used to connect multichip modules on a system board

Interconnection Technologies

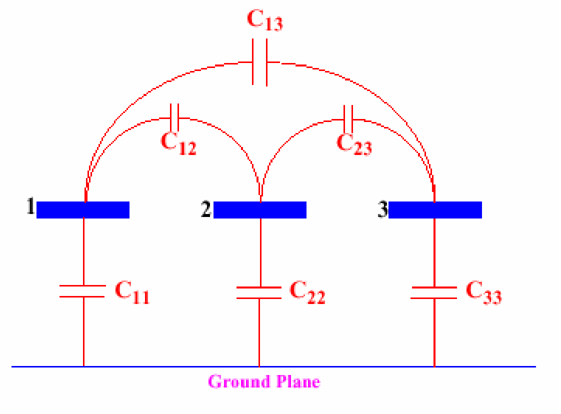
- Metallic Interconnects
- Optical Interconnects
- Superconducting Interconnects

Metallic Interconnections

Issues

- Parasitic Capacitances and Inductances
- Reduction of Propagation Delays
- Reduction of Crosstalk Effects
- Reduction of Electromigration-Induced Failure

Parasitic Capacitances



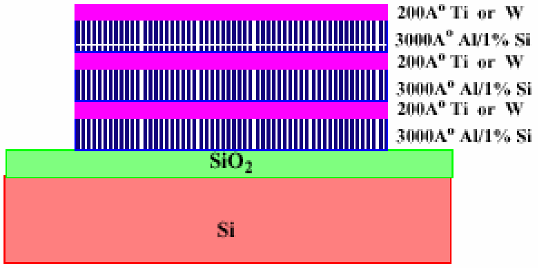
Parasitic Capacitances

An accurate modeling of the capacitances must include the contribution of the fringing fields as well as the shielding effects due to the presence of the neighboring conductors.

Multilevel and Multilayer Interconnections

- Level – Conductors separated by an insulator
- Layer - Different conductors tiered together in one level

Multilayer Interconnects



Reduction of electromigration is reported with layers of two or more metals in the same level of the interconnection.

Metallic Interconnections

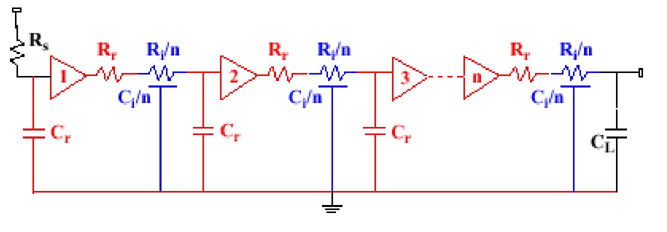
- Transistors can be scaled down in size such that the device delay decreases in direct proportion to the device dimensions.
- If the interconnections are scaled down, it results in RC delays that begin to dominate the chip performance.
- For the submicron-geometry chips, it is the interconnection delays rather than the device delays that determine the chip performance.

Active Interconnections

- New approaches are needed to lower the interconnection delays.
- One solution may be to replace the passive interconnections by the active interconnections by inserting inverters or repeaters at appropriate spacings.

Active Interconnections

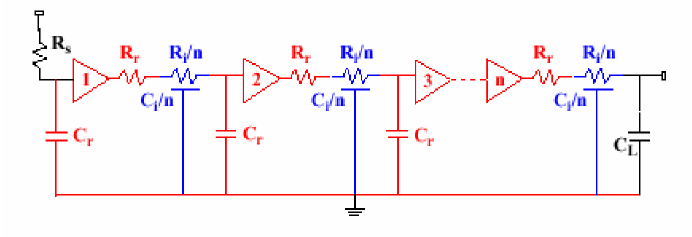
Driven by Minimum Size Inverters



- Ri = Total resistance of the interconnect line
- Ci = Total capacitance of the interconnect line
- Rr = Output resistance of the inverter
- Cr = Input capacitance of the inverter
- Rs = Resistance of the GaAs MESFET
- CL = Load capacitance
- n = Number of inverters

Active Interconnections

Driven by Minimum Size Inverters

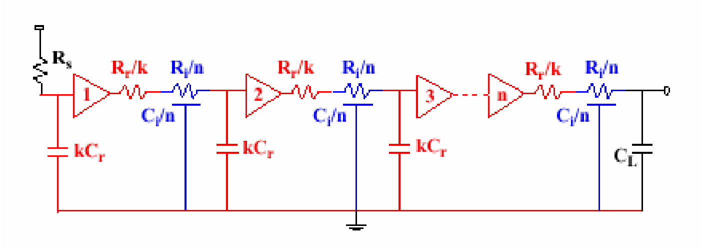


Optimum number of inverters is given by

$$n = \sqrt{\frac{R_i C_i}{2.3 R_r C_r}}$$

Active Interconnections

Driven by Optimum Size Inverters

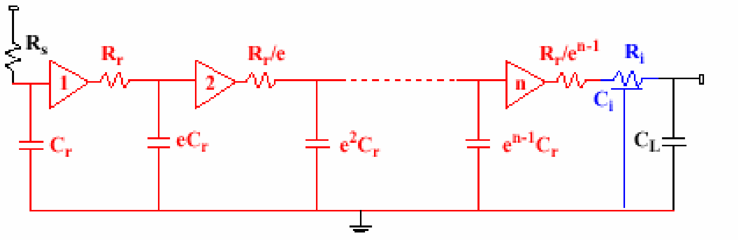


Propagation time can be improved by increasing the size of the inverters by a factor of k given by

$$k = \sqrt{\frac{R_r C_i}{R_i C_r}}$$

Active Interconnections

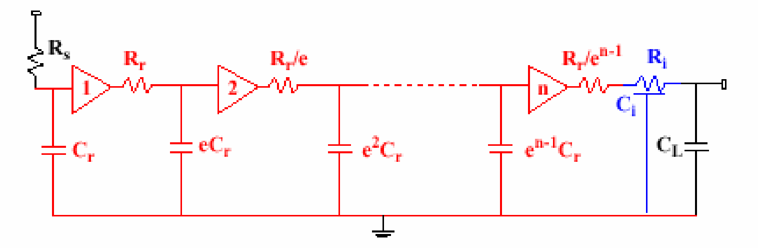
Driven by Cascaded Inverters



The optimal delay is obtained by using a sequence of n inverters that increase gradually in size, each by a factor of e = 2.71828 over the previous one.

Active Interconnections

Driven by Cascaded Inverters



Optimum value of n is given by

$$n = \ln\left[\frac{C_i}{C_r}\right]$$

Active Interconnections

Propagation Time vs. Driving Mechanism for Several Interconnection Lengths

Interconnection Material: Aluminum ($\rho = 3\ \mu\Omega \cdot \text{cm}$)

(Interconnection Width = Interconnection Separation = 1 μm; Load = 100 fF; Source Resistance = 700 Ω)

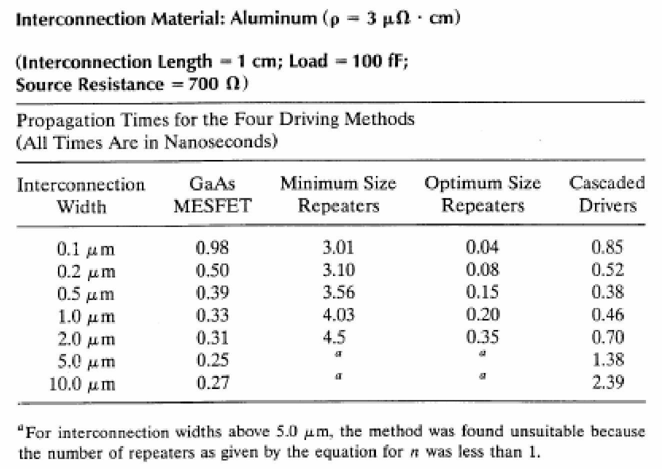
Propagation Times for the Four Driving Methods
(All Times Are in Nanoseconds)

Interconnection Length	GaAs MESFET	Minimum Size Repeaters	Optimum Size Repeaters	Cascaded Drivers
1 mm	0.05	[a]	[a]	0.24
2 mm	0.08	[a]	[a]	0.27
5 mm	0.17	2.31	0.11	0.34
1 cm	0.33	4.16	0.20	0.46
2 cm	0.80	7.87	0.29	0.76
5 cm	3.5	18.98	0.54	2.79
10 cm	15.1	37.51	0.97	11.49

[a] For interconnection lengths below 2 mm, the method was found unsuitable because the number of repeaters as given by the equation for *n* was less than 1.

Active Interconnections

Propagation Time vs. Driving Mechanism for Several Interconnection Widths



Interconnection Material: Aluminum ($\rho = 3\ \mu\Omega \cdot \text{cm}$)

(Interconnection Length = 1 cm; Load = 100 fF; Source Resistance = 700 Ω)

Propagation Times for the Four Driving Methods
(All Times Are in Nanoseconds)

Interconnection Width	GaAs MESFET	Minimum Size Repeaters	Optimum Size Repeaters	Cascaded Drivers
0.1 μm	0.98	3.01	0.04	0.85
0.2 μm	0.50	3.10	0.08	0.52
0.5 μm	0.39	3.56	0.15	0.38
1.0 μm	0.33	4.03	0.20	0.46
2.0 μm	0.31	4.5	0.35	0.70
5.0 μm	0.25	[a]	[a]	1.38
10.0 μm	0.27	[a]	[a]	2.39

[a] For interconnection widths above 5.0 μm, the method was found unsuitable because the number of repeaters as given by the equation for n was less than 1.

Superconducting Interconnects

The advent of high-critical-temperature superconductors has opened up the possibility of realizing high-density and very fast superconducting interconnections on the Silicon as well as GaAs-based ICs.

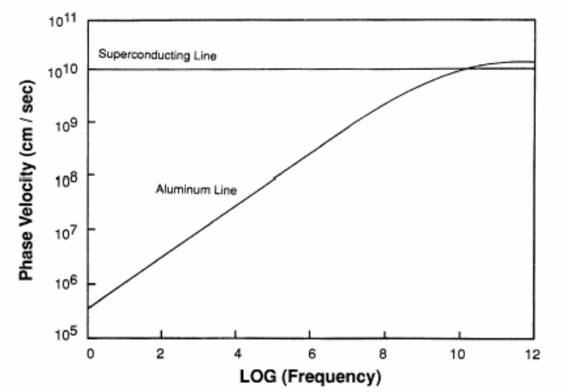
Superconducting Interconnects

Advantages

- Propagation time is much smaller as compared to that on a normal metal interconnection.
- There is virtually no signal dispersion for frequencies up to several tens of gigahertz.

Superconducting Interconnects

Comparison with Normal Metal Interconnects

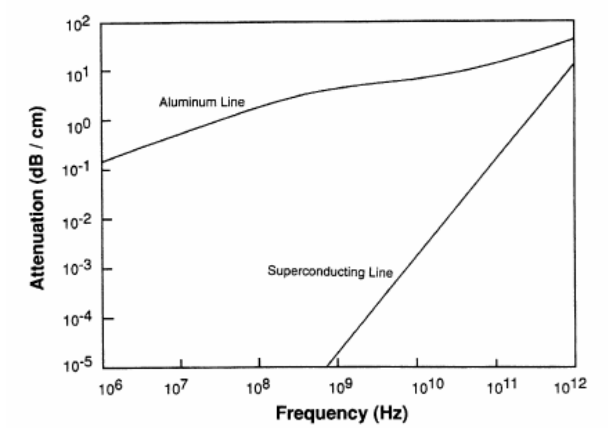


Phase velocities for superconducting and normal Al lines at 77°K

$(W = 2\mu m, t_c = 0.5\mu m, t_d = 1\mu m, t_g = 1\mu m)$

Superconducting Interconnects

Comparison with Normal Metal Interconnects



Attenuations for superconducting and normal Aluminum lines at 77° K

$(W = 2\mu m, t_c = 0.5\mu m, t_d = 1\mu m, t_g = 1\mu m)$

Optical Interconnections

- As an alternative to electrical interconnections, optical interconnections have emerged which offer fast, reliable and noise-free data transmission.
- So far, they have been used for computer-to-computer communications and processor-to-processor interconnects.
- Their applicability at lower levels of the packaging hierarchy such as for module-to-module connections at the board level, for chip-to-chip connections at the module level and for gate-to-gate connections at the chip level is under investigation.

Optical Interconnects

Advantages

- Free from any capacitive loading effects.
- Do not suffer from crosstalk.
- Speed of propagation of a signal determined by the speed of light and the refractive index of the optical transmission medium only.
- Do not suffer from electromigration-induced failure.

Optical Interconnects

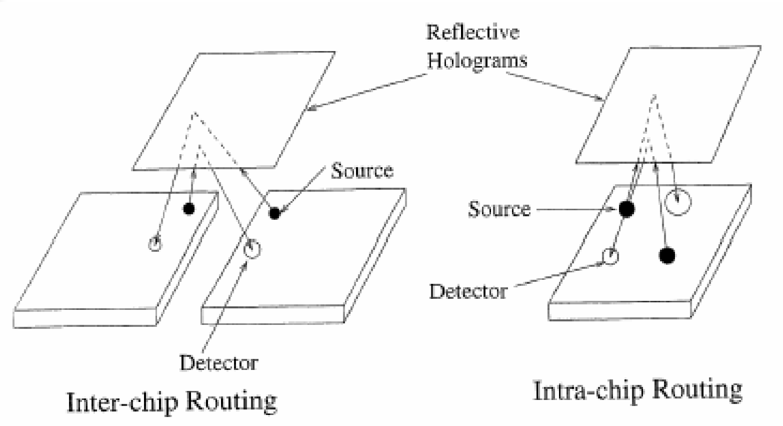
More Advantages

- Metallic interconnections have a limitation on the number of pinouts available on a chip.
- Optical chip-to-chip interconnections can be anchored directly to the interior of a chip rather than to a pin on its perimeter.
- Chip-to-chip optical interconnections operate at much higher speeds allowing the multiplexing of a large number of I/O signals in a single I/O fiber.

Optical Interconnects
Configurations

- Thin-Film Waveguides
- Optical Fibers
- Free-Space or Holographic

Optical Interconnects
Free-Space Configurations



Propagation Delays

Definitions

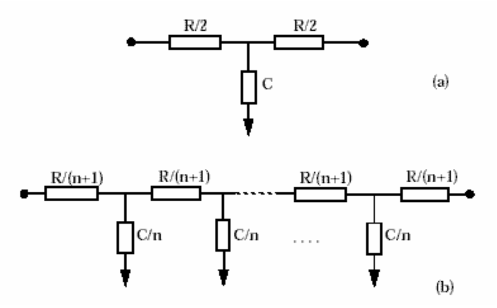
- Delay Time

  Time required by the output signal (current or voltage) to reach 50% of its steady state value
- Rise Time

  Time required by the output signal to rise from 10% to 90% of its steady state value
- Propagation Time

  Time required by the output signal to reach 90% of its steady state value

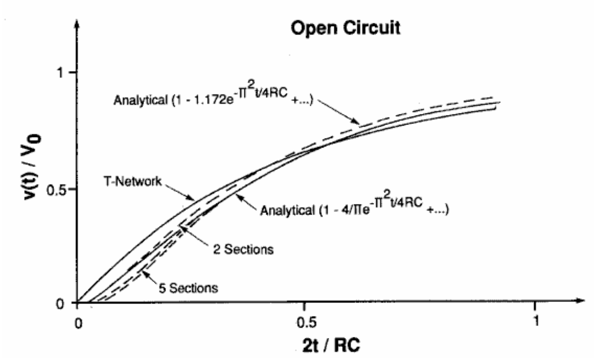
A Resistive Interconnection as a Ladder Network



- T-network of a resistive interconnection (fig. a) can be modeled as an n-stage ladder RC network (fig. b) under open circuit, short circuit as well as capacitive loading conditions.

A Resistive Interconnect as a Ladder Network

Open Circuit Interconnection



Comparison of output voltage versus time for an open circuited interconnection obtained by using the equation, obtained by a numerical simulation of the T-network and those obtained by numerical simulations of the ladder network with different number of stages.

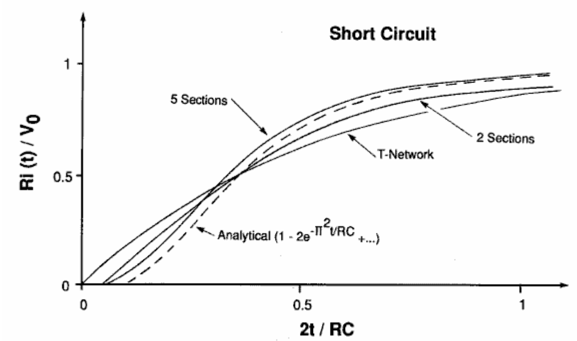
A Resistive Interconnect as a Ladder Network

Capacitively Loaded Interconnection

- An interconnection line loaded with a capacitance C_L
- For a wide range of C_L/C values, a five-stage ladder network yields sufficient accuracy.

A Resistive Interconnect as a Ladder Network

Short Circuited Interconnection



Comparison of the plots of the output current versus time for a short circuited interconnection obtained by using the above equation, obtained by a numerical simulation of the T-network and those obtained by numerical simulations of the ladder network with different number of stages.

Interconnect Parameters

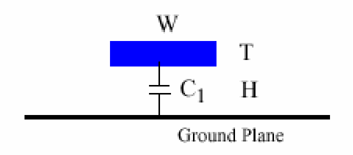
- Parameters of an electrical interconnection: series resistance, capacitance and inductance
- Series resistance can be rather easily determined by the interconnection material and dimensions
- Parasitic capacitances and inductances associated with the interconnections in the high density environment of the integrated circuit have become the primary factors in the evolution of the very high speed integrated circuit technology
- An accurate modeling of the capacitances must include the contribution of the fringing fields as well as the shielding effects due to the presence of the neighboring conductors

Approximate Capacitance Formulas

- For accurately determining the interconnection capacitances on the VLSI circuits, two- and three-dimensional effects must be taken into account.
- However, this requires rigorous numerical analysis which can be too time consuming.
- Approximate formulas to estimate the interconnect capacitances are sometimes desirable.
- A few empirical formulas are suggested by Sakurai and Tamaru for a few interconnection structures.

Approximate Capacitance Formulas

Single Line on a Ground Plane



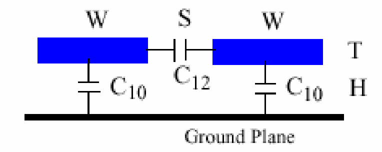
- The capacitance C1 per unit length can be estimated from the approximate formula:

$$C_1 = \varepsilon_{ox}\left[1.15\left(\frac{W}{H}\right) + 2.80\left(\frac{T}{H}\right)^{0.222}\right]$$

- ε_{ox} is the dielectric constant of the insulator such as SiO_2 for which $\varepsilon_{ox} = 3.9 \times 8.855 \times 10^{-14}$ F/cm.
- The relative error of the formula is within 6% for $0.3<(W/H)<30$ and $0.3<(T/H)<30$.

Approximate Capacitance Formulas

Two Lines on a Ground Plane



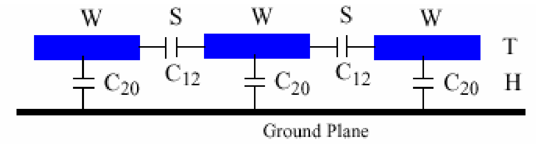
- The total capacitance C_2 of each line per unit length includes the ground capacitance C_{10} and the coupling capacitance C_{12} between the lines, i.e., $C_2 = C_{10} + C_{12}$

$$C_2 = C_1 + \varepsilon_{ox}\left[0.03\frac{W}{H} + 0.83\frac{T}{H} - 0.07\left(\frac{T}{H}\right)^{0.222}\right]\left(\frac{S}{H}\right)^{-1.34}$$

- The relative error of the formula is less than 10% for 0.3<(W/H)<10, 0.3<(T/H)<10 and 0.5<(S/H)<10

Approximate Capacitance Formulas

Three Lines on a Ground Plane



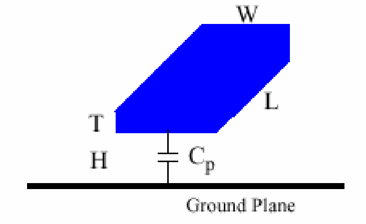
- The total capacitance of each line includes the ground capacitance C_{20} and the coupling capacitance C_{12} between the lines. For example, the total capacitance C_3 of the middle line per unit length is equal to $C_{20} + 2C_{12}$

$$C_3 = C_1 + 2\varepsilon_{ox}\left[0.03\frac{W}{H} + 0.83\frac{T}{H} - 0.07\left(\frac{T}{H}\right)^{0.222}\right]\left(\frac{S}{H}\right)^{-1.34}$$

- The relative error of the formula is less than 10% for 0.3<(W/H)<10, 0.3<(T/H)<10 and 0.5<(S/H)<10

Approximate Capacitance Formulas

Single Plate with Finite Dimensions on a Ground Plane



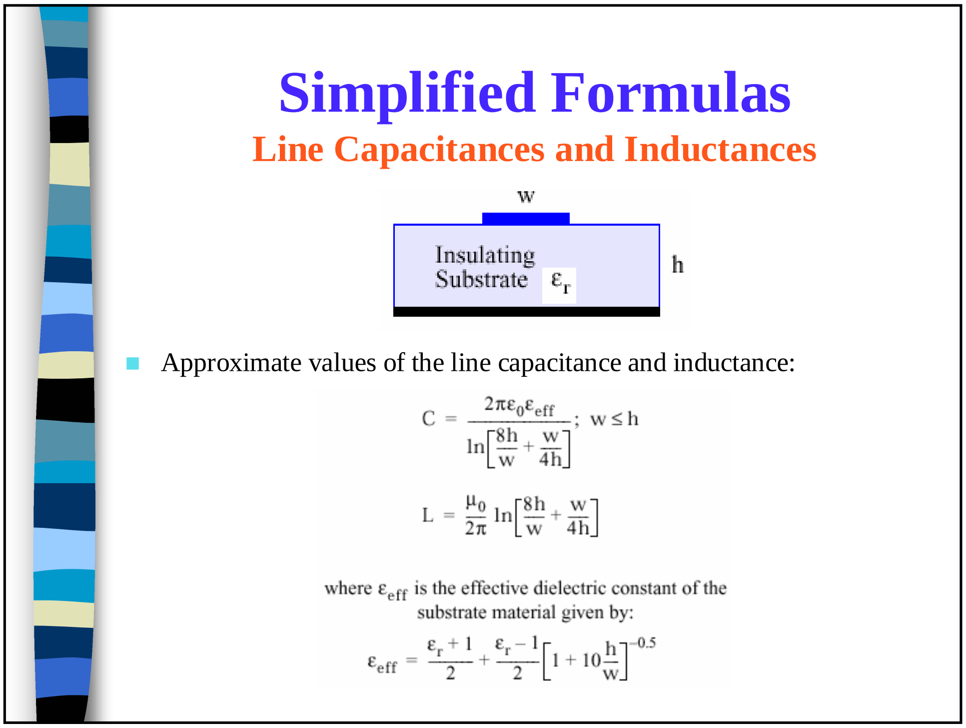
- The capacitance Cp between the plate and the ground includes the three-dimensional effects.

$$C_p = \varepsilon_{ox}\left[1.15\frac{LW}{H} + 2.8(L+W)\left(\frac{T}{H}\right)^{0.222} + 4.12H\left(\frac{T}{H}\right)^{0.728}\right]$$

- The relative error of the formula is within 10% for 0<(W/L)<1, 0.5<(W/H)<40 and 0.4<(T/H)<10

Simplified Formulas for Interconnect Capacitances and Inductances on Silicon and GaAs Substrates

- Insulating substrates such as Cr-doped GaAs have emerged as alternatives to silicon.
- This is partially because the interconnections fabricated on these substrates offer considerably lower capacitances than those fabricated on silicon.
- A few simplified formulas for the capacitances and inductances for interconnections fabricated on these substrates are available in the literature.



Simplified Formulas

Line Capacitances and Inductances

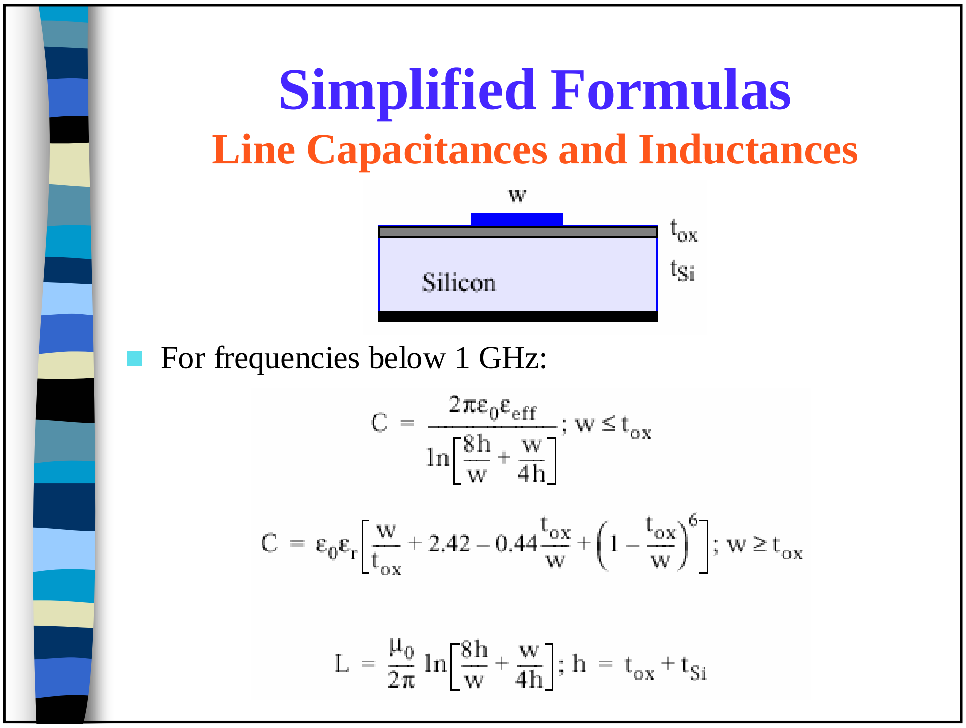
- Approximate values of the line capacitance and inductance:

$$C = \frac{2\pi\varepsilon_0\varepsilon_{eff}}{\ln\left[\frac{8h}{w} + \frac{w}{4h}\right]};\ w \le h$$

$$L = \frac{\mu_0}{2\pi}\ln\left[\frac{8h}{w} + \frac{w}{4h}\right]$$

where ε_{eff} is the effective dielectric constant of the substrate material given by:

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left[1 + 10\frac{h}{w}\right]^{-0.5}$$



Simplified Formulas

Line Capacitances and Inductances

- For frequencies below 1 GHz:

$$C = \frac{2\pi\varepsilon_0\varepsilon_{eff}}{\ln\left[\frac{8h}{w} + \frac{w}{4h}\right]};\ w \le t_{ox}$$

$$C = \varepsilon_0\varepsilon_r\left[\frac{w}{t_{ox}} + 2.42 - 0.44\frac{t_{ox}}{w} + \left(1 - \frac{t_{ox}}{w}\right)^6\right];\ w \ge t_{ox}$$

$$L = \frac{\mu_0}{2\pi}\ln\left[\frac{8h}{w} + \frac{w}{4h}\right];\ h = t_{ox} + t_{Si}$$

Simplified Formulas

Self and Coupling Capacitances

- The Maxwellian capacitance matrix for an array of n conductors referring to a common ground plane:

$$\begin{bmatrix} C_{11} & C_{12} & \cdots & C_{1n} \\ C_{21} & C_{22} & \cdots & C_{2n} \\ \cdots & \cdots & \cdots & \cdots \\ C_{n1} & C_{n2} & \cdots & C_{nn} \end{bmatrix}$$

- Diagonal element C_{ii} is the self capacitance of conductor i. It is a measure of the capacitance of a single conductor when all other conductors are grounded.
- Diagonal element C_{ij} is a measure of the negative of mutual capacitance between conductors i and j.

Simplified Formulas

Maxwellian Capacitance Matrix

- For a system of five conductors on oxide passivated Si with equal line widths equal to 1 micron each and equal separations equal to 1 micron each:

Substrate: 1-μm SiO_2 on Si

$$C_{ij} = \begin{bmatrix} 0.776 & -0.043 & -0.004 & -0.002 & 0 \\ -0.044 & 0.760 & -0.045 & -0.004 & -0.001 \\ -0.004 & -0.045 & 0.759 & -0.045 & -0.004 \\ -0.001 & -0.004 & -0.045 & 0.760 & -0.044 \\ 0 & -0.002 & -0.004 & -0.044 & 0.766 \end{bmatrix} \text{pF/cm}$$

Simplified Formulas

Maxwellian Capacitance Matrix

- For a system of five conductors on GaAs with equal line widths equal to 1 micron each and equal separations equal to 1 micron each:

Substrate: GaAs

$$C_{ij} = \begin{bmatrix} 1.066 & -0.520 & -0.154 & -0.092 & -0.094 \\ -0.520 & 1.315 & -0.454 & -0.124 & -0.091 \\ -0.155 & -0.454 & 1.329 & -0.454 & -0.155 \\ -0.091 & -0.124 & -0.454 & 1.315 & -0.520 \\ -0.094 & -0.092 & -0.155 & -0.520 & 1.066 \end{bmatrix} \text{ pF/cm}$$

Simplified Formulas

Inductance Matrix

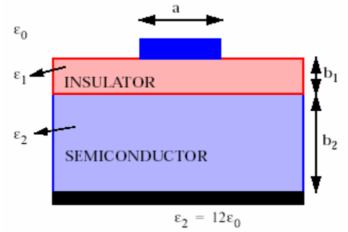
- For a system of five conductors with equal line widths of 1 micron each and equal separations of 1 micron each fabricated on either oxide-passivated silicon or GaAs substrates:

$$L_{ij} = \begin{bmatrix} 15.126 & 10.597 & 9.235 & 8.429 & 7.859 \\ 10.597 & 15.086 & 10.579 & 9.227 & 8.429 \\ 9.235 & 10.579 & 15.080 & 10.579 & 9.235 \\ 8.429 & 9.227 & 10.579 & 15.086 & 10.597 \\ 7.859 & 8.429 & 9.235 & 10.597 & 15.115 \end{bmatrix} \text{ nH/cm}$$

Interconnect Delays

- High-speed silicon and GaAs technologies have achieved propagation delays of less than 10 ps per gate.
- High electron mobility transistors (HEMTs) and modulation-doped field effect transistors (MODFETs) have switching speeds of less than 5 ps.
- Propagation delays and crosstalk noise associated with the signal transmissions on the interconnects have become the primary factors in limiting the circuit speed.
- In most cases, the interconnection delays on an IC chip account for more than 50% of the total delays.
- Comprehensive understanding of the dependence of the interconnection delays on the various interconnect parameters is urgently needed for optimum chip design.

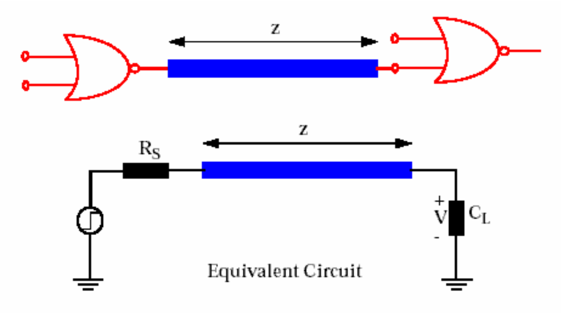
MIS Microstrip Line Model of an Interconnect



- Consider a very high speed IC chip by using a metal-insulator-semiconductor (MIS) microstrip line model for the interconnection.
- Microstrip line is formed on a surface passivated semiconductor substrate which in turn is placed on a metallized back.

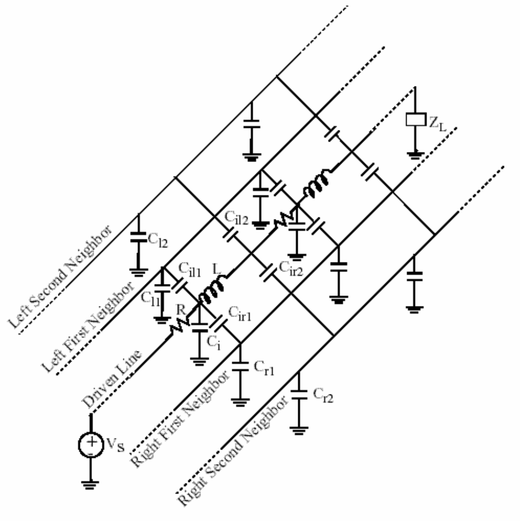
MIS Microstrip Line Model

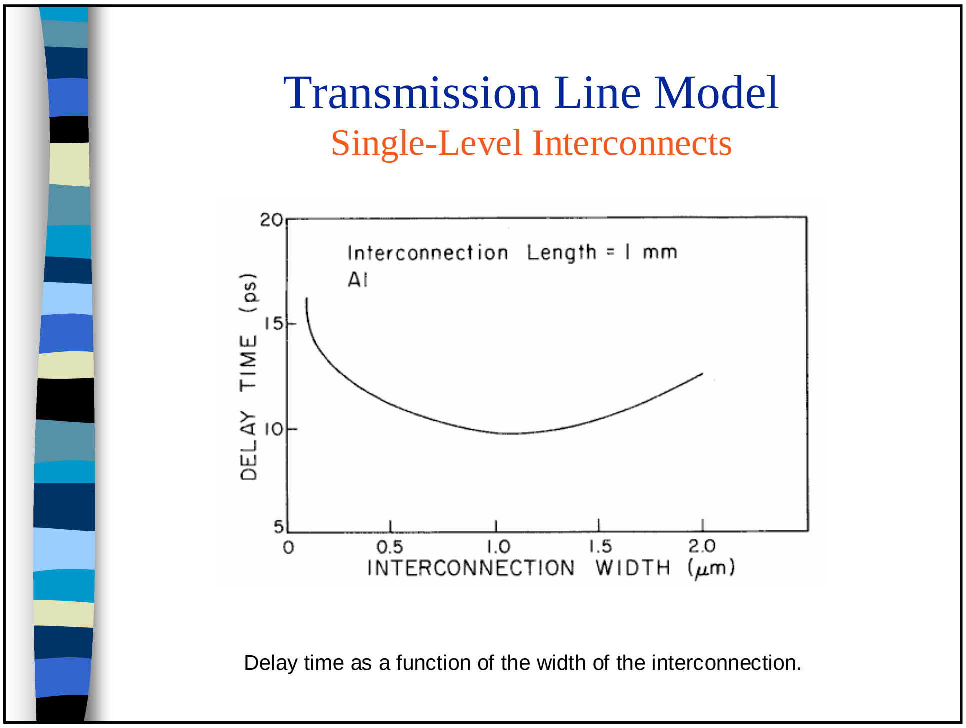
Interconnects Between Logic Gates



Transmission Line Model

Single-Level Interconnections

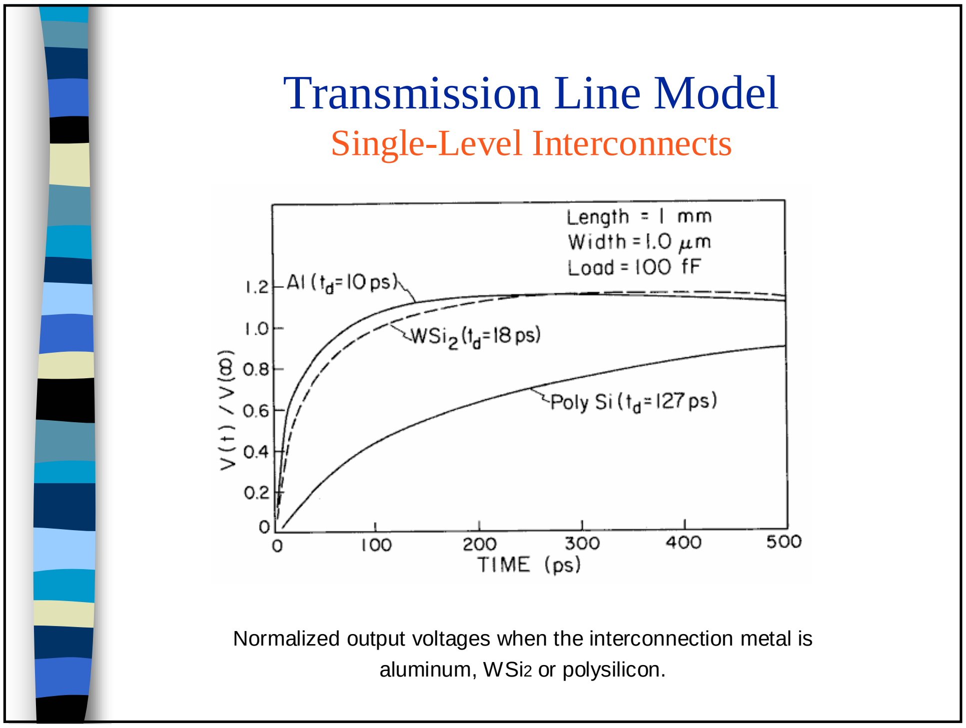




Transmission Line Model

Single-Level Interconnects

Delay time as a function of the width of the interconnection.



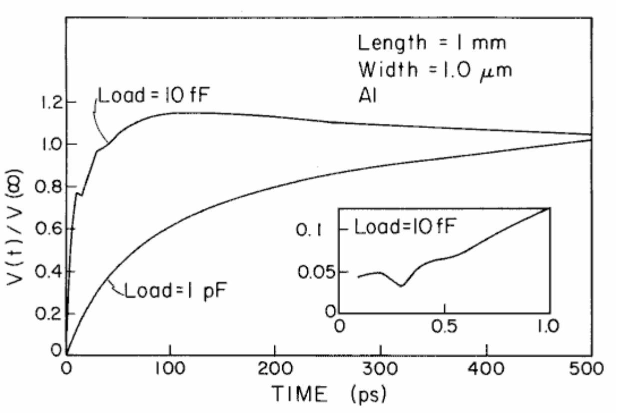
Transmission Line Model

Single-Level Interconnects

Normalized output voltages when the interconnection metal is aluminum, WSi_2 or polysilicon.

Transmission Line Model

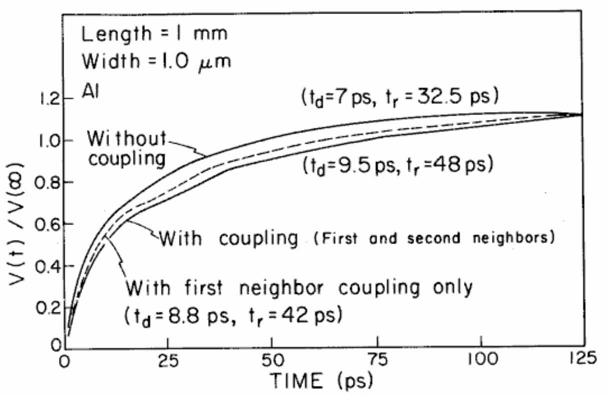
Single-Level Interconnects



Normalized output voltages for the load capacitances of 10 fF and 1 pF.

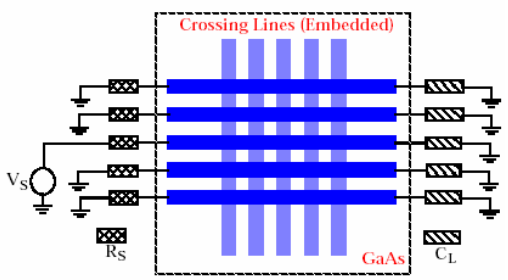
Transmission Line Model

Single-Level Interconnects



Effect of the coupling of the interconnection with the neighboring lines.

Crossing Interconnects



The interconnection lines which run parallel to each other can be studied by using the transmission line equations.

When the interconnections cross each other, the transmission line approximation is no longer valid because, in this case, the coupling of the lines is no longer uniform along the entire length of the interconnection but is rather localized to the crossing areas.

Crossing Interconnections

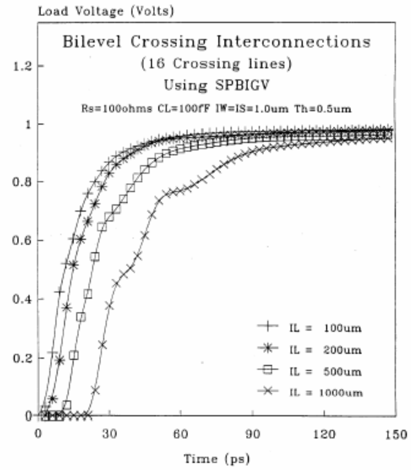
Simulation Results Using “SPBIGV”

One parameter is varied while the others are kept at:

Lengths = 100 µm
Widths = 1 µm
Thickness = 0.5 µm
Separations = 1 µm
Resistivity = 3 µΩ cm for Aluminum
Interlevel distance = 2 µm
Substrate thickness = 200 µm
R_S = 100 Ω
C_L = 100 fF
n=16

Crossing Interconnections

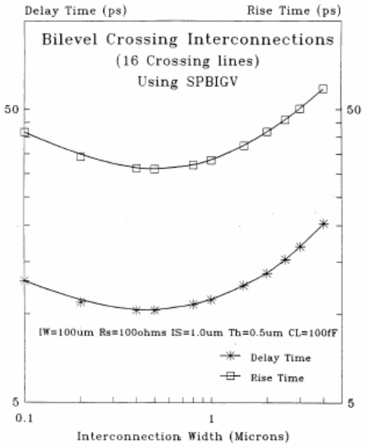
Simulation Results Using “SPBIGV”



Load voltage waveforms for several values of the interconnect lengths in the time range 0-150 ps.

Crossing Interconnections

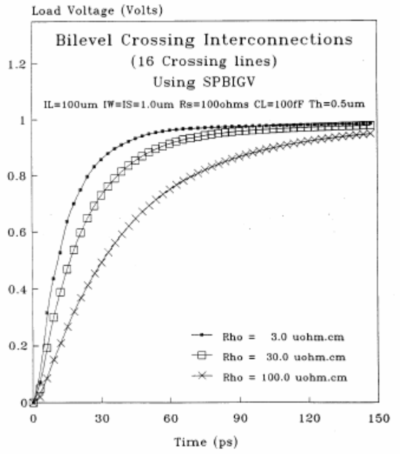
Simulation Results Using “SPBIGV”



Dependences of the delay time and rise time on the interconnection widths in the range 0.1-4 µm.

Crossing Interconnections

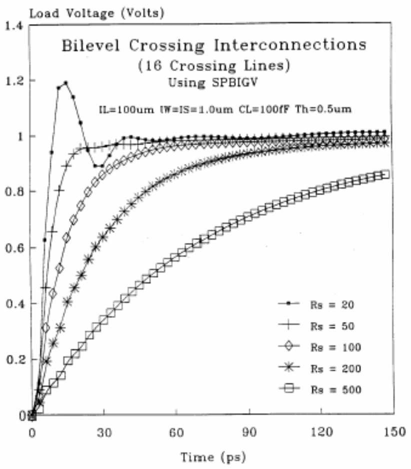
Simulation Results Using “SPBIGV”



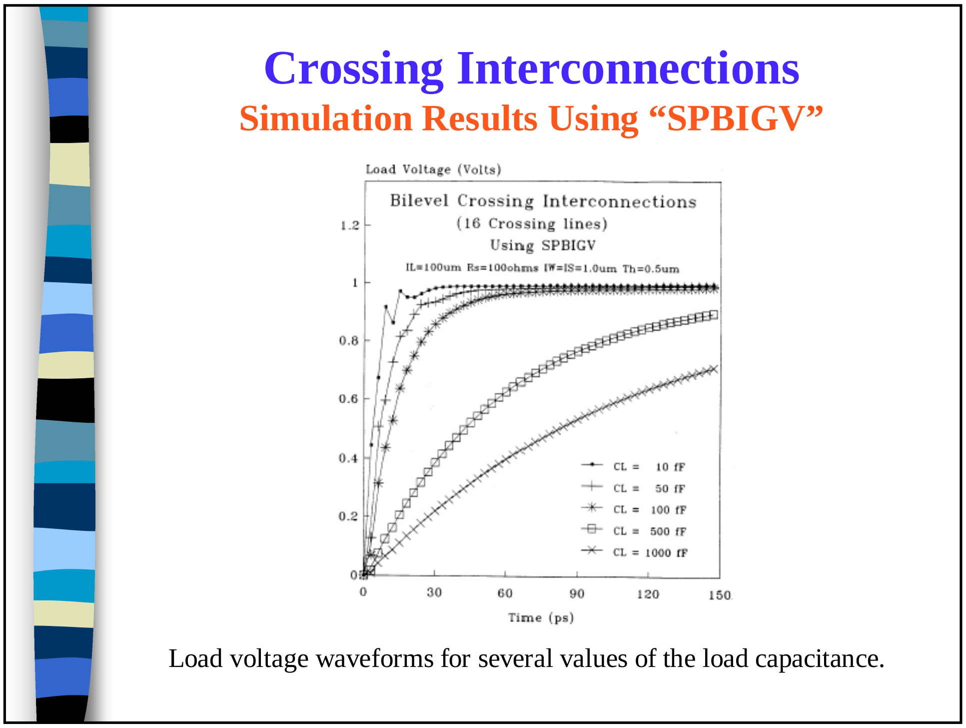
Load voltage waveforms for several values of the interconnect material resistivity in the range 0-150 ps..

Crossing Interconnections

Simulation Results Using “SPBIGV”



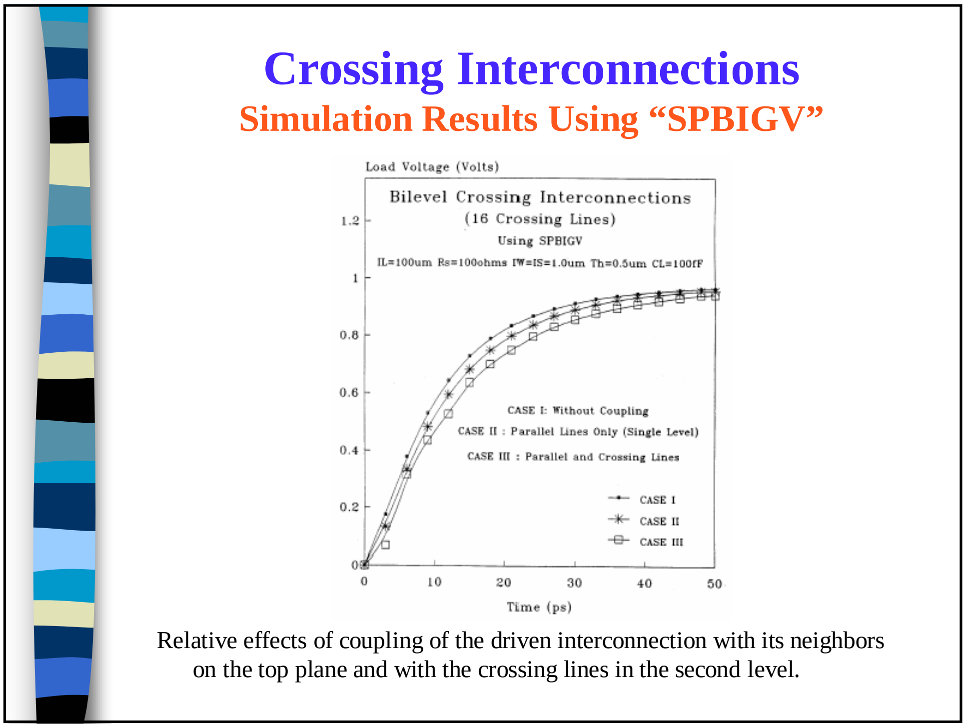
Load voltage waveforms for several values of source resistance.



Crossing Interconnections

Simulation Results Using “SPBIGV”

Load voltage waveforms for several values of the load capacitance.



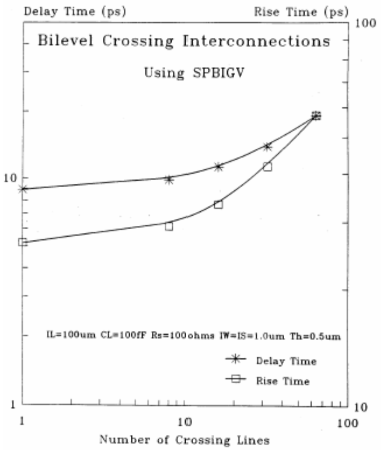
Crossing Interconnections

Simulation Results Using “SPBIGV”

Relative effects of coupling of the driven interconnection with its neighbors on the top plane and with the crossing lines in the second level.

Crossing Interconnections

Simulation Results Using “SPBIGV”



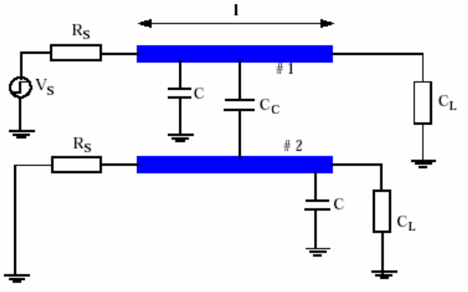
Dependences of the delay time and the rise time on the number of crossing lines in the range 1-80.

Crosstalk

- Crosstalk means the signal induced in the neighboring interconnects because of coupling capacitances and inductances.
- The crosstalk among the interconnections in single as well as multilevel configurations has become a major problem in the development of the next-generation high-speed integrated circuits.
- It is important to find methods of reducing this crosstalk.

Crosstalk Analysis

Lumped Capacitance Approximation



In the lumped capacitance model of two interconnects coupled by the capacitance C_c shown above, crosstalk voltage is defined as the voltage $V_2(t)$ induced across the load C_L on the second interconnection.

Crosstalk Analysis

Lumped Capacitance Approximation

- Amplitude of the crosstalk voltage at time t is given by:

$$V_2(t) = \frac{1}{2}\left[e^{-\left(\frac{t}{\tau_1}\right)} - e^{-\left(\frac{t}{\tau_2}\right)}\right]$$

$$\tau_1 = R(C + C_L)$$

$$\tau_2 = R(2C_c + C + C_L)$$

Crosstalk Analysis

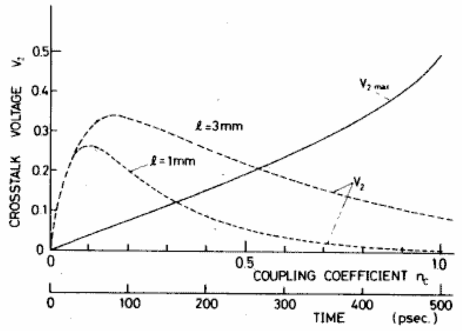
Lumped Capacitance Approximation

Maximum value of the crosstalk voltage is given by:

$$V_{2,\,\max} = \frac{1}{2}\left[e^{\left(\frac{(n_c - 1)}{2n_c}\right)\ln\left(\frac{1+n_c}{1-n_c}\right)} - e^{\left(-\frac{(n_c + 1)}{2n_c}\right)\ln\left(\frac{1+n_c}{1-n_c}\right)} \right]$$

$$n_c = \frac{C_c}{C + C_c + C_L}$$

Lumped Capacitance Approximation



Dependences of the crosstalk voltage V2 on time in the range 0-500 ps for interconnections of widths and separation equal to 2 µm, and lengths of 1 mm and 3 mm.

This figure also shows the dependence of the maximum crosstalk voltage on the coupling coefficient nc in the range 0-1.

Lumped Capacitance Approximation

It can be shown that the "lumped capacitance" approximation is applicable to interconnections which are at least a few millimeters long

and

The circuit rise time is above 200-300 ps

and

That it becomes inadequate in high-speed circuits.

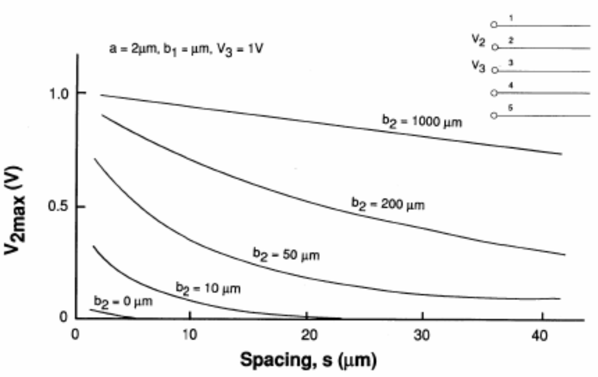
Coupled Multiconductor MIS Model

Crosstalk Reduction

For reliable operation of very high-speed very large scale integrated circuits with sufficient noise margins, it is very important to consider methods of reducing crosstalk.

Coupled Multiconductor MIS Model

Numerical Simulations



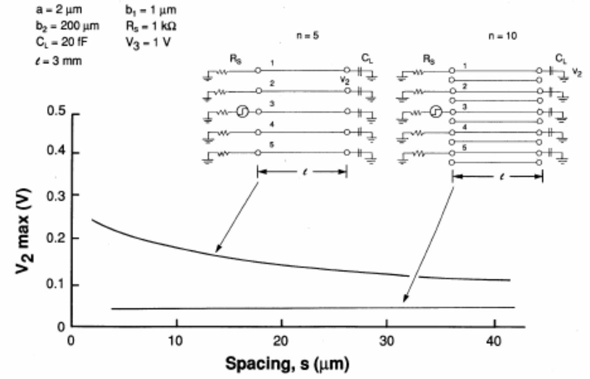
Dependence of the crosstalk coupling coefficient on spacing for several values of the substrate thickness.

One method of reducing crosstalk is to reduce the substrate thickness.

However, this method will be effective only if the substrate thickness is reduced below 10 µm.

Coupled Multiconductor MIS Model

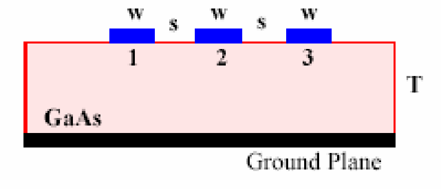
Numerical Simulations



Crosstalk voltages for two systems of five interconnections with and without the shielding ground lines between the interconnects.

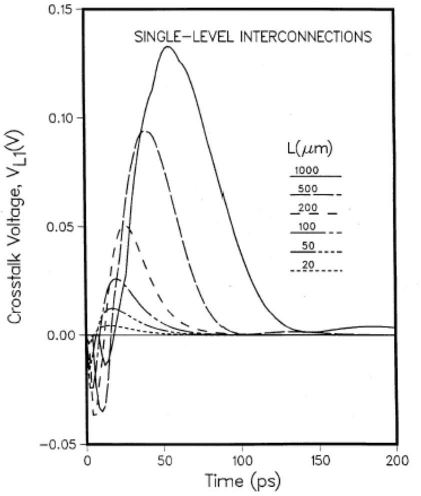
Crosstalk can also be reduced by providing shielding ground lines adjacent to the active interconnections.

Single Level Parallel Interconnects

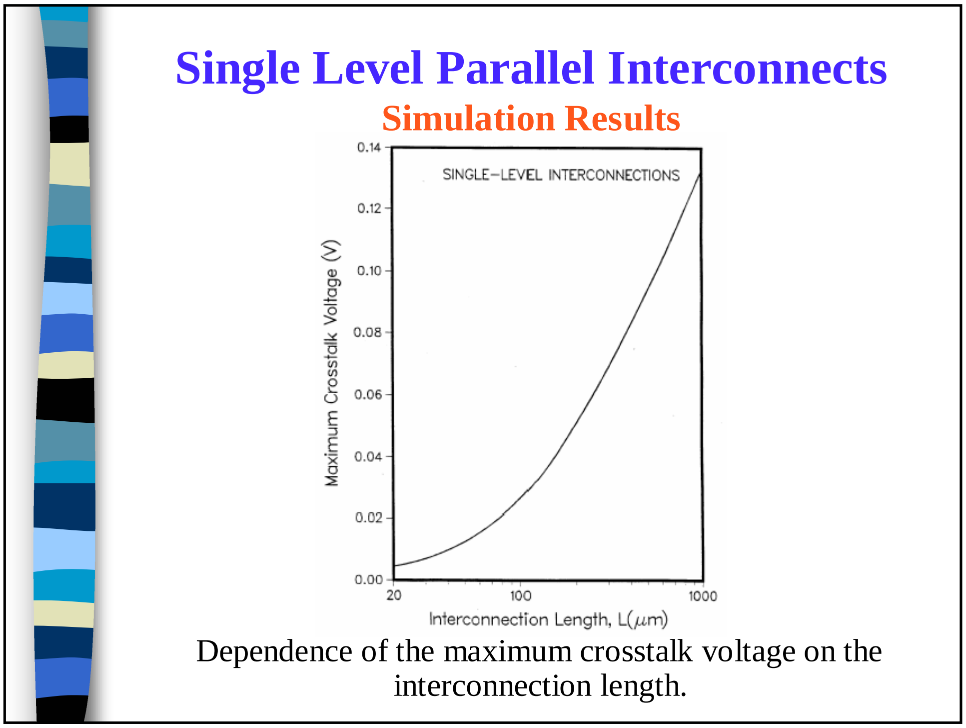


Single Level Parallel Interconnects

Simulation Results



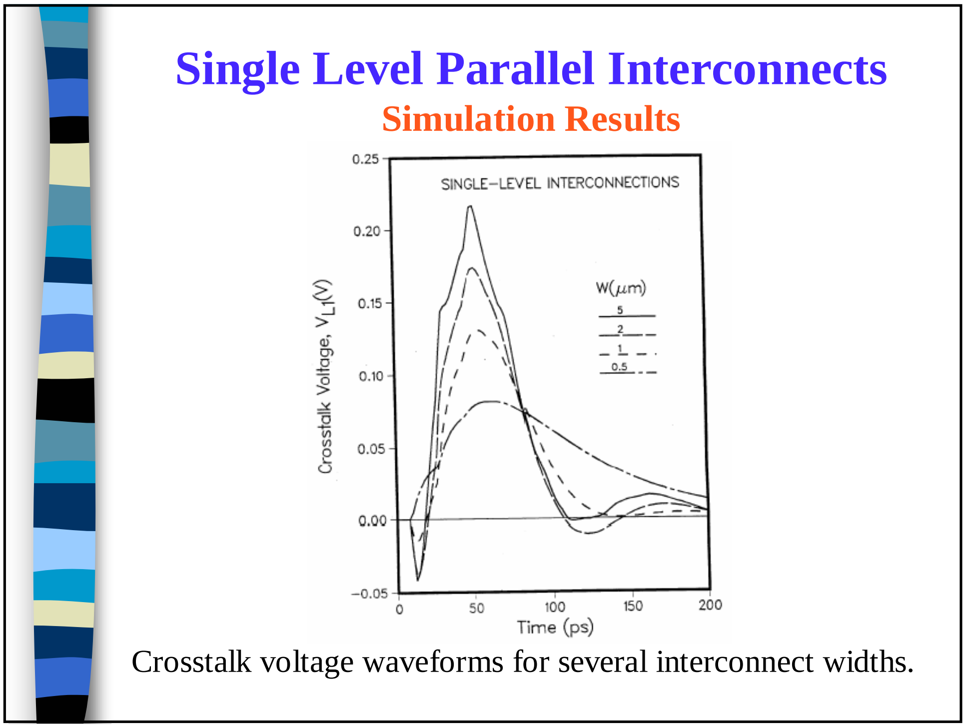
Crosstalk voltage waveforms for several interconnect lengths



Single Level Parallel Interconnects

Simulation Results

Dependence of the maximum crosstalk voltage on the interconnection length.



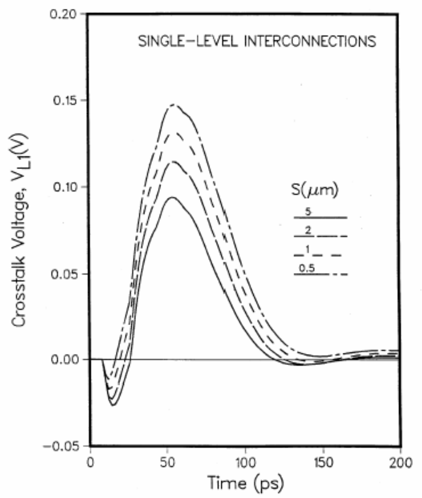
Single Level Parallel Interconnects

Simulation Results

Crosstalk voltage waveforms for several interconnect widths.

Single Level Parallel Interconnects

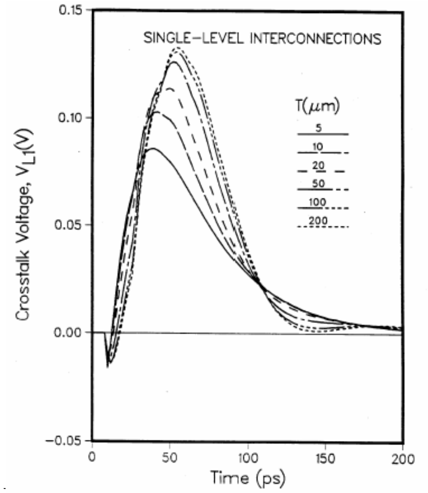
Simulation Results



Crosstalk voltage waveforms for several interconnect separations.

Single Level Parallel Interconnects

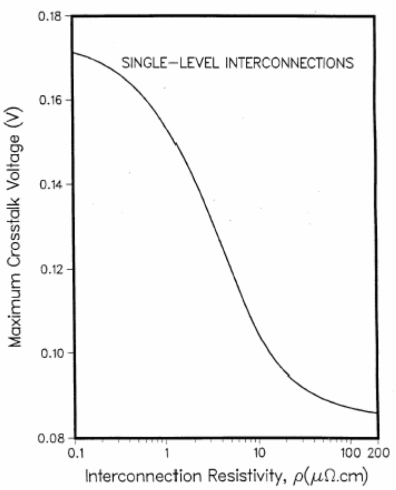
Simulation Results



Crosstalk voltage waveforms for several values of the thickness of the GaAs substrate.

Single Level Parallel Interconnects

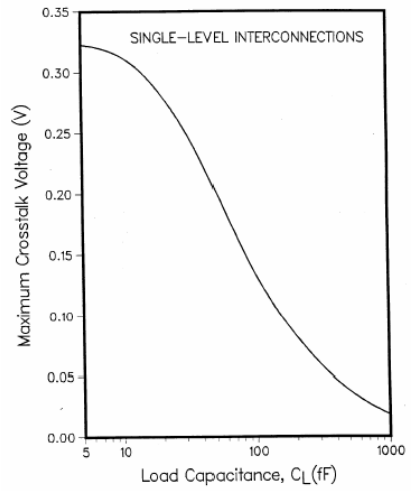
Simulation Results



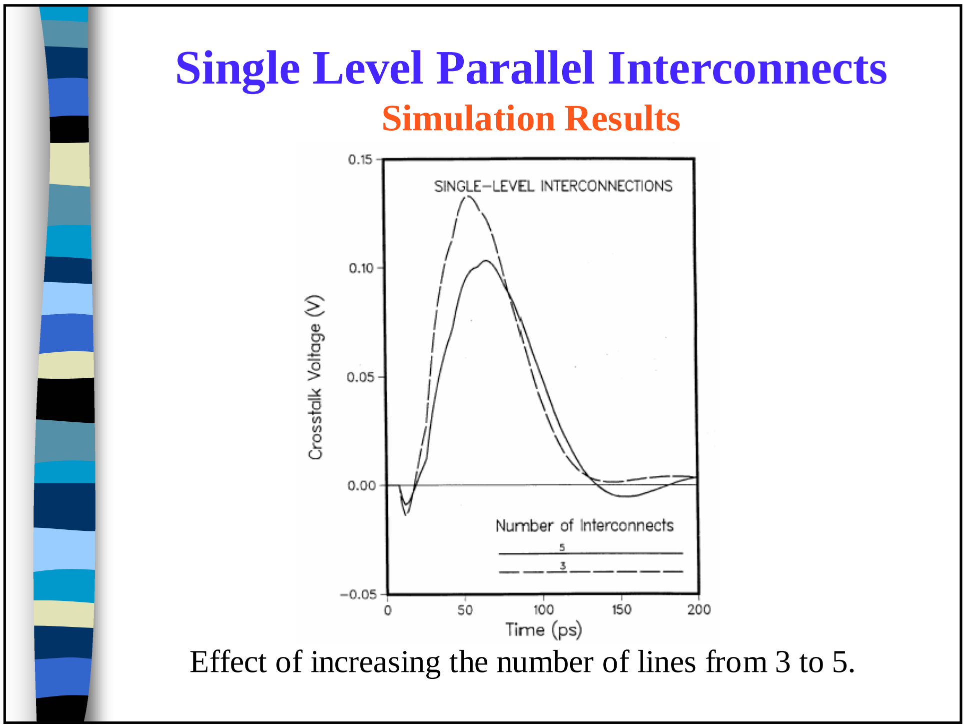
Dependences of the maximum crosstalk voltage on the interconnect material resistivity.

Single Level Parallel Interconnects

Simulation Results



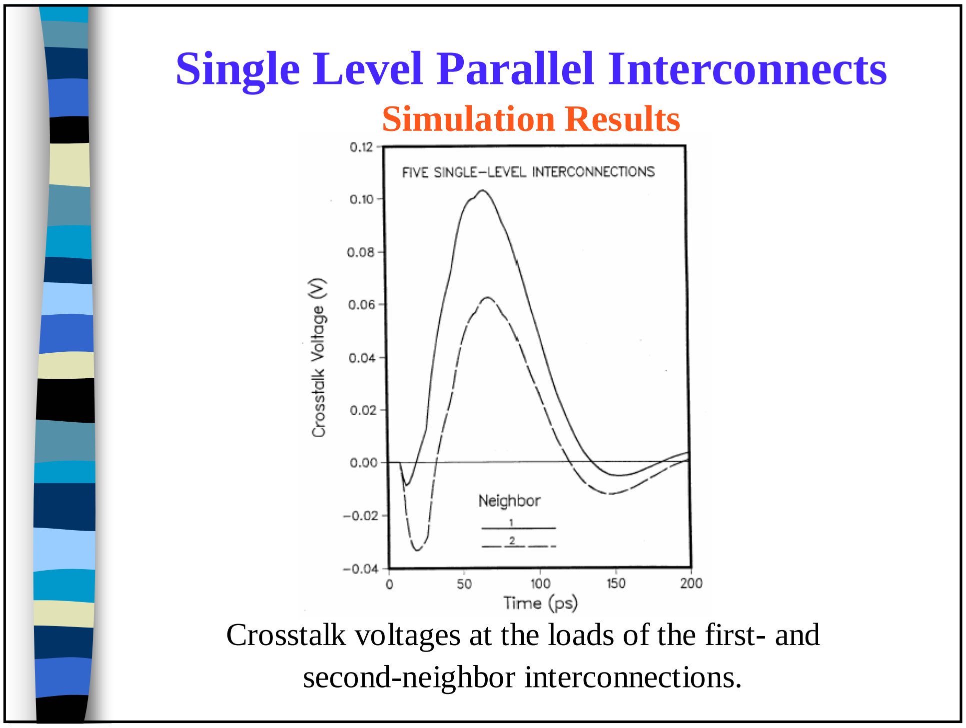
Dependences of the maximum crosstalk voltage on the load capacitance.



Single Level Parallel Interconnects

Simulation Results

Effect of increasing the number of lines from 3 to 5.

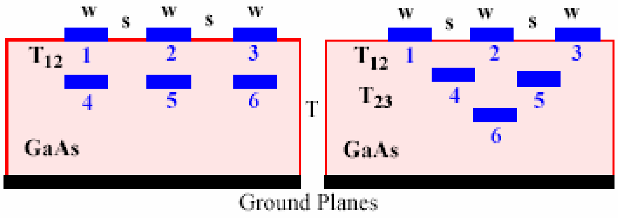


Single Level Parallel Interconnects

Simulation Results

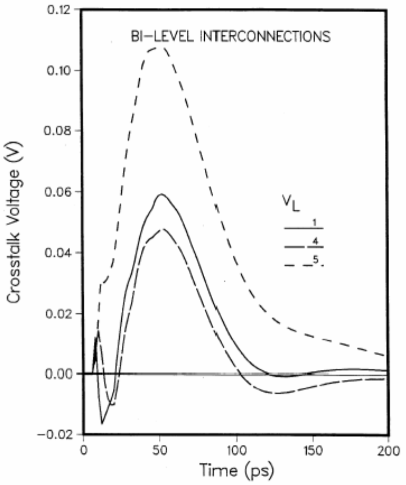
Crosstalk voltages at the loads of the first- and second-neighbor interconnections.

Bilevel and Trilevel Parallel Interconnects



Bilevel and Trilevel Parallel Interconnects

Simulation Results



Crosstalk voltage waveforms at the loads of the first, fourth and fifth interconnects for the bilevel interconnection configuration with T12 = 2 µm.

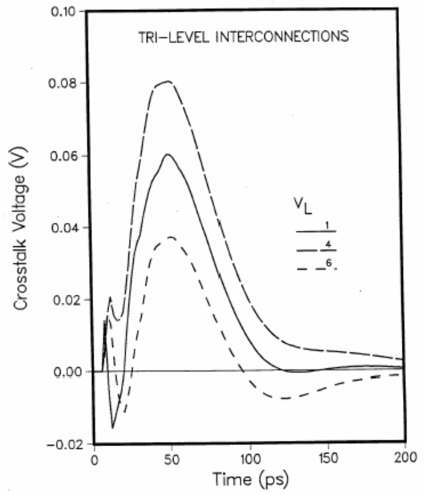
Bilevel and Trilevel Parallel Interconnects

Simulation Results

Crosstalk voltages on the first-neighbor interconnects in the bilevel configuration are almost half of those in the single-level configuration.

Bilevel and Trilevel Parallel Interconnects

Simulation Results



Crosstalk waveforms at the loads of the first, fourth and sixth interconnects for the trilevel interconnection configuration with $T_{12} = T_{23} = 2$ µm.

Bilevel Crossing Interconnects
Simulation Results

Crosstalk in the embedded crossing interconnects due to a driven interconnect printed on top of the GaAs substrate can be simulated by the computer program SPBIGV.

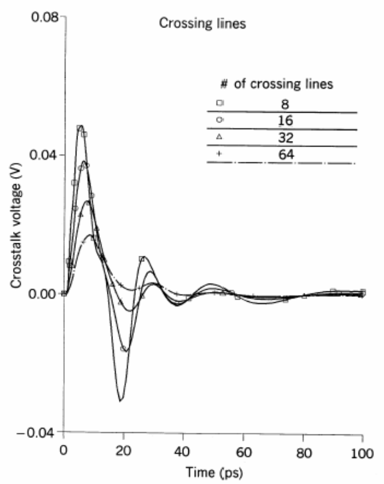
In the following results, unless otherwise specified:

Number of crossing lines is 25

Crosstalk plots are for the 13*th* crossing interconnection.

The frequency of the input square wave train is 1 GHz.

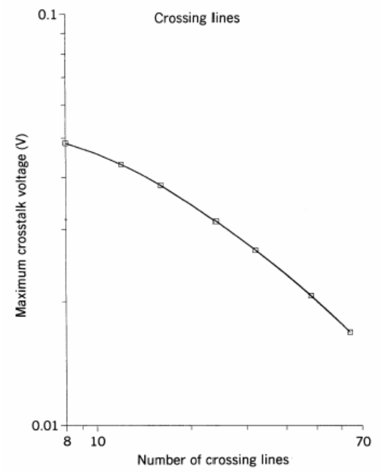
Bilevel Crossing Interconnects
Simulation Results



Crosstalk voltage waveforms for several values of the number of crossing lines.

Bilevel Crossing Interconnects

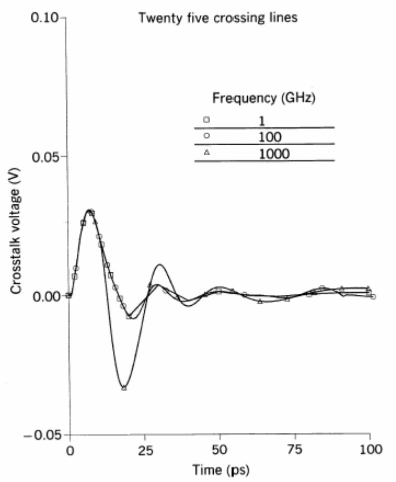
Simulation Results



Dependence of the maximum crosstalk voltage on the number of crossing lines.

Bilevel Crossing Interconnects

Simulation Results

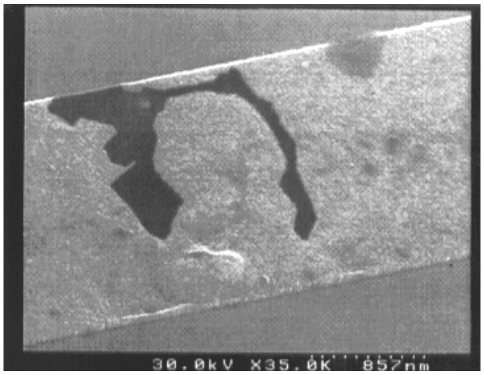


Crosstalk voltage waveforms for several frequencies of the input square wave train.

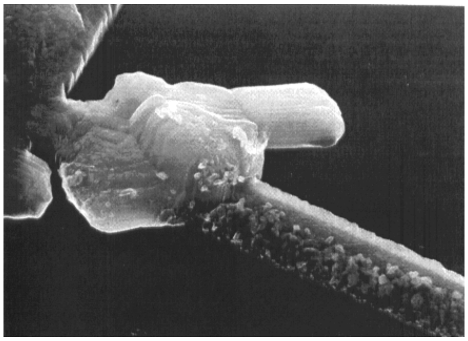
Electromigration

- "Electromigration" refers to mass transport in metals under high stress conditions such as high current densities and high temperatures.
- This presents a key problem in VLSI circuits by causing open-circuit and short circuit failures in the VLSI interconnects.

Void Formation



Hillock Formation



Problems caused by Electromigration

Joule Heating

- As the chip size decreases, heat distribution becomes a serious problem.
- For a metal wire that can afford a certain current density rate of about $10^5 A/m^2$-s before melting, joule heat generated by current density in the interconnection line exceeding half of this limit must be completely removed through the substrate and/or some passivation layer.
- Cooling rate has to be faster than the heating rate due to the current density.

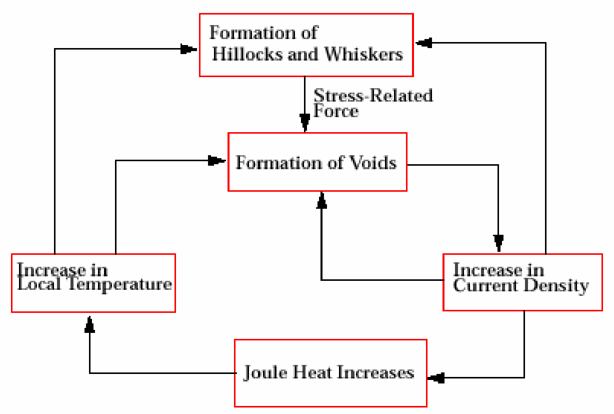
Problems caused by Electromigration

Current Crowding

- It refers to uneven distribution of currents along the metallization lines especially in metals with structural inhomogeneities.
- It can cause the atoms in the metallization lines to migrate with different velocities resulting in the formation of voids that can cause open circuit failure.

Electromigration

Mechanism



Electromigration

Median Time to Failure (MTF)

$$\mathrm{MTF} = A\,J^{-n} \exp\left(\frac{E_a}{kT}\right)$$

- E_a = Activation energy
- J = Current density
- T = Temperature in degrees Kelvin
- A = Constant depending on geometry and material
- k = Boltzmann’s constant
- n = Constant ranging from 1 to 7

Electromigration

Factors

- Current density is the key factor that contributes to electromigration. MTF decreases as the current density increases.
- Electromigration occurs in the direction from high temperature to low temperature and thermal gradients can induce a thermal force that enhances further mass transport in the metallizations.
- Line temperature is an important factor in the electromigration process. MTF decreases with the increase in the line temperature.

Electromigration

Factors

- A longer line result in a shorter lifetime as compared to a shorter line.
- Interconnection metallizations having high activation energy are desirable because they lead to enhanced stability.
- Material structure also affects the electromigration lifetime in many ways. Known aspects include grain orientation, grain size and grain boundaries.
- An ideal metallization line is the one with uniform grain size and regular grain orientation.

Electromigration Testing

Resistance Measurement

- In general, when an open-circuit failure occurs, the resistance goes up, whereas when a short-circuit failure occurs, the resistance goes down.
- Therefore, by measuring the resistance one can check whether electromigration has taken place.
- A standard method of evaluating VLSI interconnects using this approach is called "accelerated testing" in which high current density and high temperature are applied to the metallizations.

Electromigration Reduction

Using a Passivation Layer

- **Passivation:** Overcoating the substrate to prevent the formation of vacancies needed for diffusion and to presumably fill up the broken bonds on the surface of the metallization.
- With the addition of a passivation layer, the joule heat can be dissipated more easily.
- Materials mostly used are oxides and dielectric layers like SiO, Al2O3-SiO2 and P2O5-SiO2 .
- This technique has proven to be effective in improving electromigration lifetimes.

Electromigration Reduction

Using Gold Metallizations

- Interconnect system has a much better MTF than using the aluminum films.
- The key reason for this is that gold has a very high activation energy.
- Because of its inert nature, adhesion of gold to the insulating layer by chemical bonding is extremely difficult.
- Therefore, gold is used in a multilayer system where more than one layer of metallization is used to adhere to the insulator as well as to gold.

Electromigration Reduction

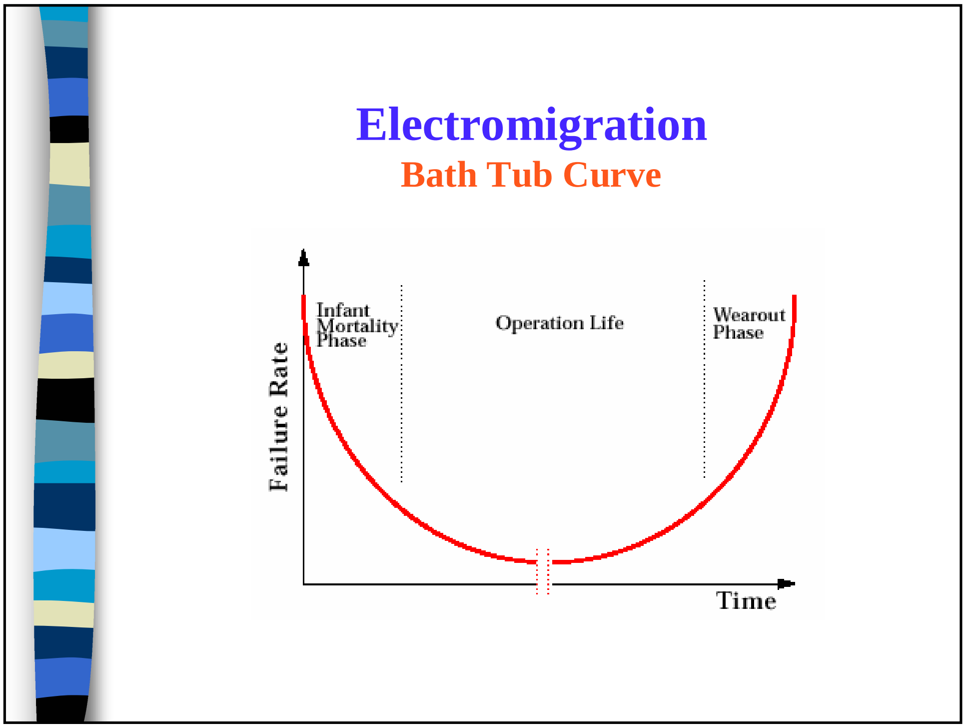
Alloying of Metallization

- The addition of correct type and concentration of alloys has also been shown to improve the electromigration lifetime.
- For example, addition of Ti-Si to Al increases the lifetime by more than an order of magnitude whereas the addition of Cr-Si does not show any noticeable improvement.
- Addition of 0.4% Cu to Al with or without the addition of Si results in better electromigration lifetimes than pure Al.

Electromigration Reduction

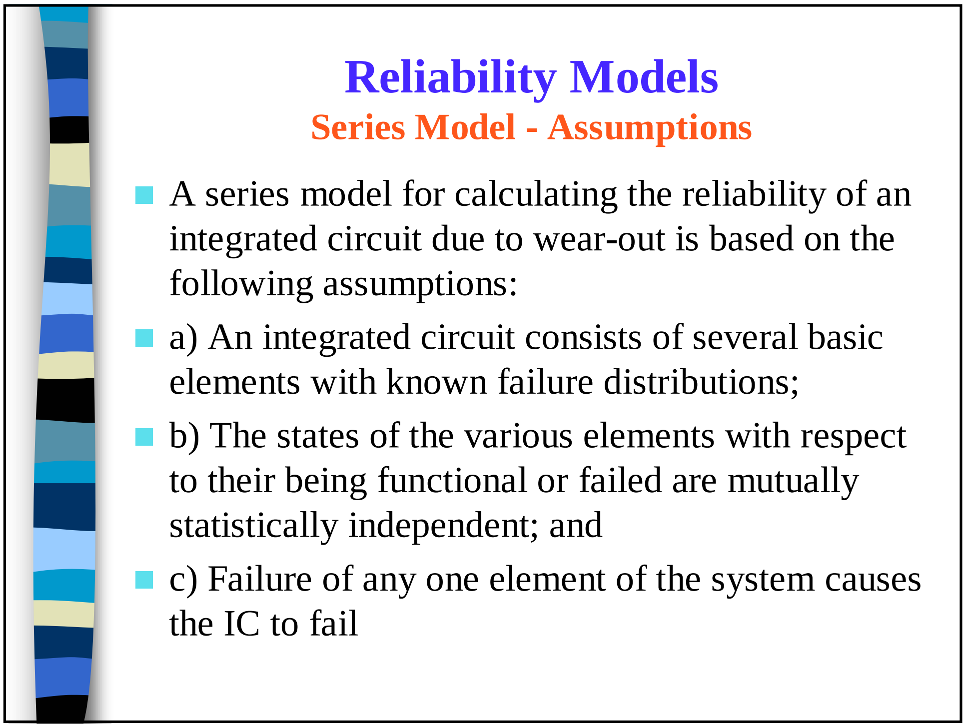
Deposition Techniques

- It has been shown that the MTF of a VLSI system has a close relationship with the employed deposition technique.
- For example, it is found that the MTF is smaller for the sputtered film technique than the e-beam deposition technique.



Electromigration

Bath Tub Curve



Reliability Models

Series Model - Assumptions

- A series model for calculating the reliability of an integrated circuit due to wear-out is based on the following assumptions:
- a) An integrated circuit consists of several basic elements with known failure distributions;
- b) The states of the various elements with respect to their being functional or failed are mutually statistically independent; and
- c) Failure of any one element of the system causes the IC to fail

Failure Analysis of Interconnection Components

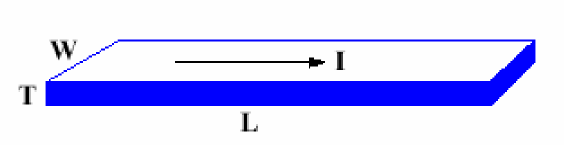
- An interconnection line on an IC chip can consist of several components such as straight segments, bends, steps, plugs and vias.
- There are also power and ground buses serving several logic gates on the chip.
- It is important to study the dependence of electromigration-induced failure of each interconnection component on the component parameters.

The Program "EMVIC"

EMVIC is an interactive program that can be used to determine the MTF for a straight segment and the values of MTF for the other interconnect components.

Failure Analysis

Straight Segment

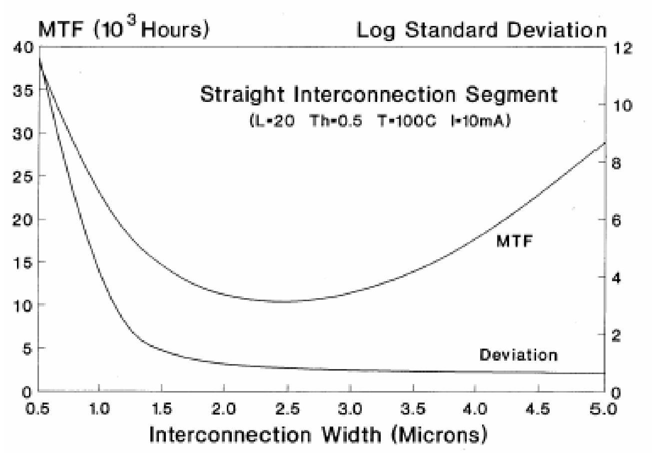


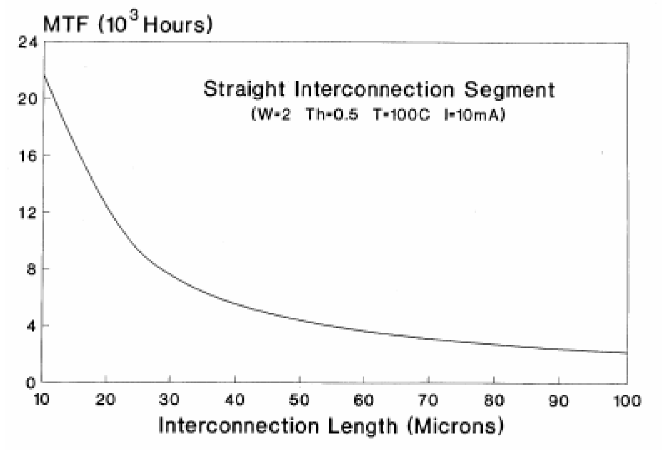
For a basic conductor element of length 10µ m, the median-time-to-failure (MTF) is given by:

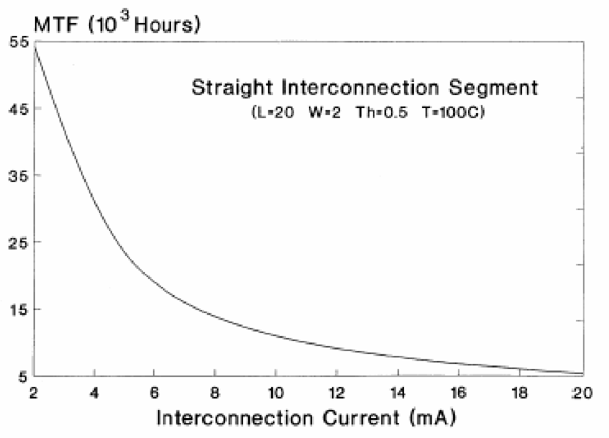
$$1523.\left(\frac{WT}{I\times 10^{5}}\right)^{n}\left(W-3.07+\frac{11.63}{W^{1.7}}\right)\exp\left(\frac{10740.74\ E_{a}}{T_{K}}\right)$$

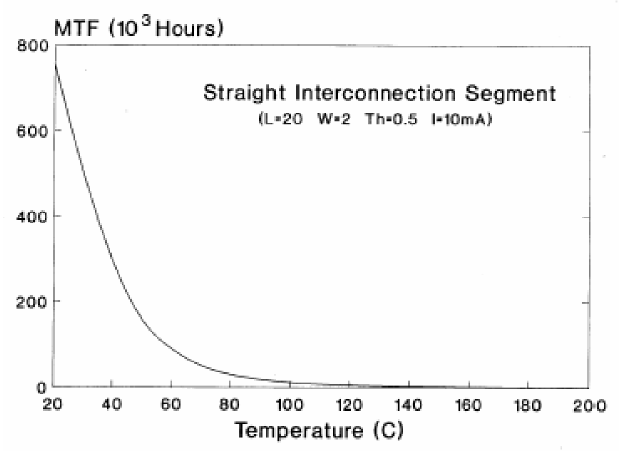
$$1523.\left(\frac{WT}{I\times 10^{5}}\right)^{n}\left(W-3.07+\frac{11.63}{W^{1.7}}\right)\exp\left(\frac{10740.74\ E_{a}}{T_{K}}\right)$$

- I is the current in mA
- n is the current density exponent
- E_a is the activation energy of the interconnect material in eV
- T_K is the temperature in ^{o}K
- W is the interconnection width in µm, and
- T is the interconnection thickness in µm.


MTF (10^3 Hours)
Log Standard Deviation
Straight Interconnection Segment
(L=20 Th=0.5 T=100C I=10mA)
MTF
Deviation
40
35
30
25
20
15
10
5
0
12
10
8
6
4
2
0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5
5.0
Interconnection Width (Microns)

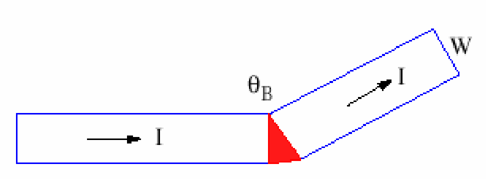

MTF (10^3 Hours)
Straight Interconnection Segment
(W=2 Th=0.5 T=100C I=10mA)
24
20
16
12
8
4
0
10
20
30
40
50
60
70
80
90
100
Interconnection Length (Microns)


MTF (10³ Hours)
Straight Interconnection Segment
(L=20 W=2 Th=0.5 T=100C)
55
45
35
25
15
5
2
4
6
8
10
12
14
16
18
20
Interconnection Current (mA)


MTF (10³ Hours)
Straight Interconnection Segment
(L=20 W=2 Th=0.5 I=10mA)
800
600
400
200
0
20
40
60
80
100
120
140
160
180
200
Temperature (C)

Failure Analysis

Bend



- The additional area in the bend (shown shaded) is equivalent to a straight segment of length and width given by:

$$L_B = \frac{\pi W \left|(180 - \theta_B)\right|}{360}$$

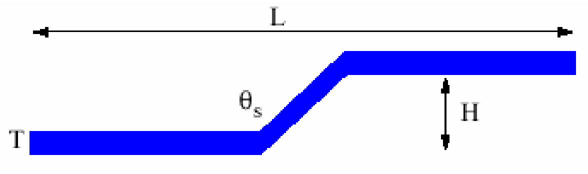
$$W_B = \frac{W^2\left(1 + \sqrt{\tan\left(\frac{\theta_B}{2}\right)}\right)}{W + L_B}$$

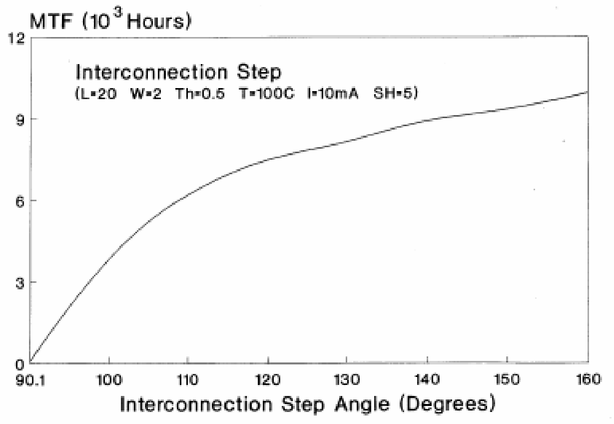
- As a first approximation, the MTF of a series combination of N elements (MTF_S) can be found by using the expression:

$$\frac{1}{MTF_s} = \frac{1}{MTF_1} + \frac{1}{MTF_2} + \ldots\ldots\ldots\ldots + \frac{1}{MTF_N}$$

Interconnect Component

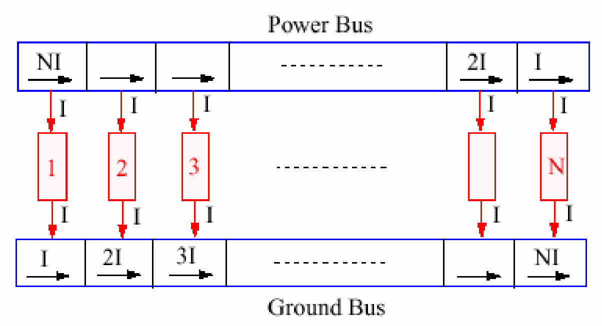
Step





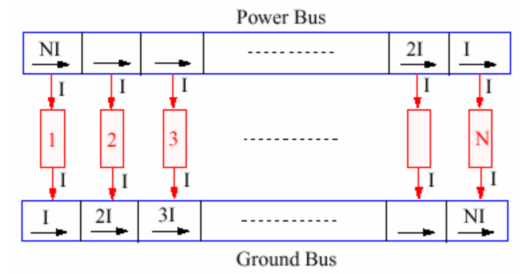
Interconnect Component

Power/Ground Bus

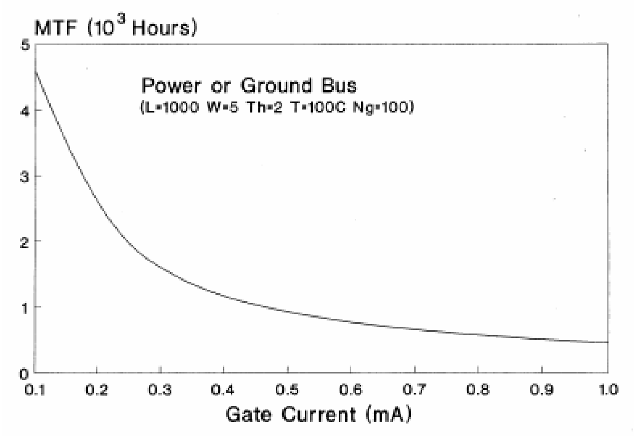


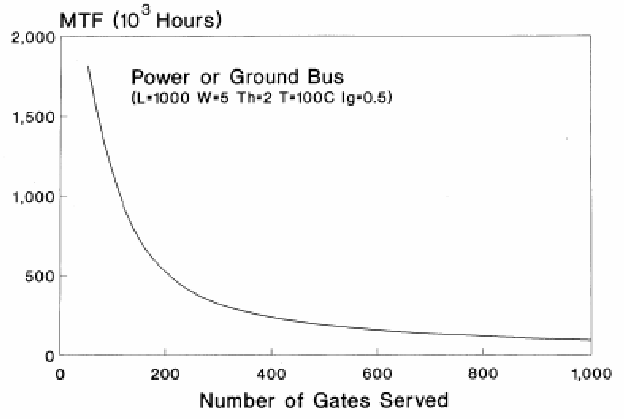
Interconnect Component

Power/Ground Bus



As shown above, a power or ground bus serving N gates on the IC chip can be modeled as a series combination of N straight segments carrying currents equal to I, 2I, 3I,.....,NI where I is the current in each gate.


MTF (10^3 Hours)
5
4
3
2
1
0
Power or Ground Bus
(L=1000 W=5 Th=2 T=100C Ng=100)
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Gate Current (mA)


MTF (10^3 Hours)
2,000
1,500
1,000
500
0
Power or Ground Bus
(L=1000 W=5 Th=2 T=100C Ig=0.5)
0
200
400
600
800
1,000
Number of Gates Served