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P.V. Ananda Mohan

VLSI Analog Filters

Active RC, OTA-C, and SC

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P.V. Ananda Mohan
Electronics Corporation of India, Ltd.
Bangalore, India

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To
Radha Nirmala

Preface

The design of mixed signal integrated circuits is of continuing interest. The most important analog blocks in these are A/D converters, D/A converters, and filters. The art of analog filter design has been documented in several classic books used in academic institutions worldwide. Some books have focused completely on one particular topic, such as switched-capacitor filters, current-mode filters, or active RC filters (based on opamps). Some books have covered all or a few of these. To the author's knowledge the most recent book appeared in 2005.

More recent industry requirements in mixed signal chips include low-voltage operation, low power requirement, and high-frequency operation. Many specialized techniques will be needed to achieve these objectives. These interesting and innovative techniques are documented in reputable journals such the *IEEE Journal of Solid-State Circuits* and *IEEE Transactions on Circuits and Systems*, among others. Hence, introducing these into the curriculum is of utmost importance so that students may graduate with up-to-date knowledge to cater to the needs of industry. In addition, it has become important to teach most relevant information in the short space of one or two semesters while giving sufficiently broad coverage of the various topics.

This book is an effort in this direction. Contemporary designs of VLSI analog filters can be classified into active RC filters, OTA (operational transconductance amplifier)-C filters, SC (switched-capacitor) filters, log-domain filters, MOSFET-C filters, current-mode filters using devices such as current conveyors or current feedback amplifiers, and so on. Among these perhaps the most popular have been the first three because of the possible ease of design, implementation, and versatility; good high-frequency performance; and the ability to work at low power supply voltages and in an acceptable dynamic range. In this book, we focus on these three areas.

The structure of the book is as follows. In Chap. 1, a general introduction to the subject of VLSI analog filters is presented. Chapter 2 deals with active RC filters

starting from amplifiers and first-order filters and considers the effect of nonidealities of the opamp and techniques for compensation of these nonidealities. Second-order active RC filters using a single amplifier, two opamps, and more opamps are covered. Only popular structures are considered with analysis presented on sensitivity to passive components and effect of opamp bandwidth. Techniques of using the finite bandwidth of opamps in active filter realization to eliminate one or both capacitors needed in a biquad realization are also considered in detail. Active RC filter design based on component simulation and operational simulation of LC ladders as well as multiloop feedback filters are considered. Noise analysis and distortion analysis are also described. Designs that can take advantage of differential output amplifiers are also described.

In Chap. 3, active filter design using OTAs and capacitors is described in detail. First-order filters, second-order filters using grounded capacitors, and filters derived through component simulation are studied in detail. Filters using OTAs with dual current outputs and with current outputs are also studied in detail. High-order filter design using some recently described analytical synthesis techniques is considered as well. The effect of nonideal frequency response of OTA and noise of OTA-C filters is discussed for various filters.

Chapter 4 deals with SC filters. The concepts of switched capacitor filter and the method of analysis using Laker's equivalent circuit are described so as to enable the reader to derive digital transfer functions of various filters. Second-order stray-insensitive filters are considered in detail since they are the most popular in industry. The optimal design of these filters to reduce area/capacitor spread/sensitivity is considered. High-order SC filters based on operational simulation are described in detail. Recent designs extend the frequency of operation of SC filters by using a variety of interesting techniques such as *N*-path filters, double-sampling, and precision opamp gain (POG). All these techniques are described in detail. The analysis techniques for the nonidealities in SC filters such as opamp offset, switch clock feedthrough, charge injection, distortion, finite gain, and bandwidth of the opamp, foldover noise, and opamp 1/f noise are described in great detail together with compensation techniques. Due to the most popular application of SC circuits being in oversampled A/D converters, a section deals exclusively with the architectures and performance-related issues. The design of low-voltage SC filters is also considered for completeness.

Several innovative designs using the techniques considered in Chaps. 2, 3, 4, and 5 have been fruitfully employed in many contemporary integrated system-on-chip (SOC) designs. In Chap. 5, several recent application-specific designs have been surveyed in order to illustrate how the theory can be applied in practice.

The book has several illustrations to explain the concepts clearly and has an extensive bibliography. Several WINSPICE-based simulation examples have been provided in Chaps. 2, 3, 4, and 5 so that the performance of the various circuits can be analyzed. The book can be used for self-study or prescribed as a textbook. The only prerequisite is a basic course in circuit analysis, and a basic knowledge of DSP fundamentals.

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Bangalore, India P.V. Ananda Mohan

Contents

Chapter 1
Introduction

The reader may be aware that today in all the appliances we use in our everyday lives such as cell phones, digital cameras, and DVD players there is emphasis on very large scale integration. The challenge of realizing complex mixed-signal systems (containing both analog and digital subsystems) in a small area with small power consumption, small weight, and the capability to work at very high frequencies of a few hundred megahertz are successfully being addressed. Moreover, the complete mixed-signal system has to be realized in silicon since it is an economical and easily available process technology compared with other process technologies such as gallium arsenide and the like. Today, radio frequency CMOS in silicon is a well-investigated area [1.1].

There has also been more emphasis on digital signal processing (DSP) since the digital signal processing–based designs can be easily programmed if necessary and most functions can be realized digitally with minimum dependence on expert analog designers. Of course, since the signals we normally encounter are analog, such as speech, audio, video, picture, and the like, there is a need for analog front-ends. These need to perform the jobs of amplification, antialiasing filtering, coding (or analog/digital conversion) at the input and similarly decoding (or digital/analog conversion) and smoothing using filters at the receiving end, as shown in Fig. 1.1.

There have been several innovations in the previous four decades to realize the analog front-ends efficiently. Filters form an important part of the front-end. In this book, we focus on the design and implementation aspects of filters in CMOS very-large-scale integration (VLSI) technology. Several books have been written on continuous-time filters covering the various types of techniques available: active resistor–capacitor (RC) filters using operational amplifiers (opamps, or OAs), log-domain filters using bipolar transistors, or operational transconductance amplifier (OTA) -capacitor (G_m-C) filters using OTAs. Discrete-time filters such as switched capacitor (SC) filters using CMOS opamps and switched-current (SI) filters also have been extensively investigated.

Although the opamp continues to be quite popular among filter designers, several new devices have been discovered over the years, especially for operation in current mode, and these have been used with some degree of success. Some of

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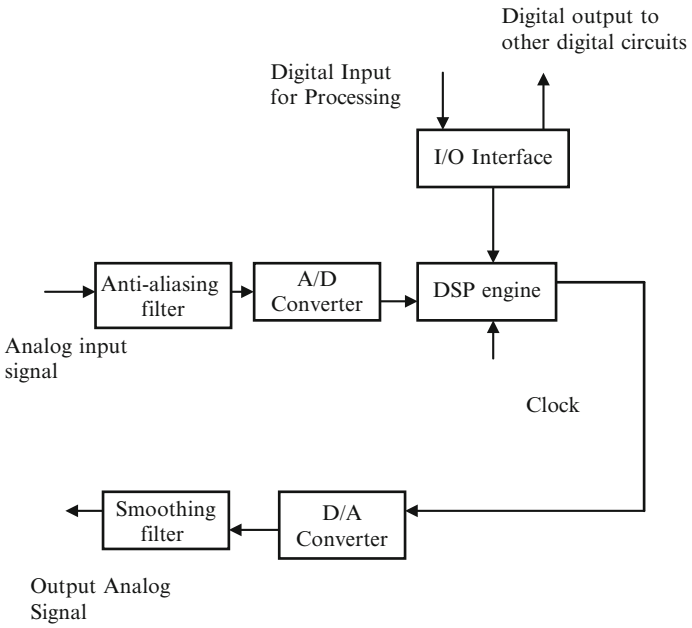

Fig. 1.1 A typical mixed-signal VLSI chip architecture

these are current conveyors (CCs), current feedback opamps (CFOAs), and current input differencing amplifiers [1.2].

In this book, we start from basic circuits such as amplifiers and first-order filters and develop from these structures for realizing high-order filters. Because of the tolerances of realized components in the standard VLSI fabrication processes, the evaluation of sensitivity of the filter parameters to pole-frequencies and pole-Q, zero-frequencies, and zero-Q are very important. Other important issues such as dynamic range, noise computation, evaluation of distortion, estimation of area, and element spread (of capacitors, resistors, transconductances, etc.) are also relevant and addressed in this book. The sensitivity and noise analysis techniques described do not change with the design approaches used in the realization of filters and can be easily applied to future evolution as well.

We make some introductory remarks in the next few sections that are applicable to the various techniques described in this book in later chapters.

1.1 Problems in Integration of Analog Filters

The difficulties faced in integration of analog filters and the requirements are well documented [1.3, 1.4, 1.5, 1.6]. These are briefly as follows.

Frequency response stability: The frequency variations due to temperature variations, and fabrication tolerances shall be reduced to much less than 1%.

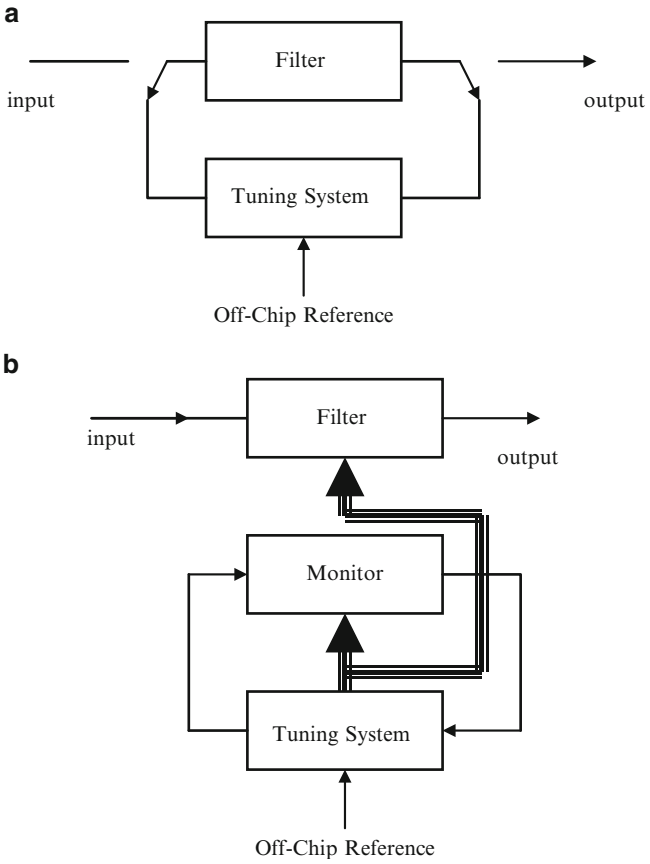

Fig. 1.2 Filter tuning methods (**a**) direct; (**b**) indirect

This may necessitate the use of automatic tuning in the case of OTA-C or continuous-time filters. Several tuning methods are available using direct or indirect methods. In the direct method shown in Fig. 1.2a, the filter is disconnected from the actual system and tuned using an off-chip reference. In the indirect method shown in Fig. 1.2b, there is no need to disconnect the filter from the main signal-processing chain. Using a similar replica filter constructed in the same environment in close proximity and tuning it, the control signals can be derived for the main filter. The two filters are believed to track well. The off-chip stable reference could be a low-temperature-coefficient resistance or a frequency of a crystal oscillator.

High-frequency performance: Parasitic capacitances as well as deteriorated high-frequency response of transistors can cause severe deviations in the realized frequency response. These put limits on the maximum frequency of operation.

Quality of passive components [1.7]: The Q of the inductors can be quite low due to the finite but not negligible series resistance of the inductors as well as resistance

of the substrate. The parameters of spiral inductors depend on the line width, spacing, number of turns, size of opening in the middle, and the type of shield placed under the inductor. Typical values of realized inductances are 2–1,000 nH. The loss of the inductors can be compensated using negative resistance in the circuit.

Resistances of 20–100 Ω per square can be realized easily. The matching accuracy of resistors can be about 0.4% by using suitable layout techniques. The temperature coefficients are typically on the order of 1,500–8,000 ppm/°C. The voltage coefficient of the realized resistances can be about 100–200 ppm/V. High-quality capacitors can be made and good matching can be achieved so that ratios can be accurately realized. The value of a resistor x can be expressed as a function of voltage across the resistor V as $x = x_o(1 + \alpha_1 V + \alpha_2 V^2)$. Note that the linearity of the resistors improves with their length.

Capacitors of various types are available with high capacitance per unit area. The fabricated capacitors of values ranging from 0.02–2.7 fF/μm^2 can be realized. The matching accuracy of capacitors can be in the range 0.05–1.5% [1.8]. The temperature coefficients will be typically on the order of 20–50 ppm/°C. A high ratio of actual capacitance to parasitic capacitance can be achieved with proper layout. The plate of the capacitor with least parasitic capacitance is called the bottom plate and the other is called top plate.

In addition to device area, other characteristics such as cleanliness of the process determine the magnitude of mismatches.

Signal-handling capability: Due to the main reason that the power supply voltages are becoming very low, achieving large signal swing needs specialized techniques.

Noise: Resistors and active devices such as opamps, transistors, and OTAs generate active and passive noise. Circuit design techniques to minimize noise are available so that the required dynamic range can be met in spite of lower power supply voltages.

1.2 Filter Design Approaches

Several design approaches are available for the design of integrated analog filters [1.9]. These are briefly described next and some of the approaches are studied in detail in Chaps. 2, 3, and 4.

1.2.1 LC Filters

Historically, LC filters were the first to be used extensively in telecommunication applications. The main advantages of LC filters are the low noise, high linearity, lack of power dissipation, and availability of powerful design tools. However, the problems of integrated inductors mentioned earlier especially the low-Q have

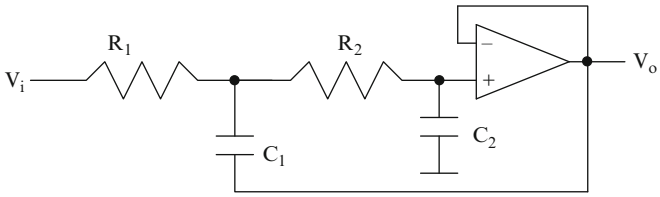

Fig. 1.3 Sallen–Key active RC filter

barred their use. Interestingly, however, RF CMOS designers prefer these once again and have devised several techniques such as lightly doped substrates [1.10, 1.11, 1.12] to overcome the limitation of low-Q (typically 5–10) of the fabricated annular or spiral on-chip inductors of a few nano-Henries using Q-enhancement through active devices.

1.2.2 Active RC Filters

Active RC filters using opamps [1.9] were extensively investigated and continue to be in use in the front-end of most analog ICs today. The designs are standardized and based on analysis of sensitivity to passive components, opamp nonidealities such as finite gain and finite bandwidth, opamp noise, and power dissipation (number of opamps); vast choice is available to the designer. Tradeoff of active and passive noise is possible. The linearity of the active RC filters is quite good due to the excellent linearity of the resistors. Some of the active RC filter structures may not be suitable for VLSI implementation since parasitic capacitances at various nodes in the active RC filters may affect the performance. However, in situations where the tolerance of components is not a problem such as antialiasing filters, active RC filters (see, e.g., Fig. 1.3) are the most popular choice.

Active RC filters of second-order (in the case of high odd-order filters, one first-order filter) are cascaded to realize high-order filters. High-order active RC filters can be derived from RLC filters using *component simulation* or *operational simulation*. In the component simulation technique, inductances are realized by opamps, resistors, and capacitors. On the other hand, in the operational simulation method, the internal working of the RLC filter is mimicked by realizing the nodal equations exactly. High-order filters based on multiple-loop feedback also have been extensively studied. More recently, new features such as availability of differential outputs have led to interesting new structures as studied in a later chapter. The existing body of knowledge on active RC filters has helped the easy generation of filter structures for other subsequent filter design methods.

1.2.3 Active R and Partially Active R Filters

The effect of opamp bandwidth on active RC filters has been studied extensively and several techniques to correct for the deviations in pole-frequency and pole-Q using predistortion, passive compensation (using additional passive components resistors or capacitors), and active compensation (using additional opamps) have been proposed. These may increase power dissipation and reduce the dynamic range. As an alternative to compensation, converting the nonideality–finite bandwidth to a possible advantage was also considered. An opamp with finite bandwidth is basically an integrator, therefore designers tried to eliminate one integrator in a second-order filter by using the inherent pole of the opamp. This led to partially active R filters (see Fig. 1.4a) needing only one capacitor per pole pair. More recently, this technique has been exploited to realize filters for very high frequencies for GSM handsets. These are discussed in detail in Chap. 2. All these filters that use resistors or capacitors invariably need the use of precision discrete components with low tolerances $<1\%$ and often need tuning of the resistors using techniques such as laser trimming in thick film hybrid circuits to bring them nearer to the correct values. In contemporary designs, tuning is performed using an array of resistors and capacitors and selecting some of these using digitally controlled switches [1.13].

Designers were later tempted to do away with the capacitors altogether and exploit the bandwidths of two opamps to realize second-order filters. Typical active R filters [1.14] are shown in Fig. 1.4b. The interesting aspect of active R filters is the dependence of pole-Q on ratios of resistors or ratios of bandwidths of opamps. Unfortunately, however, the pole frequency is dependent on the product of bandwidths of both opamps and is prone to variation with power supply voltage and temperature. Interestingly, a technique for tuning these filters [1.15] in order to realize the desired specifications was first investigated in connection with the active R filters which become an indispensable block for continuous-time filters. This method was illustrated in Fig. 1.2b.

1.2.4 SC Filters

The need for tuning continuous-time filters in order to realize the desired specifications needs additional hardware. This can be avoided by using a SC technique. The SC technique [1.16, 1.17, 1.18] uses only switches and small capacitors to realize large resistances (see Fig. 1.5). Moreover, the pass-band width and center frequency are tunable using a clock frequency. This property is known as frequency translation. Moreover, these filters can be tuned to realize desired gain, pole-frequency and pole-Q, zero frequency using digital control of programmable capacitor arrays. The advent of the SC technique has revolutionized filtering techniques as well as A/D and D/A conversion techniques and is still a

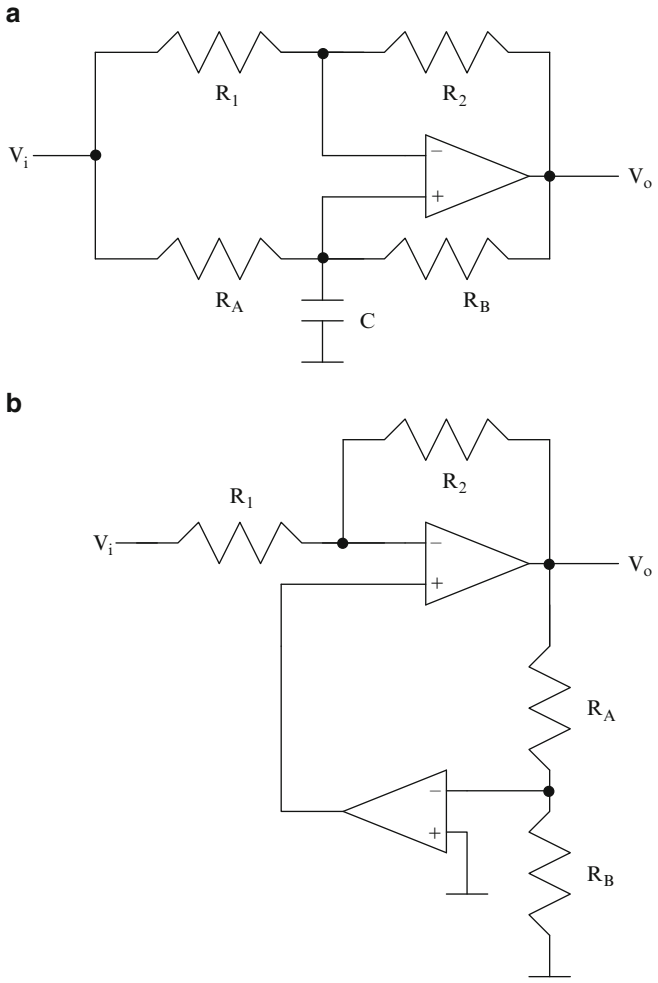

Fig. 1.4 (**a**) A partially active R filter, and (**b**) an active R filter

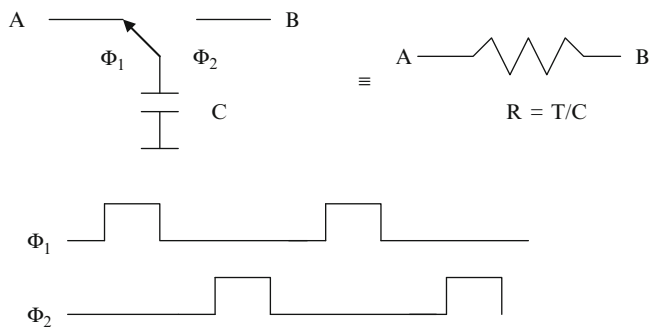

Fig. 1.5 A switched capacitor used to realize a resistor with two-phase switching waveforms

preferred choice for implementation. Ingenious techniques to enhance performance such as double-sampling, *N*-path filter technique, offset and gain compensation, fully differential structures, and low-voltage operation are currently available. SC filters have their own disadvantages due to switch nonidealities such as clock-feedthrough, foldover noise, and opamp nonidealities such as offset voltage, noise, finite gain, and bandwidth. However, solutions to combat these are also available. In Chap. 3, we focus on SC filters in great detail.

1.2.5 OTA-C (G_m-C) Filters

Although SC filters are quite popular, their limitation has been the noise level, need for clock and inability to realize very-high-frequency filters. Hence alternative design methods that use operational transconductance amplifiers have been developed. Note that SC filters also use OTAs since capacitive load only needs to be driven thus avoiding a low impedance output stage present in opamps. The G_m-C filters using transconductance elements (voltage to current converters) have been used for quite some time. More recently, multiple-output G_ms have been employed in order to realize more flexibility, multiple outputs, current, or voltage mode operation. The OTAs are basically voltage-to-current converters and are also called G_m blocks. These can be tuned using control voltage or current and can be stacked to realize higher values. A G_m-C integrator is shown in Fig. 1.6a and an active RC integrator is shown in Fig. 1.6b. For the same capacitance, and considering $G_m = G = 1/R$, the RC integrator typically has 2–3 times lower noise than a G_m-C integrator. Alternative structures that replace resistors by G_ms in active RC integrators are also available (see Fig. 1.6c) [1.3, 1.4, 1.5, 1.6]. These are known as G_m-C-opamp filters. Fully balanced structures are usually preferred so that the filters are insensitive to parasitic interference coupled through substrate and power supply and ground lines.

1.2.6 MOSFET-C Filters

Other techniques for realizing continuous-time filters were also proposed and implemented. These use the very old idea of replacing a resistor with a MOS transistor. However, using fully differential structures, the even-order nonlinearity of such simulated resistors can be cancelled. These were termed MOSFET-C filters [1.3, 1.4, 1.5, 1.6] (see Fig. 1.6d). These can be tuned using the control voltage (gate voltages) of the MOSFETs. The linearity of these may not be as high as that of active RC filters.

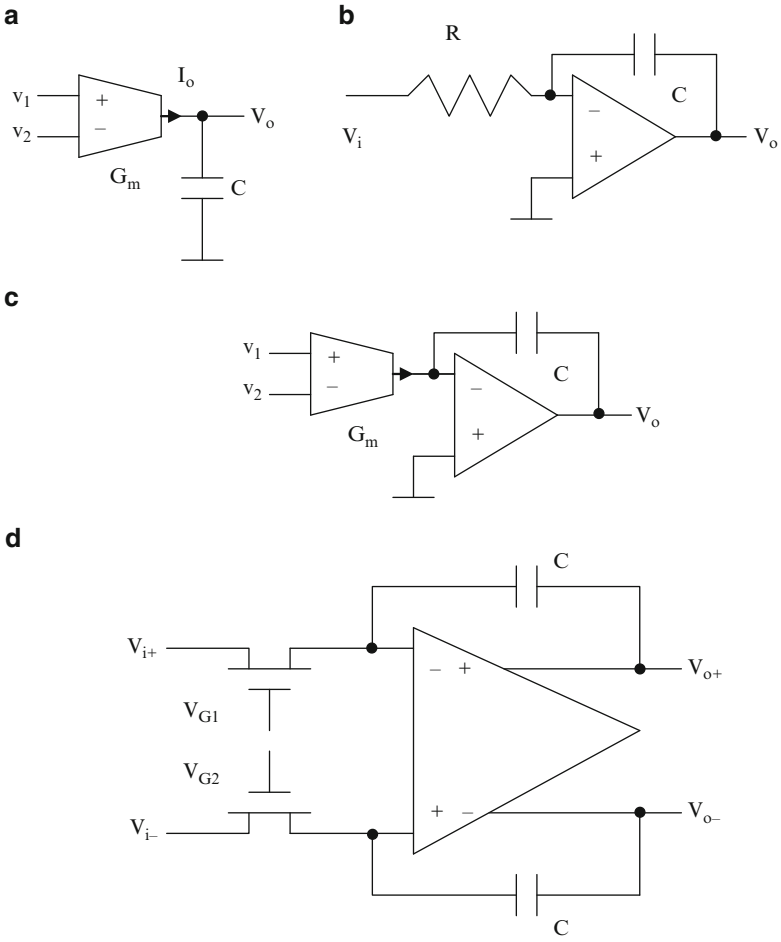

Fig. 1.6 (**a**) G_m-C integrator; (**b**) active RC integrator; (**c**) G_m-C-opamp integrator; (**d**) a MOSFET-C integrator

1.2.7 Log-Domain Filters

Other techniques are also available for continuous-time filter design that allow internal nonlinear operation of devices, and viewed as block boxes externally, they are linear. This is made possible by compressing the signal, realizing the filtering, and expanding the signal back. This may have advantage in the ICs needing low power supply voltage since only front-end and back-end work on large amplitude signals. The internally generated noise does not follow linear circuit laws. Log-domain filters belong to this class of filters [1.19, 1.20]. The input current signal is converted into voltage by a logarithmic converter (e.g., a bipolar transistor where

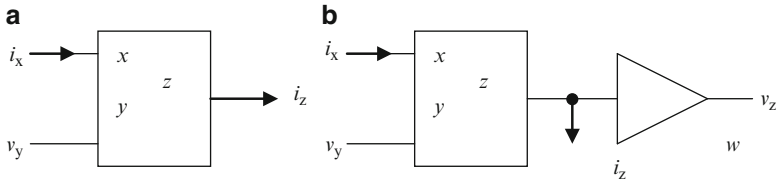

Fig. 1.7 (**a**) A CCII (second-generation current conveyor), and (**b**) a CFOA (current feedback operational amplifier)

small V_{BE} variation results because of large emitter current variations). The filter processes the compressed input signal and converts it back to linear form using an exponential converter. Using similar properties of FETs, square-root domain filters also can be constructed. In this book, we do not consider this class of filters.

1.2.8 Current-Mode Filters

The reduction of power supply voltage and need for high-frequency operation led to yet another interesting method of realizing analog filters using current-mode operation. It is well known that a common-base amplifier works in current mode and has a very good high-frequency performance. The circuit elements such as the current conveyor (see Fig. 1.7) based on this concept were proposed for instrumentation applications as early as 1972 [1.21]. There has been a revival of this area of research more recently and the availability of commercial devices such as the current feedback operational amplifier (CFOA) has further enriched this area. Numerous current-mode elements have been introduced and applications to filters, oscillators, and in some cases nonlinear blocks have been extensively studied. These also need precise external resistors and capacitors to realize complete filters and tuning these circuits may be quite involved. We do not address this area in this book.

Note, however, that circuits using one type of active element can be converted into circuits using other active elements by simple techniques.

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Chapter 2
Active RC Filters Using Opamps

In this chapter, we consider the design aspects of active resistor–capacitor (RC) filters using operational amplifiers (opamps). This topic has been covered extensively in the past three decades in several classic textbooks [2.1, 2.2, 2.3, 2.4, 2.5, 2.6, 2.7, 2.8, 2.9, 2.10, 2.11, 2.12, 2.13]. There are numerous second-order filters structures available in the literature using one, two, three, or four opamps [2.14]. The choice of a particular structure is dependent on (a) the number of opamps used, (b) power consumption, (c) orthogonal control of pole-frequency, pole-Q, gain and transmission zeroes, (d) component spread, and (e) sensitivity to passive and active components. The designer shall also consider the dynamic range available through noise and distortion analysis. We illustrate the concepts through some examples chosen among several well-known structures. This enables readers to derive for themselves the results for other circuits of interest.

2.1 Amplifiers Using Opamps

In this section we consider finite gain inverting and noninverting amplifiers. The opamp frequency-dependent gain $A(s)$ is modeled by a single-pole model given by

$$A(s) = -\frac{B}{s + \omega_a} \tag{2.1}$$

where B is the gain bandwidth product denoted as $A_o\omega_a$, A_o is the dc gain, and ω_a is the open-loop cutoff frequency. Usually ω_a is very small, for example, the popular bipolar opamp μA741, say $2\pi \times 10$ rad/s and $A_o = 100{,}000$ for a typical bipolar opamp, so that $B = 2\pi \times 10^6$ rad/s. Taking into account the finite bandwidth of the opamp, the gain of the inverting amplifier of Fig. 2.1a can be derived as

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DOI 10.1007/978-0-8176-8358-0_2,

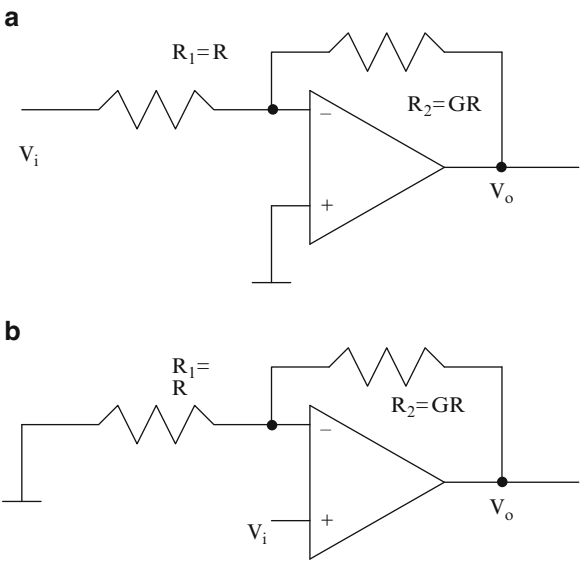


Fig. 2.1 (**a**) An inverting amplifier, and (**b**) a noninverting amplifier

$$\frac{V_o}{V_i} = -\frac{G}{1+\frac{(G+1)s}{B}} \tag{2.2}$$

where $G = R_2/R_1$. Thus, effectively, the cutoff frequency or bandwidth of the inverting amplifier is $B/(G + 1)$. In a similar manner, the gain of the noninverting amplifier of Fig. 2.1b can be derived as

$$\frac{V_o}{V_i} = \frac{(G+1)}{1+\frac{(G+1)s}{B}} \tag{2.3}$$

where $G = R_2/R_1$. Note that the cutoff frequency of a unity gain buffer (noninverting amplifier), that is, $G = 0$, is B whereas for an inverting amplifier of gain unity, the bandwidth is $B/2$ [2.15].

Considering the frequency response of the form (ignoring the frequency-independent gain factor),

$$A(s) = \frac{V_o}{V_i} = \frac{1}{1+as} \tag{2.4a}$$

where $a = 1/B$ and B is the unity gain bandwidth of the opamp, the gain and phase are given approximately for frequencies far smaller than the bandwidth B of the opamp as

$$A = \sqrt{(A(j\omega))^2} \cong 1 - \frac{a^2\ \omega^2}{2} \tag{2.4b}$$

$$\varphi \cong -a\,\omega \tag{2.4c}$$

The use of finite gain amplifiers in filters will lead to certain undesirable problems due to the introduced phase shift, which is considered in a later section.

To extend the frequency response (increase the bandwidth) of the amplifier, it is necessary to use passive or active compensation techniques [2.16]–[2.21]. In these, we effectively realize a transfer function of the form

$$A(s) = \frac{V_o}{V_i} = -\frac{K(1+as)}{1+as+b\,s^2} \tag{2.5}$$

where $a = \alpha/B$ and $b = \beta/B^2$. As a result, the gain and phase become

$$A = \sqrt{(A(j\omega))^2} \cong 1 + b\,\omega^2 \tag{2.6a}$$

$$\varphi \cong -ab\,\omega^3 \tag{2.6b}$$

Thus the phase response will have a third-order dependence on (ω/B) against first-order dependence for an uncompensated opamp given by (2.4c).

One method of *passive compensation* [2.16] is shown in Fig. 2.2a, wherein a capacitor C_c across the input resistor is used. The transfer function of this circuit can be obtained as

$$\frac{V_o}{V_i} = -\frac{R_2}{R_1}\,\frac{(1+s\,C_c\,R_1)}{1+\frac{s}{B}\left(1+\frac{R_2}{R_1}\right)+s^2\left(\frac{C_c\,R_2}{B}\right)} \tag{2.7}$$

Thus, under the condition $C_c\,R_1 = \frac{1}{B}\left(1+\frac{R_2}{R_1}\right)$, the first-order terms dependent on B will become equal, thus reducing the effect of finite bandwidth of the opamp on the amplifier frequency response.

Another technique, known as *active compensation*, uses another OA to compensate the effect of finite bandwidth of the opamp [2.18] and is shown in Fig. 2.2b. The pair of OAs together as shown within dotted lines is denoted as "composite OA." The transfer function of this circuit is given by

$$\frac{V_o}{V_i} = -\frac{R_2}{R_1}\,\frac{\left(1+\frac{s}{B_2}\right)}{1+\frac{s}{B_2}+\frac{s^2}{B_1\,B_2}\left(1+\frac{R_2}{R_1}\right)} \tag{2.8}$$

Thus, without needing any matching of bandwidths of the opamps, the circuit realizes active compensation. In the case of a unity gain buffer [2.17], the circuit of Fig. 2.2c has the gain given by

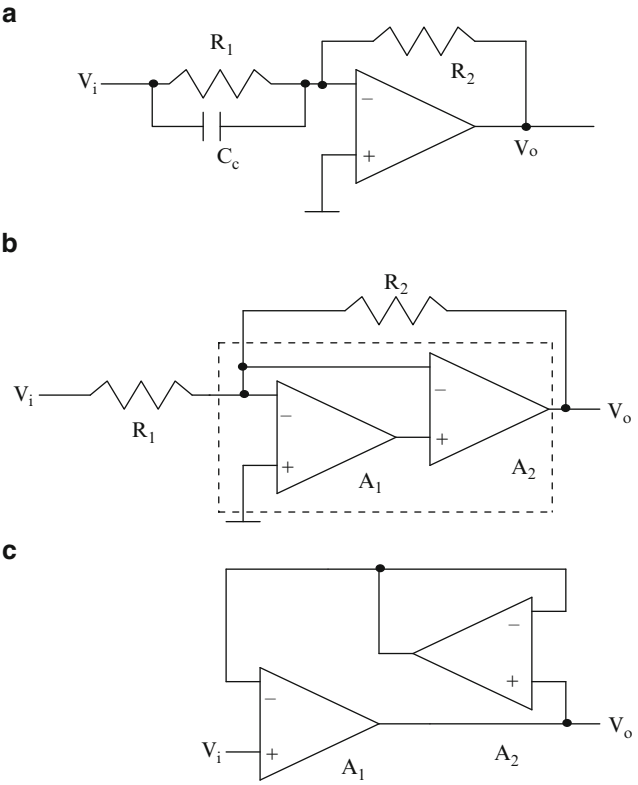


Fig. 2.2 Improved inverting amplifiers (**a**) using passive compensation, (**b**) using active compensation, and (**c**) improved buffer ((c) Adapted from [2.17] ©IEEE 1979)

$$\frac{V_o}{V_i} = \frac{\left(1 + \frac{s}{B_2}\right)}{1 + \frac{s}{B_1} + \frac{s^2}{B_1 B_2}} \tag{2.9}$$

Note that matching of OA bandwidths is needed to achieve exact compensation.

Example 2.1 Using WINSPICE, evaluate the frequency response of the actively compensated inverting amplifier for gain 10 of Fig. E.2.1. Use the opamp macromodel with opamp finite dc gain 100,000 and bandwidth 1 MHz. Compare the results with the uncompensated amplifier of Fig. 2.1a.

The SPICE code is listed below. Note that the opamp is modeled as a controlled voltage source with gain 100,000 using dependent voltage source E1 and the finite bandwidth is modeled by a first-order RC network (using R7, C2) with a pole-frequency of 1 MHz. The bandwidth expansion can be observed. Note that peaking can occur in the resultant composite amplifier frequency response.

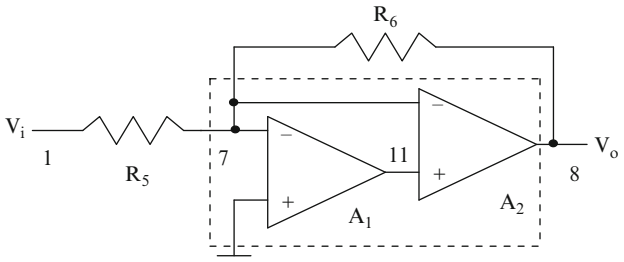


Fig. E.2.1

```
*Nonideal composite inverting amplifier
Vin1 1 0 ac 1 v
R5 1 7 1 k
R6 7 8 10 k
E1 0 9 7 0 100,000
R7 9 10 1 k
C2 10 0 15.9 uf
E2 11 0 10 0 1
E3 0 12 7 11 100,000
R8 12 13 1 k
C3 13 0 15.9 uf
E4 8 0 13 0 1
*Nonideal Inverting amplifier
R1 1 2 1 K
R2 2 6 10 k
E5 0 4 2 0 100,000
R3 4 5 1 k
C1 5 0 15.9 uf
E6 6 0 5 0 1
.ac dec 10 1 100,000 K
```

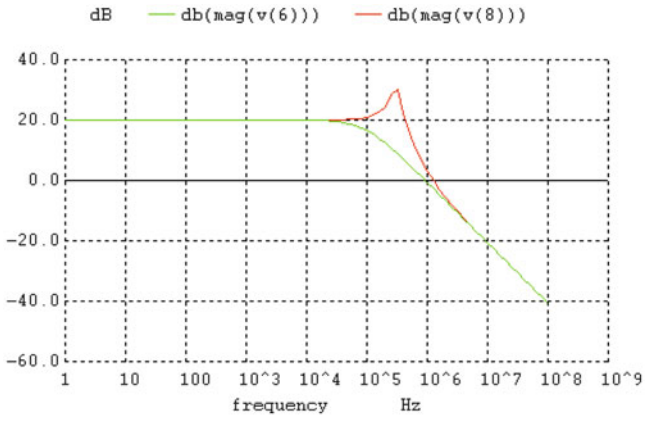
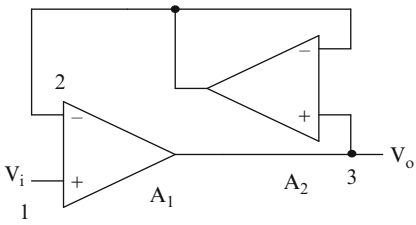


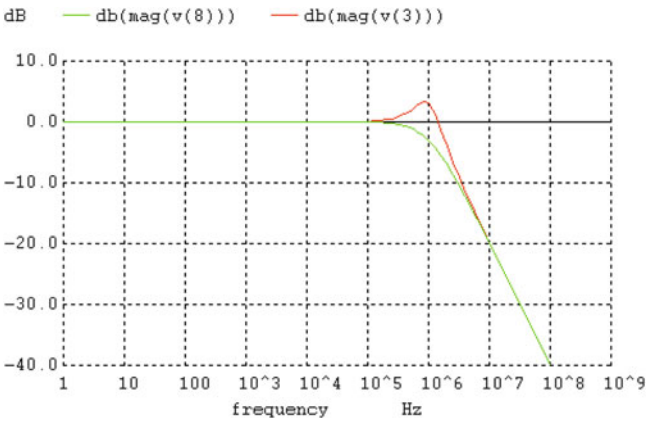
Fig. E.2.2



Example 2.2 Using WINSPICE, evaluate the frequency response of the actively compensated buffer amplifier of Fig. E.2.2. Use the opamp macro model with opamp finite dc gain 100,000 and bandwidth 1 MHz.

The SPICE listing is given below. The bandwidth enhancement can be seen clearly.

```
*Nonideal composite noninverting buffer amplifier
Vin1 1 0 ac 1 v
E1 4 0 1 2 100,000
R1 4 5 1 k
C1 5 0 15.9 uf
E2 3 0 5 0 1
E3 6 0 3 2 100,000
R3 6 7 1 k
C2 7 0 15.9 uf
E4 2 0 7 0 1
E5 9 0 1 8 100,000
R4 9 10 1 K
C3 10 0 15.9uF
E6 8 0 10 0 1
.ac dec 10 1 100,000 K
```



Another interesting active compensation scheme was suggested by Boutin [2.19], which uses a negative impedance converter (NIC). This circuit, presented in Fig. 2.3a, has the transfer function given by

$$\frac{V_o}{V_i} = -\frac{R_2}{R_1}\left(\frac{1}{1+\frac{s}{B}\left(1+\frac{R_2}{R_1}-\frac{R_2}{R_N}\right)}\right) \tag{2.10}$$

Evidently, under the condition $\frac{1}{R_1}+\frac{1}{R_2}=\frac{1}{R_N}$, the gain will be frequency independent. Note, however, that we need an ideal negative resistance, which is not possible in practice.

Two circuits for obtaining negative resistance are presented in Fig. 2.3b, c. Note that in both these circuits, a resistance R is placed between V_i and $2V_i$, thus effectively making a current $(V_i - 2V_i)/R = -V_i/R = V_i/(-R)$ to flow simulating a negative resistance. Since the opamp is nonideal, these two circuits realize a nonideal negative resistance.

The use of the negative resistance [2.20] of Fig. 2.3b in the circuit of Fig. 2.3a in place of $-R_N$ yields the circuit of Fig. 2.3d, whose transfer function is given by

$$\frac{V_o}{V_i} = -\frac{R_2}{R_1}\left(\frac{1+\frac{2s}{B_2}}{1+s\left(\frac{2}{B_2}-\frac{1}{B_1}\left(\frac{R_2}{R_1}+1-\frac{R_2}{R_3}\right)\right)+\frac{2s^2}{B_1 B_2}\left(\frac{R_2}{R_1}+1-\frac{R_2}{R_3}\right)}\right) \tag{2.11}$$

Under the condition $\frac{1}{R_1}+\frac{1}{R_2}=\frac{1}{R_3}$, the first-order terms become equal, thus achieving compensation.

Example 2.3 Analyze using SPICE the compensated amplifier using NIC shown in Fig. E.2.3.

Note that $R_3 = -R_1R_2/(R_1 + R_2)$ is chosen for exact compensation. The uncompensated amplifier response is also presented to illustrate the bandwidth enhancement.

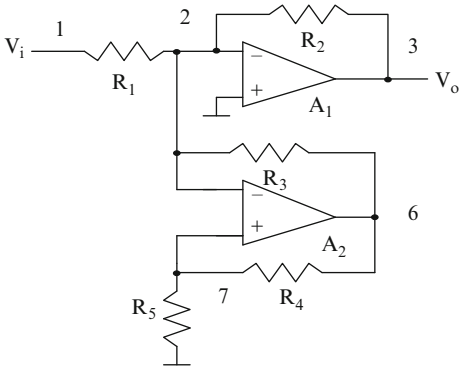


Fig. E.2.3

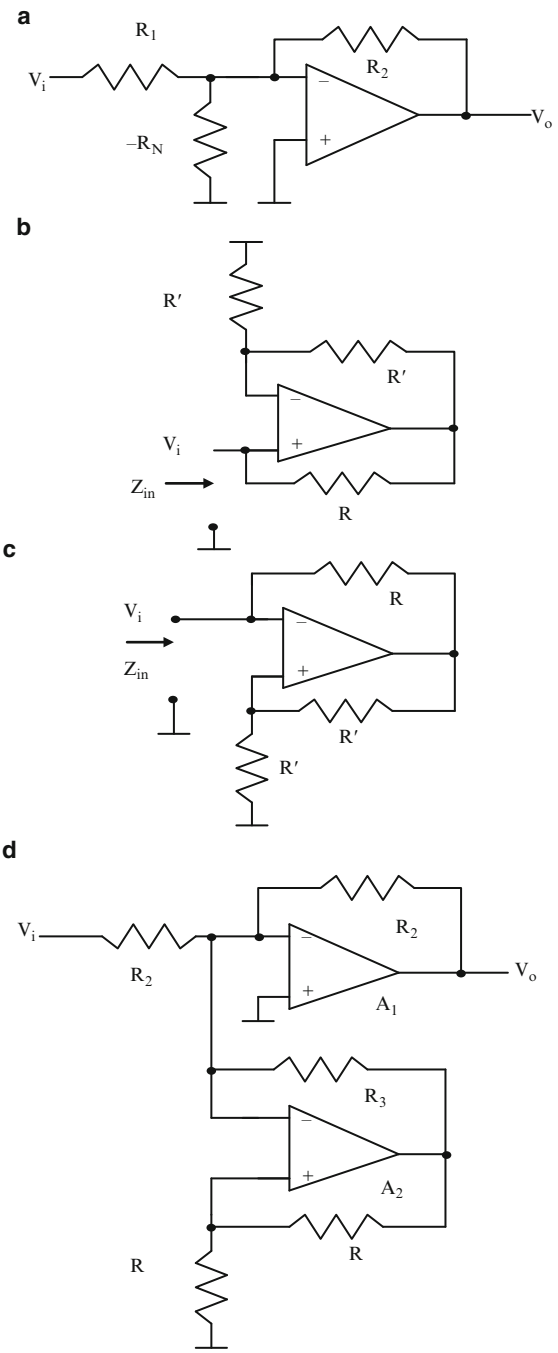
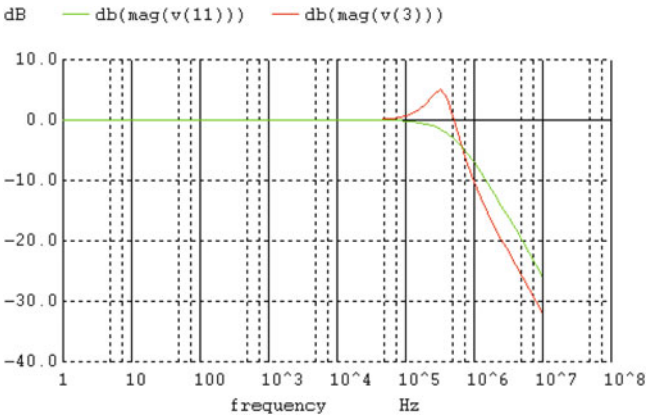


Fig. 2.3 (**a**) Boutin's active compensation scheme of amplifier using NIC, (**b**) and (**c**) circuits for NIC realization, and (**d**) complete circuit following (a) and (b) ((a) Adapted from [2.19] ©IEE 1981, (d) Adapted from [2.20] ©AEU 1988)

```
*Amplifier using NIC compensation
R1 1 2 1 K
R2 2 3 1 K
R3 2 6 500
R4 6 7 1 k
R5 7 0 1 K
E1 0 4 2 0 100,000
R6 4 5 1 k
C1 5 0 15.9 uf
E2 3 0 5 0 1
E3 8 0 2 7 100,000
R7 8 9 1 K
C2 9 0 15.9 uf
E4 6 0 9 0 1
*Normal amplifier
R8 1 10 1 K
R9 10 11 1 K
E5 0 12 10 0 100,000
R10 12 13 1 k
C3 13 0 15.9 uf
E6 11 0 13 0 1
vin 1 0 ac 1 V
.ac dec 10 1 100,00 K
```



2.2 Integrators Using Opamps

An inverting integrator using an opamp is shown in Fig. 2.4a. In the case of an opamp with infinite bandwidth, the transfer function realized is

$$\frac{V_o}{V_i} = -\frac{1}{sCR} \tag{2.12a}$$

The transfer function of the integrator taking into account the model of (2.1) is given by

$$\frac{V_o}{V_i} = -\frac{1}{sCR\left(1+\frac{1}{BCR}+\frac{s}{B}\right)} \tag{2.12b}$$

Thus, a real pole is created because of the finite bandwidth of the OA. Expressing the integrator transfer function as

$$\frac{V_o}{V_i} = -\frac{1}{R(j\omega)+jX(j\omega)} \tag{2.13a}$$

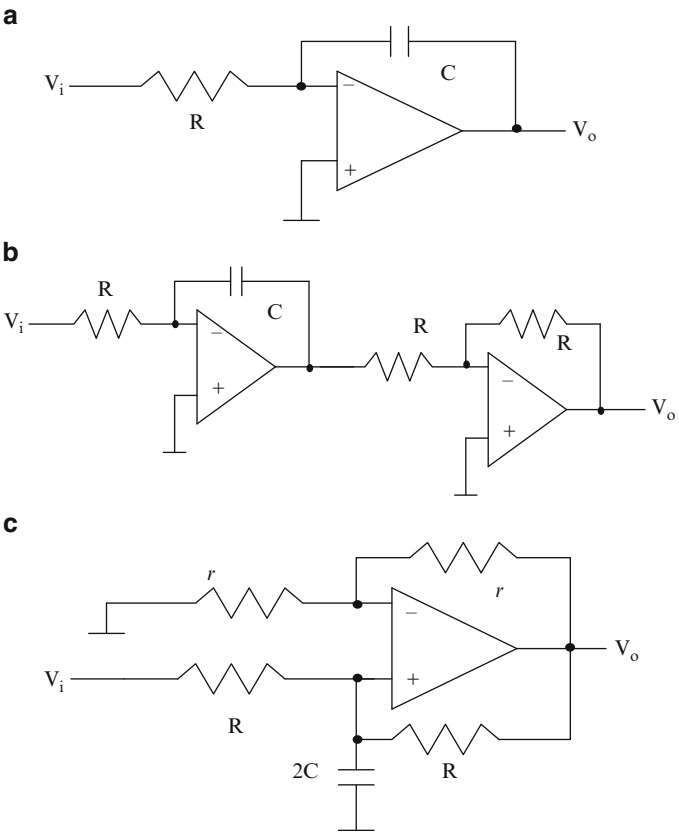


Fig. 2.4 (**a**) An inverting integrator (**b**) a non-inverting integrator and (**c**) Deboo's non-inverting integrator, Actively compensated integrators: (**d**) Akerberg–Mossberg scheme [2.24], (**e–g**) Brackett and Sedra schemes [2.21] and (**h**) Ravichandran and Rao [2.18] (**b–d**),(**f**),(**g**) Adapted from [2.21] ©IEEE 1976)

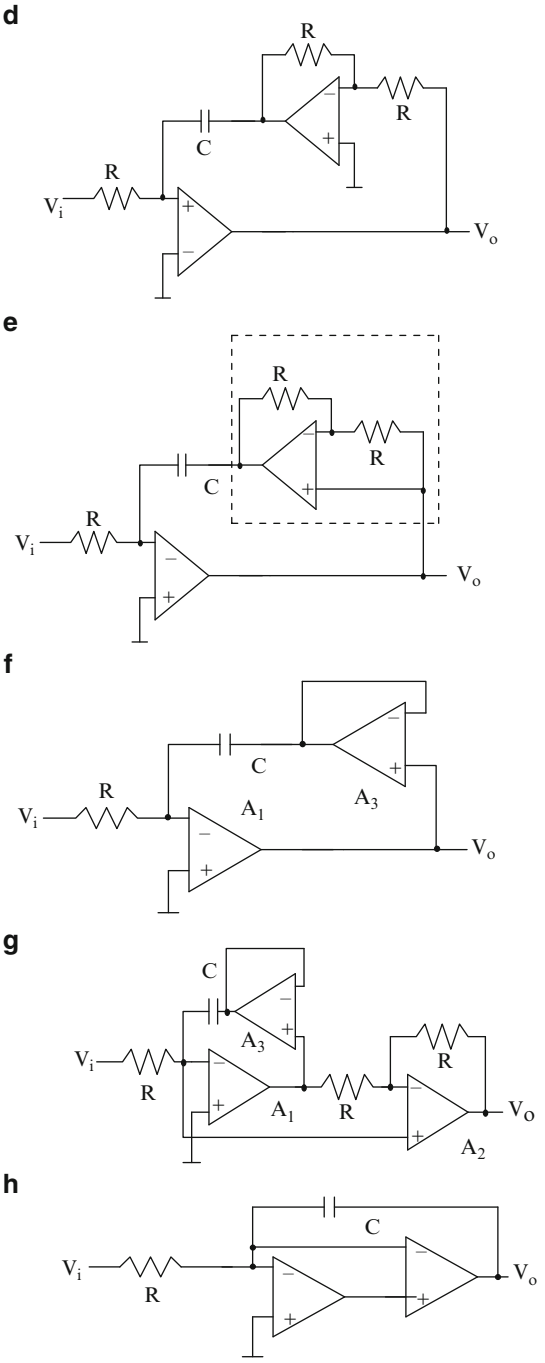


Fig. 2.4 (continued)

its Q-factor [2.21] can be defined as

$$Q_{integ} = \frac{X(j\omega)}{R(j\omega)} \tag{2.13b}$$

Thus, for the integrator of Fig. 2.4a, using (2.12b) and (2.13b) we obtain the Q-factor as

$$Q_{integ} = -\left(\frac{B}{\omega} + \frac{1}{\omega CR}\right) \tag{2.14}$$

A noninverting integrator can be obtained by cascading an inverting integrator with a unity gain inverting amplifier [2.21] as shown in Fig. 2.4b. The transfer function of this integrator, taking into account the nonideal opamp, is given by

$$\frac{V_o}{V_i} = \frac{1}{\left(sCR + \frac{s}{B} + \frac{s^2 CR}{B}\right)\left(1 + \frac{2s}{B}\right)} \tag{2.15a}$$

The Q-factor for this integrator can be obtained using (2.13b) as

$$Q_{integ} = -\left(\frac{BCR + 1 - \frac{2\omega^2 CR}{B}}{3\omega CR + \frac{2\omega}{B}}\right) \cong -\frac{B}{3\omega} \tag{2.15b}$$

Evidently, the Q-factor is lower than that of the inverting integrator given by (2.14).

Since the noninverting integrator of Fig. 2.4b needs two opamps, a single amplifier-based integrator has been suggested by Deboo [2.22] (shown in Fig. 2.4c). The transfer function of this integrator is given by

$$\frac{V_o}{V_i} = \frac{1}{sCR + \frac{2s}{B} + \frac{2s^2 CR}{B}} \tag{2.16a}$$

The resulting Q-factor can be derived as

$$Q_{integ} = -\left(\frac{BCR + 2}{2\omega CR}\right) \cong -\frac{B}{2\omega} \tag{2.16b}$$

Note that the Deboo integrator uses a negative resistance formed by resistors R', r, and r and opamp A_1 (see Fig. 2.3b). Its Q-factor is less than that of the inverting integrator but more than the two-amplifier based noninverting integrator of Fig. 2.4b.

The Q-factor of the noninverting integrator can be made equal to that of the inverting integrator by using an ingenious integrator described by Akerberg and

Mossberg [2.24] and shown in Fig. 2.4d. The transfer function of this integrator can be derived as

$$\frac{V_o}{V_i} = \frac{\left(1+\frac{2s}{B}\right)}{\frac{2s^3CR}{B^2} + s^2\left(\frac{2}{B^2}+\frac{CR}{B}\right) + s\left(\frac{1}{B}+CR\right)} \tag{2.17a}$$

The resulting Q-factor is given as

$$Q_{integ} = -\left(\frac{\frac{B}{\omega}+\frac{1}{\omega CR}+\frac{4\omega}{CRB^2}}{1-\frac{4\omega^2}{B^2}}\right) \cong \frac{B}{\omega} \tag{2.17b}$$

Another actively compensated integrator [2.21] is shown in Fig. 2.4e, which realizes the same transfer function as that of Fig. 2.4d. Note that the block within dotted lines has a gain $\frac{1}{1+\frac{2s}{B_2}}$ and the opamp A_1 is an inverting amplifier, whereas in the circuit of Fig. 2.4d, the opamp A_1 is a noninverting amplifier and A_2 and resistor R realize a gain $\frac{-1}{1+\frac{2s}{B_2}}$. Thus, the circuit is the same except for the sign of the integrator transfer function.

Active compensation also can be achieved using a buffer amplifier [2.21] as shown in Fig. 2.4f. The transfer function of this circuit can be derived as

$$\frac{V_o}{V_i} = \frac{-\left(1+\frac{s}{B_3}\right)}{sCR\left(1+\frac{1}{CRB_1}+\frac{s}{B_1}\left(1+\frac{1}{CRB_3}\right)+\frac{s^2}{B_1B_3}\right)} \tag{2.18}$$

A noninverting integrator can be obtained with the same integrator Q-factor by augmenting the compensated inverting integrator of Fig. 2.4f using an additional opamp and two resistors, as shown in Fig. 2.4g. The transfer function of this circuit [2.21] is given as

$$\frac{V_o}{V_i} = \frac{\left(1+\frac{s}{B_3}\right)}{sCR\left(1+\frac{1}{CRB_1}+\frac{s}{B_1}\left(1+\frac{1}{CRB_3}\right)+\frac{s^2}{B_1B_3}\right)} \frac{\left(1+\frac{2s}{B_1}\right)}{\left(1+\frac{2s}{B_2}\right)} \tag{2.19}$$

It can be seen that when $B_1 = B_2$, the second fraction will become unity, thus realizing the same transfer function as an inverting integrator except for the sign.

We next consider another actively compensated integrator [2.18] shown in Fig. 2.4h that does not need any additional passive components. The transfer function of this integrator can be derived as

$$\frac{V_o}{V_i} = \frac{-\left(1+\frac{s}{B_2}\right)}{\frac{s^3CR}{B_1B_2}+\frac{s^2}{B_1B_2}(1+B_1CR)+sCR} \tag{2.20a}$$

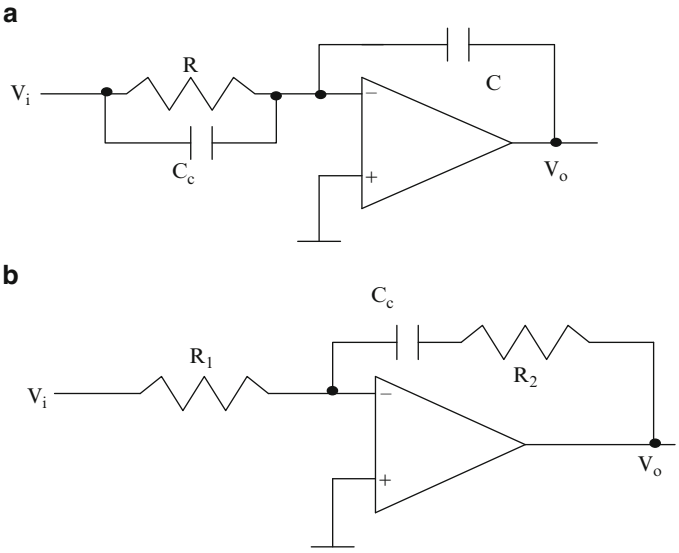


Fig. 2.5 (**a**, **b**) Passive compensation of inverting integrators

The resulting Q-factor (assuming $B_1 = B_2 = B$) is given as

$$Q_{integ} = -\left(\frac{B^3 + \frac{\omega^2}{CR}}{\omega^3 + \frac{B\omega}{CR}}\right) = -\left(\frac{\frac{B^3}{\omega^3} + \frac{\omega_o}{\omega}}{1 + \frac{B\omega_o}{\omega^2}}\right) \tag{2.20b}$$

For $\omega_o = 1/CR = \omega$,

$$Q_{integ} = -\left(\frac{\frac{B^3}{\omega^3} + 1}{1 + \frac{B}{\omega}}\right) \cong -\frac{B^2}{\omega^2} \tag{2.20c}$$

which is much larger than B/ω of an uncompensated integrator.

An integrator can be compensated by adding a small capacitance C_c across the input feeding resistance R [2.23] as shown in Fig. 2.5a. The transfer function of this circuit can be obtained as

$$\frac{V_o}{V_i} = \frac{-(1 + s\,C_c R)}{sCR\left(1 + \frac{s}{B}\left(1 + \frac{C_c}{C}\right) + \frac{1}{BCR}\right)} \tag{2.21a}$$

Evidently, under the condition

$$C_c = \frac{C}{BCR - 1} \cong \frac{1}{BR} \tag{2.21b}$$

compensation is achieved.

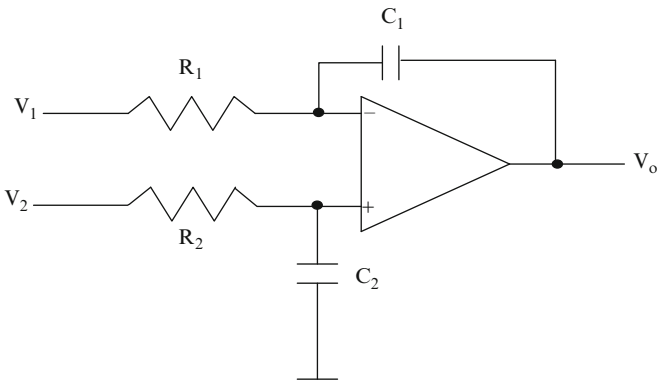


Fig. 2.6 A differential integrator

In another technique [2.25] shown in Fig. 2.5b, an integrator has been shown to be compensated using an additional series resistance with the integrating capacitor. In this technique, the transfer function can be obtained as

$$\frac{V_o}{V_i} = -\frac{1}{sCR_1}\left(\frac{(1+sCR_2)}{1+\frac{1}{BCR_1}+\frac{s}{B}\left(1+\frac{R_2}{R_1}\right)}\right) \tag{2.22}$$

It can be seen that under the condition $BCR_2 = \left(1+\frac{R_2}{R_1}\right)$, the s-terms in the numerator and denominator are equal thus achieving first-order cancellation of the effect of the finite bandwidth on the amplifier.

A differential integrator is shown in Fig. 2.6 whose transfer function considering an ideal opamp is given by

$$V_o = \frac{-V_1\,(1+s\,C_2\,R_2)+V_2\,(1+s\,C_1\,R_1)}{s\,C_1\,R_1\,(1+s\,C_2\,R_2)} \tag{2.23}$$

Thus, a differential integrator is obtained when $C_1R_1 = C_2R_2$, that is, the two time constants shall match.

2.3 First-Order Filters Using Opamps

2.3.1 Low-Pass Filters

A first-order low-pass filter can be obtained by damping the integrator capacitor in the integrators described earlier as shown in Fig. 2.7a. The transfer function of this circuit is given by

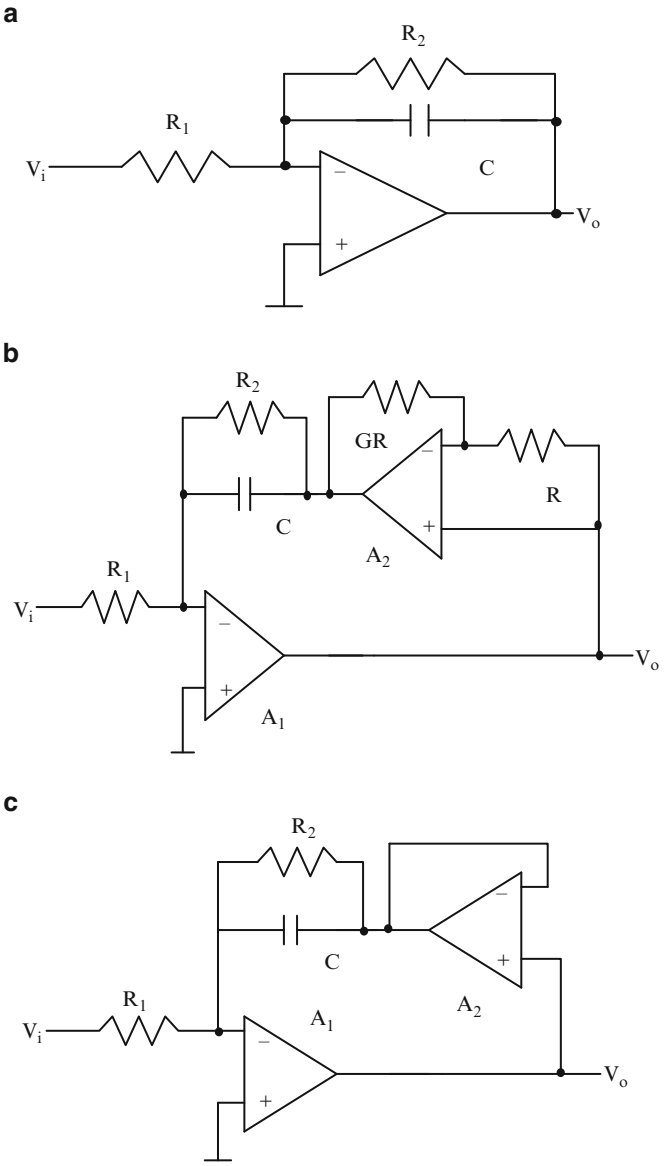


Fig. 2.7 (**a**) A first-order low-pass filter, (**b**) and (**c**) actively compensated first-order low-pass filters

$$\frac{V_o}{V_i} = -\frac{R_2}{R_1}\left(\frac{1}{1 + s\left(C R_2 + \frac{1}{B}\left(1 + \frac{R_2}{R_1}\right)\right) + s^2\left(\frac{C R_2}{B}\right)}\right) \tag{2.24}$$

showing that two real poles exist. The circuit can be compensated using another OA with two resistors as shown in Fig. 2.7b. The resulting transfer function can be shown to be

$$\frac{V_o}{V_i} = -G\left(\frac{1 + \frac{(G+1)s}{B_2}}{1 + s\left(C R_2 + \frac{G+1}{B_1}\right) + s^2\left(\frac{(G+1)^2}{B_1 B_2} + \frac{C R_2}{B_1}\right) + \frac{s^3 C R_2 (G+1)}{B_1 B_2}}\right) \tag{2.25}$$

where $G = R_2/R_1$. Note that the first-order term $s(G + 1)/B$ in the numerator and denominator (assuming $B_1 = B_2 = B$) will compensate the lossy integrator.

An alternative compensated lossy integrator is shown in Fig. 2.7c whose transfer function is given by

$$\frac{V_o}{V_i} = -G\left(\frac{1 + \frac{s}{B_2}}{1 + s\left(C R_2 + \frac{G+1}{B_1}\right) + s^2\left(\frac{(G+1)}{B_1 B_2} + \frac{C R_2}{B_1}\right) + \frac{s^3 C R_2}{B_1 B_2}}\right) \tag{2.26}$$

2.3.2 *First-Order All-Pass Filters*

We next consider the realization of first-order all-pass filters [2.26] which is possible using the two circuits of Fig. 2.8a, b. The transfer functions of these circuits are, respectively, as follows.

$$\frac{V_o}{V_i} = \frac{(1 - sCR)}{(1 + sCR)\left(1 + \frac{2s}{B}\right)} \tag{2.27a}$$

and

$$\frac{V_o}{V_i} = -\frac{(1 - sCR)}{(1 + sCR)\left(1 + \frac{2s}{B}\right)} \tag{2.27b}$$

2.4 Sallen–Key Active RC Low-Pass Filter

Consider the Sallen–Key active RC filter [2.27] of Fig. 2.9a. We use this as a vehicle to explain the design concepts. Consider that the opamp has finite gain A. Then, the following equations can be easily written at the nodes 1, 2, and 3,

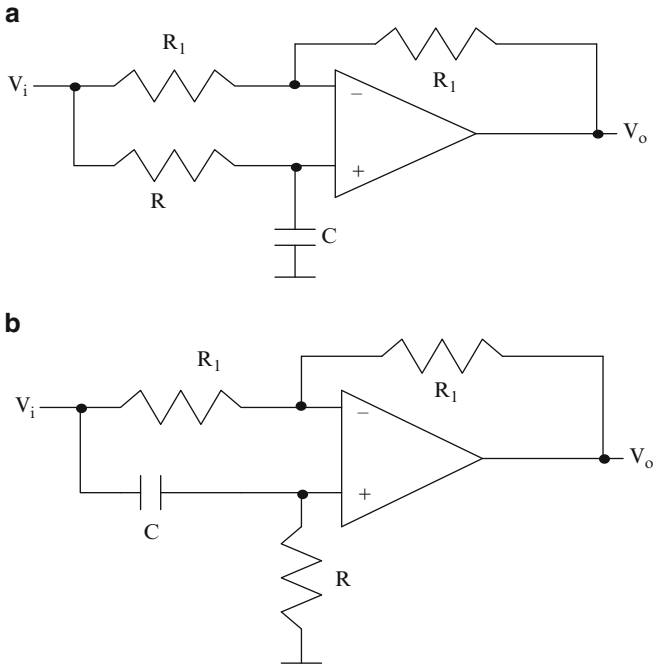


Fig. 2.8 (**a**, **b**) First-order all-pass filters using one opamp

$$\frac{V_i - V_1}{R_1} + \frac{V_2 - V_1}{R_2} + (V_0 - V_1)sC_1 = 0 \tag{2.28a}$$

$$\frac{V_1 - V_2}{R_2} = V_2\, s\, C_2 \tag{2.28b}$$

$$\left(V_2 - \frac{V_0}{K}\right)A = V_0 \tag{2.28c}$$

where A is the gain of the opamp. Solving these equations, we obtain the transfer function of the filter as

$$\frac{V_o}{V_i} = \frac{K}{s^2 C_1 C_2 R_1 R_2 \left(1+\frac{K}{A}\right) + s\left((C_1 R_1 + C_2 (R_1 + R_2))\left(1+\frac{K}{A}\right) - K C_1 R_1\right) + \left(1+\frac{K}{A}\right)} \tag{2.29a}$$

Note that in the case where we consider an ideal opamp (i.e., $A = \infty$), the transfer function of (2.29a) is simplified as

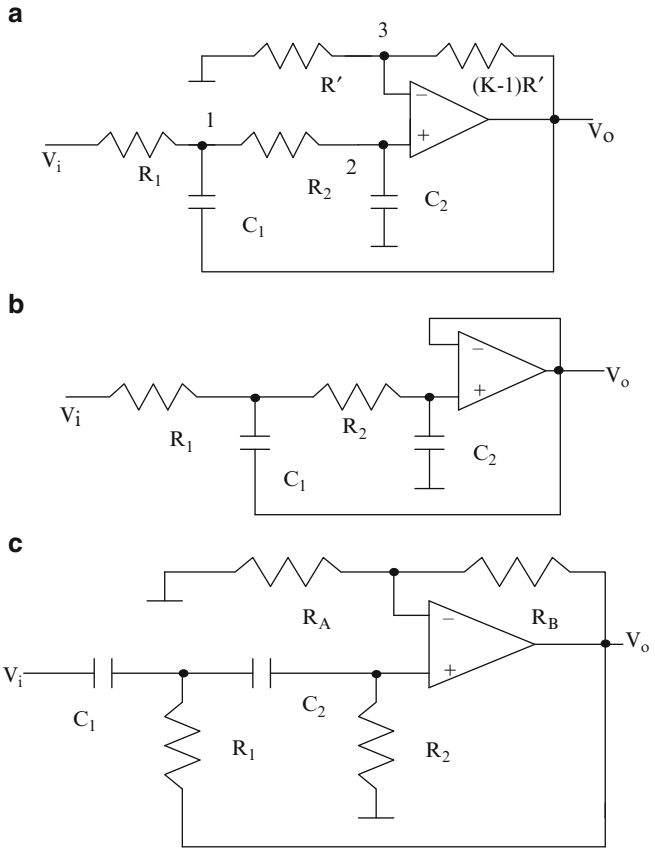


Fig. 2.9 (**a**) Sallen–Key active RC low-pass filter using amplifier gain K, (**b**) with $K = 1$ using a buffer, and (**c**) Sallen–Key high-pass filter using a noninverting amplifier of gain K

$$\frac{V_o}{V_i} = \frac{K}{s^2\ C_1\ C_2\ R_1\ R_2 + s(C_1\ R_1 + C_2\ (R_1 + R_2) - K\ C_1\ R_1) + 1} \tag{2.29b}$$

The next step is to match the transfer function with the desired second-order low-pass transfer function. Since the s-term and s^2 term in the numerator are zero, the transfer function is a low-pass type. The denominator of the transfer function can be compared with the standard second-order denominator

$$D(s) = s^2 + s\left(\frac{\omega_o}{Q_p}\right) + {\omega_p}^2 \tag{2.30a}$$

to obtain the pole-frequency and pole-Q as follows.

$$\omega_p = \frac{1}{\sqrt{C_1\ C_2\ R_1\ R_2}} \tag{2.30b}$$

and

$$Q_p = \frac{\sqrt{C_1\ C_2\ R_1\ R_2}}{(C_1\ R_1 + C_2\,(R_1 + R_2) - K\,C_1\ R_1)} \tag{2.30c}$$

There are many component choices possible. However, two popular choices are (a) using equal resistors ($R_1 = R_2 = R$) and equal capacitors ($C_1 = C_2 = C$) and $K > 1$; (b) $K = 1$ (see Fig. 2.9b) using unequal resistors and capacitors.

In choice (a), the expressions for pole-frequency and pole-Q simplify as

$$\omega_p = \frac{1}{RC} \text{ and } Q_p = \frac{1}{3 - K} \tag{2.31}$$

For choice (b), the corresponding expression for pole-frequency is given by (2.30b) and the expression for pole-Q is

$$Q_p = \sqrt{\frac{C_1}{C_2}}\frac{\sqrt{R_1\ R_2}}{(R_1 + R_2)} \tag{2.32a}$$

It can be seen from (2.32a) that the spread in capacitor values can be minimized when $R_1 = R_2$:

$$\frac{C_1}{C_2} = 4\,Q_p^2 \tag{2.32b}$$

which can be quite large for large Q_p values.

It is thus easily possible to design the circuit for a given pole-frequency and pole-Q Q_p. Note that the dc gain in both cases can be obtained by substituting $s = j\omega = 0$ in (2.29b). There is no degree of freedom to control the dc (low-frequency) gain. On the other hand, in choice (a), the pole-Q is independently controlled by K. The property of independent control of pole-frequency, pole-Q, and gain is known as *orthogonal tunability*.

2.4.1 *Effect of Finite Gain of the Opamp*

Next, let us consider the effect of opamp finite dc gain. Evidently, by matching denominator coefficients of the denominator of (2.29a) with (2.30a), the pole-frequency is seen to be independent of the finite gain of the opamp. However, the pole-Q is dependent on A as follows.

$$Q_p = \frac{\left(1+\frac{K}{A}\right)\sqrt{C_1\ R_1\ C_2\ R_2}}{\left((C_1\ R_1 + C_2\ (R_1+R_2)\right)\left(1+\frac{K}{A}\right) - K\,C_1\ R_1)} \tag{2.33}$$

Evidently, for large gain of the opamp, the sensitivity to A becomes zero as A tends to the limit ∞.

2.4.2 *Effect of Finite Bandwidth of the Opamp*

On the other hand, let us investigate the effect of finite bandwidth of the opamp. For this purpose, we need to employ the single-pole model of the opamp. Note that the opamp is usually designed to be a three-pole system [2.28] and has a dominant pole which is at very low frequencies, and has second and third poles at very large frequencies. The dominant pole is intentionally created by connecting a compensation capacitor inside the opamp circuitry by the opamp designer. Such an approach ensures stability of the opamp when 100% negative feedback is used, for example, when the opamp is connected as a buffer.

From (2.29a), using the model of (2.1), we obtain the denominator of the transfer function as a third-degree expression:

$$D(s) = \left(s^3\ \frac{C_1\ C_2\ R_1\ R_2\,K}{B} + s^2\left(C_1\ C_2\ R_1\ R_2 + \frac{K}{B}\left(C_1\ R_1 + C_2\ (R_1+R_2)\right)\right)\right.$$
$$\left. + s\left(C_1\ R_1 + C_2\ (R_1+R_2) - K\,C_1\ R_1 + \frac{K}{B}\right) + 1\right) \tag{2.34}$$

Evidently, a parasitic real pole is created and the original (ideal) pole-frequency and pole-Q would have changed. It is therefore necessary to find out the deviation in pole-frequency and pole-Q of the active filter due to the opamp finite bandwidth. The cubic equation can be solved to find the roots and from that information, the real pole, pole-frequency, and pole-Q corresponding to the complex pole pair can be estimated. However, most often, designers need to have a quick assessment of the expected deviations.

For this purpose, an approximation suggested by Akerberg and Mossberg [2.24] can be used. In this, the s^3 term is written as $-s{\omega_p}^2$ so that the third-order system becomes a second-order system. From this, the modified pole-frequency and pole-Q can be found following the conventional definitions. Note, however, that this is true for high pole-Qs. For low pole-Qs, one can find them by exactly solving the cubic equation. Using the Akerberg–Mossberg approximation, we have from (2.34), the approximated denominator of the transfer function as

$$\begin{aligned} \mathrm{D}'(\mathrm{s}) = s^2 \left(C_1\ C_2\ R_1\ R_2 + \frac{K}{B}(C_1\ R_1 + C_2\ (R_1 + R_2)) \right) \\ + s\,(C_1\ R_1 + C_2\,(R_1 + R_2) - K\,C_1\ R_1) + 1 \end{aligned} \tag{2.35}$$

Thus, the shifted pole-frequency $\hat{\omega}_p$ and shifted pole-Q $\hat{Q}_p$ can be seen by identifying (2.35) with

$$s^2 \left(\frac{1}{\hat{\omega}_p^2} \right) + s \left(\frac{1}{\hat{\omega}_p\, \hat{Q}_p} \right) + 1$$

as

$$\frac{\omega_p^2}{\hat{\omega}_p^2} = 1 + \frac{K}{B}(C_1\ R_1 + C_2\,(R_1 + R_2))\,\omega_p^2 \tag{2.36}$$

and

$$\frac{1}{\hat{\omega}_p\ \hat{Q}_p} = \frac{1}{\omega_p\ Q_p} \tag{2.37}$$

Evidently, from (2.36), we can observe that the pole-frequency $\hat{\omega}_p$ decreases due to opamp finite bandwidth and we note also from (2.37) that the pole-Q $\hat{Q}_p$ increases by a similar amount. As an illustration for case (b), $K = 1$, we have

$$\frac{\omega_p^2}{\hat{\omega}_p^2} = 1 + \left(2\,Q_p + \frac{1}{Q_p} \right) \frac{\omega_p}{B} \tag{2.38a}$$

and for case (a), $K \neq 1$,

$$\frac{\omega_p^2}{\hat{\omega}_p^2} = 1 + 3 \left(3 - \frac{1}{Q_p} \right) \frac{\omega_p}{B} \tag{2.38b}$$

Note that several solutions have been suggested to get rid of the problem of opamp finite bandwidth by (a) *predistortion*, (b) *passive compensation* of opamp, and (c) *active compensation* of opamp. However, these need either extra passive or active components or the performance of the compensated filters varies with power supply voltage and temperature. The predistortion technique is based on (2.38a) and considers the design of the circuit with lower pole-Q and higher pole-frequency than desired.

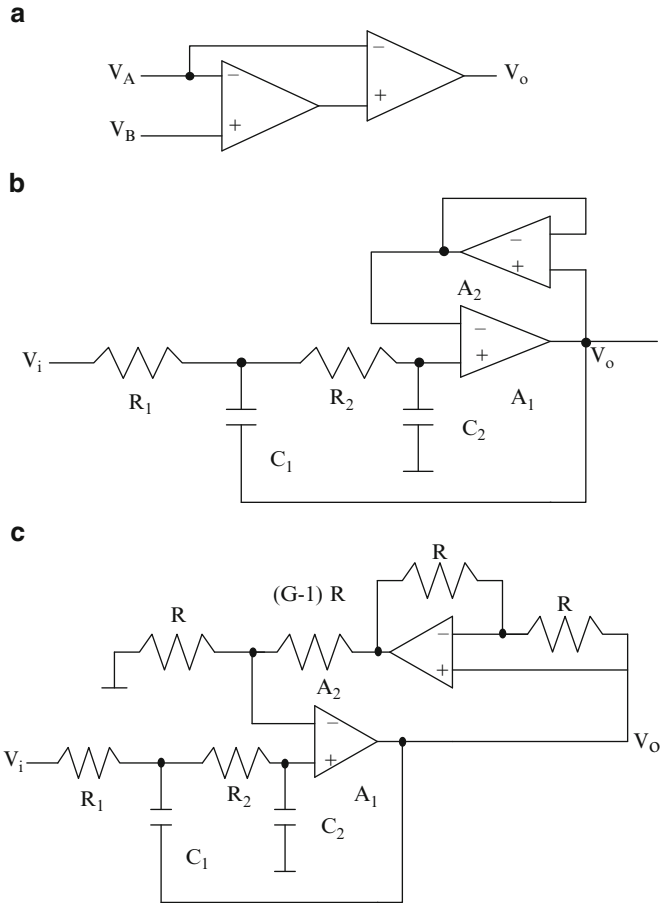


Fig. 2.10 (**a**) A composite opamp, (**b**) Sallen–Key filter with $K = 1$ using composite opamp-based buffer, and (**c**) Sallen–Key filter using composite opamp for $K \neq 1$

2.4.3 Active Compensation of Sallen–Key Filter with K = 1

The Sallen–Key filter using the composite opamp of Fig. 2.10a to realize a unity gain buffer is shown in Fig. 2.10b. The transfer function of the buffer stage using composite opamps is given by (2.9). The denominator of the transfer function of the actively compensated Sallen–Key filter of Fig. 2.10b is given by

$$D(s) = s^4\left(\frac{C_1\,C_2\,R_1\,R_2}{B^2}\right) + s^3\left(\frac{C_1\,C_2\,R_1\,R_2}{B} + \frac{C_1\,R_1 + C_2\,R_1 + C_2\,R_2}{B^2}\right)$$
$$+ s^2\left(\frac{1}{B^2} + \frac{C_2\,R_1 + C_2\,R_2}{B} + C_1\,C_2\,R_1\,R_2\right) + s\left(\frac{1}{B} + C_2\,R_1 + C_2\,R_2) + 1\right) \tag{2.39}$$

Using Akerberg–Mossberg approximation, it can be shown that the modified pole-frequency is given as

$$\frac{\omega_p^2}{\widehat{\omega}_p^2} = 1 + \frac{\omega_p}{Q_p B} \tag{2.40}$$

which may be compared with (2.38a) to note the significant improvement.

A noninverting amplifier needed in the Sallen–Key filter can also be actively compensated using the circuit shown in Fig. 2.10c within dotted lines which needs an additional OA and two resistors. The transfer function of this block is

$$H(s) = \frac{G\left(1 + \frac{sG}{B_2}\right)}{1 + \frac{Gs}{B_1} + \frac{G^2 s^2}{B_1 B_2}} \tag{2.41}$$

Under the matching condition $B_1 = B_2$, this composite amplifier also realizes a third-order dependence of phase but much larger than that of a buffer due to the G^3 term. The reader is urged to study the effect of using this compensated Sallen–Key filter.

2.4.4 Sensitivity Analysis

The active and passive components used in filters typically have large tolerances due to manufacturing processes. The effect of these variations on the pole-frequency and pole-Q from the nominal design values of the filters needs to be analyzed. This can be carried out through sensitivity analysis. The sensitivity of a filter parameter such as transfer function magnitude H to a component x_i is defined as

$$S_{x_i}^H = \frac{\partial H}{\partial x_i} \cdot \frac{x_i}{H} = \frac{\partial H}{H} \Big/ \frac{\partial x_i}{x_i} = \frac{\%\ change\ in\ H}{\%\ change\ in\ x_i} \tag{2.42}$$

In other words, we would like to know the percentage change in H for a given change of 1% in component value. Generally, the sensitivity should be small and closer to unity. Note that the sensitivity can be positive or negative, meaning that H may increase due to the 1% increase in component value or may decrease.

The computation of sensitivity can be easily done by noting some tricks. As an illustration, consider the following expression for pole-frequency of a typical active RC filter,

$$\omega_o = \frac{1}{\sqrt{R_1\ R_2\ C_1\ C_2}} \tag{2.43}$$

The following can be easily written,

$$S_{R_1}^{\omega_o} = S_{R_2}^{\omega_o} = S_{C_1}^{\omega_o} = S_{C_2}^{\omega_o} = -\frac{1}{2}$$

In other words, if the term under consideration is in the denominator, the sensitivity will have negative sign and the "exponent" of that variable in the expression is the sensitivity.

Some general formulae are presented next. The sensitivity of a fraction (p/q) to any component can be shown to be

$$S_x^{p/q} = S_x^p - S_x^q \tag{2.44}$$

As an illustration, consider the sensitivity evaluation of Q_p given by (2.30c) to the various components:

$$Q_p = \frac{\sqrt{C_1\ C_2\ R_1\ R_2}}{(C_1\ R_1 + C_2\,(R_1 + R_2) - K\,C_1\ R_1)} = \frac{N}{D} \tag{2.45}$$

We have

$$\begin{aligned} S_{C_1}^{Q_p} &= S_{C_1}^N - S_{C_1}^D = \frac{1}{2} - \frac{C_1\ R_1 - K\,C_1\ R_1}{C_1\ R_1 + C_2\,(R_1 + R_2) - K\,C_1\ R_1} \\ &= \frac{1}{2} - \frac{C_1\ R_1\,(1-K)\,Q_p}{\sqrt{C_1\ R_1\ C_2\ R_2}} \end{aligned} \tag{2.46a}$$

The expressions for other sensitivities can be very similarly written as follows.

$$S_{R_1}^{Q_p} = S_{R_1}^N - S_{R_1}^D = \frac{1}{2} - \frac{Q_p\,(C_1\ R_1 + C_2\ R_1 - K\,C_1\ R_1)}{\sqrt{C_1\ R_1\ C_2\ R_2}} \tag{2.46b}$$

$$S_{R_2}^{Q_p} = S_{R_2}^N - S_{R_2}^D = \frac{1}{2} - \frac{C_2\ R_2\ Q_p}{\sqrt{C_1\ R_1\ C_2\ R_2}} \tag{2.46c}$$

$$S_{C_2}^{Q_p} = S_{C_2}^N - S_{C_2}^D = \frac{1}{2} - \frac{C_2\,(R_1 + R_2)\,Q_p}{\sqrt{C_1\ R_1\ C_2\ R_2}} \tag{2.46d}$$

$$S_K^{Q_p} = S_K^N - S_K^D = \frac{K\,C_1\ R_1\ Q_p}{\sqrt{C_1\ R_1\ C_2\ R_2}} \tag{2.46e}$$

It is very important to remember that sensitivity formulae should be written for the original equation with all component values distinctly present. As an illustration for the choice $K = 1, R_1 = R_2$ the sensitivities are as follows.

$$S_{C_1}^{Q_p} = -S_{C_2}^{Q_p} = \frac{1}{2}, S_{R_1}^{Q_p} = S_{R_2}^{Q_p} = 0$$

For the case $K \neq 1$, we have the following.

$$S_{C_1}^{Q_p} = 2\,Q_p - \frac{1}{2}, S_{R_1}^{Q_p} = \frac{3\,Q_p}{2} - 1, S_{R_2}^{Q_p} = \frac{1}{2} - Q_p, S_{C_2}^{Q_p} = \frac{1}{2} - 2\,Q_p, S_K^{Q_p} = 3\,Q_p - 1$$

It will be useful to substitute the parameter under consideration in the sensitivity expression to get a meaningful insight to the magnitude of the sensitivity. For example, in (2.46) above, the value of Q_p has been substituted to obtain the various sensitivities in terms of Q_p. At this stage, the assumptions made in design such as $R_1 = R_2$, and so on can be made. The reader is referred to Appendix A for information on the evaluation of the overall variation in the magnitude of the transfer function.

In the earlier section, we considered a single-amplifier low-pass filter. A high-pass filter can be easily obtained by replacing resistors with capacitors and capacitors with resistances. This leads to a transformation known as low-pass to high-pass transformation denoted as an $s \rightarrow 1/s$ transformation. A high-pass filter thus obtained is shown in Fig. 2.9c.

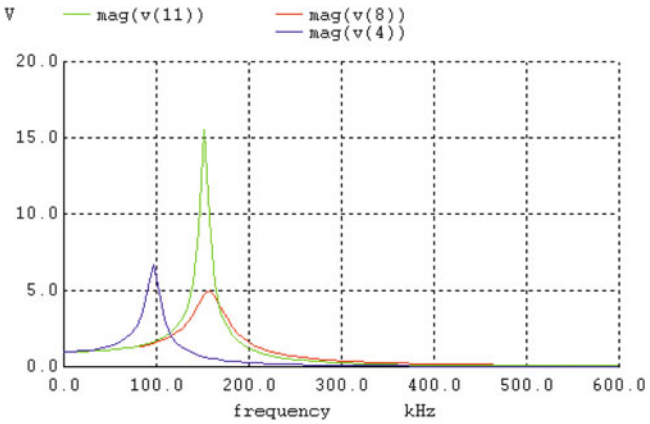
Example 2.4 Analyze using SPICE, the Sallen–Key filter using (a) an ideal unity gain amplifier, (b) using a μA 741 operational amplifier, and (c) an actively compensated unity gain amplifier. We use the model of the μA741 opamp. The ideal pole-frequency and pole-Q are 159.09 KHz and 5, respectively.

The SPICE listing and frequency responses for the three cases are presented below. The actual 741 model is defined as a subcircuit Xopamp. This is available from manufacturers at their websites. It can be seen that a nonideal opamp results in a decrease in pole-frequency and increase in pole-Q. On the other hand, the use of an actively compensated opamp results in a pole-frequency closer to the ideal value and Q enhancement is still present.

```
*Uncompensated Sallen–Key filter using opamp macromodel (infinite bandwidth)
Vin 1 0 1v ac
R3 1 6 1 K
R4 6 7 1 K
C3 6 8 10 nF
C4 7 0 .10 nF
E1 8 0 7 0 1
*Uncompensated Sallen–Key filter using Actual 741 model.
R1 1 2 1 K
```

```
R2 2 3 1 K
C1 2 4 10 nF
C2 3 0 .10 nF
xopamp1 3 4 vpos vneg 4 xyz
v1 vpos 0 dc 12
v2 0 vneg dc 12
*Actively Compensated Sallen–Key filter
R5 1 9 1 K
R6 9 10 1 K
C5 9 11 10 nF
C6 10 0 .10 nF
Xopamp2 10 12 vpos vneg 11 xyz
Xopamp3 11 12 vpos vneg 12 xyz
.ac lin 100 10 600 K
.subckt xyz 1 2 3 4 5
c1 11 12 8.661E-12
c2 6 7 30.00E-12
dc 5 53 dx
de 54 5 dx
dlp 90 91 dx
dln 92 90 dx
dp 4 3 dx
egnd 99 0 poly(2) (3.0) (4.0) 0 .5 .5
fb 7 99 poly(5) vb vc ve vlp vln 0 10.61E6–10E6 10E6 +10E6 –10E6
ga 6 0 11 12 188.5E-6
gcm 0 6 10 99 5.961E-9
iee 10 4 dc 15.16E-6
hlim 90 0 vlim 1 K
q1 11 2 13 qx
q2 12 1 14 qx
r2 6 9 100.0E3
rc1 3 11 5.305E3
rc2 3 12 5.305E3
re1 13 10 1.836E3
re2 14 10 1.836E3
ree 10 99 13.19E6
r01 8 5 50
ro2 7 99 100
rp 3 4 18.16E3
vb 9 0 dc 0
vc 3 53 dc 1
ve 54 4 dc 1
vlim 7 8 dc 0
vlp 91 0 dc 40
vln 0 92 dc 40
```

.model dx D(Is = 800.0E–18 Rs = 1)
.model qx NPN(Is = 800E–18 Bf = 93.75)
.ends



The SPICE simulation of the second-order Sallen–Key low-pass filter using a unity gain amplifier is presented next. The CMOS opamp Schematic [2.103] is shown in Fig. E.2.4. The program listing also gives an ideal Sallen–Key filter for comparison. The filter is designed for a pole-frequency of 795.45 KHz and pole-Q of 2.5.

*Sallen–Key ideal opamp
R3 1 6 100 K
R4 6 7 100 K
C3 6 8 10 pF
C4 7 0 0.4 pF
E1 8 0 7 0 1

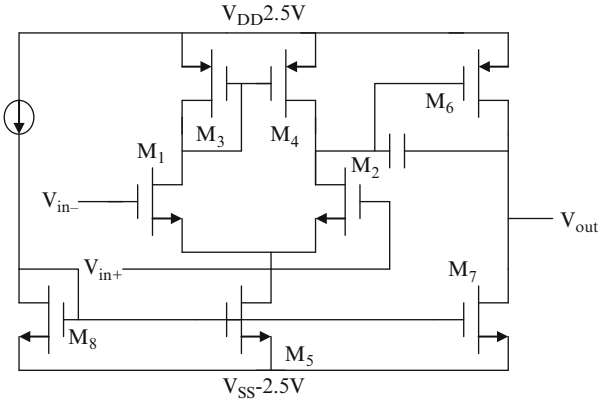
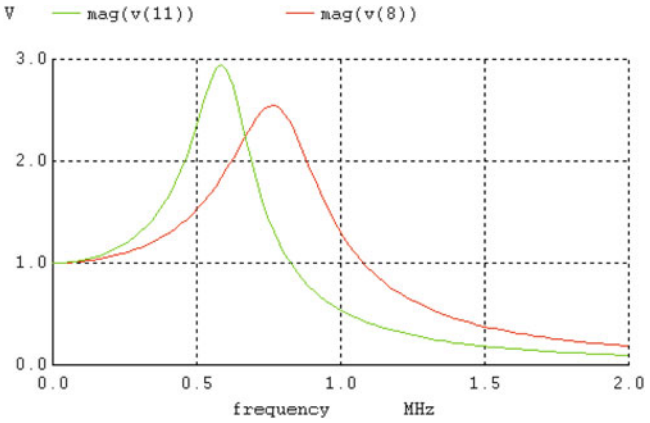


Fig. E.2.4 SPICE code of opamps (Adapted from [2.103]©OUP 2002)

```
*Sallen–Key filter using CMOS opamp
Vin 1 0 0.1v ac
R5 1 9 100 K
R6 9 10 100 K
C5 9 11 10 pF
C6 10 0 0.4 pf
Xopamp1 10 11 11 vpos vneg OPAMP
.ac lin 100 10 2000 K
v1 vpos 0 dc 2.5
v2 0 vneg dc 2.5
.SUBCKT OPAMP 1 2 6 8 9
M1 4 2 3 3 NMOS1 W = 3U L = 1U AD = 18P AS = 18P PD = 18U PS = 18U
M2 5 1 3 3 NMOS1 W = 3U L = 1U AD = 18P AS = 18P PD = 18U PS = 18U
M3 4 4 8 8 PMOS1 W = 15U L = 1U AD = 90P AS = 90P PD = 42U PS = 42U
M4 5 4 8 8 PMOS1 W = 15U L = 1U AD = 90P AS = 90P PD = 42U PS = 42U
M5 3 7 9 9 NMOS1 W = 4.5U L = 1U AD = 27P AS = 27P PD = 21U PS = 21U
M6 6 5 8 8 PMOS1 W = 94U L = 1U AD = 564P AS = 564P PD = 200U PS =
    200U
M7 6 7 9 9 NMOS1 W = 14U L = 1U AD = 84P AS = 84P PD = 40U PS = 40U
M8 7 7 9 9 NMOS1 W = 4.5U L = 1U AD = 27P AS = 27P PD = 21U PS = 21U
CC 5 6 3.0P
.MODEL NMOS1 NMOS VTO = 0.70 KP = 110U GAMMA = 0.4 LAMBDA =
    0.04 PHI = 0.7 MJ = 0.5 MJSW = 0.38 CGBO = 700P CGSO = 220P CGDO =
    220P CJ = 770U CJSW = 380P LD = 0.016U TOX = 14N
.MODEL PMOS1 PMOS VTO = -0.70 KP = 50U GAMMA = 0.57 LAMBDA =
    0.05 PHI = 0.8 MJ = 0.5 MJSW = 0.35 CGBO = 700P CGSO = 220P CGDO =
    220P CJ = 560U CJSW = 350P LD = 0.014U TOX = 14N
IBIAS 8 7 30U
.ENDS
.END
```



2.5 Second-Order Filters Based on Multiple Feedback

2.5.1 *Friend's Biquad*

There are other second-order filters using a single opamp known as *single-amplifier biquads* (SAB) that can realize many transfer functions based on the choice of component values. One such popular biquad is known as *Friend's biquad* [2.29]. This is shown in Fig. 2.11a and is also known as a *multiple feedback* filter since it uses both negative and positive feedback. This circuit, however, cannot realize a low-pass and all-pass transfer function for which alternative circuits shown in Figs. 2.12 and 2.13 can be used. We first denote

$$V_x = \alpha V_i + \beta V_o \tag{2.47}$$

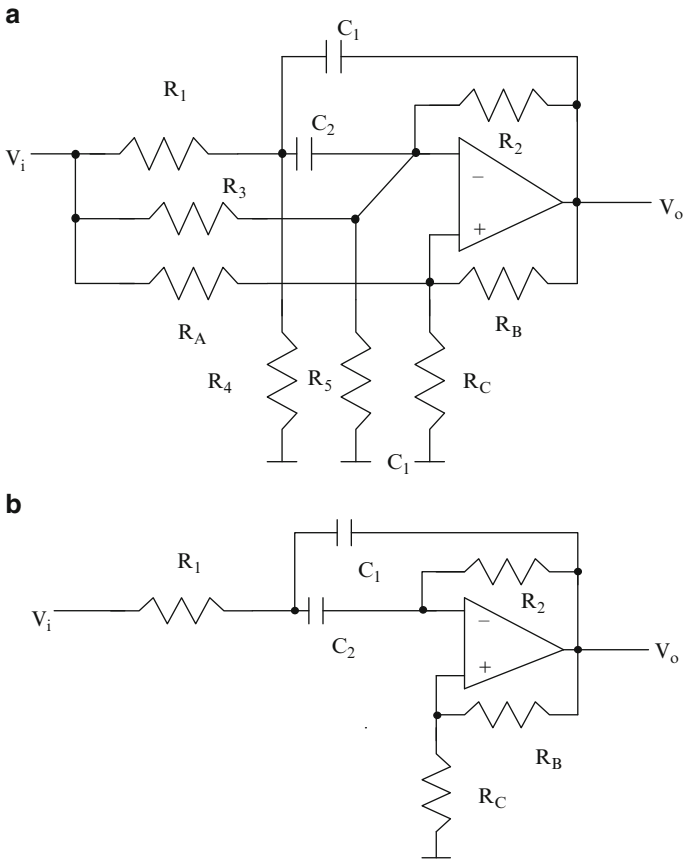


Fig. 2.11 (**a**) Friend's biquad, and (**b**) Deliyannis band-pass filter (Adapted from [2.29] ©IEEE 1975)

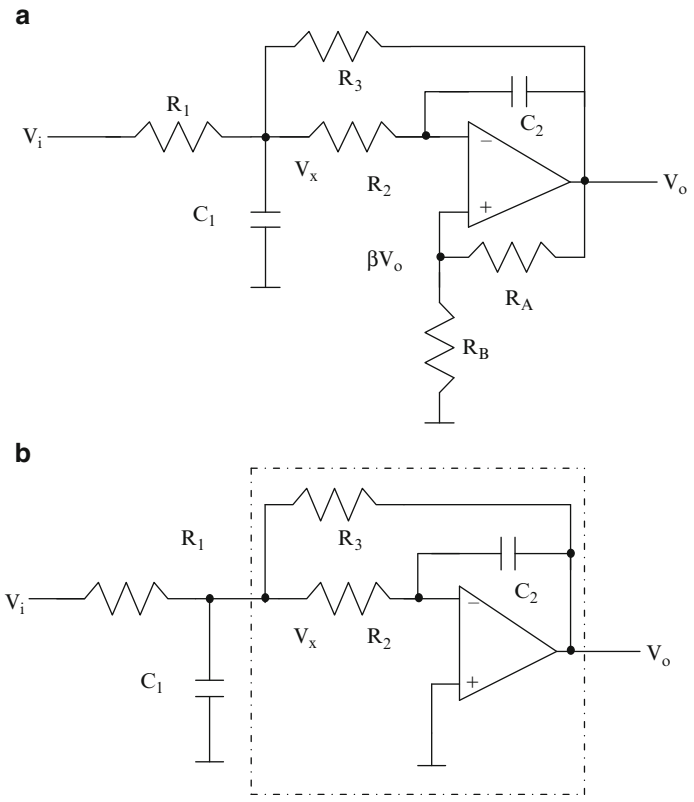


Fig. 2.12 (**a**) Multiple feedback- type second-order active RC low-pass filter with positive feedback, and (**b**) with no positive feedback (Adapted from [2.29] ©IEEE 1975)

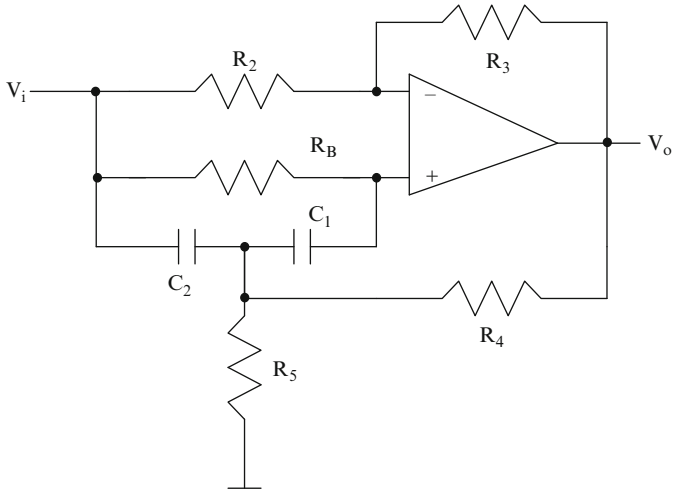


Fig. 2.13 Steffen's all-pass-type single-amplifier biquad (Adapted from [2.29] ©IEEE1975)

where

$$\alpha = \frac{R_C\ R_B}{R_A\ R_B + R_B\ R_C + R_A\ R_C} \tag{2.48}$$

and

$$\beta = \frac{R_C\ R_A}{R_A\ R_B + R_B\ R_C + R_A\ R_C} \tag{2.49}$$

The transfer function of the circuit of Fig. 2.11a can be derived as

$$\frac{V_o}{V_i} = -\frac{s^2\,\alpha C_2\ C_1 + s\left(\alpha C_2\left(\frac{1}{R_1}+\frac{1}{R_4}\right) - \frac{C_2}{R_1} - (C_1+C_2)\left(\frac{\alpha}{R_2}+\frac{\alpha}{R_5}-\frac{1-\alpha}{R_3}\right) + \left(\frac{1}{R_1}+\frac{1}{R_4}\right)\left(\frac{\alpha}{R_2}+\frac{\alpha-1}{R_5}+\frac{\alpha}{R_5}\right)\right)}{s^2\ C_2\ C_1\,(1-\beta) + s\left((C_1+C_2)\left(\frac{1-\beta}{R_2}-\frac{\beta}{R_3}-\frac{\beta}{R_5}\right) - \frac{\beta C_2}{R_1} - \frac{\beta C_2}{R_4}\right) + \left(\frac{1}{R_1}+\frac{1}{R_4}\right)\left(\frac{1-\beta}{R_2}-\frac{\beta}{R_3}-\frac{\beta}{R_5}\right)} \tag{2.50}$$

Note that the several degrees of freedom available can be used to realize a desired numerator of the transfer function. In the case of band-pass realization, R_3, R_5, and R_A are not needed. This means from (2.48) that $\alpha = 0$. Note that R_4 helps to control the gain. In the case where arbitrary gain can be accepted, R_4 need not be used. In this simple case known as Deliyannis band-pass biquad [2.31] shown in Fig. 2.11b, the transfer function simplifies as

$$\frac{V_o}{V_i} = -\frac{s\left(\frac{C_2}{R_1\,(1-\beta)}\right)}{s^2\ C_2\ C_1 + s\left(\left(\frac{(C_1+C_2)}{R_2}\right) - \frac{\beta C_2}{(1-\beta)R_1}\right) + \frac{1}{R_1\,R_2}} \tag{2.51}$$

Note that the pole-frequency is independent of β and β can be used to control the Q. Tradeoff between the spread of passive components (capacitors and resistors) and sensitivity can be achieved by proper choice of β and component values.

Denoting for simplicity $C_1 = C$, $C_2 = c^2C$, $R_1 = R$, and $R_2 = r^2R$, from the denominator of (2.51) we can obtain

$$\omega_o = \frac{1}{rcCR} \tag{2.52a}$$

and

$$Q_p = \frac{rc}{1 + c^2 - \frac{\beta}{(1-\beta)}\ r^2\ c^2} \tag{2.52b}$$

Note that for the case of no positive feedback (i.e., $\beta = 0$) the value of r is minimum when $c = 1$ and is then $r = 2Q_p$. Evidently, the resistor spread is $4{Q_p}^2$

which is very large for large Q_p values. The natural question that arises is the choice of r, c, and β values to reduce the sensitivity to component values. The opamp finite gain A can be considered in the above expression for Q_p by substituting $\beta = \beta_o - \frac{1}{A}$ where β_o is the ideal positive feedback factor given as $R_C/(R_C + R_B)$. This can be verified to be true by the reader by writing the equation for the voltage V_P at the inverting input of the opamp. Thus, the sensitivity to amplifier finite gain A can be obtained as follows.

Denoting $K = \frac{\beta}{1-\beta}$, we have $S_\beta^K = \frac{1}{1-\beta}$. Then, $S_K^{Q_p} = Krc\,Q_p$ and noting that $S_A^\beta = \frac{1}{A\beta_o - 1}$, we have

$$S_A^{Q_p} = S_\beta^{Q_p} \cdot S_A^\beta = S_K^{Q_p} \cdot S_\beta^K \cdot S_A^\beta = \frac{rc\,Q_p\,\beta}{(1-\beta)^2} \frac{1}{(A\,\beta_o - 1)} = \frac{rc\,Q_p}{A\left(1 - \frac{A\beta_o - 1}{A}\right)^2} \tag{2.53}$$

Since A is very large, this expression tends to zero thus obscuring the effect of finite but large A and its variations. Moschytz [2.32, 2.33] introduced a figure of merit known as the *gain sensitivity product* (GSP) which is defined as

$$GSP = A\,S_A^{Q_p} \tag{2.54}$$

The result is that $S_A^{Q_p}$ multiplied by A will not tend to zero but to a finite value:

$$GSP = AS_A^{Q_p} = \frac{rc\,Q_p}{(1-\beta_o)^2} \tag{2.55a}$$

Note that $\beta_o \cong \frac{1+c^2}{1+c^2+r^2}$ which can be obtained by equating the denominator of (2.52b) to zero implying very large Q_p values. Using this expression in (2.55a), we obtain the GSP in terms of the values c, r, and Q_p. Since Q_p is given as a design parameter, r and c need to be chosen to reduce the GSP.

$$GSP = \frac{(1 + c^2 + r^2\ c^2)^2\ Q_p}{r^3\ c^3} \tag{2.55b}$$

In the case of no positive feedback, under the optimum condition $c = 1$, $r = 2$ Q_p, the GSP is $2{Q_p}^2$. The GSP in the case of existence of positive feedback can be optimized by differentiating (2.55b) with respect to r or c and finding when it is minimum. Differentiating (2. 55b) with respect to r, the GSP can be found to be minimum under the condition

$$r^2 = \frac{3(1 + c^2)}{c^2} \tag{2.56a}$$

and the value of the GSP is

$$\text{GSP}_{\min 1} = \frac{16\,Q_p\,\sqrt{1+c^2}}{3\sqrt{3}} \tag{2.56b}$$

In a similar manner, differentiating (2.55b) with respect to c, the GSP can be found to be minimum under the condition

$$c^2 = \frac{3}{\left(1+r^2\right)} \tag{2.57a}$$

and the value of the GSP is

$$\text{GSP}_{\min 2} = \frac{16\,Q_p\,\left(1+r^2\right)^{3/2}}{3\,r^3\,\sqrt{3}} \tag{2.57b}$$

As an illustration for $c = 1$ from (2.56a) and (2.56b), we have $r = \sqrt{6}$, $GSP_{\min 1} = \frac{16\,Q_p\,\sqrt{2}}{3\sqrt{3}} = 4.354\,Q_p$ and for $c = 1$ from (2.57a) and (2.57b), we have $r = \sqrt{2}$, $GSP_{\min 2} = \frac{8\,Q_p}{\sqrt{2}} = 5.656\,Q_p$. The values of β_o for both these cases are, respectively, $\beta_o = \frac{1-\frac{\sqrt{3}}{Q_p\,\sqrt{2}}}{4-\frac{\sqrt{3}}{Q_p\,\sqrt{2}}}$ and $\beta_o = \frac{1-\frac{1}{Q_p\,\sqrt{2}}}{2-\frac{1}{Q_p\,\sqrt{2}}}$. As an illustration for $Q_p = 10$, the various cases yield the GSP as (a) $\beta_o = 0$, GSP $= 200$, (b) $\beta_o = 0.2334$, GSP $= 43.54$, and (c) $\beta_o = 0.48167$, GSP $= 56.56$.

2.5.2 *Multiple Feedback-Type Low-Pass Filter Due to Friend*

The biquad described in the previous section cannot realize a low-pass transfer function. An alternative circuit due to Friend [2.29] is considered next. This circuit is shown in Fig. 2.12a and has a transfer function given by

$$\frac{V_o}{V_i} = -\frac{1}{(1-\beta)} \times \frac{1}{s^2\,C_1\,C_2\,R_1\,R_2 + s\left(C_2\,R_1\,R_2\left(\frac{1}{R_1}+\frac{1}{R_2}+\frac{1}{R_3}\right) - \frac{\beta}{(1-\beta)}C_1\,R_1\right) + \frac{R_1}{R_3} - \frac{\beta}{(1-\beta)}} \tag{2.58a}$$

Note that when positive feedback does not exist (i.e., $\beta = 0$ or the noninverting input of the opamp is grounded), the circuit reduces to that shown in Fig. 2.12b. It still realizes a low-pass filter transfer function at the output and in addition a band-pass transfer function at the internal node:

$$\frac{V_x}{V_i} = -\left(\frac{V_o}{V_i}\right) s\,C_2\,R_2 \quad \text{when } \beta = 0 \tag{2.58b}$$

This circuit can be interpreted as having a lossy simulated inductance-based tank circuit. The lossy inductance realized by the circuit within dotted lines is based on a Ford and Girling [2.34] configuration and realizes an inductance of value $C_2R_2R_3$ and is shunted by a resistance R_2 in parallel with R_3. In the circuit of Fig. 2.12b, the pole-frequency can be seen to be independent of R_1 and R_1 can be used to control the dc gain R_3/R_1:

$$\omega_p^2 = \frac{1}{C_1\, C_2\, R_2\, R_3}, \quad Q_p = \sqrt{\frac{C_1}{C_2}} \cdot \frac{R_1\sqrt{R_2\, R_3}}{R_1\, R_2 + R_2\, R_3 + R_1\, R_3} \tag{2.59}$$

The capacitor spread can be seen to be minimum when $R_1 = R_2 = R_3$, yielding $\frac{C_1}{C_2} = 9\, Q_p^2$.

In the case of positive feedback being used (i.e., $\beta \neq 0$), the circuit can be designed for chosen C_1, C_2, and β values so as to realize the desired gain, pole-frequency, and pole-Q. The value of R_2 can be estimated first and then R_1 and R_3 can be obtained:

$$R_2 = \frac{\frac{1}{Q_p} \pm \sqrt{\frac{1}{Q_p^2} - 4(H_o + 1)\left(\frac{C_2}{C_1} - \frac{\beta}{1-\beta}\right)}}{2(H_o + 1)\,\omega_p\, C_2} \tag{2.60a}$$

$$R_1 = \frac{1}{H_o\,(1-\beta)\,\omega_p^2\, C_1\, C_2\, R_2} \tag{2.60b}$$

and

$$R_3 = \frac{H_o\,(1-\beta)\,R_1}{1 + H_o\,\beta} \tag{2.60c}$$

where H_o is the dc gain of the low-pass filter given by

$$H_o = \frac{1}{(1-\beta)\left(\frac{R_1}{R_3}\right) - \beta} \tag{2.60d}$$

Among the two solutions possible for R_2, the choice of negative sign in (2.60a) yields a lower spread.

The circuits of Figs. 2.11a and 2.12 cannot realize a second-order all-pass transfer function. A solution is to use an alternative configuration due to Steffen [2.29], shown in Fig. 2.13. The transfer function of this circuit can be derived as

$$\frac{V_o}{V_i} = -\frac{s^2\, C_2\, C_1 + s\left(\frac{C_1 + C_2}{R_B} - \frac{C_1\, R_3}{R_2}\left(\frac{1}{R_4} + \frac{1}{R_5}\right)\right) + \left(\frac{1}{R_4} + \frac{1}{R_5}\right)\frac{1}{R_B}}{s^2\, C_2\, C_1 + s\left(\frac{C_1}{R_5} + \frac{C_1 + C_2}{R_B} - \frac{C_1\, R_3}{R_2\, R_4}\right) + \left(\frac{1}{R_4} + \frac{1}{R_5}\right)\frac{1}{R_B}} \tag{2.61}$$

The condition for realizing an all-pass transfer function is that the coefficient of the "s" term in the numerator must be equal and opposite in sign to that in the denominator yielding

$$2\left(\frac{C_1+C_2}{R_B}\right)-\frac{C_1\,R_3}{R_2}\left(\frac{2}{R_4}+\frac{1}{R_5}\right)+\frac{C_1}{R_5}=0 \tag{2.62}$$

Next, assuming that $C_1 = C_2 = C$ and with chosen value of G_2/G_3, we have

$$R_5=\frac{\mu\,Q_p}{2\,C_2\;\omega_p} \tag{2.63a}$$

where

$$\mu=1+\frac{R_3}{R_2}. \tag{2.63b}$$

Next, R_4 can be obtained as

$$\frac{1}{R_4}=\frac{-\,G_5\,(4-3\mu)\pm\sqrt{G_5^2\;(4-3\mu)^2-8(1-\mu)(4\,C_1\;C_2\;\omega_p^2+G_5^2\,(2-\mu))}}{4(1-\mu)} \tag{2.63c}$$

Finally, R_B can be evaluated from the expression for pole-frequency as

$$G_B=\frac{C_1\;C_2\;\omega_p^2}{(G_4+G_5)} \tag{2.63d}$$

Example 2.5 Using SPICE, taking into account the finite bandwidth of the opamp, plot the response of the band-pass filter of Fig. E.2.5. Evaluate the poles and plot the group delay versus frequency.

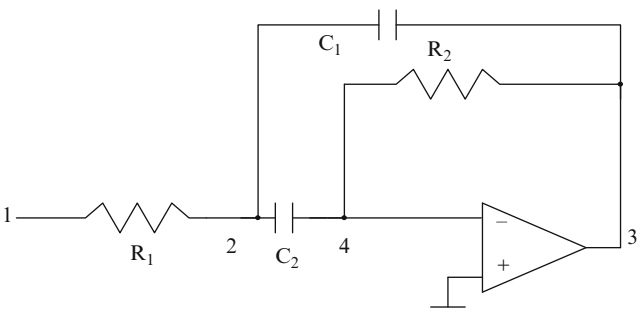


Fig. E.2.5a

This band-pass filter has a pole-frequency of 40 KHz and pole-Q of 20. The midband gain is 800. The effect of opamp finite bandwidth is to create a parasitic real pole and perturb the actual poles. The *.pz* command prints the poles and zeroes. The frequency response using ideal opamp and opamp with finite bandwidth 1 MHz are plotted in Fig. E.2.5b. The group delay is also plotted as a function of frequency by giving the *.plot gd(v(3))* command in Fig. E.2.5c.

```
*Multiple feedback SAB
R1 1 2 62.5
R2 4 3 100 K
C1 2 3 1590 pf
C2 2 4 1590 pf
E1 0 5 4 0 100,000
R4 5 6 1 k
C3 6 0 15.9 uf
E2 3 0 6 0 1
*Multiple feedback band-pass filter using ideal opamp
R11 1 7 62.5
R21 9 8 100 K
C11 7 8 1590 pf
C21 7 9 1590 pf
E3 0 8 9 0 10,000,000
vin 1 0 ac 1v
*.ac lin 1,000 10,000 100 K
.PZ 1 0 3 0 VOL PZ
pole(1) = –1.63576e + 07,0.000000e + 00
pole(2) = –3.62826e + 03,1.559514e + 05
pole(3) = –3.62826e + 03,–1.55951e + 05
zero(1) = 0.000000e + 00,0.000000e + 00
```

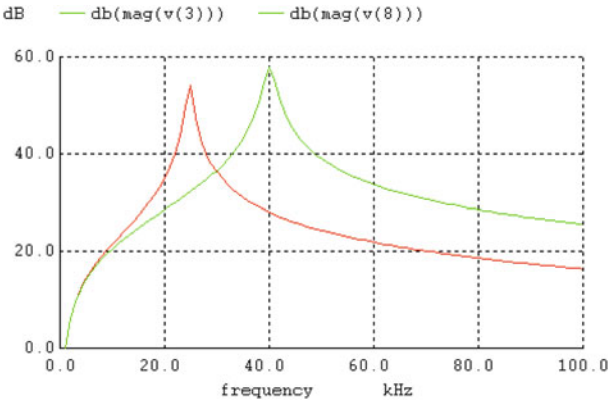


Fig. E.2.5b

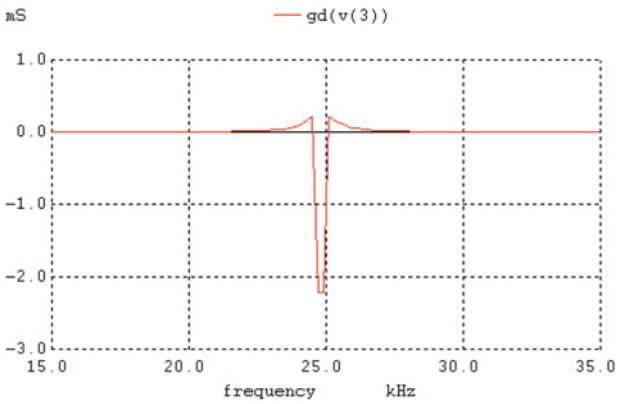


Fig. E.2.5c

The following describes a variable center frequency band-pass filter (by varying R5 for three values) with constant bandwidth and constant peak value considering an ideal opamp (see Fig. E.2.5d).

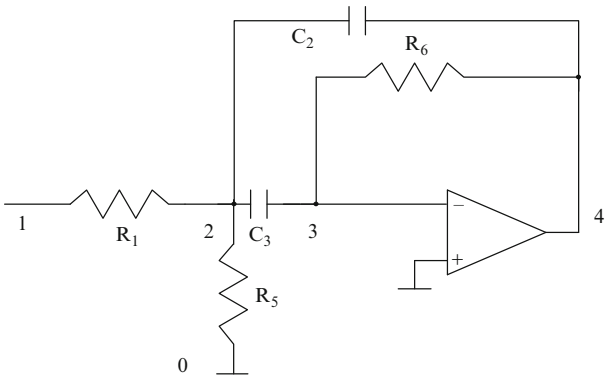


Fig. E.2.5d

```
* SA Bandpass
R1 1 2 3181.5
R5 2 0 15
C3 2 3 10000 pf
C2 2 4 10000 pf
R6 3 4 6363
E1 0 5 3 0 100,000
R4 5 6 1 k
C5 6 0 15.9 uf
E2 4 0 6 0 1
vin 1 0 ac 1v
*.ac dec 1,000 10 10,000 K
.control
destroy all
```

```
let ii = 0
while ii < 5
alter R5 = 15 + 20 * ii
ac dec 1,000 10 10,000 k
let ii = ii + 1
plot mag(ac1.v(4)) mag(ac3.v(4)) mag(ac5.v(4))
end
```

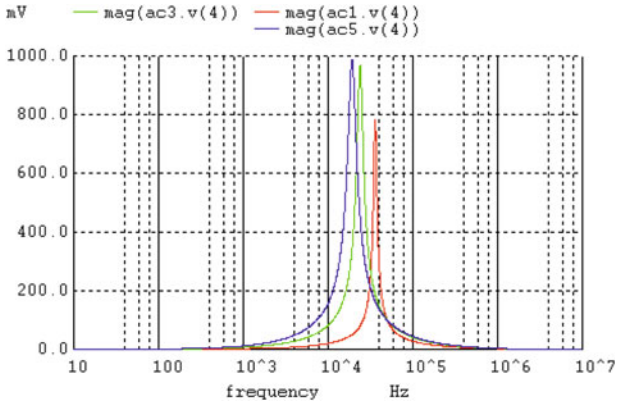


Fig. E.2.5e

Example 2.6 Find the magnitude and group delay of the transfer function of the MFB all-pass filter of Fig. E.2.6a. Find the response of the notch filter obtained using different feedforward gain defined by $R_4/(R_3 + R_4)$.

Note that the magnitude of an all-pass transfer function ideally should be flat (close to unity). The error is amplified and presented in Fig. E.2.6. The group delay response is shown in Fig E.2.6. The frequency response of the notch filter is shown in Fig. E.2.6d. (The same program with $R_3 = 2$K will realize a Notch filter (see

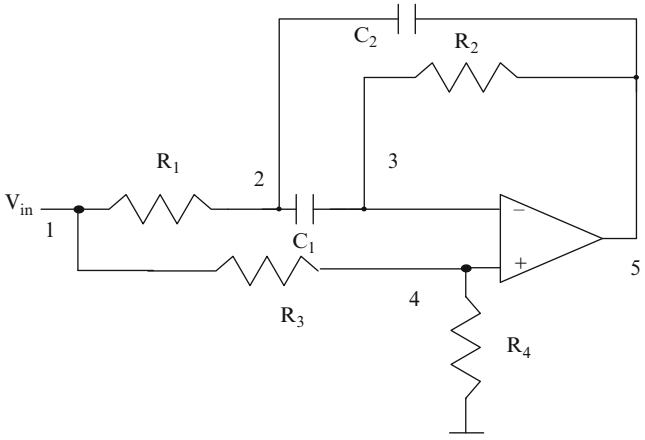


Fig. E.2.6a

Fig. E.2.6d)). Note that the opamp dc gain is very large, meaning that it is ideal. The reader is urged to find the responses with finite opamp bandwidth.

```
* Circuit MFB all-pass/Notch
R1 1 2 1 k
R2 3 5 400 k
C1 2 3 0.0001 uf
C2 2 5 0.0001 uf
R3 1 4 2k
R4 4 0 400 k
E1 6 0 4 3 10,000,000
R5 6 7 1 k
C3 7 0 15.9 uf
E2 5 0 7 0 1
vin 1 0 ac 1 v
.ac lin 99 1k 99 K
```

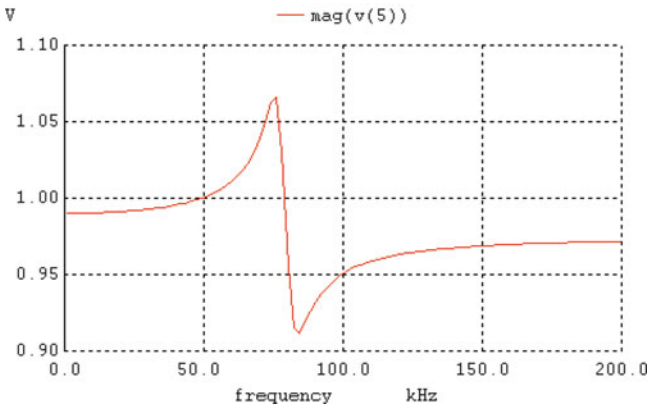


Fig. E.2.6b

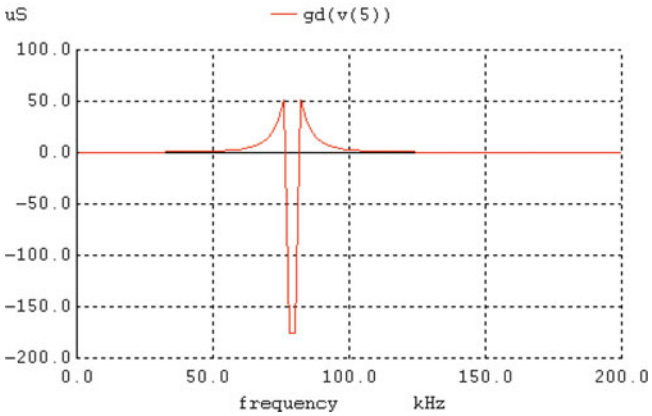


Fig. E.2.6c

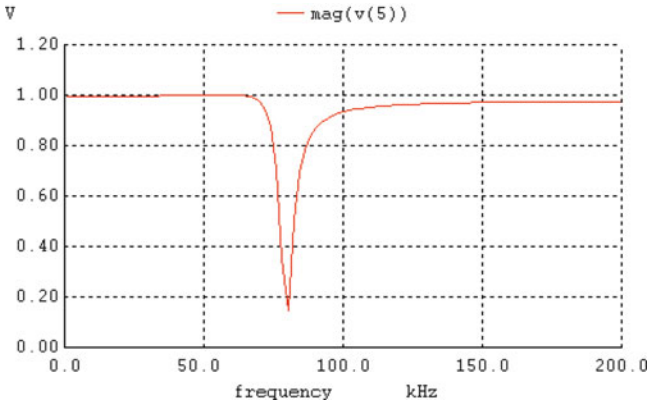


Fig. E.2.6d

2.5.3 Active Filters Using Single Fully Differential Amplifier

A very recent development is the easy availability of opamps with differential outputs. A typical filter using a current input that exploits this property [2.35, 2.36] is shown in Fig. 2.14a. Note that in this circuit, the noninverting input of the opamp is grounded. Moreover, in addition to the usual output of the opamp, an inverted output is also available which can be used to provide positive feedback. This technique eliminates the need for the two resistors providing positive feedback using resistors R_A and R_B; see, for example, Fig. 2.12a. For simplicity, an inverting block of gain -1 is shown in Fig. 2.14a. The input impedance realized by this block is as shown in Fig. 2.14b.

In the absence of feedback, the input impedance of the circuit is thus that of a lossy resonator (see block within dotted lines in Fig. 2.11b). At the resonance frequency, $\frac{1}{2\pi\sqrt{C_f\, R R_f\, C}}$, the input impedance is resistive $\left(\frac{R R_f}{R+R_f}\right)$. In the presence of C_{pf}, however, the input impedance comprises an additional capacitance C_{pf} and a negative resistance of value $-R\frac{C_f}{C_{pf}}$ as shown in Fig. 2.14b. Thus, the effect of positive feedback is to increase the effective capacitance from C to $C + C_{pf}$ and to decrease the damping. The input admittance is still that of a RLC tank circuit. For an appropriate choice of C_{pf} such that

$$-R\frac{C_f}{C_{pf}} + \left(\frac{R R_f}{R+R_f}\right) = 0 \quad \text{or} \quad C_{pf} = C_f\left(1 + \frac{R}{R_f}\right) \tag{2.64}$$

the resistance across the tank circuit can be completely cancelled thus realizing an oscillator with a frequency of oscillation given by

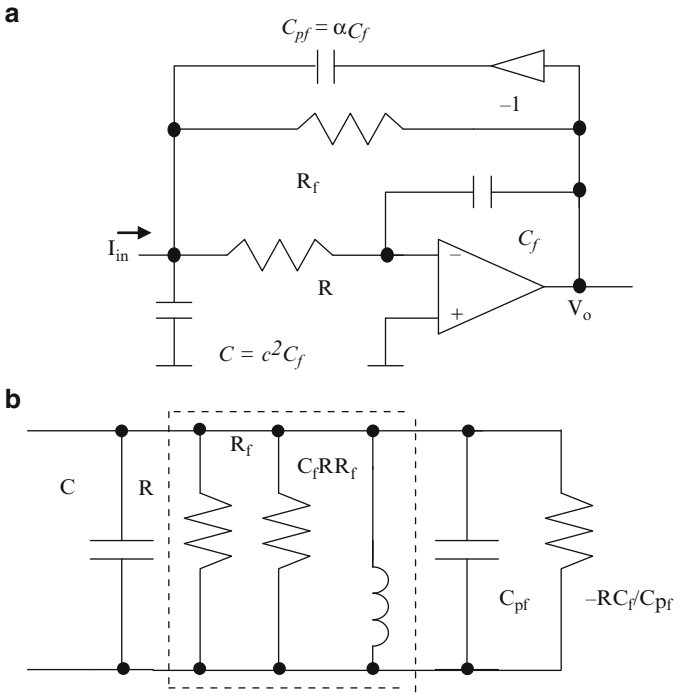


Fig. 2.14 (**a**) Multiple feedback filter using differential output opamp; (**b**) input impedance (Adapted from [2.35] ©IEEE 2008)

$$f_{osc} = \frac{1}{2\pi\sqrt{(C + C_{pf})\, C_f\, R\, R_f}} \tag{2.65}$$

The transfer function of the realized filter of Fig. 2.14a taking into account the finite gain of the opamp A can be obtained as

$$\frac{V_o}{I_{in}} = -\frac{R_f}{D(s)}$$

where

$$D(s) = s^2 R R_f \left(C + C_{pf}\right) C_f \left(1 + \frac{1}{A}\right) + s\left(C_f \left(R + R_f\right)\left(1 + \frac{1}{A}\right) - C_{pf}\, R_f + \frac{\left(C + C_{pf}\right) R_f}{A}\right) + \left(1 + \frac{1}{A}\right) \tag{2.66}$$

Considering first the case of an opamp with infinite gain, denoting $C = c^2 C_f$, $C_{pf} = \alpha C_f$, $R_f = r^2 R$, the pole-frequency ω_p, and the pole-Q Q_p can be written as follows.

$$\omega_p = \frac{1}{C_f R r \sqrt{c^2 + \alpha}} \tag{2.67a}$$

$$Q_p = \frac{r\sqrt{c^2 + \alpha}}{r^2(1-\alpha)+1} \tag{2.67b}$$

Note that α indicates the amount of positive feedback. Techniques for arriving at an optimum choice of the various degrees of freedom α, c, and r for given R and C values to arrive at a desirable solution to minimize the active and passive sensitivities or the spread in component values have been described in detail in [2.36].

It must have been noted that single-amplifier structures do not have flexibility in controlling the pole-frequency, gain, and pole-Q independently using separate noninteracting controls except in a few cases. Moreover, these generally have high sensitivities and require a large spread in component values. This is the reason for preferring multiple amplifier biquads.

2.6 Biquads Using Two Opamps

2.6.1 GIC-Based Biquads

A GIC (generalized impedance converter) [2.37] is shown in Fig. 2.15a. This circuit realizes an input impedance given by

$$Z_{in} = \frac{Z_1\, Z_3\, Z_5}{Z_2\, Z_4} \tag{2.68}$$

Note by virtue of the high gain of the opamps, all internal inverting and noninverting input nodes of the opamps are at the same voltage. It is interesting to see that a lossless grounded inductance can be realized when either Z_2 or Z_4 is a capacitor:

$$Z_{in} = \frac{sC_2R_1R_3R_5}{R_4} \text{ in the case } Z_2 = 1/sC_2 \text{ or } Z_{in} = \frac{sC_4R_1R_3R_5}{R_2} \text{ in the case } Z_4 = 1/sC_4$$

$$\begin{aligned} Z_{in} &= \frac{s\,C_2\,R_1\;R_3\;R_5}{R_4} \quad \text{in the case } Z_2 = 1/sC_2 \quad \text{or} \quad Z_{in} \\ &= \frac{s\,C_4\,R_1\;R_3\;R_5}{R_2} \quad \text{in the case } Z_4 = 1/sC_4 \end{aligned} \tag{2.69}$$

The value of the inductance can be changed by any one of the various resistors. They can be chosen equal for convenience as well.

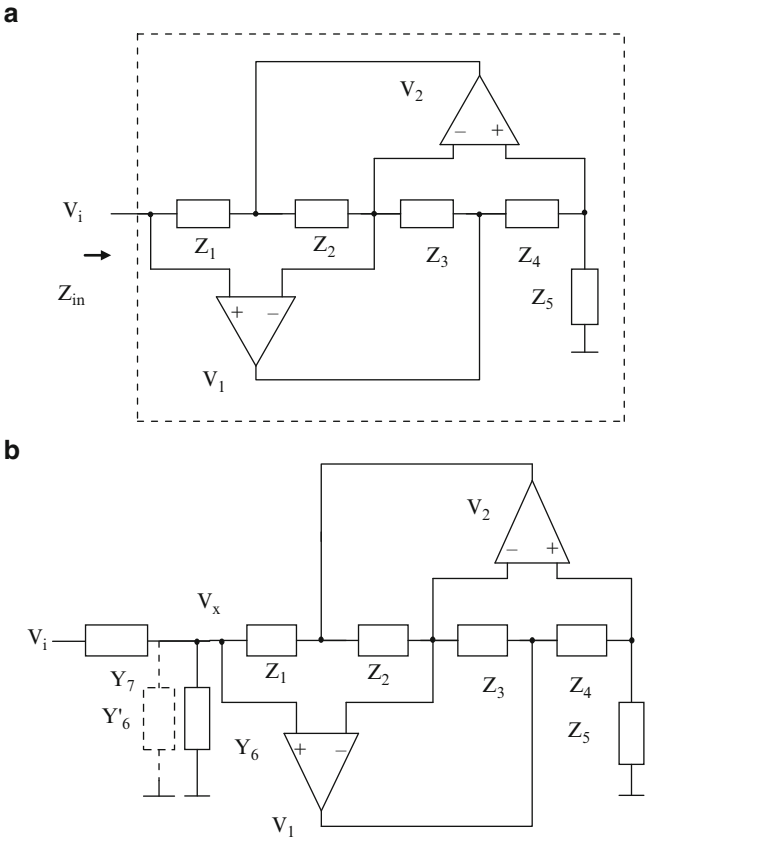


Fig. 2.15 (**a**) A Generalized impedance converter, and (**b**) application of (a) to realize a second-order filter

As an alternative, if both Z_2 and Z_4 are capacitors, a grounded frequency-dependent negative resistance can be obtained with input impedance of the form s^2D:

$$Z_{in} = s^2\ R_1\ R_3\ R_5\ C_2\ C_4 \tag{2.70}$$

For $s = j\omega$, evidently $Z_{in} = -\omega^2\ R_1\ R_3\ R_5\ C_2\ C_4$ which means that a negative resistance is realized (due to the negative sign) which is frequency-dependent due to the ω^2 term.

As yet another alternative, by choosing two of the impedances Z_1, Z_3, and Z_5 as capacitors, a grounded supercapacitance with impedance of the form $1/(s^2C)$ can be obtained. As an illustration, for $Z_1 = 1/sC_1$ and $Z_3 = 1/sC_3$, we have

$$Z_{in} = \frac{R_5}{s^2\ C_1\ C_3\ R_2\ R_4} \tag{2.71}$$

The application of these to realize high-order filters is shown later.

It is easy to build second-order filters based on classical RLC circuits based on the use of LC tank circuits. For example, a band-pass filter or a high-pass filter can be obtained as shown in Fig. 2.15b by choosing $Y_6 = sC_6$, $Y_7 = 1/R_7$, or $Y_6 = 1/R_6$, $Y_7 = sC_7$. In the case of a band-pass filter, the pole-Q can be controlled using R_7 whereas in the case of a high-pass filter, the pole-Q can be controlled by R_6.

The various transfer functions in the case of the choice of $Y_2 = sC_2$, are as follows.

$$\frac{V_x}{V_i} = \frac{s\,C_2\;Y_4\;Y_7}{s^2\;C_2\;Y_4\;C_6 + s\,C_2\;Y_4\;Y_7 + Y_1\;Y_3\;Y_5} \tag{2.72a}$$

$$\frac{V_1}{V_i} = \frac{(Y_4\;+Y_5)s\,C_2\;Y_7}{s^2\;C_2\;Y_4\;C_6 + s\,C_2\;Y_4\;Y_7 + Y_1\;Y_3\;Y_5} \tag{2.72b}$$

$$\frac{V_2}{V_i} = \frac{Y_7\,(s\,C_2\;Y_4 - Y_3\;Y_5)}{s^2\;C_2\;Y_4\;C_6 + s\,C_2\;Y_4\;Y_7 + Y_1\;Y_3\;Y_5} \tag{2.72c}$$

It may be noted that only the band-pass transfer function is available as V_x and V_1 outputs and the other transfer function is not useful.

In the case with $Z_4 = 1/sC_4$, we have

$$\frac{V_x}{V_i} = \frac{s\,C_4\;Y_2\;Y_7}{s^2\;C_4\;Y_2\;C_6 + s\,C_4\;Y_2\;Y_7 + Y_1\;Y_3\;Y_5} \tag{2.73a}$$

$$\frac{V_1}{V_i} = \frac{(sC_4\;+Y_5)\,Y_2\;Y_7}{s^2\;C_4\;Y_2\;C_6 + s\,C_4\;Y_2\;Y_7 + Y_1\;Y_3\;Y_5} \tag{2.73b}$$

$$\frac{V_2}{V_i} = \frac{Y_7\,(s\,C_2\;Y_4 - Y_3\;Y_5)}{s^2\;C_4\;Y_2\;C_6 + s\,C_4\;Y_2\;Y_7 + Y_1\;Y_3\;Y_5} \tag{2.73c}$$

Note that only (2.37a) realizes a useful transfer function.

The denominator of the transfer function of the general structure of Fig. 2.15b taking into account the finite bandwidth B of the opamp and assuming identical opamps is given as

$$D(s) = (Y_1\;Y_5\;Y_3 + Y_2\;Y_4\;Y_6) + (Y_1 + Y_6)(Y_3 + Y_2)(Y_4 + Y_5)\left(\frac{s}{B} + \frac{s^2}{B^2}\right) \tag{2.74}$$

For the choice $Y_2 = sC_2$, $Y_6 = sC_6$, and all other admittances as resistors, to realize a band-pass filter transfer function at V_A, (2.74) becomes

$$D(s) = s^4 \frac{C_6\, C_2}{B^2}(Y_4 + Y_5) + s^3\left(\frac{C_6\, C_2}{B}(Y_4 + Y_5) + \frac{(Y_4 + Y_5)(C_6\, Y_3 + C_2\, Y_1 + C_2\, Y_6) + Y_2\, Y_4\, Y_6}{B^2}\right) + s^2\left(C_2\, Y_4\, Y_6 + \frac{(Y_4 + Y_5)(Y_1 + Y_6)\, Y_3}{B^2} + \frac{(Y_4 + Y_5)(C_6\, Y_3 + C_2\, Y_1 + C_2\, Y_6)}{B}\right) + s\left(C_2\, Y_4\, Y_6 + \frac{(Y_4 + Y_5)(Y_1 + Y_6)\, Y_3}{B}\right) + Y_1\, Y_5\, Y_3 \tag{2.75}$$

The resulting modified pole-frequency can be calculated by looking at the s^0 and s^2 terms under the condition $Y_1 = Y_3 = Y_4 = Y_5 = 1/R$, $Y_2 = Y_6 = sC$, and $R_6 = RQ_p$.

$$\frac{\omega_o^2}{\hat{\omega}_o^2} = 1 + 2\left(2 + \frac{1}{Q_p}\right)\frac{\omega_p}{B} \tag{2.76}$$

Note that the results are same in the case $Y_4 = sC_4$ and $Y_1 = Y_3 = Y_2 = Y_5 = 1/\mathrm{R}$.

2.6.2 *Two-Amplifier Biquads Derived from Single-Amplifier Biquads*

The single opamp-based biquads described earlier have used noninverting input of the opamp as well. However, in order to reduce the effect of parasitic capacitances at the inverting input of the opamp, it is useful to derive filters using opamps with grounded noninverting input. Equivalent filter configurations can be derived based on the nodal voltage simulation technique [2.38]. In this technique, the equations at the internal nodes of the original circuit are realized in a different way so that the opamp noninverting inputs can be grounded.

As an illustration, consider the active RC filter of Fig. 2.12a redrawn in Fig. 2.16a. At node A, we have

$$\frac{V_x}{R_2} + V_o\, s\, C_2 = \beta\, V_o\left(\frac{1}{R_2} + s\, C_2\right) \tag{2.77}$$

which can be rewritten as

$$\frac{V_x}{R_2} + V_o\, s\, C_2\,(1 - \beta) - \left(\frac{\beta}{R_2}\right) V_o = 0 \tag{2.78}$$

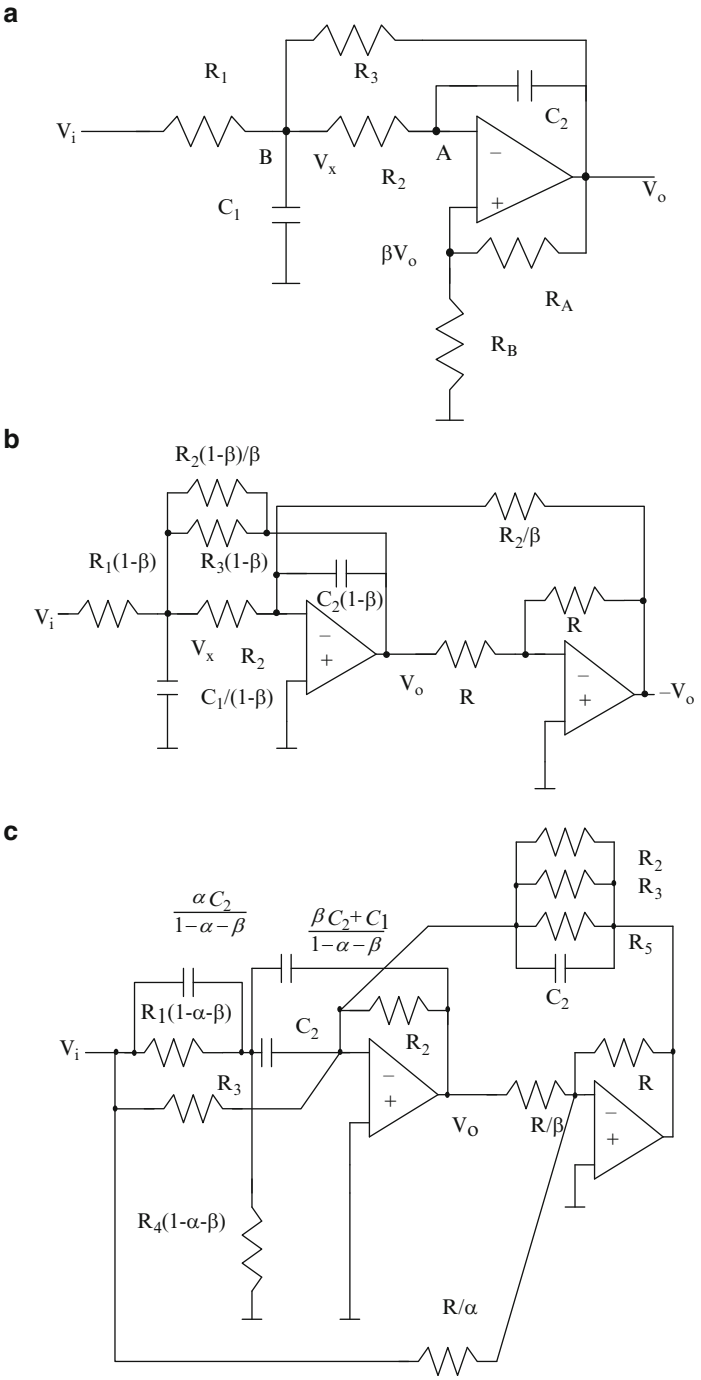


Fig. 2.16 (**a**) Multiple feedback-type low-pass biquad, (**b**) circuit derived using nodal voltage simulation, and (**c**) circuit derived from Friend's biquad (c Adapted from [2.38] ©IEE 1984)

This equation is implemented as shown in Fig. 2.15b using resistors R_2, capacitor $C_2(1-\beta)$, resistor R_2/β, and inverting amplifier of gain 1. Similarly, at node B, we have in the circuit of Fig. 2.15a

$$\frac{V_i}{R_1}+\frac{V_o}{R_3}+\frac{\beta V_o}{R_2}=V_x\left(\frac{1}{R_1}+\frac{1}{R_2}+\frac{1}{R_3}+sC_1\right) \tag{2.79a}$$

This can be rewritten first as

$$\frac{V_i-V_x}{R_1}+(V_o-V_x)\left(\frac{1}{R_3}+\frac{\beta}{R_2}\right)=V_x\left(\frac{1-\beta}{R_2}+sC_1\right) \tag{2.79b}$$

and next by dividing throughout by $(1-\beta)$ as

$$\begin{aligned}&\frac{V_i-V_x}{(1-\beta)R_1}+(V_o-V_x)\left(\frac{1}{R_3\,(1-\beta)}+\frac{\beta}{R_2\,(1-\beta)}\right)\\&\quad=V_x\left(\frac{1}{R_2}+\frac{sC_1}{(1-\beta)}\right)\end{aligned} \tag{2.79c}$$

in order to retain R_2 the same from V_x to virtual ground already present for realizing (2.79a) so that at node V_x, we obtain the same equation as in Fig. 2.16a. Note that all resistors and capacitors are realizable since $0<\beta<1$.

This technique was originally used for the Friend–Deliyannis biquad [2.29] of Fig. 2.11a which realizes exactly the same transfer function. The resulting two-amplifier circuit is presented in Fig. 2.16c for completeness. The circuit still has one internal node at which the parasitic capacitance can be absorbed by the capacitor C_2.

2.7 Biquads Using More Than Two Opamps

2.7.1 KHN Biquad

The well-known *Kerwin–Huelsman–Newcomb* (KHN) biquad [2.39] also known as the *state variable biquad* is presented in Fig. 2.17a. This circuit using three opamps realizes high-pass, band-pass, and low-pass transfer functions at the output terminals of the three opamps. The transfer functions of this circuit can be derived as follows.

$$\frac{V_{LP}}{V_i}=\frac{\frac{R_6\left(1+\frac{R_3}{R_4}\right)}{(R_5+R_6)}}{s^2\,C_1\,C_2\,R_1\,R_2+s\frac{C_1\,R_1\,R_5}{(R_5+R_6)}\left(1+\frac{R_3}{R_4}\right)+\frac{R_3}{R_4}} \tag{2.80a}$$

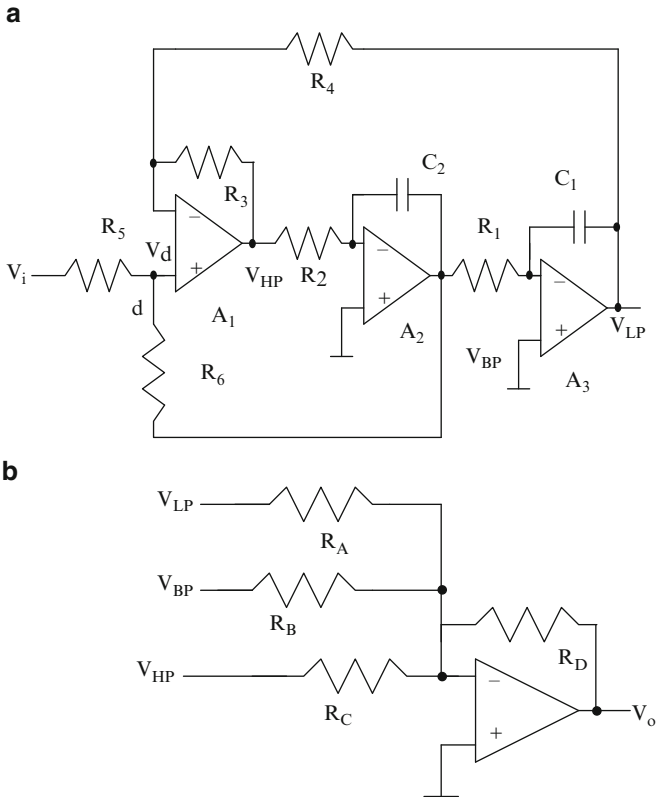


Fig. 2.17 (**a**) KHN Biquad, and (**b**) additional circuit to obtain a general biquadratic transfer function

$$V_{BP} = -\,s\,C_1\,R_1\,V_{LP} \tag{2.80b}$$

$$V_{HP} = s^2\,C_1\,R_1\,C_2\,R_2\,V_{LP} \tag{2.80c}$$

Evidently, all three transfer functions are available. The choice of components $R_1 = R_2 = R, C_1 = C_2 = C, R_4 = R_3$ simplifies these transfer functions as

$$\frac{V_{LP}}{V_i} = \frac{\dfrac{2R_6}{(R_5+R_6)}}{s^2\,C^2\,R^2 + s\dfrac{2CR\,R_5}{(R_5+R_6)} + 1}, \quad V_{BP} = -sCR\,V_{LP}, \quad V_{HP} = s^2\,C^2\,R^2\,V_{LP} \tag{2.81}$$

Evidently, the pole-frequency $\omega_p = 1/CR$ and the pole-Q is given by

$$Q_p = \frac{R_5+R_6}{2R_5} \quad \text{or} \quad \frac{R_6}{R_5} = 2\,Q_p - 1 \tag{2.82}$$

Thus, the circuit has low pole-Q sensitivities and low pole-frequency sensitivities and has the capability for orthogonal tuning of the pole-frequency and pole-Q. The dc gain of the low-pass filter can be seen to be $\left(2-\frac{1}{Q_p}\right)$ which cannot be independently controlled.

It is interesting to note that at node "d", a notch transfer function is realized [2.41]:

$$\frac{V_d}{V_i}=\frac{\frac{R_6}{(R_5+R_6)}\left(s^2\ C^2\ R^2+1\right)}{s^2\ C^2\ R^2+s\frac{2CR\,R_5}{(R_5+R_6)}+1} \tag{2.83}$$

The three outputs of the three opamps in the KHN biquad can be summed using an additional summing amplifier as shown in Fig. 2.17b. The resulting transfer function is given by

$$\frac{V_o}{V_i}=-\frac{s^2\ C^2\ R^2\frac{R_D}{R_C}-sCR\left(2-\frac{1}{Q_p}\right)\frac{R_D}{R_B}+\frac{R_D}{R_A}\left(2-\frac{1}{Q_p}\right)}{s^2\ C^2\ R^2+s\left(\frac{2CR\,R_5}{R_5+R_6}\right)+1} \tag{2.84}$$

Taking into account the finite gain bandwidth product of the three opamps, assuming identical opamps with $B_1=B_2=B_3=B$ and denoting $\tau=CR$, the denominator of the transfer function can be derived as

$$D(s)=2\,s^5\,\frac{\tau^2}{B^3}+s^4\left(\frac{5\tau^2}{B^2}+\frac{4\tau}{B^3}\right)+s^3\left(\frac{6\tau}{B^2}+\frac{4\tau^2}{B}+\frac{2}{B^3}\right)+s^2\left(\tau^2+\frac{1}{B^2}+\frac{2\tau}{B}+\frac{2\beta\tau}{B}\right)+s\left(\frac{2\beta}{B}+2\beta\tau\right)+1 \tag{2.85}$$

Thus the perturbed pole-frequency and pole-Q can be expressed as

$$\frac{\omega_p^2}{\hat{\omega}_p^2}=1+\frac{2\,\omega_p}{B}\left(1+\frac{1}{2\,Q_p}\right)+\frac{\omega_p^2}{B^2} \tag{2.86a}$$

and

$$\frac{\omega_p\ Q_p}{\hat{\omega}_p\ \hat{Q}_p}=1+\frac{\omega_p}{B}\left(1-4\,Q_p\right)-\frac{6\,\omega_p^2\ Q_p}{B^2}-2\,Q_p\left(\frac{\omega_p^3}{B^3}\right) \tag{2.86b}$$

In the KHN biquad, the front-end opamp uses both inputs of the opamps. Hence parasitic capacitance at the noninverting input may affect the frequency response. An alternative circuit known as the *Tow–Thomas biquad* is considered next.

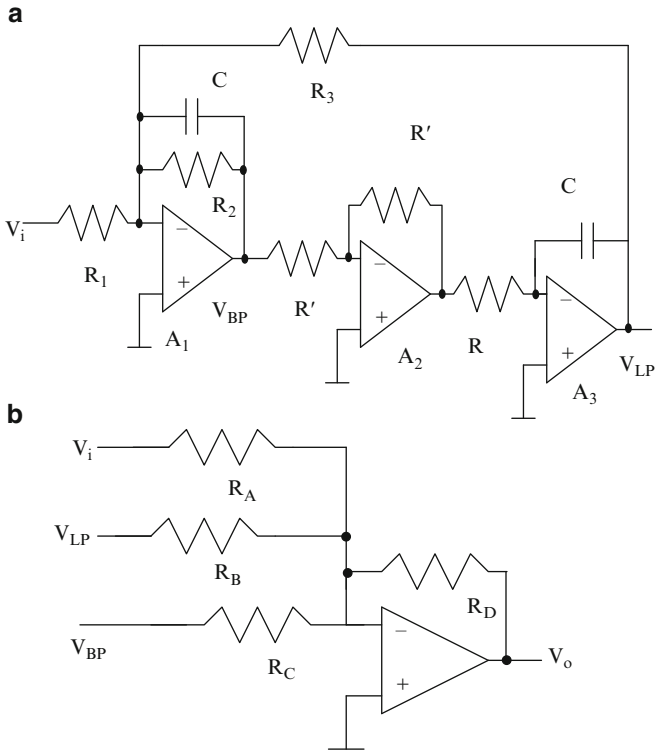


Fig. 2.18 (**a**) Tow–Thomas biquad, and (**b**) summing amplifier to realize a general biquadratic transfer function

2.7.2 Tow–Thomas Biquad

This circuit and the KHN biquad are known as *two-integrator loops*. Essentially, the Tow–Thomas biquad [2.23, 2.42] shown in Fig. 2.18a uses an inverting lossy integrator formed by R_1, R_2, R_3, C, and OA $A_1$and a noninverting lossless integrator formed by R', R, C, and OAs A_2 and A_3 in a feedback loop. The transfer functions of this circuit can be derived as

$$\frac{V_{LP}}{V_i} = -\frac{\frac{R}{R_1}}{s^2\, C^2\, R^2 + sC\frac{R^2}{R_2} + 1}, \quad V_{BP} = -sCR\, V_{LP} \tag{2.87}$$

under the condition $R_3 = R$. Note that an inverting low-pass transfer function is available at the output of opamp 2. Evidently the pole-Q is dependent on R_2/R_3 and the pole-frequency is dependent on R and C. The low-pass transfer function exhibits a dc gain of R/R_1 and the band-pass transfer function has a center frequency gain of R_2/R_1. This circuit evidently enjoys low sensitivities of pole-frequency and pole-Q to passive components.

It is possible to derive a general biquad by using an extra summing amplifier to combine the input and low-pass and band-pass outputs as shown in Fig. 2.18b. The transfer function of this circuit is given by

$$\frac{V_o}{V_i} = -\frac{s^2\, C^2\, R^2\, \frac{R_D}{R_A} + +sCR\left(\frac{R}{R_2}\frac{R_D}{R_A} - \frac{R_D}{R_C}\right) + \frac{R_D}{R_A} - \frac{R_D}{R_B}\frac{R}{R_1}}{s^2\, C^2\, R^2 + sC\frac{R^2}{R_2} + 1} \tag{2.88}$$

Taking into account the finite gain bandwidth product of the three opamps, assuming identical opamps with $B_1 = B_2 = B_3 = B$ and denoting $\tau = CR$, the denominator of the transfer function can be derived as

$$\begin{aligned} D(s) = {} & 2\,s^5\,\frac{\tau^2}{B^3} + s^4\left(\frac{2\tau}{B^3}\left(1 + \frac{1}{Q_p} + \frac{R}{R_1}\right) + \frac{5\tau^2}{B^2} + \frac{2\tau}{B^3}\right) \\ & + s^3\left(\frac{4\tau^2}{B} + \frac{2\tau}{B^2\,Q_p} + \frac{3\tau}{B^2}\left(2 + \frac{1}{Q_p} + \frac{R}{R_1}\right) + \frac{2}{B^3}\left(1 + \frac{1}{Q_p} + \frac{R}{R_1}\right)\right) \\ & + s^2\left(\tau^2 + \frac{\tau}{B}\left(2 + \frac{1}{Q_p} + \frac{R}{R_1}\right) + \frac{2}{B^2\,Q_p} + \frac{3\tau}{B\,Q_p} + \frac{1}{B^2}\left(1 + \frac{1}{Q_p} + \frac{R}{R_1}\right)\right) \\ & + s\left(\frac{1}{B\,Q_p} + \frac{\tau}{Q_p}\right) + 1 \end{aligned} \tag{2.89}$$

Thus the perturbed pole-frequency and pole-Q can be expressed as

$$\frac{\omega_p^2}{\hat{\omega}_p^2} = 1 + \frac{\omega_p}{B}\left(2 + \frac{4}{Q_p} + \frac{R}{R_1}\right) + \frac{\omega_p^2}{B^2}\left(1 + \frac{3}{Q_p} + \frac{R}{R_1}\right) \tag{2.90a}$$

and

$$\begin{aligned} \frac{\omega_p\, Q_p}{\hat{\omega}_p\, \hat{Q}_p} = {} & 1 + \frac{\omega_p}{B}\left(1 - 4\,Q_p\right) - \frac{\omega_p^2\, Q_p}{B^2}\left(6 + \frac{5}{Q_p} + \frac{3R}{R_1}\right) - 2\,Q_p\left(\frac{\omega_p^3}{B^3}\right) \\ & \times \left(1 + \frac{1}{Q_p} + \frac{R}{R_1}\right) \end{aligned} \tag{2.90b}$$

Example 2.7 Plot the low-pass and band-pass transfer functions of the Tow–Thomas biquad shown in Fig. E.2.7. using a nonideal macromodel of the opamp. The biquad is designed for a pole-frequency = 100 KHz, midband gain of band-pass response, and pole-Q of 40.

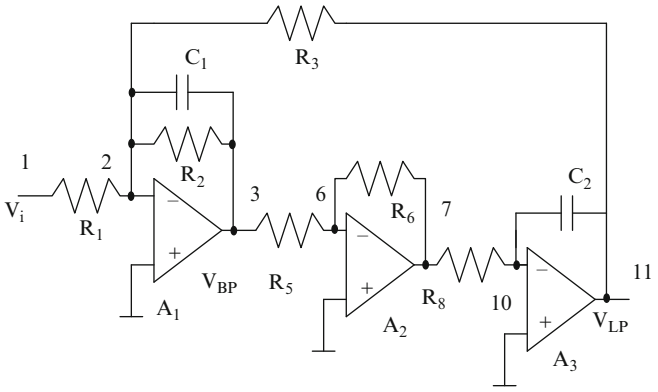
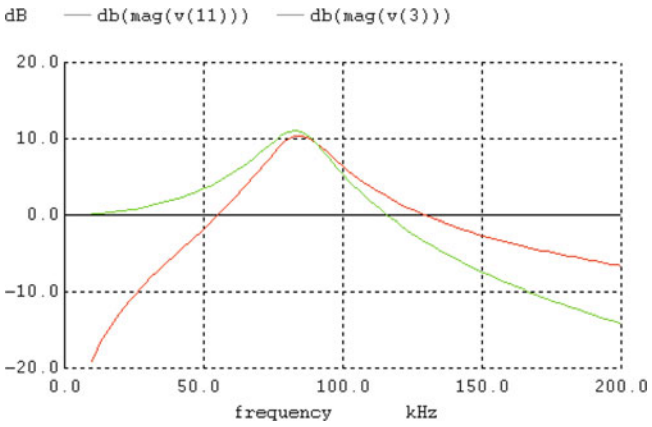


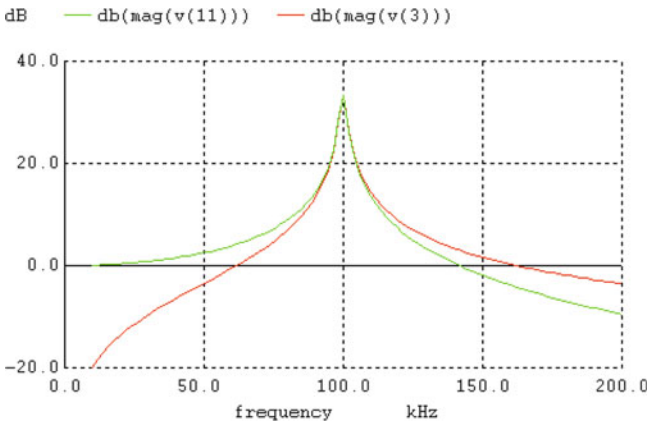
Fig. E.2.7

The two transfer functions can be seen to have slightly different peaks so that scaling will be necessary to equalize the outputs. The pole-frequency evidently has decreased due to the finite bandwidth of the opamps.

```
*Tow–Thomas biquad
R1 1 2 10 K
R2 2 3 400 K
C1 2 3 159 pf
R3 2 11 10 K
E1 0 4 2 0 100,000
R4 4 5 1 k
C3 5 0 15.9 uf
E2 3 0 5 0 1
R5 3 6 10 K
R6 6 7 10 K
E3 0 8 6 0 100,000
R7 8 9 1 k
C4 9 0 15.9 uf
E4 7 0 9 0 1
R8 7 10 10 K
C2 10 11 159 pf
E5 0 12 10 0 100,000
R9 12 13 1 k
C5 13 0 15.9 uf
E6 11 0 13 0 1
vin 1 0 ac 1v
.ac dec 1000 1 1,500 k
```



(**a**) With 1 MHz bandwidth opamps



(**b**) With opamp bandwidth 100 MHz

2.7.3 Akerberg–Mossberg Biquad

Akerberg and Mossberg [2.24] suggested an active compensation technique without using any additional components. The noninverting integrator realization based on this approach has already been described in Fig. 2.4d. The denominator of the transfer function of this biquad shown in Fig. 2.19 can be derived as

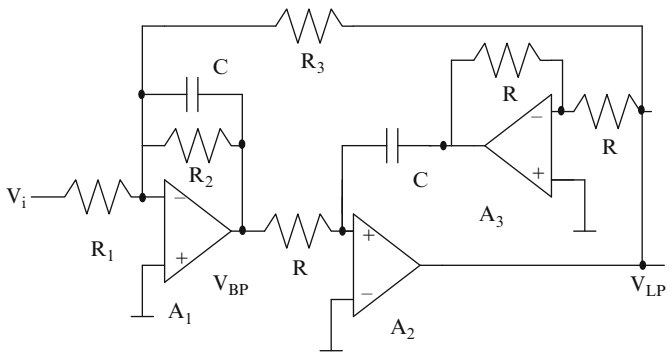


Fig. 2.19 Akerberg–Mossberg biquad

$$D(s) = s^5\left(\frac{2\tau^2}{B^3}\right) + s^4\left(\frac{2\tau}{B^3\,Q_p} + \frac{6\tau}{B^3} + + \frac{3\tau^2}{B^2}\right) + s^3\left(\frac{4}{B^3} + \frac{5\tau}{B^2} + \frac{2}{B^3\,Q_p} + \frac{3\tau}{B^2\,Q_p} + \frac{2\tau^2}{B}\right) + s^2\left(\frac{2}{B^2} + \frac{3\tau}{B} + \frac{3}{B^2\,Q_p} + \frac{2\tau}{B\,Q_p} + \tau^2\right) + s\left(\frac{1}{B\,Q_p} + \frac{\tau}{Q_p} + \frac{2}{B}\right) + 1 \tag{2.91}$$

Thus the perturbed pole-frequency and pole-Q can be expressed as

$$\frac{\omega_p^2}{\hat{\omega}_p^2} = 1 + \frac{\omega_p}{B}\left(3 + \frac{2}{Q_p}\right) + \frac{\omega_p^2}{B^2}\left(2 + \frac{3}{Q_p}\right) \tag{2.92a}$$

and

$$\frac{\omega_p\,Q_p}{\hat{\omega}_p\,\hat{Q}_p} = 1 + \frac{\omega_p}{B} - \frac{\omega_p^2\,(5\,Q_p + 3)}{B^2} - (2 + 4\,Q_p)\left(\frac{\omega_p^3}{B^3}\right) \tag{2.92b}$$

It may be seen by comparing (2.92) with (2.90) that the pole-Q variation is much smaller than in the Tow–Thomas biquad.

2.7.4 Scaling for Optimal Dynamic Range

A good design practice in both KHN and Tow–Thomas biquads is to choose equal time constants for both integrators for high pole-Q designs. This choice has the advantage that the maxima of all the outputs of the opamps tend to be the same for

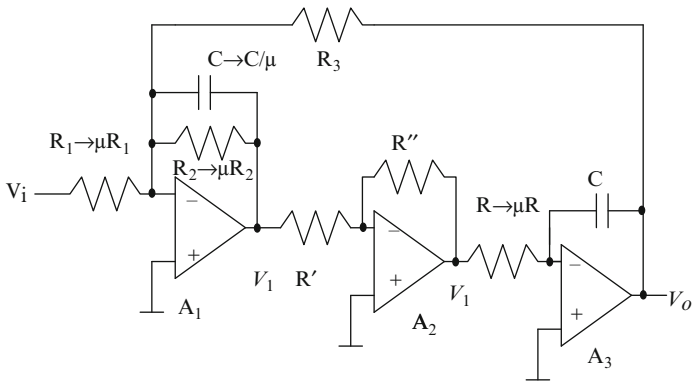


Fig. 2.20 Procedure for scaling for optimal dynamic range in Tow–Thomas biquad

high pole-Q designs. For low pole-Q designs, however, it is necessary to find the maximum of the transfer functions at all three outputs of the three opamps (in the case of the Tow–Thomas biquad only two) and then they need to be scaled to bring these maxima to the maximum of the actual given transfer function. This procedure is known as *scaling for optimal dynamic range*. The advantage of this step is explained next using Fig. 2.20.

Consider that we are interested in the desired output V_o. Its maximum value (i.e., $|V_o(j\omega)|_{\max}$) can be estimated. Similarly, the output V_1 and $-V_1$ will have a maximum value $|V_1(j\omega)|_{\max}$ which may occur at a different frequency. It may happen that these two maxima are widely different in magnitudes. The purpose of dynamic range scaling is to equalize these maxima by introducing a scaling factor μ such that $\mu|V_1(j\omega)|_{\max} = |V_o(j\omega)|_{\max}$. This ensures that the input signal can be increased safely and either V_o or V_1 saturate at the same input level. This scaling to change V_1 to μV_1 can be accomplished by changing R_2 and C in the feedback path of opamp A_1 to μR_2 and C/μ. Since the gain of the stage using resistors R' and R'' is unity, these can be retained as they are. Since the output V_1 has changed, the loop gain can be kept constant by changing R to μR in the third stage. The maxima of the second-order transfer function can be obtained through closed-form formulae [2.40] presented in Appendix B or by plotting to find out the maximum.

2.7.5 *Variants of Tow–Thomas and KHN Biquads*

Several alternative forms of TT and KHN biquads can be derived by using the nodal voltage simulation technique [2.41] from the single amplifier multiple-feedback low-pass filter of Fig. 2.16a. Note that earlier, circuits using only the inverting input of the opamp were derived. On the other hand, in these circuits (see, e.g., Fig. 2.16c), an internal node still existed where parasitic capacitances were present.

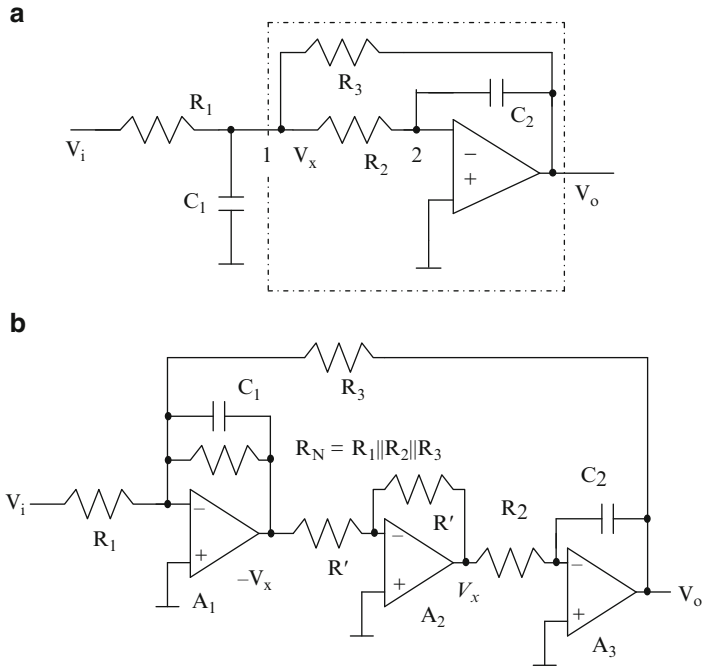


Fig. 2.21 (**a**) Multiple-feedback low-pass filter, and (**b**) circuit derived from (a) using nodal voltage simulation (Adapted from [2.41] ©IEEE 1985)

These internal nodes also can be eliminated by applying the nodal voltage simulation technique described next.

Consider the multiple feedback active RC filter of Fig. 2.21a. By writing nodal equations at nodes 1 and 2, the circuit of Fig. 2.21b can be constructed. Note that $-V_x$ is realized first and then using an inverting amplifier of unity gain, V_x is realized. The circuit used to realize V_o from V_x is preserved. Thus the nodal voltages are preserved in the new circuit. The similarity of the circuit of Fig. 2.21b to the Tow–Thomas biquad can be observed except that the damping (pole-Q determining) resistor is dependent on three resistors R_1, R_2, and R_3 in which place a single resistor R_N can be used to control the pole-Q.

We next consider the circuit of Fig. 2.22a, which is Fig. 2.12a redrawn for convenience. The equivalent circuit shown in Fig. 2.22b can be derived easily. Note that this circuit uses four opamps. The circuit cannot, however, realize a band-pass transfer function at node x similar to that in Fig. 2.22a. The transfer function of the circuit of Fig. 2.22b without considering the relationship of component values to those in the circuit of Fig. 2.22a can be seen to be

$$\frac{V_o}{V_i} = \frac{-1/R_1}{s^2\, C_1\, C_2\, R_4 + s\left(\frac{C_2\, R_4}{R_6} - \frac{C_1\, R_4}{R_5}\right) + \left(\frac{1}{R_7} - \frac{R_4}{R_5\, R_6}\right)} \tag{2.93}$$

Under the condition $C_1 = C_2 = C$, $R_7 = R_4 = R$, and $R_6 = Q_o R_4$, $R_5 = R_4/m$, we have

$$Q_p = \frac{\sqrt{(Q_o - m)\,Q_o}}{1 - m\,Q_o} \quad \text{and} \quad \omega_p = \omega_o \sqrt{1 - \frac{m}{Q_o}} \tag{2.94a}$$

The pole-Q sensitivities are as follows.

$$S_m^{Q_p} = -\frac{m}{2(Q_o - m)} + \frac{Q_p}{\sqrt{1 - \frac{m}{Q_o}}} \tag{2.94b}$$

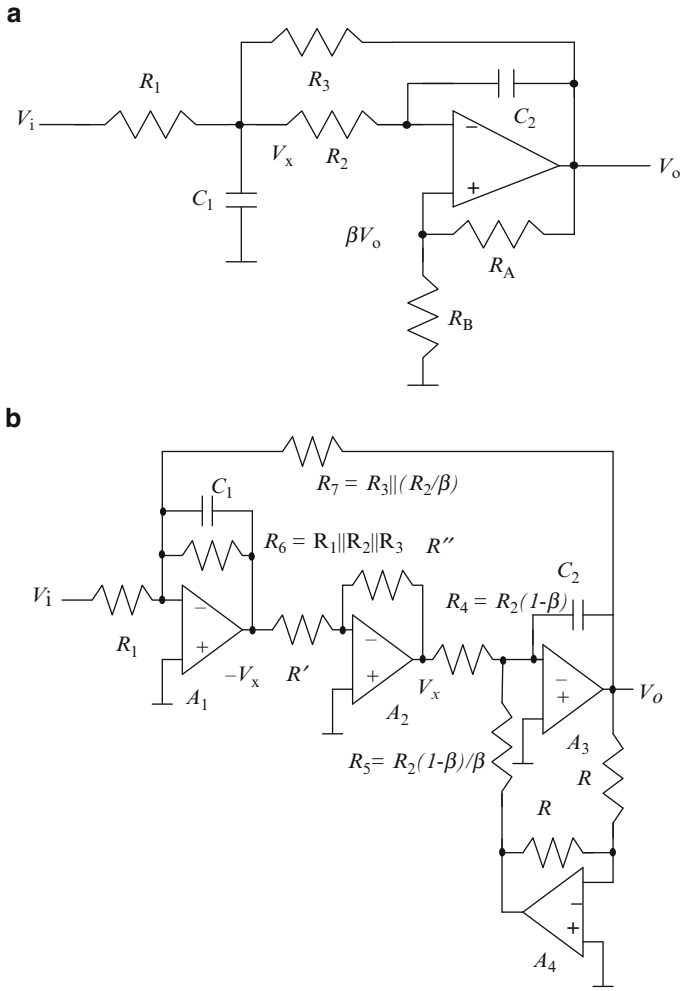


Fig. 2.22 (**a**) A multiple-feedback low-pass filter with positive feedback, (**b**) circuit obtained by nodal voltage simulation, (**c**) modification of (b), and (**d**) modification of (c) ((*b–d*) Adapted from [2.41] ©IEEE 1985)

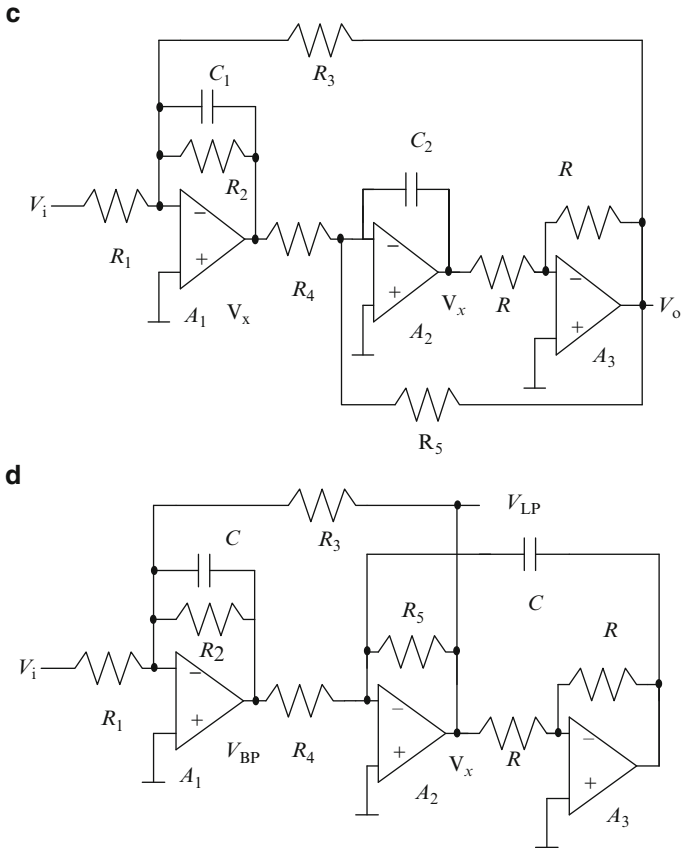


Fig. 2.22 (continued)

Thus, the Q_p-sensitivities can be large for finite m.

The circuit of Fig. 2.22b can be simplified as shown in Fig. 2.22c needing only three opamps. This circuit has same design equations as that of Fig. 2.22b. We next observe that the circuit of Fig. 2.22c can be rearranged to obtain another circuit shown in Fig. 2.22d which realizes effectively a noninverting integrator akin to the Akerberg–Mossberg biquad. Note, however, the advantage is the reduction in the spread of component values while achieving phase compensation. It is important to note that the polarity of the opamp input terminals is different in the Akerberg–Mossberg biquad.

In order to reduce the capacitor spread, a negative resistance realized using opamp A_2, resistors $(\alpha - 1)R, R$, and R_F can be shunted to ground at the V_x terminal as shown in Fig. 2.23a [2.43]. The corresponding circuit obtained by nodal voltage simulation is as shown in Fig. 2.23b. The transfer function of this circuit can be obtained as

$$\frac{V_o}{V_i} = \frac{-1/R_1}{s^2\, C_1\, C_2\, R_2 + s\, C_2\, R_2 \left(\frac{1}{R_N} - \frac{1}{R_5}\right) + \frac{1}{R_3}} \tag{2.95}$$

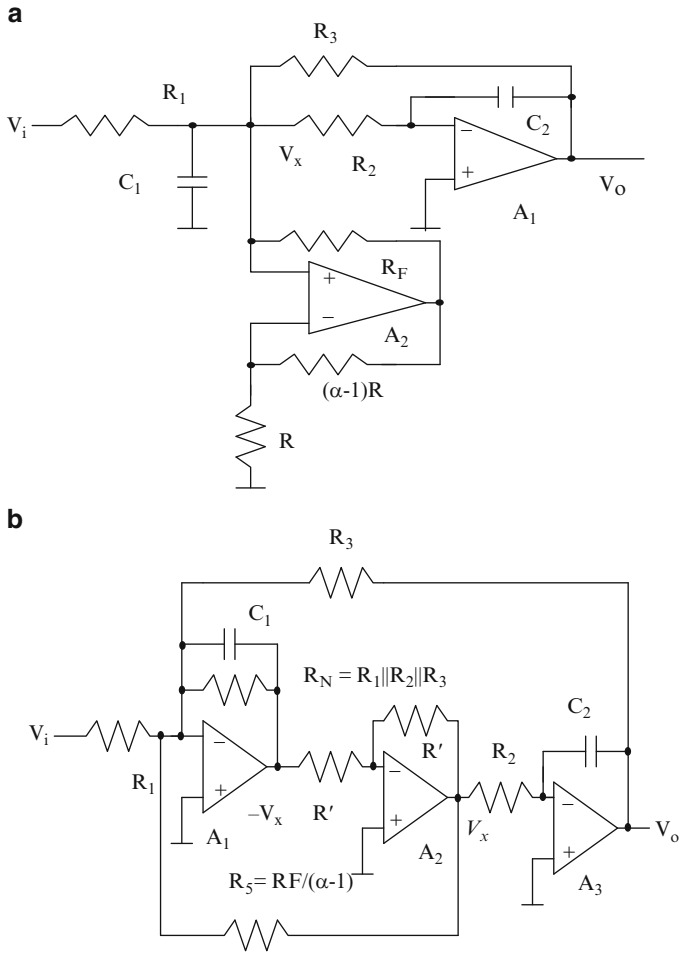


Fig. 2.23 (**a**) A multiple-feedback active RC filter using negative resistance for Q-enhancement, and (**b**) circuit obtained from (a) using nodal voltage simulation (Adapted from [2.41] ©IEEE 1985)

Thus although the pole-frequency is the same as that without the use of negative resistance, pole-Q is affected by R_5. For the choice $C_1 = C_2 = C$, $R_3 = R_2 = R$, we have $S_{R_5}^{Q_p} = -\frac{Q_p R_2}{R_5}$ and $S_{R_N}^{Q_p} = \frac{Q_p R_2}{R_N}$ which can be large and $S_{R_2}^{Q_p} = -1$.

Nodal voltage simulation technique can be applied to the KHN biquad redrawn in Fig. 2.24a as well since it uses one opamp where both input terminals are used. The circuit of Fig. 2.24b is the exact equivalent of the KHN biquad and needs four opamps and has the four transfer functions LP, BP, HP, and band-reject types at the outputs of the four opamps. Two rearrangements of this circuit are shown in Fig. 2.24c, d that do not change the internal transfer functions but change the sign

of the LP transfer function. In the circuit of Fig. 2.24c, the integrator and amplifier positions are changed. It uses a differential integrator formed by opamps A_2 and A_3, resistors R around A_2, resistors R_4, R_7 (=R_2), and capacitor C_2, and a noninverting integrator formed by resistors R around opamp A_5, and R_1,C_1 around OA A_4. Note that the high-pass transfer function is not realized. On the other hand, in the circuit of Fig. 2.24d, both feedback loops feed to the input opamp A_1. The circuit uses two noninverting integrators. Note that the circuit of Fig. 2.24d only realizes HP, BP, and LP transfer functions. These modifications have been used in deriving SC (switched-capacitor) filters.

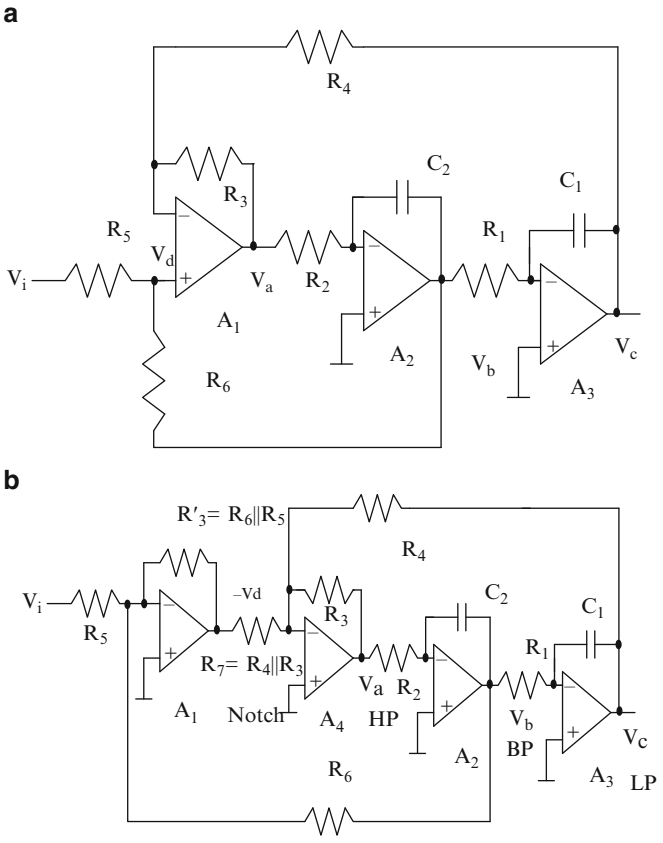


Fig. 2.24 (**a**) KHN biquad, (**b**) circuit obtained by nodal voltage simulation of (a), (**c**) modification of (b), and (**d**) another modification which feeds both outputs to the first opamp suitable for deriving SC filters (Adapted from [2.41] ©IEEE 1985)

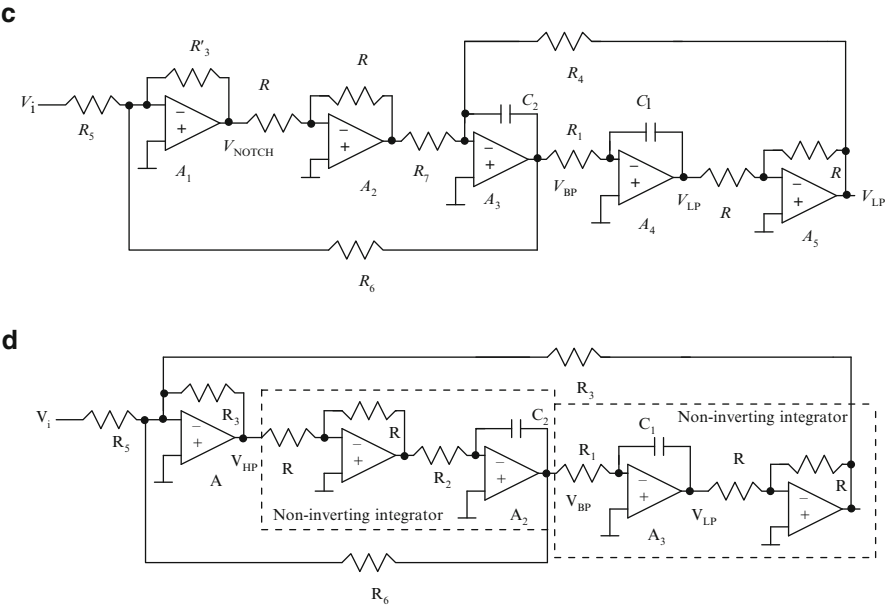


Fig. 2.24 (continued)

2.7.6 *Tarmy–Ghausi–Moschytz Three Opamp Biquad and Its Variations*

This is an interesting biquad [2.44, 2.45] which uses two first-order all-pass networks in a negative feedback loop. In this circuit, shown in Fig. 2.25a, the OA A_2 resistors R', R, and C (and similarly the OA A_3 resistors R', R, and C) realize a first-order all-pass transfer function H(s) given by

$$H(s) = \frac{1 - sCR}{1 + sCR} \tag{2.96}$$

The transfer function of this circuit can be derived as

$$\frac{V_o}{V_i} = -\frac{R_3}{R_1\left(1 + \frac{R_3}{R_2}\right)} \frac{\left(s^2\ C^2\ R^2 + 2sCR + 1\right)}{\left(s^2\ C^2\ R^2 + s\frac{2CR\left(\frac{R_3}{R_2} - 1\right)}{\left(1 + \frac{R_3}{R_2}\right)} + 1\right)} \tag{2.97}$$

Even though there are real zeroes, these do not affect the transfer function much. The pole-frequency and pole-Q can be derived as $\omega_p = \frac{1}{CR}$ and $Q_p = \frac{\left(1 + \frac{R_3}{R_2}\right)}{2\left(\frac{R_3}{R_2} - 1\right)}$.

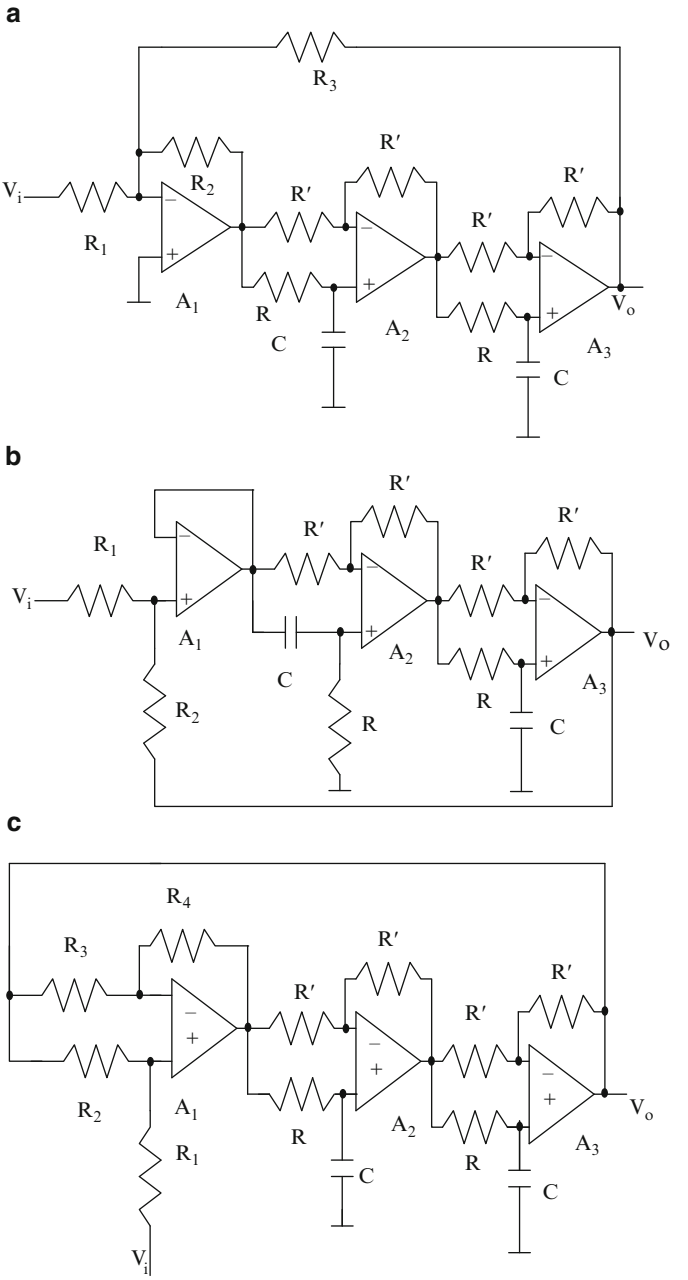


Fig. 2.25 (**a**) Tarmy–Ghausi band-pass filter modification due to Moschytz, (**b**) and (**c**) modifications of (a) to decrease the pole-Q sensitivity

The mid-band gain (i.e., gain at ω_p) is $\frac{R_3}{R_1}\frac{(2Q_p-1)}{2}$. Note that the sensitivity of Q_p to R_3/R_2 is large:

$$S_{\frac{R_3}{R_2}}^{Q_p} = -Q_p + \frac{1}{4Q_p} \tag{2.98}$$

Several interesting solutions [2.46, 2.47] have been suggested in the literature to reduce the pole-Q sensitivity. These use different techniques of implementation of the feedback loop while retaining the two first-order all-pass filters.

In the circuit of Fig. 2.25b, note that one inverting first-order all-pass filter and one noninverting first-order all-pass filter are used. The transfer function of this circuit can be derived as

$$\frac{V_o}{V_i} = -\frac{R_2}{(2R_1+R_2)}\frac{\left(s^2\ C^2\ R^2 - 2sCR + 1\right)}{\left(s^2\ C^2\ R^2 + s\frac{2CR}{(2R_1+R_2)} + 1\right)} \tag{2.99a}$$

The resulting pole-Q is given as

$$Q_p = \frac{R_1}{R_2} + \frac{1}{2} \tag{2.99b}$$

and the midband gain is unity. Thus, it is seen that the sensitivity of pole-Q is reduced considerably. In the alternative circuit shown in Fig. 2.25c, the realized transfer function is

$$\frac{V_o}{V_i} = \frac{\left(s^2\ C^2\ R^2 - 2sCR + 1\right)}{\left(s^2\ C^2\ R^2 + s\frac{2CR(2R_3\ R_1 + R_2\ R_3 - R_4\ R_2)}{R_2\ (R_3+R_4)} + 1\right)} \tag{2.100}$$

The resulting pole-Q under the condition $R_3 = R_4$ is given as

$$Q_p = \frac{R_2}{2R_1} \tag{2.101}$$

Thus, in this case as well, the Q-sensitivity is considerably reduced.

2.8 Second-Order Active Filters Using Amplifier Pole and One Capacitor

2.8.1 Using Single Capacitor

We consider a differentiator circuit shown in Fig. 2.26a. The transfer function of this circuit considering a nonideal opamp is given by

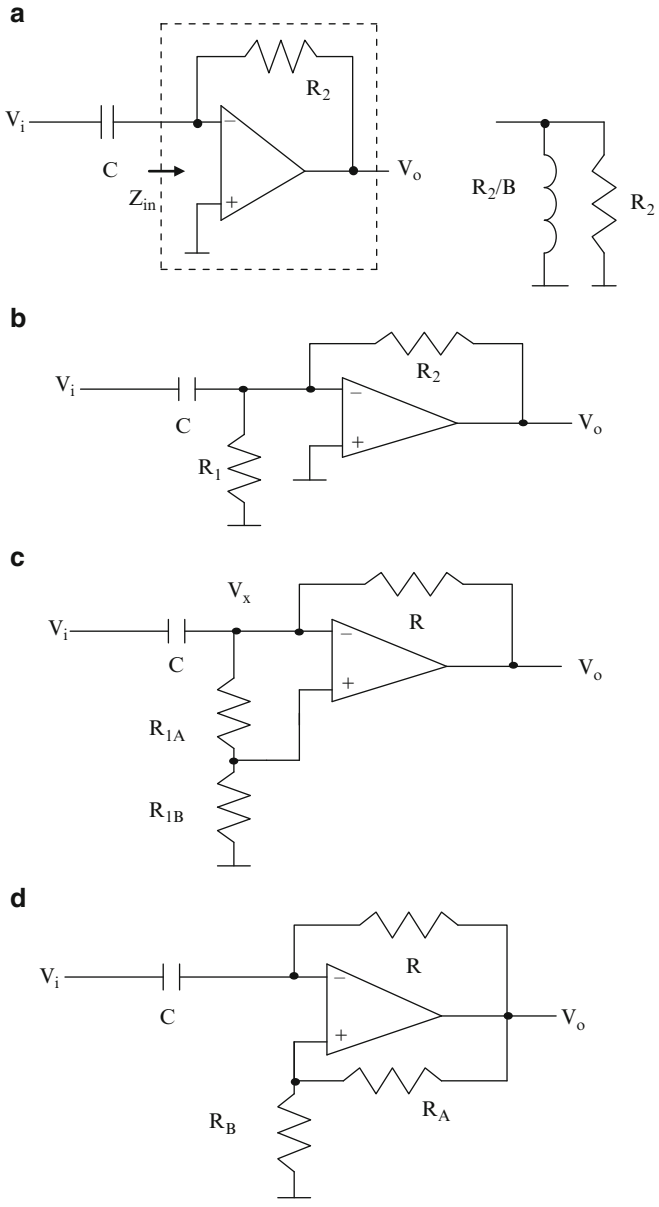


Fig. 2.26 (**a**) An active RC differentiator behaving as a second-order band-pass filter, (**b**) modification of (a) to realize variable pole-Q, (**c**) modification of (b) to change pole-frequency, (**d**) modification of (a) using positive feedback, (**e**) Rao and Srinivasan's low-pass/band-pass filter, (**f**) simplification of (e) to realize a low-pass/band-pass filter, and (**g**) a simplification of (e) to realize a notch filter (b Adapted from [2.48] © IEEE1977, d,e Adapted from [2.49] ©IEEE 1979, f, g adapted from [2.52] ©IEEE 1979)

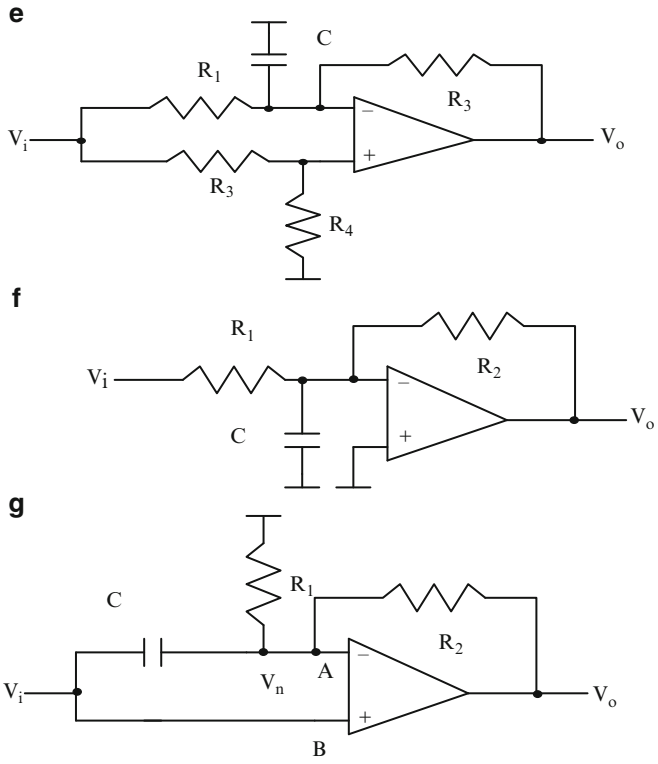


Fig. 2.26 (continued)

$$\frac{V_o}{V_i} = -\frac{-sB}{\left(s^2 + \frac{s}{CR_2} + \frac{B}{CR_2}\right)} \tag{2.102}$$

This is a band-pass transfer function with the pole-frequency being $\omega_p = \sqrt{\frac{B}{CR_2}}$ and $Q_p = \sqrt{BCR_2}$. Interestingly maximum $\omega_p Q_p = B$ thus showing that a band-pass filter with large pole-frequencies can be realized with moderate Q. It is interesting to note that a high-pass transfer function is realized at the inverting input of the OA. It may be appreciated that in effect the opamp with feedback resistor R_2 realizes a grounded inductor of value R_2/B shunted by a resistance R_2 as shown in Fig. 2.26a. Note that the addition of a resistance [2.48] as shown in Fig. 2.26b facilitates changing the pole-Q without changing the pole-frequency. The resulting transfer function of this circuit is given as

$$\frac{V_o}{V_i} = -\frac{-sB}{\left(s^2 + \frac{s}{C}\left(\frac{1}{R_1} + \frac{1}{R_2}\right) + \frac{B}{CR_2}\right)} \tag{2.103}$$

Thus, the pole-Q can be controlled by R_1. Note, however, that the resulting ω_p $Q_p = \frac{BR_1}{R_1+R_2}$ is less than B. The pole-frequency of the filter can be controlled by using a potential divider formed by resistors R_{1A} and R_{1B} in place of the resistor R_1 in Fig. 2.26b as shown in Fig. 2.26c. Note that the opamp is characterized in this case by the equation $V_o = -V_x\beta B/s$ effectively showing that the bandwidth has become βB where $\beta = \frac{R_{1A}}{R_{1A}+R_{1B}}$. Note, however, that modified bandwidth βB is less than the actual bandwidth B.

The realizable pole-Q can be enhanced using positive feedback [2.49] as shown in Fig. 2.26d. This circuit realizes a transfer function given by

$$\frac{V_o}{V_i} = -\frac{-sB}{\left(s^2 + s\left(\frac{1}{CR} - \beta B\right) + \frac{(1-\beta)B}{CR}\right)} \tag{2.104}$$

where $\beta = \frac{R_B}{R_A+R_B}$.

Interestingly, arbitrary pole-Q can be realized but the pole-frequency is also dependent on β. The circuit will realize a sinusoidal oscillator when $\beta = \frac{1}{BCR}$. The resulting frequency of oscillation is given as $B\sqrt{\beta(1-\beta)}$ showing that the maximum frequency of oscillation is $B/2$ when $\beta = 1/2$. The use of a positive feedback factor β larger than $1/BCR$ will lead to a relaxation oscillator. Most textbooks describe this circuit as a relaxation oscillator that can generate square and triangular waveforms [2.50].

Another interesting filter based on opamp pole [2.51] is presented in Fig. 2.26e. Note that this circuit realizes a transfer function given by

$$\frac{V_o}{V_i} = -\frac{s\beta B + \frac{B}{C}\left(\frac{\beta-1}{R_1} + \frac{\beta}{R_2}\right)}{\left(s^2 + \frac{s}{C}\left(\frac{1}{R_1} + \frac{1}{R_2}\right) + \frac{B}{CR_2}\right)} \tag{2.105}$$

where $\beta = \frac{R_4}{R_3+R_4}$. Note that under the condition $\beta = \frac{R_2}{R_1+R_2}$, a band-pass transfer function is realized. When $\beta = 0$ (see Fig. 2.26f), a low-pass transfer function is realized [2.52] as can be easily guessed by noting that the opamp with feedback resistance R_2 realizes a lossy grounded inductance that together with resistor R_1 (as shown before; see Fig. 2.26a) and capacitor C forms a RLC tank circuit. When $\beta = 1$ (in which case $R_4 = \infty$ and $R_3 = 0$; see Fig. 2.26g), a notch transfer function is realized [2.52] at the inverting input of the OA suggesting that a floating inductance is realized between A and B terminals with a parasitic resistance as shown in the equivalent circuit in Fig. 2.26g. At the output of OA A_1, a low-pass transfer function is realized:

$$\frac{V_n}{V_i} = -\frac{s^2 + \frac{B}{CR_2}}{\left(s^2 + \frac{s}{C}\left(\frac{1}{R_1} + \frac{1}{R_2}\right) + \frac{B}{CR_2}\right)} \tag{2.106a}$$

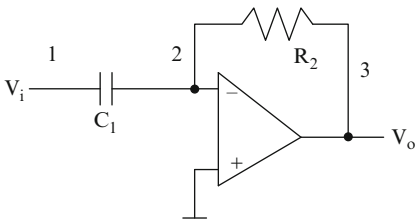


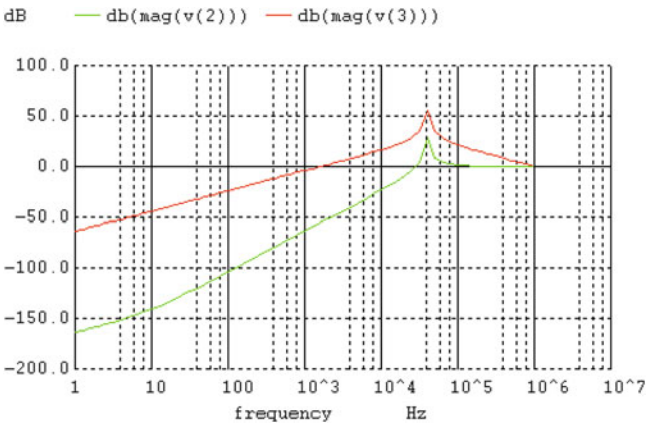
Fig. E.2.8

$$\frac{V_o}{V_i} = -\frac{\frac{B}{C}\left(\frac{1}{R_1}+\frac{1}{R_2}\right)}{\left(s^2+\frac{s}{C}\left(\frac{1}{R_1}+\frac{1}{R_2}\right)+\frac{B}{CR_2}\right)} \tag{2.106b}$$

Example 2.8 Determine the frequency response at the output and inverting input of the opamp of the differentiator using a nonideal opamp with finite bandwidth of 1 MHz (Fig. E.2.8).

It can be seen that the differentiator circuit behaves as a band-pass filter and at virtual ground node, a high-pass response can be seen. The midband gain of the band-pass response is $BCR = 628$ and pole-frequency is 40 KHz.

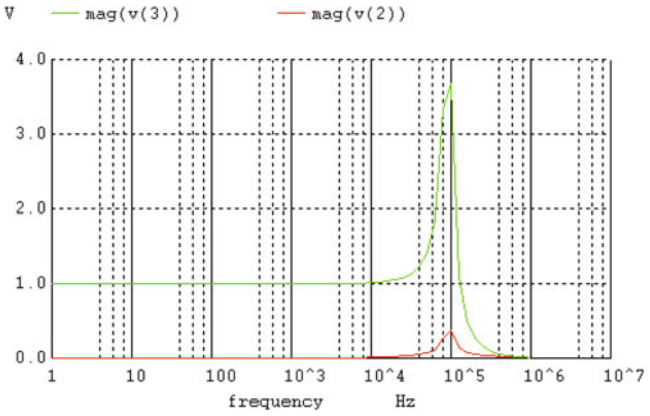
```
*Nonideal differentiator
C1 1 2 0.1 uf
R1 2 3 1 K
E1 0 4 2 0 100,000
R3 4 5 1 k
C3 5 0 15.90 uf
E2 3 0 5 0 1
vin 1 0 ac 1 v
.ac dec 10 1 1,000 K
```



Example 2.9 Determine the frequency response at the output and inverting input of the opamp of the active-G_m-RC filter of Fig. 2.26f using a nonideal opamp with finite bandwidth of 1 MHz.

It can be seen that a low-pass response is realized at the output of the opamp and a band-pass response at the inverting input of the opamp. The pole-frequency is 91.84 Hz.

```
*Low-pass filter using amplifier pole
vin 1 0 ac 1 v
R1 1 2 18.86 K
C1 2 0 0.001 uf
R2 2 3 18.86 K
E1 0 4 2 0 100,000
R3 4 5 1 K
C3 5 0 15.90 uf
E2 3 0 5 0 1
.ac dec 10 1 1,000 K
```



2.8.2 *Second-Order Filters Using Only Resistors and Amplifier Poles*

The capacitors can be eliminated altogether in active filters by using the poles of two opamps and only resistors. This is feasible by recognizing the fact that the opamp basically is an integrator and hence two-integrator loops can be built to realize biquadratic transfer functions. The simplest two-integrator loop using opamps and resistors is shown in Fig. 2.27a. The transfer function of this circuit is given by

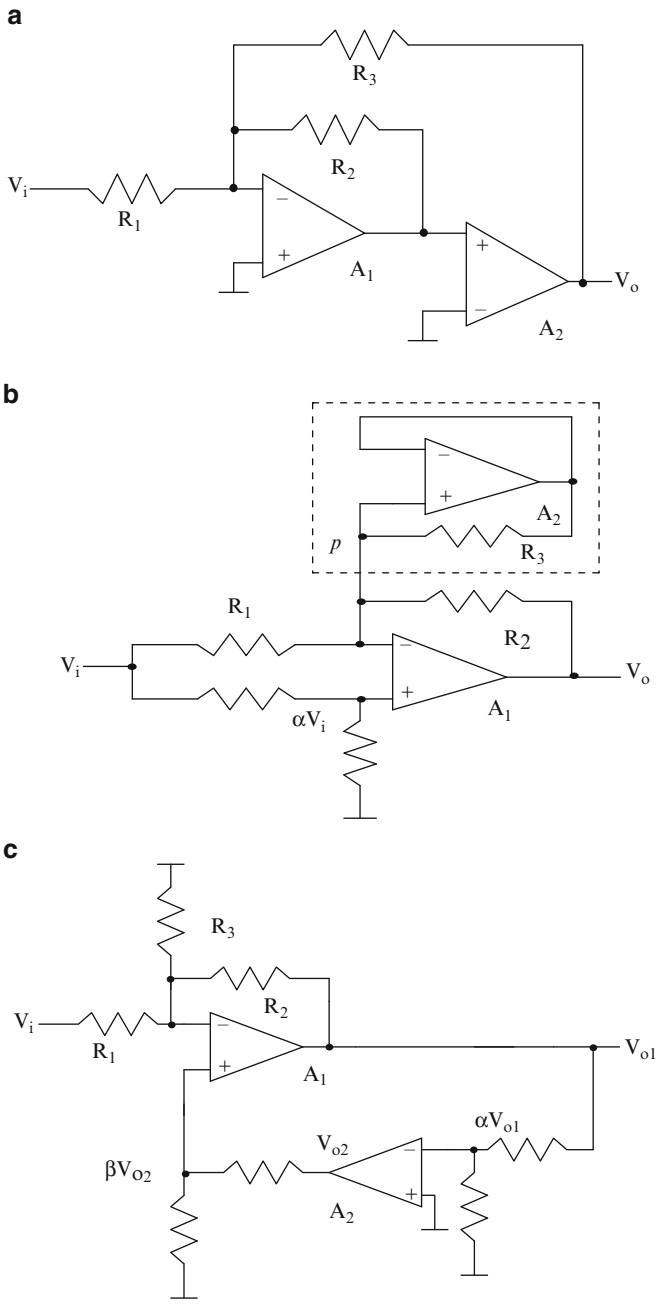


Fig. 2.27 Active R-filters: (**a**) based on two-integrator loop, (**b**) Ananda–Mohan structure based on Rao–Srinivasan filter of Fig. 3.25e, (**c**) Mitra–Aatre structure. Active R filters due to (**d**) and (**e**) Rao and Srinivasan [2.55] and (**f**) Schaumann [2.56] (**b**) Adapted from [2.53] ©IEE 1980, (**c**) Adapted from [2.54] ©IEEE 1976, (**d**,**e**) Adapted from [2.55] ©IEE 1974, (**f**) Adapted from [2.56] ©IEE 1974)

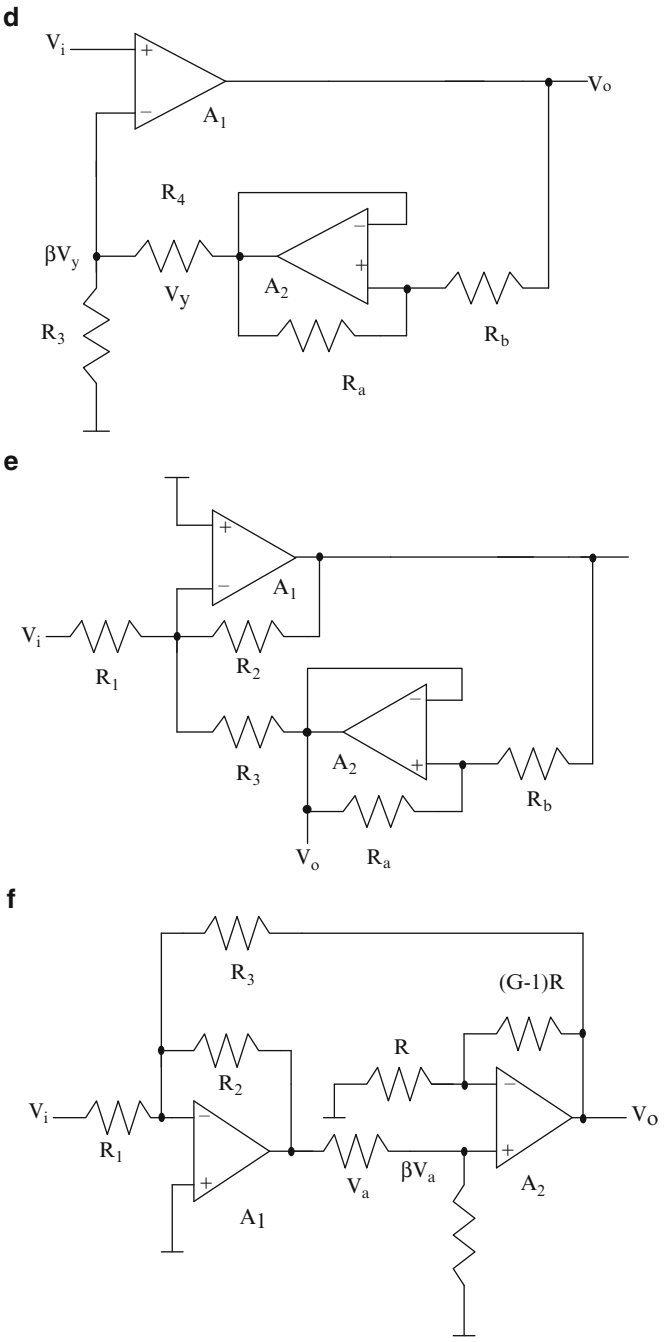


Fig. 2.27 (continued)

$$\frac{V_n}{V_i} = -\frac{-\frac{R_3}{R_1}}{\left(\frac{s^2}{B_1 B_2}\left(\frac{R_3}{R_1}+\frac{R_3}{R_2}+1\right)+\frac{s}{B_2}\left(\frac{R_3}{R_2}\right)+1\right)} \tag{2.107a}$$

and

$$\frac{V_a}{V_o} = -\frac{s}{B_2} \tag{2.107b}$$

Thus the dc gain is given by R_3/R_1 and independent control of pole-frequency and pole-Q is not possible. A band-pass transfer function is also available (see (2.107b)).

Another active R filter can be obtained from the low-pass filter derived from the Rao and Srinivasan filter using the opamp pole and one capacitor as shown in Fig. 2.26e [2.51] by replacing the capacitor C with a lossy simulated capacitor using the amplifier pole [2.53]. The resulting circuit is shown in Fig. 2.27b. Note that the OA A_2 and resistor R_3 will yield an input impedance at the terminal p given by

$$Z_{in} = R_3 + \frac{B_2\ R_3}{s} \tag{2.108}$$

The resulting transfer functions of the circuit at both outputs of the opamps are given by

$$\frac{V_o}{V_i} = -\frac{\left(\frac{1-\alpha}{R_1}-\frac{\alpha}{R_2}-\frac{\alpha}{R_4}\right)+\frac{s}{B_2}\left(\frac{1-\alpha}{R_1}-\frac{\alpha}{R_2}-\frac{\alpha}{R_3}-\frac{\alpha}{R_4}\right)}{\left(\frac{s^2}{B_1 B_2}\left(\frac{1}{R_1}+\frac{1}{R_2}+\frac{1}{R_3}+\frac{1}{R_4}\right)+s\left(\frac{1}{B_1}\left(\frac{1}{R_1}+\frac{1}{R_2}+\frac{1}{R_4}\right)+\frac{1}{B_2 R_2}\right)+\frac{1}{R_2}\right)} \tag{2.109a}$$

and

$$\frac{V_x}{V_i} = -\frac{\frac{s}{B_1 R_1}+\frac{\alpha}{R_2}}{\left(\frac{s^2}{B_1 B_2}\left(\frac{1}{R_1}+\frac{1}{R_2}+\frac{1}{R_3}+\frac{1}{R_4}\right)+s\left(\frac{1}{B_1}\left(\frac{1}{R_1}+\frac{1}{R_2}+\frac{1}{R_4}\right)+\frac{1}{B_2 R_2}\right)+\frac{1}{R_2}\right)} \tag{2.109b}$$

Evidently, a band-pass transfer function and a low-pass filter transfer function can be realized at V_o when

$$\frac{1-\alpha}{R_1} = \frac{\alpha}{R_2}+\frac{\alpha}{R_4} \tag{2.110a}$$

$$\frac{1-\alpha}{R_1} = \frac{\alpha}{R_2}+\frac{\alpha}{R_3}+\frac{\alpha}{R_4} \tag{2.110b}$$

Note also that V_x realizes a band-pass transfer function when $\alpha = 0$.

Mitra and Aatre [2.54] have described an active-R filter using opamps as shown in Fig. 2.27c. The transfer function of this circuit can be derived as

$$\frac{V_{o1}}{V_i} = \frac{-\frac{sB_1}{R_1}}{s^2\left(\frac{1}{R_1}+\frac{1}{R_2}+\frac{1}{R_3}\right)+\frac{sB_1}{R_3}+\alpha\beta B_1\, B_2\left(\frac{1}{R_1}+\frac{1}{R_2}+\frac{1}{R_3}\right)} \tag{2.111}$$

This realizes a band-pass transfer function with a center frequency gain R_2/R_1, and pole-frequency and pole-Q given as

$$\omega_p = \sqrt{\alpha\beta B_1\, B_2} \tag{2.112a}$$

$$Q_p = \sqrt{\frac{\alpha\beta B_2}{B_1}}\left(\frac{R_2}{R_1}+\frac{R_2}{R_3}+1\right) \tag{2.112b}$$

Thus the pole-Q is controlled by ratios of resistors and ratios of bandwidths of the opamps and the pole-frequency is dependent on opamp bandwidths. The maximum pole-frequency is evidently B where $B_1 = B_2 = B$ and $\alpha = \beta = 1$. Note that either α or β will be sufficient so that two resistors can be saved.

Rao and Srinivasan [2.55] have described an active R filter using two opamps which is presented in Fig. 2.27d. This uses the capacitor simulation circuit described earlier (see Fig. 2.27b). The transfer function of this circuit can be derived as

$$\frac{V_o}{V_i} = \left(\frac{1}{\beta}\right)\left(\frac{1+K\left(\frac{s}{B_2}\right)}{1+\frac{s}{\beta B_1}+\frac{Ks^2}{\beta B_1\, B_2}}\right) \tag{2.113}$$

where $K = 1+\frac{R_b}{R_a}$ and $\beta = \frac{R_3}{R_3+R_4}$.

For high pole-Q designs, (2.113) realizes a band-pass response. Note also that V_y is a low-pass transfer function:

$$\frac{V_y}{V_i} = \left(\frac{1}{\beta}\right)\left(\frac{1}{1+\frac{s}{\beta B_1}+\frac{Ks^2}{\beta B_1\, B_2}}\right) \tag{2.114}$$

Rao and Srinivasan have also suggested another circuit [2.55] shown in Fig. 2.27e for realizing a low-pass transfer function:

$$\frac{V_o}{V_i} = \left(\frac{-\frac{1}{R_1}}{\frac{1}{R_2}+\frac{1}{R_3}+s\left(\frac{K}{B_2R_2}+\frac{1}{B_1}\left(\frac{1}{R_1}+\frac{1}{R_2}+\frac{1}{R_3}\right)\right)+\frac{s^2}{KB_1\, B_2}\left(\frac{1}{R_1}+\frac{1}{R_2}+\frac{1}{R_3}\right)}\right) \tag{2.115}$$

Schaumann [2.56] has proposed another active R filter which is presented in Fig. 2.27f whose transfer functions are given by

$$\frac{V_a}{V_i} = \left(\frac{\frac{1}{R_1}\left(\frac{s}{B_2} + \frac{1}{G}\right)}{\frac{1}{GR_2} + \frac{\beta}{R_3} + s\left(\frac{1}{B_2 R_2} + \frac{1}{GB_1}\left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}\right)\right) + \frac{s^2}{B_1 B_2}\left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}\right)} \right) \tag{2.116a}$$

and

$$\frac{V_o}{V_i} = \left(\frac{\frac{1}{\beta R_1}}{\frac{1}{GR_2} + \frac{\beta}{R_3} + s\left(\frac{1}{B_2 R_2} + \frac{1}{GB_1}\left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}\right)\right) + \frac{s^2}{B_1 B_2}\left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}\right)} \right) \tag{2.116b}$$

Note that although V_o/V_i is a useful transfer function, V_a/V_i is not a useful transfer function. Schaumann suggests tuning the circuit for pole-Q, gain, and pole-frequency using R_3, R_1, and β, respectively.

The various configurations of active R filters have shown that ratios of resistors or ratios of bandwidths of opamps can control the gain and pole-Q whereas the pole-frequency is still dependent on absolute values of bandwidths of both opamps which vary with temperature and power supply voltage. Hence active R filter designers have suggested the concept of master–slave tuning which laid the foundation of continuous-time filter tuning. This topic is discussed at a later stage in this book.

Example 2.10 Determine the frequency response at the output and inverting input of the opamp of the active-R filter using two nonideal opamps. Study the effect of an opamp second pole also (Fig. E.2.10).

Note that the opamp second pole is modeled by R_5 and C_4 for one opamp and by R_7 and C_6 for another opamp. The effect of the second pole at 1.5 MHz is to cause Q-enhancement and a shift in the peak frequency. The filter has a radian pole-frequency of $B/\sqrt{3}$. The band-pass midband gain is 1. The pole-Q is $\sqrt{3}$.

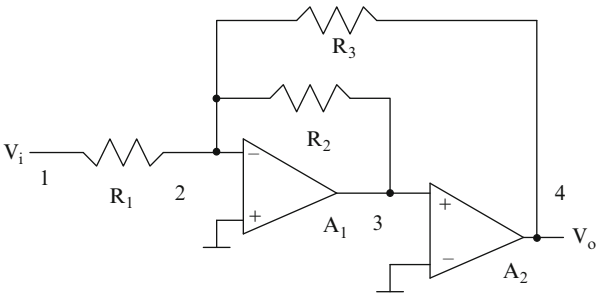
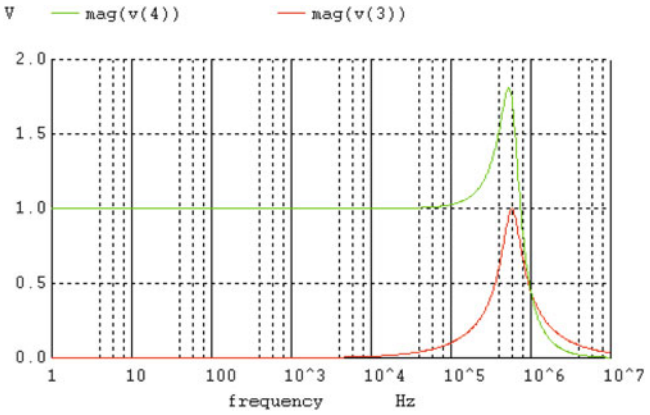


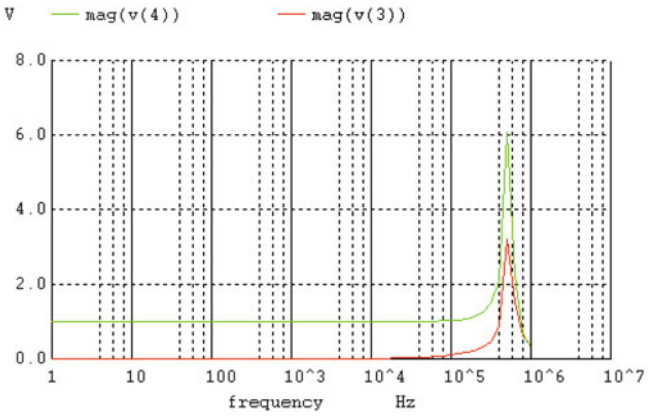
Fig. E.2.10

*Active R filter
R1 1 2 1 k
R2 2 3 1 k
R3 2 4 1 k
E1 0 5 2 0 100,000
R4 5 6 1 k
C3 6 0 15.90 uf
E2 3 0 6 0 1
E3 7 0 3 0 100,000
R5 7 8 1 K
C4 8 0 15.9 uf
E4 4 0 8 0 1
vin 1 0 ac 1 v
.ac dec 10 1 1,000 K



*Active R filter using second pole
R1 1 2 1 k
R2 2 3 1 k
R3 2 4 1 k
E1 0 5 2 0 100,000
R4 5 6 1 k
C3 6 0 15.90 uf
E2 9 0 6 0 1
R5 9 10 1 K
C4 10 0 106.15 pf
E3 3 0 10 0 1
E4 7 0 3 0 100,000
R6 7 8 1 k
C5 8 0 15.9 uf
E5 11 0 8 0 1
R7 11 12 1 k

```
C6 12 0 106.15 pf
E6 4 0 12 0 1
vin 1 0 ac 1 v
.ac dec 10 1 1,000 K
```



2.9 Active Filters Based on RLC Ladder Filters

Thus far, we have considered the design of active RC filters using the cascade technique. The advantage of this technique is that proven and high-performance biquads can be chosen to realize the high-order filters. But this technique has the drawback that there is no interaction between the various biquads. Thus, the individual biquad performance gets transferred to the output of the high-order filter. On the other hand, doubly terminated passive ladder filters using inductances, capacitances, and resistors have been found to exhibit very low sensitivity due to the coupling that exists among all the components in the ladder filters. Any variation in any one component will propagate to the source end as well as termination end and the resulting frequency response has very low sensitivity. This fact has been pointed out by Orchard [2.57] in his famous argument.

Consider, for instance, a high-order filter with equiripple pass-band. This implies that there are several points of inflection in the pass-band. At these critical frequencies, the derivative of the transfer function is zero. Thus, it follows that the sensitivity to any component at these frequencies is zero. Therefore by having several frequencies at which sensitivity of the transfer function is zero, in between these frequencies also, sensitivity tends to be low. This has been extensively verified by simulation for the past few decades. Hence, active filters based on RLC prototype ladder filters tend to lead to low-sensitivity designs.

Thus low-sensitivity active RC filters can be derived by imitating the RLC ladder filters. There are other techniques of high-order filter design that are not

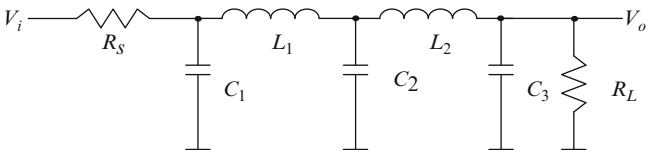


Fig. 2.28 A RLC prototype fifth-order low-pass ladder filter

based on simulation of RLC ladders. These are based on multiloop feedback technique. Both these topics are covered in the next two sections.

Active filters can be derived from RLC filters using two methods. In one method, for example, the inductors in the RLC low-pass filter prototype of Fig. 2.28 are replaced by active simulated inductances. This technique is known as the *component simulation technique*. In the second option, the *internal working* of the prototype RLC is filter is mimicked. By this, we mean that the nodal voltage equations are realized as being the same. This technique is known as the *operational simulation technique*.

Even though the component simulation technique is feasible, it will usually lead to a large number of components for realizing a floating inductor especially as compared to the operational simulation method.

2.9.1 Component Simulation Technique

In order to realize the circuit of Fig. 2.28 evidently one needs floating inductors. In a previous section, grounded inductance simulation based on GIC was described (see Fig. 2.15a). Other alternatives also exist. Consider another grounded inductance realization circuit shown in Fig. 2.29a [2.58]. The grounded inductance needs to have an input impedance of sL. The basic principle of inductance simulation is shown in Fig. 2.29b. The following equation describing the current through an inductor and the voltage across it can be written to mimic an inductor:

$$I_{in} = \frac{V_i}{sL} = \frac{V_i - V_o}{R_1} \tag{2.117}$$

Thus, we have to realize V_o from V_i such that

$$\frac{V_o}{V_i} = 1 - \frac{R_1}{sL} = 2 - \left(1 + \frac{R_1}{sL}\right) \tag{2.118}$$

so that a resistance inserted between V_i and V_o simulates an inductance.

We need to generate a voltage V_o from the input voltage V_i. The gain of 2 is achieved by using a noninverting amplifier formed by opamp A_2 and two resistors R'. The transfer function $\left(1 + \frac{1}{sCR_2}\right)$ is obtained by using the subcircuit shown in

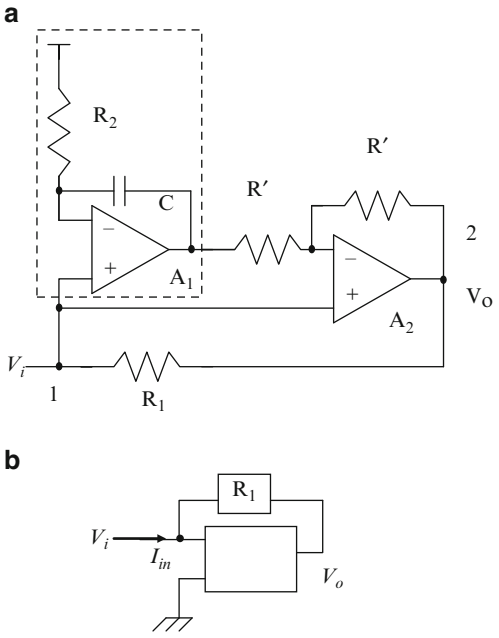


Fig. 2.29 (**a**) A grounded inductance simulator, and (**b**) the basic principle of grounded inductance simulation (Adapted from [2.58] ©IEEE 1967)

Fig. 2.29a in dotted lines and the needed inversion is carried out by the opamp A_2. It should be noted that the block used to realize the voltage transfer function $(1 - (R_1/sL))$ must have high input impedance. The inductance realized is given by CR_1R_2.

For the realization of floating inductance, it is required to augment the circuit of grounded inductance shown in Fig. 2.29b, by lifting the grounded terminal off the ground and connecting another similar circuit back to back as shown in Fig. 2.30a. The active RC implementation is as shown in Fig. 2.30b. Note that $(V_a - V_b)$ is available across the resistance R which is integrated using capacitors C and opamps A_1 and A_2. These outputs of the integrators are added appropriately with the terminal voltages V_a and V_b to realize V_x and V_y such that

$$V_y = V_b + \frac{V_a - V_b}{sCR} \tag{2.119a}$$

and

$$V_x = V_a + \frac{V_b - V_a}{sCR} \tag{2.119b}$$

Thus, the currents flowing into the terminal A and B are $\frac{V_a - V_x}{R}$ and $\frac{V_b - V_y}{R}$ which correspond to a floating inductance of value CR^2. Note that the circuit needs two capacitors and $R_1 = R_2 = R$.

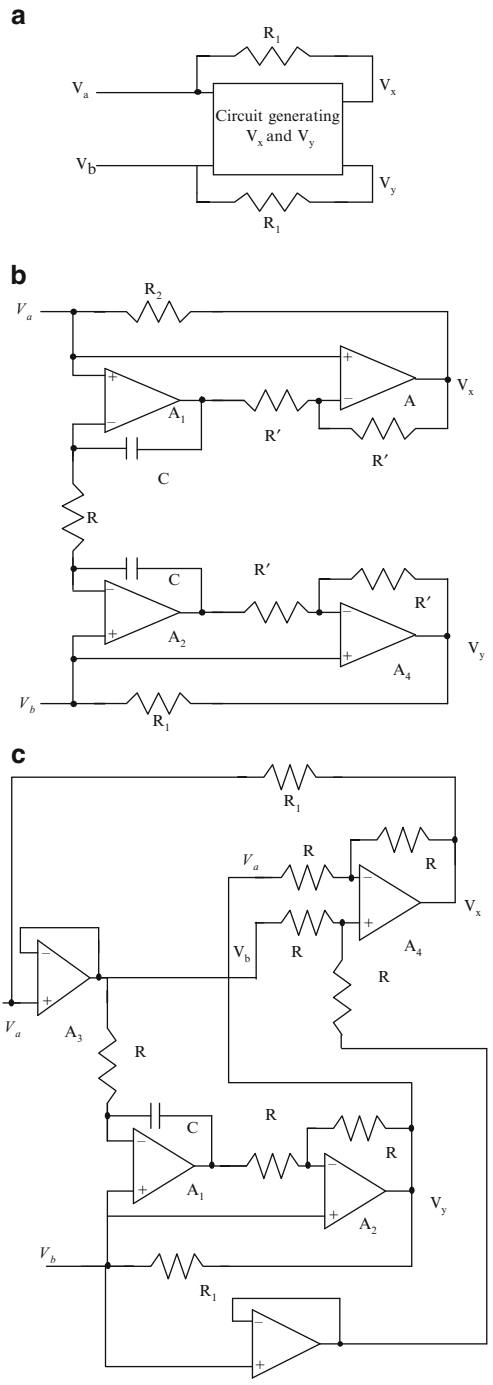


Fig. 2.30 (**a**) A floating inductance simulation scheme based on the grounded inductance of Fig. 2.29a, (**b**) conceptual model ((b) Adapted from [2.58] ©IEEE 1967) of floating inductance realization, and (**c**) another floating inductance simulation circuit

A modified circuit that needs only one capacitor is shown in Fig. 2.30c. Note that the buffer-connected opamps A_3 and A_5 are needed to isolate loading of the V_a and V_b terminal by the resistor R. In the conceptual model of floating inductance realization shown in Fig. 2.30a, it can be seen that

$$\frac{V_a - V_x}{R} = \frac{V_y^{'} - V_b}{R} \tag{2.119c}$$

or alternatively, we have

$$V_x = V_a + V_b - V_y \tag{2.119d}$$

Hence V_y can be realized using the modified grounded inductance circuit as shown in Fig. 2.30c and using an additional OA A_4 and four equal resistors, V_x can be realized. It may be noted the circuits of Fig. 2.30b, c rely on matching of components for exact floating inductance realization.

All-pole high-pass filters can be easily realized using the grounded inductances described above. Floating inductances can be avoided in the design of all-pole low-pass filters using the concept of FDNR which is considered next.

2.9.2 FDNR-Based Filters

Bruton [2.59] has introduced the concept of *frequency-dependent negative resistance* (FDNR) in order to facilitate easy realization of low-pass active RC ladder filters. Consider once again the prototype of Fig. 2.31a. Bruton suggested dividing all the impedances by s so that the transfer function remains unchanged. Then the following equivalences will occur.

R changes to $\frac{R}{s}$ (a capacitor of value 1/R)

$\frac{1}{sC}$ changes to $\frac{1}{s^2 C}$ (a frequency-dependent negative resistance $D \equiv -1/(\omega^2 C)$)

sL changes to L, a resistance.

Thus, floating inductances are transformed to floating resistances and resistors are transformed to capacitors and capacitors are transformed to grounded FDNRs as shown in Fig. 2.31b. The impedance $-1/(\omega^2 C)$ is real and negative and hence is a negative resistance, however, it is frequency-dependent due to the ω^2 term. Fortunately, grounded FDNR can be easily realized using a GIC (generalized impedance converter) studied in Fig. 2.15a. Note, however, that unlike the RLC prototype, the low-pass filter does not have a dc response as needed for a low-pass filter, since input is fed through a series capacitor. This situation can be remedied by shunting the input and load capacitors by resistances which, of course, changes the frequency response slightly.

Note, however, that this technique is applicable only for low-pass ladder filters. The FDNR is also known as supercapacitance.

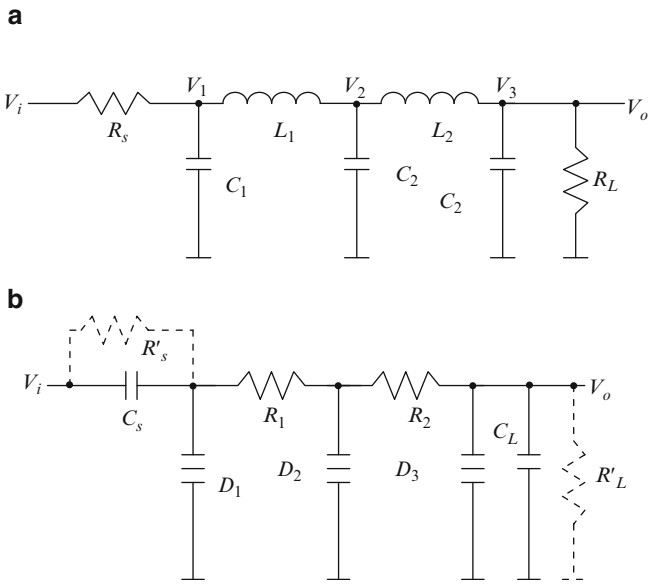


Fig. 2.31 (**a**) A fifth-order low-pass ladder filter prototype, and (**b**) a grounded FDNR-based circuit derived from (a)

2.9.3 Active RC Ladder Filters Based on Operational Simulation

2.9.3.1 Low-Pass Ladder Filters

In this technique, the nodal voltage equations are realized. As an illustration, consider the RLC low-pass all-pole ladder filter prototype shown in Fig. 2.32a. One can easily write the nodal voltage equations at nodes 1, 2, and 3 as follows.

$$\frac{V_i - V_1}{R_s} + I_1 = s C_1 V_1 \tag{2.120a}$$

$$I_1 = \frac{V_2 - V_1}{s L_1} \tag{2.120b}$$

$$I_2 = \frac{V_2 - V_3}{s L_2} \tag{2.120c}$$

$$-(I_1 + I_2) = \frac{V_2}{s C_2} \tag{2.120d}$$

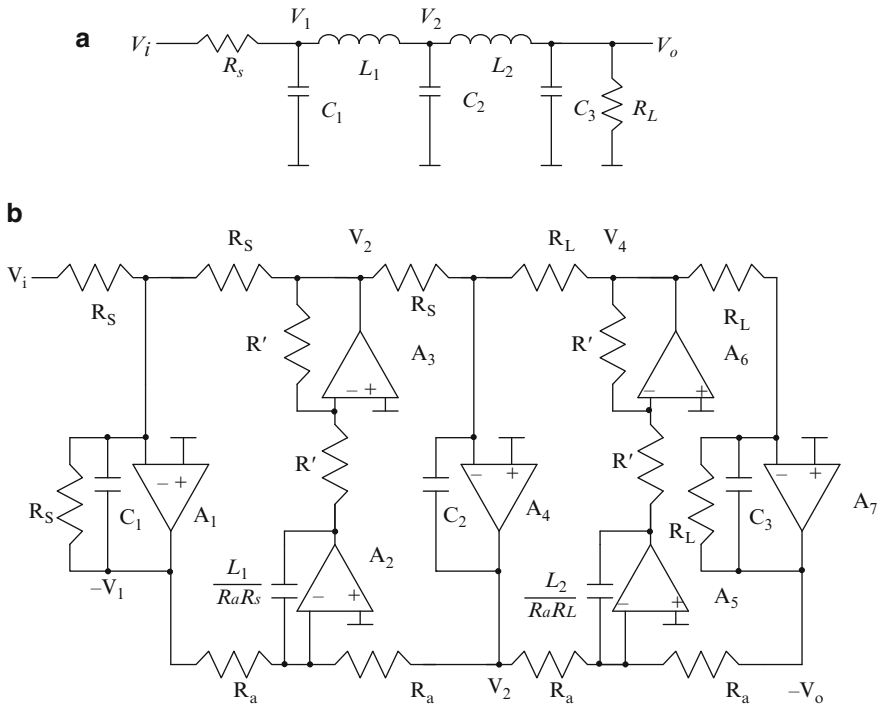


Fig. 2.32 (**a**) A passive RLC ladder prototype, and (**b**) a leap-frog active ladder filter derived from (a)

$$I_2 - V_o\, s\, C_3 = \frac{V_o}{R_L} \tag{2.120e}$$

Note that by considering $-V_1$, V_2 and $-V_0$ are realized at the outputs of the OAs, these equations can be easily realized as shown in the complete circuit of Fig. 2.32b. Note that the currents through the inductors I_1 and I_2 are also realized at the outputs of OAs A_3 and A_6 as I_1R and I_2R using noninverting integrators formed by (A_2 and A_3) and (A_5 and A_6) and associated resistors and capacitors, respectively. All the equations (2.120) can be realized using integrators. The termination resistances R_s and R_L will form part of the damped integrators as shown. The inductance and capacitance values in the prototype directly correspond to the integrating capacitors. The elegance of obtaining the circuit from the prototype of Fig. 2.32a has been noted.

Note that in a good design, there is an additional scaling step for optimal dynamic range. This requires that the currents through the inductors and voltages across the capacitors (i.e., the state variables realized at the output terminals of the various opamps) need to be analyzed to find their maximum value across the complete frequency range and then these voltages would be scaled to be equal.

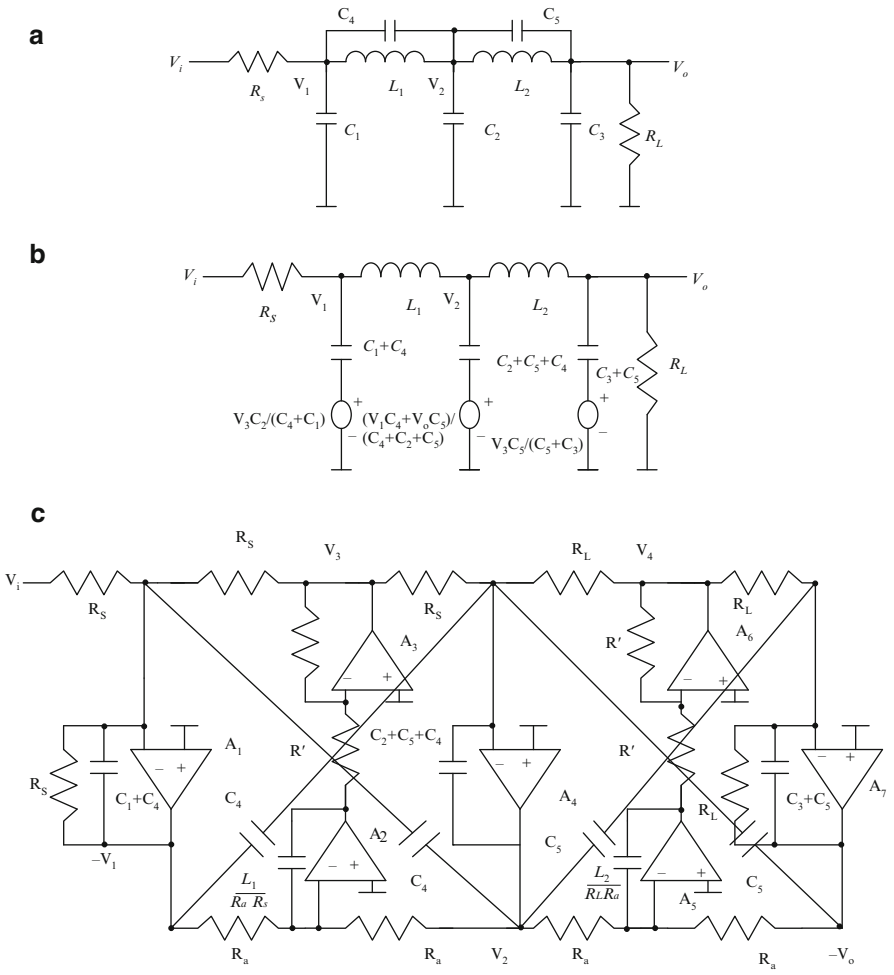


Fig. 2.33 (**a**) A passive RLC fifth-order elliptic low-pass ladder filter prototype, (**b**) an equivalent of (a), and (**c**) leap-frog active ladder filter derived from (b)

The scaling procedure has been illustrated in Fig. 2.20 for the case of the Tow–Thomas biquad which in fact is based on an operational simulation of a second-order singly terminated filter (R_s or $R_L = 0$).

For several years, the operational simulation of low-pass elliptic filters was not easy. However, during the course of research on SC filters, Allstot, Brodersen, and Gray [2.60] suggested an ingenious technique of realizing low-pass elliptic filters. This approach is considered briefly next. In this method, the nodal equations at nodes V_1, V_2, and V_3 in the prototype filter of Fig. 2.33a are rewritten so that by augmenting additional components, the low-pass filter structure can still be used. The circuit of Fig. 2.33b can be seen to be the exact equivalent of the prototype fifth-order elliptic low-pass filter circuit of Fig. 2.33a, wherein new voltage sources

are introduced. Also, note that the original grounded capacitor values C_1, C_2, and C_3 are increased. This circuit can be realized by the active RC filter of Fig. 2.33c in which the two pairs of cross-coupling capacitors facilitate the realization of the two pairs of transmission zeroes. Note that for each floating capacitor in the prototype, we have used two cross-coupling capacitors. However, it has been shown by Allstot, Brodersen, and Gray [2.60] that the mismatch of these capacitors does not affect the frequency response of the realized filter.

Example 2.11 Plot the frequency response of (a) the third-order elliptic ladder filter using SPICE and (b) leap-frog simulation of this filter considering the opamps to be nonideal. (c) Use an Akerberg–Mossberg type integrator for the middle integrator and evaluate the behavior.

```
*Third Order RLC Elliptic filter
Rs 1 22 1,000
RL 23 0 1,000
C21 22 0 1,203 pf
L21 22 23 962 uh
C22 22 23 201 pf
C23 23 0 1,203 pf
```

The operational simulation yields the active RC filter of Fig. E.2.11a. It can be seen that there is undesirable peaking at the pass-band edge and the transmission zero is obscured. The use of the Akerberg–Mossberg type of noninverting integrator improves the frequency response as shown (see Fig. E.2.11b).

```
* Third order leap-frog ladder filter
R1 1 2 1 K
R7 8 2 1 k
```

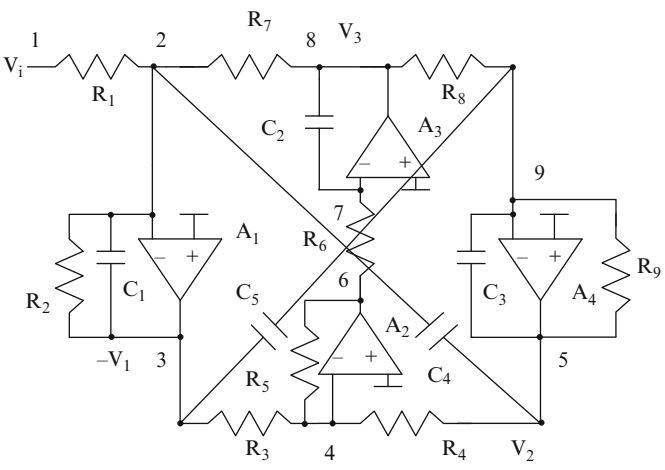
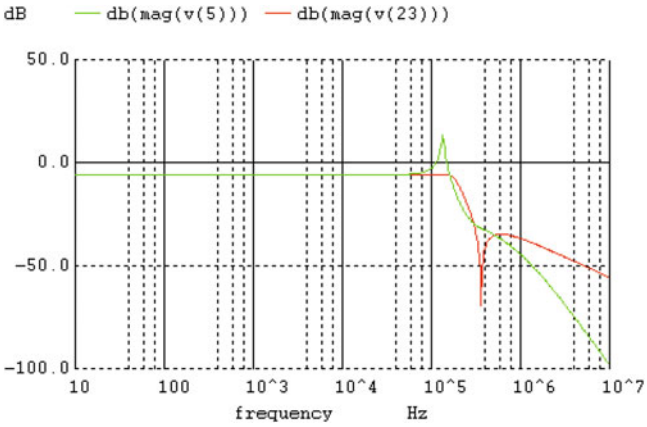


Fig. E.2.11a

R2 2 3 1 k
C1 2 3 1,404 pf
C2 8 7 962 pf
R6 6 7 1 k
R5 4 6 1 k
R3 3 4 1 k
R4 4 5 1 k
R8 8 9 1 k
R9 9 5 1 K
C3 9 5 1,404 pf
C4 2 5 201 pf
C5 3 9 201 pf
E1 0 10 2 0 100,000
R10 10 11 1 k
C6 11 0 15.9 uf
E2 3 0 11 0 1
E3 0 12 4 0 100,000
R11 12 13 1 k
C7 13 0 15.9 uf
E4 6 0 13 0 1
E5 0 14 7 0 100,000
R12 14 15 1 k
C8 15 0 15.9 uf
E6 8 0 15 0 1
E7 0 16 9 0 100,000
R13 16 17 1 k
C9 17 0 15.9 uf
E8 5 0 17 0 1
vin 1 0 ac 1 v
.ac dec 10 1 1,000 k



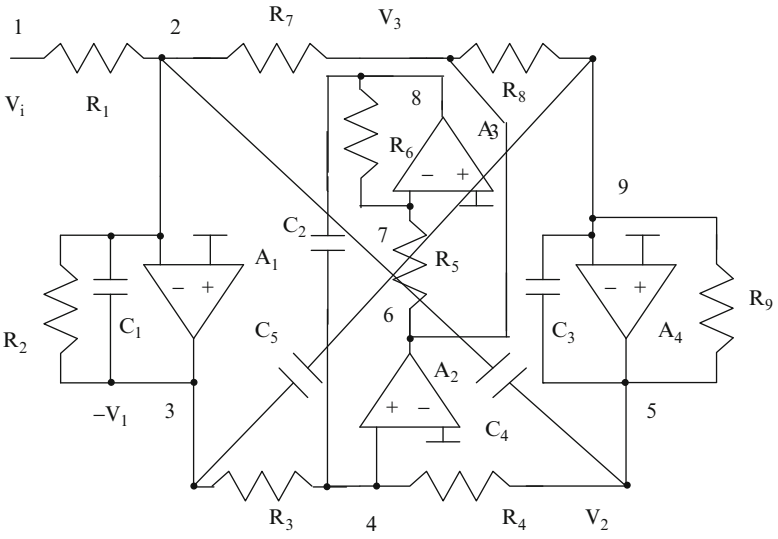
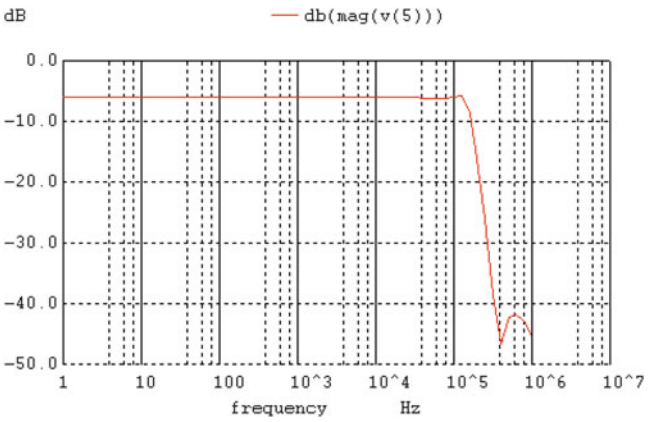


Fig. E.2.11b

* Third order leap-frog ladder filter Akerberg–Mossberg
R1 1 2 1 K
R7 6 2 1 k
R2 2 3 1 k
C1 2 3 1,404 pf
C2 4 8 962 pf
R5 6 7 1 k
R6 7 8 1 k
R3 3 4 1 k
R4 4 5 1 k
R8 6 9 1 k
R9 9 5 1 K
C3 9 5 1,404 pf
C4 2 5 201 pf
C5 3 9 201 pf
E1 0 10 2 0 100,000
R10 10 11 1 k
C6 11 0 15.9 uf
E2 3 0 11 0 1
E3 12 0 4 0 100,000
R11 12 13 1 k
C7 13 0 15.9 uf
E4 6 0 13 0 1
E5 0 14 7 0 100,000
R12 14 15 1 k

```
C8 15 0 15.9 uf
E6 8 0 15 0 1
E7 0 16 9 0 100,000
R13 16 17 1 k
C9 17 0 15.9 uf
E8 5 0 17 0 1
vin 1 0 ac 1 v
.ac dec 10 1 1,000 k
```



2.9.3.2 Band-Pass Filters

It may be pointed out that using low-pass to band-pass transformation, from the low-pass all-pole filter structure of Fig. 2.32a, we can obtain the band-pass filters. Note that LP to BP transformation transforms a lossless integrator to a resonator with infinite Q whereas a damped integrator is converted to a resonator with finite Q. The LP to BP transformation is given as $s \rightarrow \frac{s^2+\omega_o^2}{Bs}$ where the cutoff frequency of the prototype low-pass filter is 1 rad/s, ω_o is the desired center frequency of the band-pass filter, and B is the 3-dB bandwidth of the desired band-pass filter. Note that this transformation yields geometrically symmetric responses which means that there are two frequencies ω_1, ω_2 corresponding to a given gain such that $\omega_o = \sqrt{\omega_1\ \omega_2}$. Using the LP to BP transformation, an integrator and first-order low-pass filter will yield, respectively,

$$\frac{1}{s} \rightarrow \frac{Bs}{s^2+\omega_o^2} \text{ and } \frac{a}{s+a} \rightarrow \frac{aBs}{s^2+aBs+\omega_o^2}$$

For operational simulation of BP filters from the LC prototype, the signs of the integrators in the low-pass prototype need to be preserved. Moreover, the

summation of the inputs as needed in a low-pass filter needs to be done in the case of a band-pass filter as well.

The nodal voltages V_1 and V_3 can be expressed first from the prototype of Fig. 2.34a as follows.

$$\frac{V_i}{R_s} - V_1\left(\frac{1}{R_s} + s(C_1 + C_2)\right) + V_3\, s\, C_2 + \frac{(V_3 - V_1)}{s\, L_2} = 0 \tag{2.121a}$$

$$V_1\, s\, C_2 - V_3\, s(C_2 + C_3) - \frac{V_3}{R_L} + \frac{V_1 - V_3}{s\, L_2} = 0 \tag{2.121b}$$

By substituting for s, the LP to BP transformation $\frac{\left(s^2 + \omega_o^2\right)}{Bs}$, we obtain the following two equations after little manipulation:

$$\frac{s\, V_i\, B}{(C_1 + C_2)R_s} - V_1\left(s^2 + \frac{sB}{(C_1 + C_2)R_s} + \omega_o^2\right) + V_3\left(s^2 + \omega_o^2\right)\frac{C_2}{(C_1 + C_2)} + \frac{(V_3 - V_1)\, s^2\, B^2}{(C_1 + C_2)\left(s^2 + \omega_o^2\right) L_2} = 0 \tag{2.122a}$$

$$V_1\left(s^2 + \omega_o^2\right)\frac{C_2}{(C_2 + C_3)} - V_3\left(s^2 + \frac{sB}{(C_2 + C_3)R_L} + \omega_o^2\right) + \frac{(V_1 - V_3)\, s^2\, B^2}{(C_2 + C_3)\left(s^2 + \omega_o^2\right) L_2} = 0 \tag{2.122b}$$

These equations can be implemented by the block diagram of Fig. 2.34b. Any well-known biquad can be employed in the band-pass filter realization. The use of the Tow–Thomas biquad for this purpose is shown in Fig. 2.34c in the complete sixth-order band-pass filter derived from a third-order all-pole low-pass prototype active RC filter. Note that the low-pass prototype can be scaled first for optimal dynamic range and the resulting LP prototype circuit can be used directly to obtain the band-pass filter that will yield an optimal dynamic range solution at the nodes of the corresponding third-order prototype. However, for high pole-Q designs, within the three two-integrator loops, scaling needs to be done by choosing equal time constants for the integrators.

2.9.4 *Operational Simulation of High-Pass Filters: Yoshihoro's Technique*

The techniques presented above do not work easily for realizing high-pass filters. Some solutions have been suggested in the literature but they are very complex. The reader is referred to Brackett and Sedra [2.1] for more information. Yoshihoro's nodal voltage simulation technique [2.61] can be used to realize

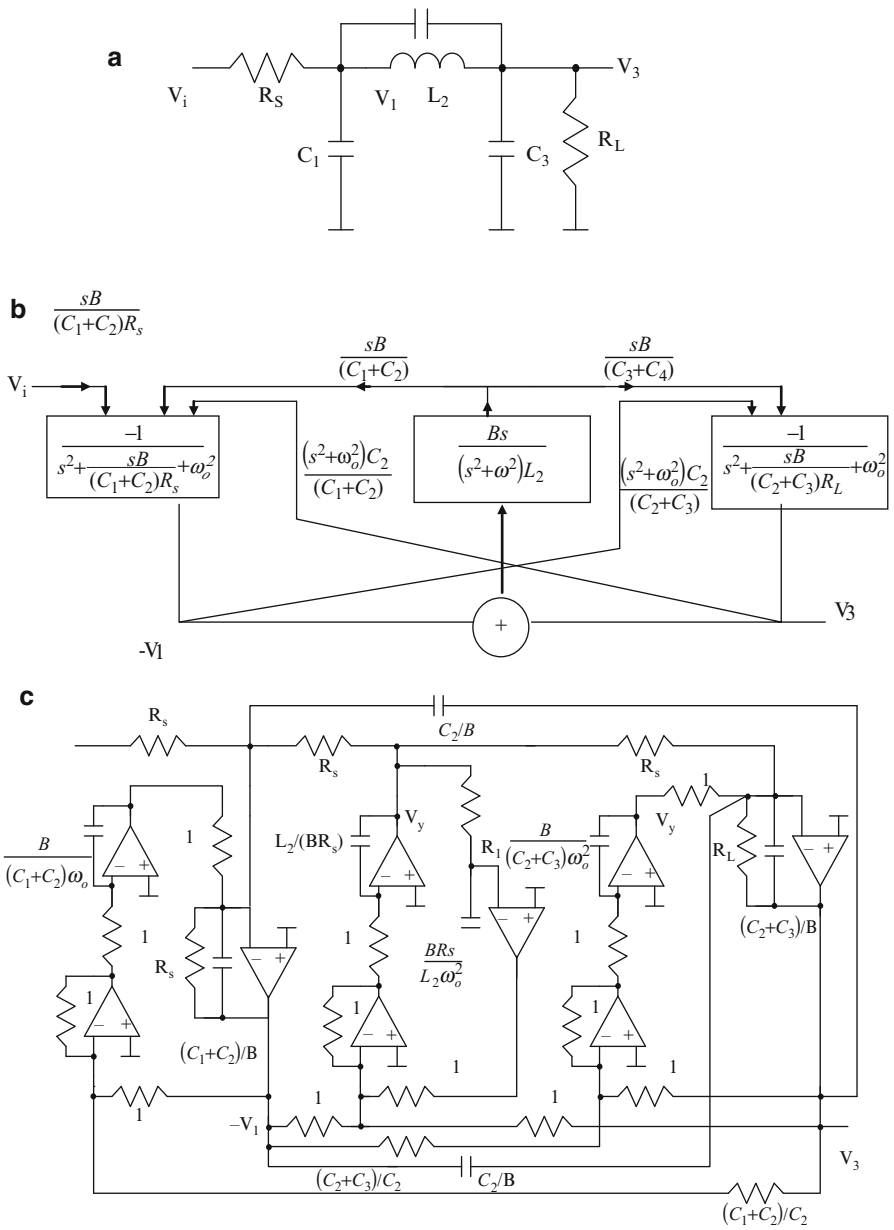


Fig. 2.34 (**a**) A third-order all-pole low-pass filter, (**b**) block diagram obtained by LP to BP transformation from (**a**), and (**c**) complete sixth-order band-pass active RC filter obtained from (**b**) (b Adapted from [2.63] ©IEE 1980)

high-pass filters based on RLC ladder filters [2.62]. Consider the prototype third-order elliptic high-pass shown in Fig. 2.35a. The equations for the node voltages V_x and V_o can be easily written in terms of the neighboring node voltages as follows by simple analysis.

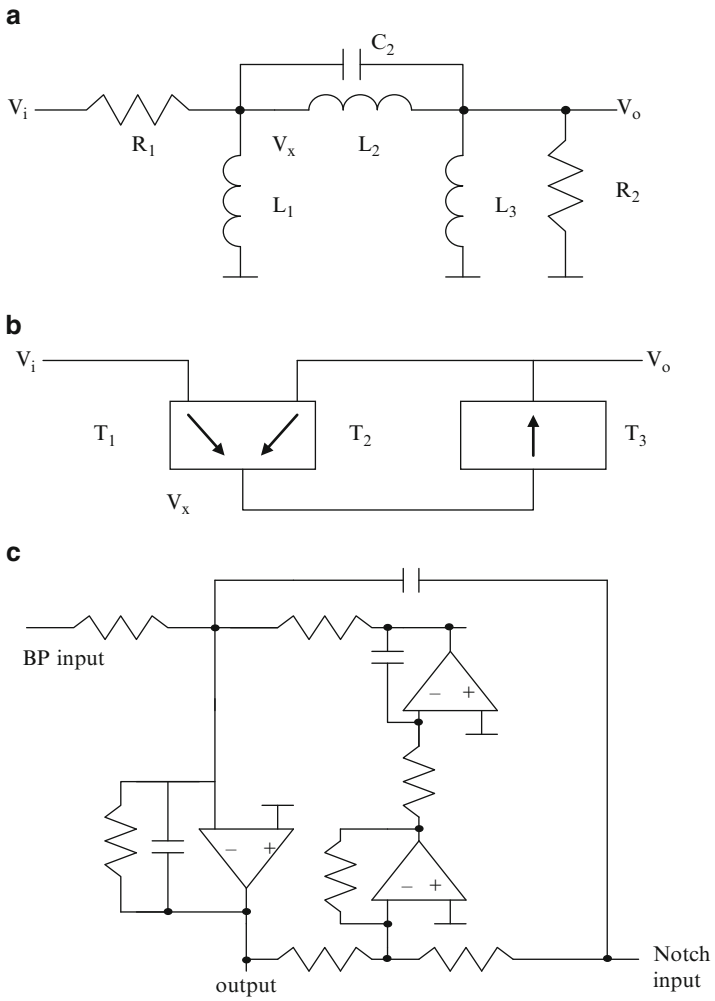
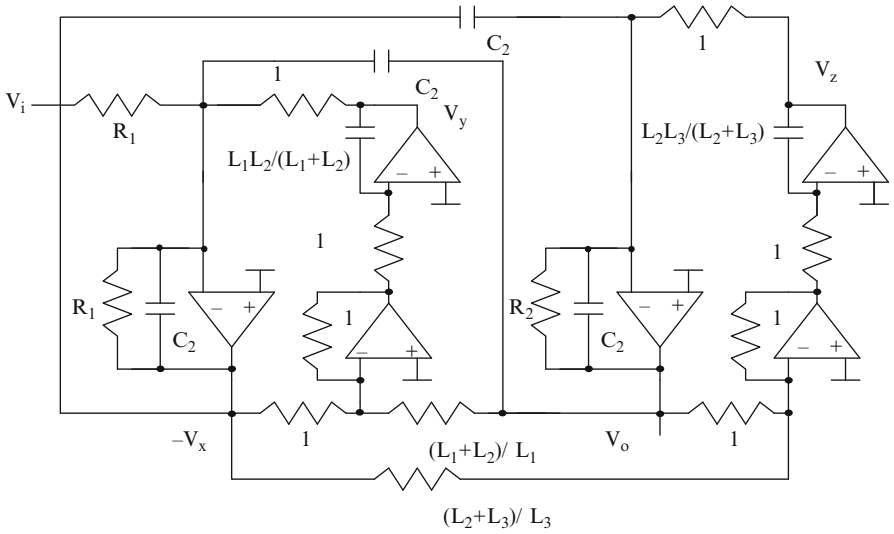


Fig. 2.35 (**a**) A third-order elliptic high-pass filter, (**b**) block diagram of filter obtained using Yoshihoro's technique, (**c**) second-order active RC BP/notch filter that can be used in (b), (**d**) complete high-pass filter, and (**e**) equivalent model of (d) (Adapted from [2.62] ©IEE 1988)

d



e

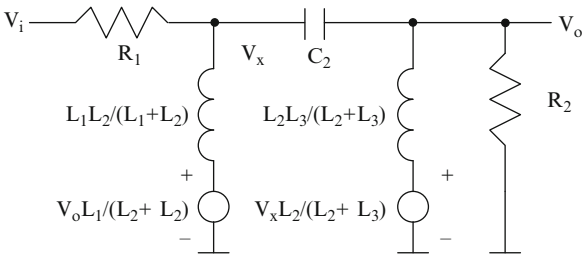


Fig. 2.35 (continued)

$$V_x = V_i \left(\frac{\frac{s}{C_2 R_1}}{s^2 + \frac{s}{C_2 R_1} + \frac{1}{C_2}\left(\frac{1}{L_1} + \frac{1}{L_2}\right)} \right) + V_o \left(\frac{s^2 + \frac{1}{L_2 C_2}}{s^2 + \frac{s}{C_2 R_1} + \frac{1}{C_2}\left(\frac{1}{L_1} + \frac{1}{L_2}\right)} \right)$$
$$= V_i T_1 + V_o T_2 \tag{2.123a}$$

$$V_0 = V_x \left(\frac{s^2 + \frac{1}{L_2 C_2}}{s^2 + \frac{s}{C_2 R_2} + \frac{1}{C_2}\left(\frac{1}{L_2} + \frac{1}{L_3}\right)} \right) = V_x T_3 \tag{2.123b}$$

Thus these two equations enable us to construct the block diagram of Fig. 2.35b where T_1, T_2, and T_3 are biquadratic transfer functions. Note also that T_1 and T_2 share the same denominator. The Tow–Thomas biquad circuit with appropriate

feedforward branches as shown in Fig. 2.35c can realize a band-pass and notch transfer function at the same output terminal, however, with a negative sign (i.e., $-V_x$ is realized). A similar circuit with only the input to realize a notch transfer function, can be used to realize (2.123b). Since this transfer function also is an inverting type, the desired V_o will be realized. Interconnection of these two second-order filters will realize the complete band-pass filter as shown in Fig. 2.35d. Note that as compared to the low-pass elliptic filter, two opamps forming a noninverting integrator are additionally needed. The equivalent circuit realized can be drawn as shown in Fig. 2.35e.

Note that in the case of all-pole high-pass filters, the inductor L_2 will be absent and hence, the resistors $(L_1 + L_2)/L_1$ and $(L_2 + L_3)/L_3$ are not needed (they do not exist) and the capacitor values $L_1L_2/(L_1 + L_2)$ and $L_2L_3(L_2 + L_3)$ become L_1 and L_3, respectively. The voltages V_y and V_z correspond to the currents through the shunt inductors in the equivalent circuit of Fig. 2.35e which need to be estimated to determine their peak values to facilitate scaling for optimal dynamic range.

2.9.5 *Operational Simulation of General-Parameter Ladder Filters*

Note that Yoshihoro's method can easily be used for general-parameter ladder filters as well [2.63]. Note that these general-parameter filters are not derived from the low-pass prototypes using frequency transformation. As an illustration, consider the twelfth-order band-pass filter of Fig. 2.36a. The block diagram shown in Fig. 2.36b can be easily obtained. The various band-pass and notch transfer functions are as follows.

Biquad 1:

$$T_{i1} = \left(\frac{\frac{s}{C_2 R_s}}{s^2 + \frac{s}{C_2 R_s} + \frac{1}{C_2}\left(\frac{1}{L_1} + \frac{1}{L_2}\right)} \right) \tag{2.124a}$$

$$T_{31} = \left(\frac{s^2 + \frac{1}{L_2 C_2}}{s^2 + \frac{s}{C_2 R_s} + \frac{1}{C_2}\left(\frac{1}{L_1} + \frac{1}{L_2}\right)} \right) \tag{2.124b}$$

Biquad 2:

$$T_{13} = \left(\frac{C_2}{C_2 + C_3 + C_4} \frac{s^2 + \frac{1}{L_2 C_2}}{s^2 + \frac{1}{(C_2 + C_3 + C_4)}\left(\frac{1}{L_2} + \frac{1}{L_4}\right)} \right) \tag{2.124c}$$

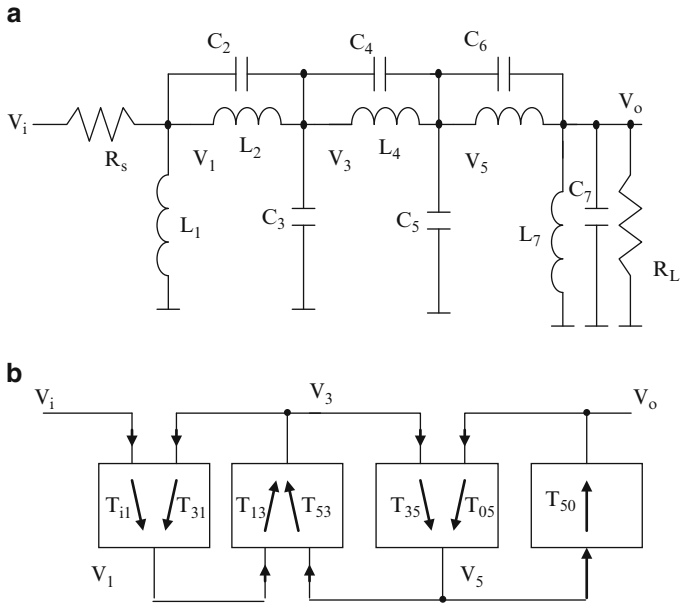


Fig. 2.36 (**a**) A general-parameter filter prototype, (**b**) block diagram of the filter obtained from (a) using Yoshihoro's method (Adapted from [2.63] ©IEEE 1980)

$$T_{53} = \left(\frac{C_4}{C_2 + C_3 + C_4} \frac{s^2 + \frac{1}{L_4\, C_4}}{s^2 + \frac{1}{(C_2 + C_3 + C_4)} \left(\frac{1}{L_2} + \frac{1}{L_4} \right)} \right) \tag{2.124d}$$

Biquad 3:

$$T_{35} = \left(\frac{C_4}{C_4 + C_5 + C_6} \frac{s^2 + \frac{1}{L_4\, C_4}}{s^2 + \frac{1}{(C_4 + C_5 + C_6)} \left(\frac{1}{L_4} + \frac{1}{L_6} \right)} \right) \tag{2.124e}$$

$$T_{05} = \left(\frac{C_6}{C_4 + C_5 + C_6} \frac{s^2 + \frac{1}{L_6\, C_6}}{s^2 + \frac{1}{(C_4 + C_5 + C_6)} \left(\frac{1}{L_4} + \frac{1}{L_6} \right)} \right) \tag{2.124f}$$

Biquad 4:

$$T_{50} = \left(\frac{C_6}{C_6 + C_7} \frac{s^2 + \frac{1}{L_6\, C_6}}{s^2 + s \frac{1}{(C_6 + C_7) R_L} + \frac{1}{(C_6 + C_7)} \left(\frac{1}{L_6} + \frac{1}{L_7} \right)} \right) \tag{2.124g}$$

Since only band-pass and notch transfer functions are needed, the biquad of Fig. 2.35c can be used to obtain the complete circuit. Note that scaling can be done easily by knowing the maxima of all the voltages at various nodes in the prototype circuit. There is no need to compute the various inductor currents.

2.10 Multiloop Feedback-Based Active RC Filters

We next consider another technique for realizing high-order filters with low sensitivity. This is known as multiple-loop feedback [2.64]. There are various options available for the filter designer choosing this technique. These are discussed next.

2.10.1 FLF (Follow-the-Leader Feedback)

The follow-the-leader feedback structure is shown in Fig. 2.37a. This structure is designed to realize a low-pass prototype transfer function at output V_o. Usually, for convenience all the blocks $T_1 - T_n$ can be chosen to be identical. Using LP to BP transformation, a $2n$th-order band-pass filter can be realized. The multipliers β_i and summer are realized using one opamp and various resistors. The various q_is can be positive or negative depending on the required transfer function. The transfer function of this circuit can be derived as

$$\frac{V_o}{V_i} = -\frac{p_1\,(\beta_1 + \beta_2\,T_1 + \beta_3\,T_1\,T_2 + \beta_4\,T_1\,T_2\,T_3)}{1 + q_1\,T_1 + q_2\,T_1\,T_2 + T_1\,T_2\,T_3\,q_3} \tag{2.125}$$

Considering a first-order low-pass filter with transfer function $\frac{a}{s+a}$ to be used for all T_is, the denominator of the transfer function can be seen to be (after multiplying with $(s + a)^3$)

$$D(s) = s^3 + s^2\,a(3 + q_1) + s\,a^2\,(3 + 2\,q_1 + q_2) + a^3\,(1 + q_1 + q_2 + q_3) \tag{2.126}$$

From the desired denominator of the transfer function, the various q_i values and a need to be determined. The next step is to determine various β_i values to obtain the desired transfer function by matching the coefficients of s, s^2, and s^3 terms in the numerator. In the third-order case, the equations obtained are linear and can be solved for q_1, q_2, and q_3 choosing a. Solutions that give positive values for various q_i are preferable to avoid additional opamps. The value of a can be chosen so that q_1 is positive and iteratively, q_2 and q_3 values can be calculated by matching the coefficients. Note that all the blocks can also have different transfer functions.

The individual blocks are of second-order band-pass type after LP → BP transformation and have the same center frequency ω_o. Their transfer function with pole-frequency normalized ω_o to unity is given by

$$T_i(s) = H_i \frac{\left(\frac{s}{Q_i}\right)}{s^2 + \frac{s}{Q_i} + 1} \tag{2.127}$$

where H_i is the midband gain.

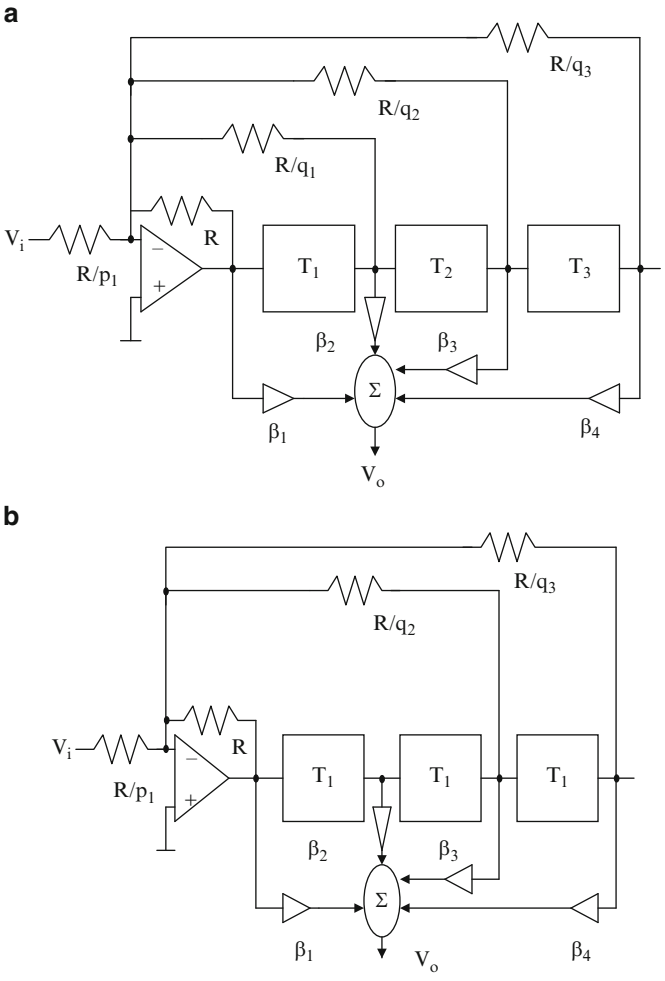


Fig. 2.37 Multiple-loop feedback structures of various types: (**a**) FLF, (**b**) PRB, (**c**) SCF, (**d**) MLF, (**e**) IFLF, and (**f**) MSF ((**d–f**) Adapted from [2.64] ©IEEE 1979)

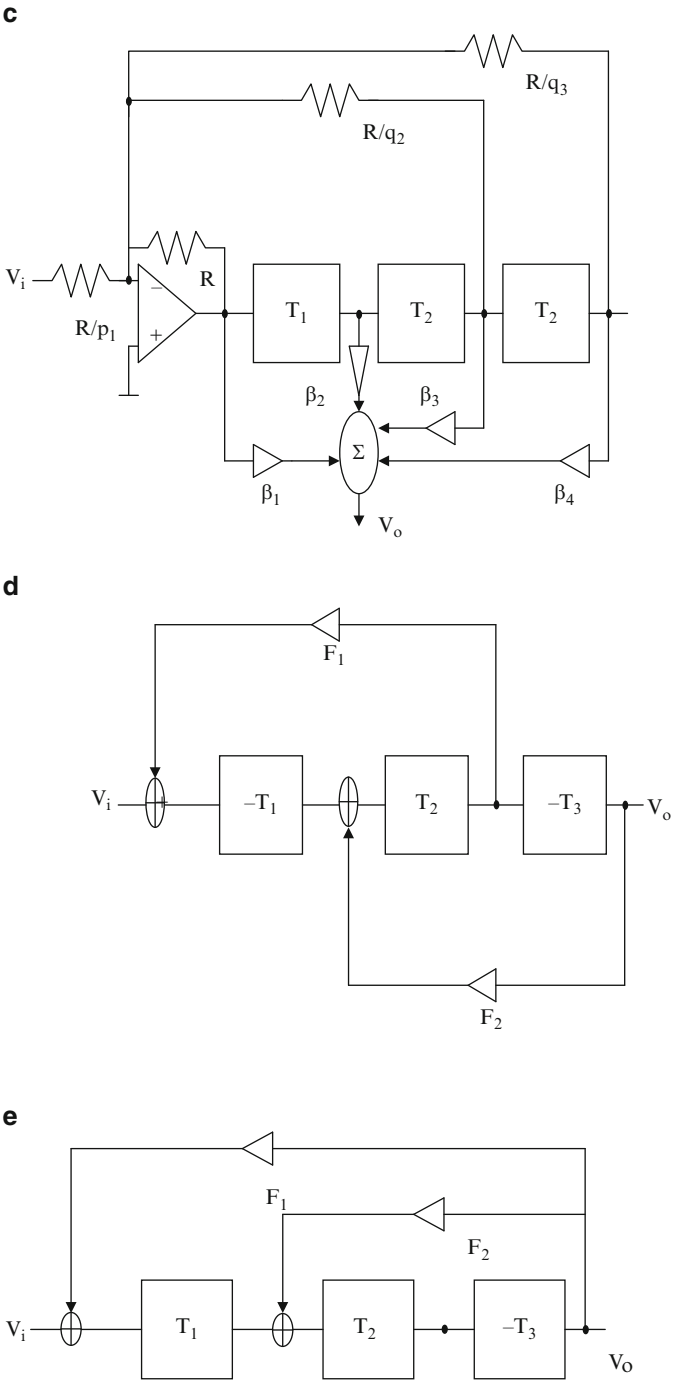


Fig. 2.37 (continued)

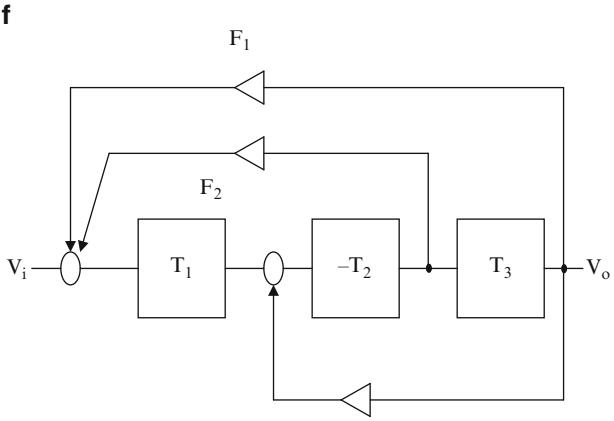


Fig. 2.37 (continued)

2.10.2 PRB (Primary Resonator Block) Structure

The PRB (primary resonator block) shown in Fig. 2.37b is a special case of FLF and is obtained by deleting the first feedback loop, that is, by making $q_1 = 0$. Note also that all blocks are identical in this case. For the third-order case, from (2.126), we obtain the denominator of the transfer function as

$$D(s) = s^3 + 3a\,s^2 + s\,a^2\,(3 + q_2) + a^3\,(1 + q_2 + q_3) \tag{2.128}$$

Thus, a can be obtained from the desired denominator of the transfer function directly and using this value, q_2 and q_3 can be determined. This structure is easier to design. Note that the use of identical blocks reduces the engineering effort such as the design of the filter and enhances reproducibility. The circuit cannot be scaled for optimal dynamic range since all blocks have the same gain H_i. As an illustration for the realization of the third-order Butterworth transfer function whose denominator is $s^3 + 2s^2 + 2s + 1$, the design values are $a = 2/3$, $q_2 = 3/2$, and $q_3 = 7/8$.

2.10.3 SCF (Shifted Companion Form) Structure

We next consider another multiloop feedback technique as shown in Fig. 2.37c. Note that this structure is a modification of FLF obtained by removing the first feedback loop and making all the blocks $T_2, T_3, \ldots, T_{n-1}, T_n$ identical whereas T_1 is

different. Denoting the gain of the block T_1 as H_1 and that of the other blocks as H_2, the resulting denominator of the transfer function is given as

$$D(s) = s^3 + 3a\,s^2 + s\,a^2\,(3 + q_2\,H_1\,H_2) + a^3\,(1 + q_2\,H_1\,H_2 + q_3\,H_1\,H_2^2) \tag{2.129}$$

A comparison of (2.128) and (2.129) shows that although the a value is the same, $q_2H_1H_2$ and $q_3H_1H_2^2$ can be determined iteratively. The additional degrees of freedom in H_1 and H_2 can help to optimize the dynamic range.

2.10.4 Multiloop Feedback (MLF) Structure

The multiloop feedback (MLF) structure shown in Fig. 2.37d is similar to the leap-frog structure. However, note that in the leap-frog structure, the intermediate blocks have an infinite Q-factor and terminating blocks have a finite pole-Q. On the other hand, in a MLF structure, the individual blocks can have finite pole-Qs. This may be a benefit in practical situations where nonidealities of active or passive devices make the circuit Q finite. Note that the feedforward portion is not shown in Fig. 2.37d.

2.10.5 IFLF (Inverse Follow-the-Leader Feedback) Structure

In the IFLF (inverse follow-the-leader feedback) structure of Fig. 2.37e, the output is weighted and fed to the inputs of various blocks. The transfer function of this circuit can be seen to be

$$\frac{V_o}{V_i} = -\frac{T_3}{1 + F_2\,T_2\,T_3 + F_1\,T_1\,T_2\,T_3} \tag{2.130}$$

Note that this transfer function is similar to that of the FLF structure given in (2.125) with $q_1 = 0$.

2.10.6 MSF (Minimum Sensitivity Feedback) Structure

We finally consider a generalized version known as MSF (minimum sensitivity feedback) shown in Fig. 2.37f from which all other configurations can be derived. The transfer function of this circuit is given as

$$\frac{V_o}{V_i} = -\frac{T_1\ T_2\ T_3}{1 + F_2\ T_1\ T_2 + F_3\ T_2\ T_3 + F_1\ T_1\ T_2\ T_3} \tag{2.131}$$

Laker, Schaumann, and Ghausi [2.64] have thoroughly investigated all these structures given in Fig. 2.37a–f. Their recommended design procedure is to choose all the center frequencies the same. The gains and Q_is can, however, be different and chosen a priori. Then, the feedback coefficients are selected to minimize the sensitivity of the realized filters. The sensitivity can be considered to be of two parts: one due to the individual T_i block and another due to the feedback. Their sensitivity evaluation considered the passive sensitivities only. They have also assumed that statistical correlation among components exists only within a section.

The PRB type, FLF, and IFLF types do not need any sensitivity optimization. Only MSF-type filters need optimization. In these, the high-Q sections are not necessarily most critical. Optimized LF and MLF active filters yield the lowest sensitivities in the pass-band. Optimized FLF active filters generally yield lower sensitivities than LF designs at the band edges and in the stop-band. The typical results for a three-section Butterworth band-pass filter are presented in Fig. 2.38. It can be seen that the RLC filter exhibits good performance and cascade design is poorest among these. Among others, FLF gives the best performance. The reader is referred to [2.64] for an exhaustive discussion on the design of multiloop feedback filters.

2.11 Noise in Active RC Filters

The dynamic range of active RC filters is limited by the noise in active RC filters. The noise arises because of two sources: (a) resistor noise (also called *inherent noise* excluding noise of resistors used for canceling dc offset), and (b) noise due to opamp. The opamp noise can be modeled by an input referred noise voltage source and noise current source as shown in Fig. 2.39b whereas a resistor noise can be modeled as shown in (a). The contribution due to the noise current source is dependent on the resistances in the active RC filter whereas the noise voltage source is independent of the resistances. The noise voltage and current sources are specified by the noise power spectral density expressed as voltage square/Hertz and current square/Hertz. Thus, depending on the frequency band of measurement, these will be weighted to obtain the total noise by adding them since they are uncorrelated. The resistor noise of a resistor R is modeled by a noise voltage source e_{nr} in series with an ideal noise-free resistor R and the power spectral density is expressed as

$$e_{nr}^2 = 4kTRB \tag{2.132}$$

where k is Boltzmann's constant $1.3806503 \times 10^{-23}$ J/K and T is the absolute temperature in degrees with B the bandwidth of the measurement.

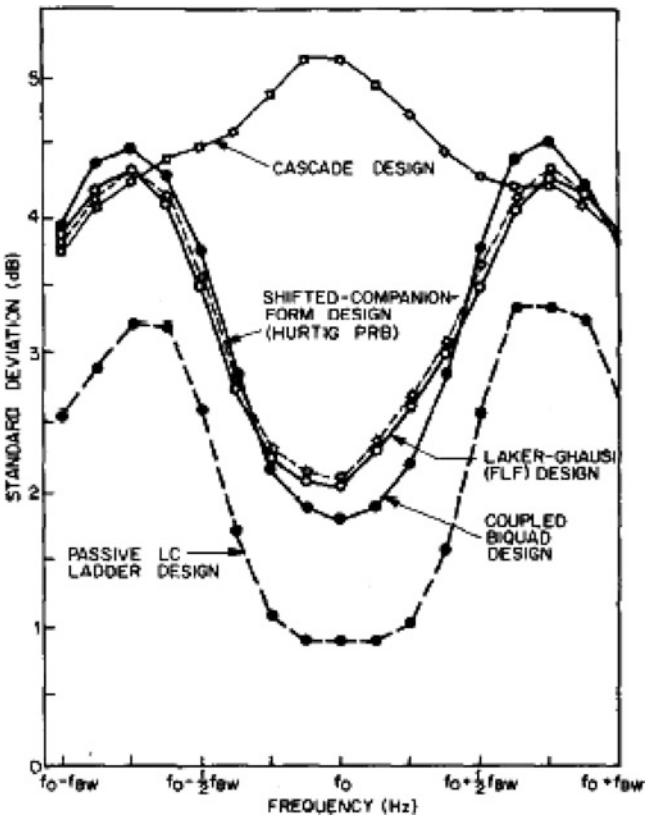


Fig. 2.38 Monte Carlo simulation results of sixth-order Butterworth (three-section) filters of different topologies with passive component tolerance assumed 1.732% (Adapted from [2.64] ©IEEE 1979)

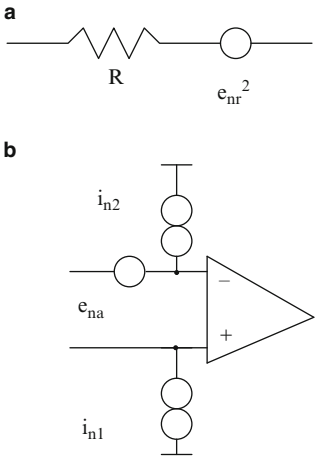


Fig. 2.39 Noise models (**a**) of a resistor, and (**b**) of an opamp

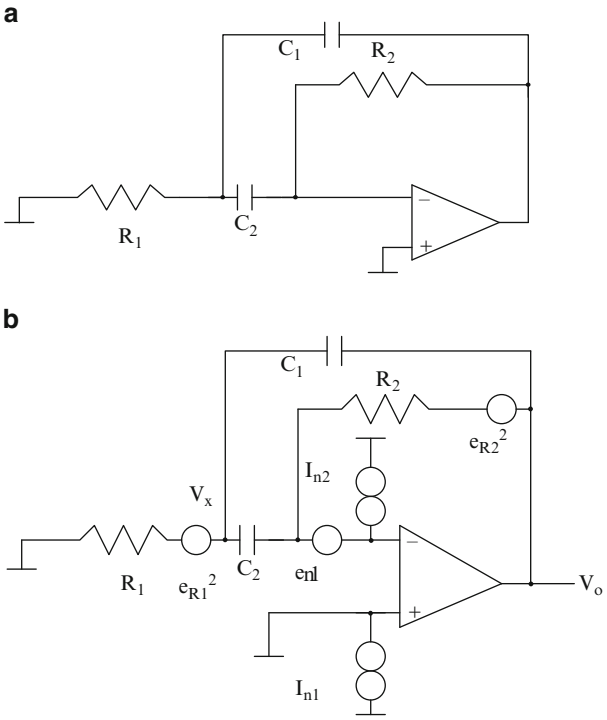


Fig. 2.40 (**a**) A multiple feedback active RC filter, and (**b**) circuit of (**a**) with various noise sources

The noise analysis of active devices and resistors can be carried out in one analysis and then estimated [2.65, 2.66]. As an illustration, consider the single amplifier band-pass filter of Fig. 2.40a. The noise equivalent circuit is as shown in Fig. 2.40b. Analyzing the circuit in the usual manner, considering the noise voltage source as a noise voltage and noise current source as a current without worrying about the fact that they are power spectral densities, first the node equations can be written as follows.

$$\frac{e_{R1}}{R_1} + V_o\, s\, C_1 + e_{n1}\, s\, C_2 = V_x \left(\frac{1}{R_1} + s(C_1 + C_2) \right) \tag{2.133a}$$

$$\frac{V_o + e_{R_2}}{R_2} + V_x\, s\, C_2 + I_{n2} = e_{n1} \left(\frac{1}{R_2} + s\, C_2 \right) \tag{2.133b}$$

Solving these two equations, we obtain

$$V_o = -\frac{\left(\begin{array}{l} \frac{e_{R1}\, s}{C_1 R_1} + e_{R_2} \left(\frac{1}{C_1 C_2 R_1 R_2} + \frac{s(C_1 + C_2)}{C_1 C_2 R_2} \right) \\ - e_{n1} \left(\frac{s}{C_1 R_1} + \frac{s(C_1 + C_2)}{C_1 C_2 R_2} + s^2 + \frac{1}{R_1 R_2 C_1 C_2} \right) + I_{n2} \left(\frac{1}{C_1 C_2 R_1} + \frac{s(C_1 + C_2)}{C_1 C_2} \right) \end{array} \right)}{s^2 + \frac{s(C_1 + C_2)}{R_2 C_1 C_2} + \frac{1}{R_1 R_2 C_1 C_2}} \tag{2.134a}$$

It can be seen that the four noise sources have different noise transfer functions. We next express (2.134a) as

$$V_o = -(e_{R1}\, H_1(s) + e_{R2}\, H_2(s) + e_{n1}\, H_3(s) + I_{n2}\, H_4(s)) \tag{2.134b}$$

Note that $H_1(s)$, $H_2(s)$, and $H_3(s)$ are dimensionless whereas $H_4(s)$ corresponds to a resistance. The total output noise e_{nt} can be found as

$$e_{nt}^2 = \left(\begin{array}{l} e_{R1}^2 \displaystyle\int_0^\infty |H_1(j\omega)|^2 d\omega + e_{R2}^2 \int_0^\infty |H_2(j\omega)|^2 d\omega + e_{n1}^2 \int_0^\infty |H_3(j\omega)|^2 d\omega \\ + I_{n2}^2 \displaystyle\int_0^\infty |H_4(j\omega)|^2\, d\omega \end{array} \right) \tag{2.135}$$

Bruton, Trofimenkoff, and Treleaven [2.65, 2.66] have given closed-form expressions for these integrals for general biquadratic transfer functions. The low-pass and band-pass transfer functions have simple solutions:

$$\int_0^\infty \left| \frac{s\,\omega_p}{s^2 + s\frac{\omega_p}{Q_p} + \omega_p^2} \right|_{s=j\omega}^2 d\omega = \frac{Q_p\,\pi\,\omega_p}{2} \tag{2.136a}$$

$$\int_0^\infty \left| \frac{\omega_p^2}{s^2 + s\frac{\omega_p}{Q_p} + \omega_p^2} \right|_{s=j\omega}^2 d\omega = \frac{Q_p\,\pi\,\omega_p}{2} \tag{2.136b}$$

Applying these relationships, corresponding to a general biquadratic transfer function given as

$$H(s) = \frac{a\,s^2 + bs + c}{s^2 + s\left(\frac{\omega_p}{Q_p}\right) + \omega_p^2} \tag{2.137}$$

we obtain the noise spectral density as

$$|H_1(j\omega)|^2 = a^2 + \frac{\omega^2\ \omega_p^2 \left(\frac{b^2 - 2ac}{\omega_p^2} - \frac{a^2}{Q_p^2} + 2\,a^2 \right)}{D} + \frac{\omega_p^4 \left(\frac{c^2}{\omega_p^4} - a^2 \right)}{D} \tag{2.138}$$

where

$$D = \omega^4 + \omega^2 \left(\frac{\omega_p^2}{Q_p^2} - 2\,\omega_p^2 \right) + \omega_p^4 \tag{2.139}$$

Hence, (2.138) can be written as

$$|H_1(j\omega)|^2 = a^2 + \left(\frac{b^2 - 2ac}{\omega_p^2} - \frac{a^2}{Q_p^2} + 2a^2\right)|H_{BP}(j\omega)|^2 + \left(\frac{c^2}{\omega_p^4} - a^2\right)|H_{LP}(j\omega)|^2$$
$$= a^2 B_x + \left(\frac{b^2 - 2ac}{\omega_p^2} - \frac{a^2}{Q_p^2} + a^2 + \frac{c^2}{\omega_p^4}\right)|H_{BP}(j\omega)|^2 \tag{2.140}$$

where B_x is the measurement bandwidth since from (2.136a) and (2.136b), $\int_0^\infty |H_{LP}(j\omega)|^2 d\omega$ and $\int_0^\infty |H_{BP}(j\omega)|^2 d\omega$ are the same. Thus from (2.140), it follows that

$$|H_1(j\omega)|^2 = a^2 B_x + \left(\frac{b^2 - 2ac}{\omega_p^2} - \frac{a^2}{Q_p^2} + a^2 + \frac{c^2}{\omega_p^4}\right)\frac{Q_p \pi \omega_p}{2} \tag{2.141}$$

As an illustration, for the high-pass case ($b = c = 0$), we have

$$|H_1(j\omega)|^2 = a^2 B + \left(-\frac{a^2}{Q_p^2} + a^2\right)\frac{Q_p \pi \omega_p}{2} \tag{2.142}$$

For the noise source e_{R2}, matching the noise transfer function (2.134a) with (2.137), we note that $a = 0, b = \frac{C_1 + C_2}{C_1 C_2 R_2}, c = \frac{1}{C_1 C_2 R_1 R_2}$ and from the general formula (2.141), we obtain the noise as $e_{R_2}^2 \left(1 + \frac{(C_1 + C_2)^2 R_1}{C_1 C_2 R_2}\right)|H_{LP}(j\omega)|^2$. In a similar manner, we obtain the total noise of the circuit of Fig. 2.40a from (2.135) as

$$e_{tn}^2 = e_{R_1}^2 \frac{1}{\omega_p^2 C_1^2 R_1^2}|H_{LP}(j\omega)|^2 + e_{R_2}^2\left(1 + \frac{(C_1 + C_2)^2 R_1}{C_1 C_2 R_2}\right)|H_{LP}(j\omega)|^2$$
$$+ i_{n2}^2\left(R_2^2 + \frac{(C_1 + C_2)^2 R_1 R_2}{C_1 C_2}\right)|H_{LP}(j\omega)|^2$$
$$+ e_{n1}^2\left(B_x + |H_{LP}(j\omega)|^2\left(\frac{1}{\omega_p^2 C_1^2 R_1^2} + \frac{2}{\omega_p Q_p C_1 R_1}\right)\right) \tag{2.143}$$

Substituting for the integrals using (2.136), we have

$$e_{tn}^2 = \left(\begin{array}{l} e_{R_1}^2 \frac{1}{\omega_p^2 C_1^2 R_1^2} + e_{R_2}^2\left(1 + \frac{(C_1 + C_2)^2 R_1}{C_1 C_2 R_2}\right) + i_{n2}^2\left(R_2^2 + \frac{(C_1 + C_2)^2 R_1 R_2}{C_1 C_2}\right) \\ + e_{n1}^2\left(\frac{1}{\omega_p^2 C_1^2 R_1^2} + \frac{2}{\omega_p Q_p C_1 R_1}\right) \end{array}\right)\frac{Q_p \pi \omega_p}{2}$$
$$+ e_{n1}^2 B_x \tag{2.144}$$

It is seen that the active noise (decided by i_{n2} and e_{n1}) and passive noise (decided by e_{R1} and e_{R2}) are dependent on the resistor and capacitor values. These can be optimized by appropriate design.

In active RC filters, the active noise can be made low by using low-noise opamps so that the resistor noise is dominant.

Consider, for example, the case $C_1 = C_2$. Evidently, for this choice in the circuit of Fig. 2.40a, we have $Q_p = \frac{1}{2}\sqrt{\frac{R_2}{R_1}}$ and $\omega_p - = \frac{1}{2Q_p\ C_1\ R_1}$ yielding from (2.144),

$$e_{tn}^2 = \left(\frac{2kT}{\pi}\left(R_2\left(2+\frac{1}{Q_p^2}\right)\right) + i_{n2}^2\ R_2^2\left(1+\frac{1}{Q_p^2}\right) + e_{n1}^2\left(4Q_p^2+4\right)\right)\frac{Q_p\,\pi\,\omega_p}{2} + e_{n1}^2\ B_x \tag{2.145}$$

Generally i_{n1} and i_{n2} of the opamp will be very small, typically $0.1\text{pA}/\sqrt{Hz}$, and hence the term containing i_{n1} can be neglected. As an illustration, for realizing $Q_p = 5$ and a pole-frequency $f_p = 1{,}000$ Hz, we obtain $\frac{R_2}{R_1} = 100$. Next, choosing $R_1 = 1\ \text{K}\Omega$ and $R_2 = 100\ \text{K}\Omega$ and considering $C_1 = C_2 = C$, we have $C = 15{,}923$ pF. Considering a typical opamp with $e_{nI} = 15$ nV/√Hz, the total noise can be found from (2.145) as

$$e_{tn}^2 = (1155.673 + 26.53)\ 10^{-12}$$

where the first term is inherent noise (passive noise) and the second term is active noise. The rms noise can be found by finding the square root of ${e_{nt}}^2$ and is thus 34.38 μV. The active noise is more than the passive noise for this circuit.

For single-amplifier filters, Bachler and Guggenbuhl [2.67, 2.68] have suggested that the passive noise can be modeled by a noise voltage source at the inverting input of the opamp and the equivalent noise resistance can be estimated as $\text{Re}\left(\frac{1}{y_{22}}\right)$ where $\left(\frac{1}{y_{22}}\right)$ is the equivalent resistance at the inverting input of the opamp with the opamp disconnected and grounding the terminal connected to the opamp output terminal and input terminal of the filter (see Fig. 2.41a). As an illustration, for the circuit of Fig. 2.41a, we have

$$\text{Re}\left(\frac{1}{y_{22}}\right) = \frac{R_2\left(1+\omega^2\left(C_2^2\ R_1\ R_2 + 2R_1^2\ C_1\ C_2 + C_2^2\ R_1^2 + C_1^2\ R_1^2\right)\right)}{\left(1-\omega^2\ R_1\ R_2\ C_1\ C_2\right)^2 + \omega^2\ \left(C_1\ R_1 + C_2\ R_1\right)^2} \tag{2.146}$$

The noise can then be evaluated from the model shown in Fig. 2.41b. Note that e_{np} and e_{na} are the active and passive noise contributions which have the same transfer function that has already been derived in (2.134a) (see e_{n1} term). Note that the denominator in (2.146) cancels with the squared magnitude of the coefficient of the e_{n1} term in (2.134a) yielding the same result as before. The total passive noise

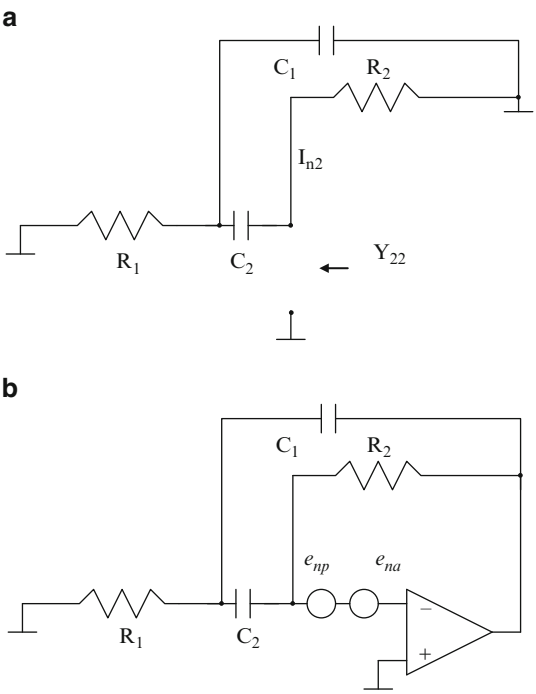


Fig. 2.41 (**a**) Circuit for estimation of passive noise of the active RC filter of Fig. 2.40b, (**b**) complete noise model

can be estimated by integrating $\frac{2kT}{\pi}\text{Re}\left(\frac{1}{y_{22}}\right)|H_n(j\omega)|^2$ where $H_n(s)$ is the transfer function of the noise source to the output of the filter. The same result can be obtained by combining the noise due to R_1 and R_2 in (2.144)

Bachler and Guggenbuhl [2.67, 2.68] have also pointed out that the noise transfer function is the same as GSP which is shown next. Considering the circuit of Fig. 2.42a, the transfer function can be written as

$$T = -\frac{t_{31}}{t_{32} + \frac{1}{A}} \tag{2.147}$$

where t_{31} is the transfer function of the three- terminal network at terminal 3 with input given at terminal 1. The GSP can then be derived as

$$GSP = A\, S_A^T = \frac{1}{t_{32} + \frac{1}{A}} \cong \frac{1}{t_{32}} \tag{2.148}$$

Next considering the noise source as shown in Fig. 2.42b, the transfer function is given as

$$\frac{V_0}{e_n} = \frac{1}{t_{32}} \tag{2.149}$$

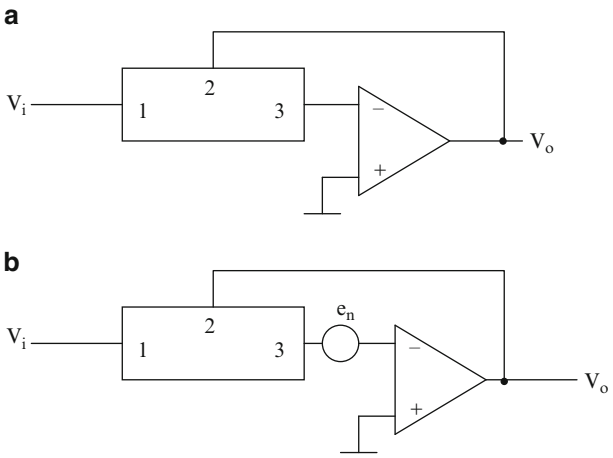


Fig. 2.42 (**a**) Circuit for estimating the GSP of an active RC circuit, and (**b**) circuit for noise estimation

From (2.148) and (2.149), we see that the GSP is the same as the noise transfer function. Note from (2.148) that the GSP is a function of frequency. It may be recalled that in our earlier definition of the GSP with respect to A, the finite gain of the opamp, the GSP was found to be dimensionless. Even though the GSP defined by (2.148) is frequency-dependent, it can be shown that the GSP value at the pole-frequency is equal to the GSP with respect to A (i.e., AS^{Q}_{A}). Thus minimizing the GSP by the proper choice of resistors and capacitor values (spreads) to reduce the active sensitivity will lead to minimization of active noise of an active RC filter, an interesting result. It is useful to note that since the passive noise is also dependent on $\mathrm{Re}\left(\frac{1}{y_{22}}\right)$, optimization of the GSP alone may not reduce passive noise.

The total noise of the filter is the sum of active and passive noise. Bachler and Guggenbuhl [2.67, 2.68] have shown that the total noise using the spread of components as a degree of freedom can be computed and optimized. This is similar to sensitivity optimization which has passive and active components. The reader is referred to their work for more information.

The application of minimization of the GSP to reduce noise has been extended to the minimization of distortion as well by Borys [2.73]. This aspect is considered next after studying distortion in active RC filters.

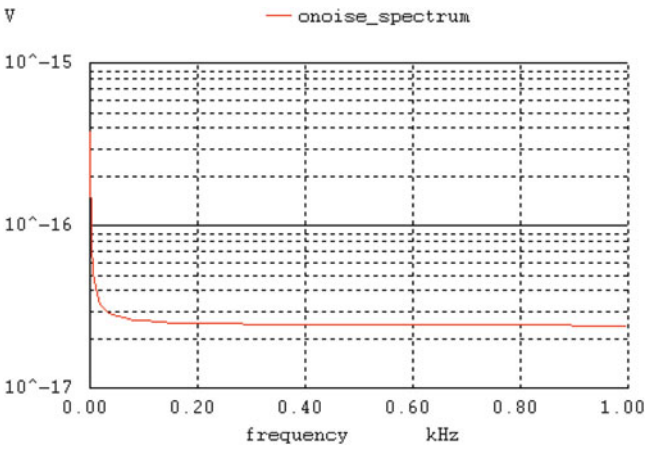
We consider SPICE-based estimation of noise of active RC filters in the next two examples.

Example 2.12 The noise voltage source will have thermal noise as well as $1/f$ noise components. These can be modeled using resistor and diode noise biased in the knee region. The amount of $1/f$ noise can be controlled by the value KF in the diode model. The biasing voltage can be defined, for example, as $V_1\ (= V_2) = 0.1$ V and a resistor R_{30} (and R_{31}) is used in series with the diode D_1 (and D_2) to generate wide-band noise. Two such independent circuits are used and the floating voltage

between these (nodes 59 and 61) is taken to remove the dc component. The noise statement has an ac reference point which in this case is one zero voltage source v_3 connected in series. The total noise as well as its various constituents such as diode resistance noise, $1/f$ noise, resistor noise, and the like, can be found by the command *print all*. The noise spectrum can be seen by the command *plot ylog onoise_spectrum*. Note also that input referred noise also can be obtained.

```
*opamp voltage noise generation
V3 58 0 ac 0
V1 58 65 dc 0.1
V2 60 0 0.1
D1 65 59 DIODE
R30 59 0 726.4
D2 60 61 DIODE
R31 61 0 726.4
E1 1 0 59 61 1

.MODEL DIODE D(AF=1.0,IS=0.001F,KF=1.667E-9)
.noise v(1) v3 dec 10 0.5 1000 1
```

```
*Opamp voltage noise generation
V3 58 0 ac 0
V1 58 65 dc 0.1
V2 60 0 0.1
D1 65 59 DIODE
R30 59 0 726.4
D2 60 61 DIODE
R31 61 0 726.4
E1 1 0 59 61 1

.MODEL DIODE D(AF=1.0,IS=0.001F,KF=1.667E-9)
.noise v(1) v3 dec 10 0.5 1000 1
```



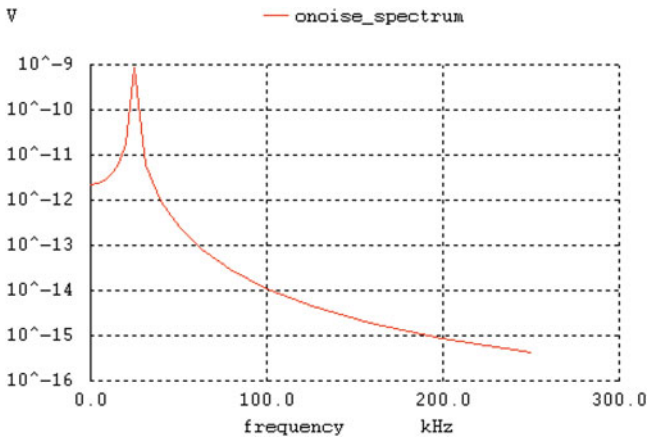
Circuit: *Opamp voltage noise generation
TEMP=27 deg C
Noise analysis ... 100%
WinSpice 3 -> print all
inoise_total = 2.534923e+06
inoise_total_d1 = 6.683765e+04
inoise_total_d1_1overf = 6.683765e+04
inoise_total_d1_id = 1.685981e-03
inoise_total_d1_rs = 0.000000e+00
inoise_total_d2 = 6.686825e+04
inoise_total_d2_1overf = 6.686825e+04
inoise_total_d2_id = 1.686753e-03
inoise_total_d2_rs = 0.000000e+00
inoise_total_r30 = 1.200609e+06
inoise_total_r31 = 1.200609e+06
onoise_total = 2.534923e-14
onoise_total_d1 = 6.683765e-16
onoise_total_d1_1overf = 6.683765e-16
onoise_total_d1_id = 1.685981e-23
onoise_total_d1_rs = 0.000000e+00
onoise_total_d2 = 6.686825e-16
onoise_total_d2_1overf = 6.686825e-16
onoise_total_d2_id = 1.686753e-23
onoise_total_d2_rs = 0.000000e+00
onoise_total_r30 = 1.200609e-14
onoise_total_r31 = 1.200609e-14

Example 2.13 The analysis of a multiple feedback band-pass filter using the opamp noise model obtained earlier is considered next. An offset compensating resistor R_3 is also used.

The complete noise model is in the subcircuit *noisyopamp*. Note that the opamp input terminals have noisy current sources which do not have a $1/f$ component and hence simple resistors can be used. The resistors R_{32} and R_{33} need to be in a closed circuit and hence zero voltage sources V17 and V18 are connected across them. The current sources are implemented by the statements FN1 in. 0 V18 1 and FN2 ninp 0 V17 1, respectively. As before the total output referred noise, input referred noise, and noise spectrum can be found as shown. The band-pass filtering of the noise spectrum is evident.

*Example MFB noise analysis
R1 1 2 62.5
R2 4 3 100 K
C1 2 3 1590 pf
C2 2 4 1590 pf
R3 71 0 62.5

```
Xopamp1 4 71 3 noisyopamp
.subckt noisyopamp 70 ninp out
V1 58 0 dc 0.1
V2 60 0 dc 0.1
D1 58 59 DIODE
R30 59 0 726.4
D2 60 61 DIODE
R31 61 0 726.4
E1 70 in. 59 61 1
V17 62 0 0
V18 63 0 0
R32 62 0 73.6
R33 63 0 73.6
FN1 in. 0 V18 1
FN2 ninp 0 V17 1

E2 15 0 ninp inp 100,000
R4 15 16 1 k
C3 16 0 15.9 uf
E3 out 0 16 0 1
.ends noisyopamp

vin 1 0 ac 0
.noise v(3) vin dec 10 0.5 300,000 1

.MODEL DIODE D(AF=1.0,IS=0.001F,KF=1.667E-9)
```



Circuit: *example MFB noise analysis

TEMP=27 deg C
Noise analysis . . . 100%
WinSpice 4 -> print all

inoise_total = 2.408588e+14
inoise_total_d:xopamp1:d1 = 2.305272e+08
inoise_total_d:xopamp1:d1_1overf = 2.305261e+08
inoise_total_d:xopamp1:d1_id = 1.118864e+03
inoise_total_d:xopamp1:d1_rs = 0.000000e+00
inoise_total_d:xopamp1:d2 = 2.305272e+08
inoise_total_d:xopamp1:d2_1overf = 2.305261e+08
inoise_total_d:xopamp1:d2_id = 1.118864e+03
inoise_total_d:xopamp1:d2_rs = 0.000000e+00
inoise_total_r1 = 6.830456e+10
inoise_total_r2 = 1.758265e+11
inoise_total_r3 = 6.852223e+10
inoise_total_r:xopamp1:r4 = 1.096356e+02
inoise_total_r:xopamp1:r30 = 7.963928e+11
inoise_total_r:xopamp1:r31 = 7.963928e+11
inoise_total_r:xopamp1:r32 = 5.818804e+10
inoise_total_r:xopamp1:r33 = 2.388947e+14
onoise_total = 2.408588e-06
onoise_total_d:xopamp1:d1 = 2.305272e-12
onoise_total_d:xopamp1:d1_1overf = 2.305261e-12
onoise_total_d:xopamp1:d1_id = 1.118864e-17
onoise_total_d:xopamp1:d1_rs = 0.000000e+00
onoise_total_d:xopamp1:d2 = 2.305272e-12
onoise_total_d:xopamp1:d2_1overf = 2.305261e-12
onoise_total_d:xopamp1:d2_id = 1.118864e-17
onoise_total_d:xopamp1:d2_rs = 0.000000e+00
onoise_total_r1 = 6.830456e-10
onoise_total_r2 = 1.758265e-09
onoise_total_r3 = 6.852223e-10
onoise_total_r:xopamp1:r4 = 1.096356e-18
onoise_total_r:xopamp1:r30 = 7.963928e-09
onoise_total_r:xopamp1:r31 = 7.963928e-09
onoise_total_r:xopamp1:r32 = 5.818804e-10
onoise_total_r:xopamp1:r33 = 2.388947e-06

2.12 Distortion in Active RC Filters

The large signal handling capability of active filters implies the use of components that collectively exhibit a linear behavior, even though the active components may be intrinsically nonlinear, such as bipolar transistors or MOS transistors. In a differential amplifier, the basic element in the opamp, the nonlinearity arises for two reasons: nonlinear V−I conversion of the input differential pair and the voltage dependence of the output impedance of the cascade devices.

If an opamp is overdriven by a large input signal, the output slews at some limiting rate determined by internal currents and capacitances. If an applied sinusoidal input signal causes the output to have the maximum slope greater than the slew rate of the opamp, the output will no longer be sinusoidal and will suffer distortion. There can be *slew-induced distortion* (SID) of amplitude in the open-loop mode of the amplifier operation but phase distortion may not exist. On the other hand, in the closed-loop mode, both will exist. Under typical operating conditions, the SID causes phase shift (phase lag) and an attenuation of the fundamental component of the input signal at the output. In active RC filters, the OA slew rate can cause distortion by creating harmonics and intermodulation products. Such degradation can lead to instability and this phenomenon is called "*jump resonance*." In such a situation, the filter will exhibit two modes of operation and will regeneratively switch back and forth between these two modes of operation.

The distortion increases with increasing input signal level between the input terminals of the opamp. The opamp input voltage, although small, will not be negligible as has been seen earlier due to the finite gain and bandwidth of the opamp. When this voltage reaches a certain threshold, nonlinearity increases. Hence, it is important to reduce the differential input voltage of the opamp to a small value. The distortion of the opamp can be considered to be at the output of the opamp (output referred distortion) or at the input of the opamp (input referred distortion). Thus the transfer function of distortion source to the opamp output in the latter case is same as that of noise as seen in Fig. 2.42b. Thus minimizing the GSP minimizes distortion and noise as well as sensitivity.

The effect of the output referred distortion can be evaluated by a figure of merit, the *distortion aggravation factor* (DAG) introduced by Billam [2.69]. Evidently, the transfer functions due to *input referred distortion* or *output referred distortion* are related by the frequency-dependent finite gain of the opamp.

Consider the Sallen and Key active RC filter schematic of Fig. 2.43 wherein the distortion is denoted by U_{in}. We evaluate DAG for this circuit as

$$DAG = \frac{V_o}{U_{in}} = \frac{s^2\ C_1\ C_2\ R_1\ R_2 + s(C_1\ R_1 + C_2\ (R_1 + R_2)) + 1}{s^2\ C_1\ C_2\ R_1\ R_2 + s(C_1\ R_1\ (1-K) + C_2\ (R_1 + R_2)) + 1} \tag{2.150}$$

Thus, DAG will be maximum at the pole-frequency ω_p given by

$$DAG_{MAX} = \frac{C_1\ R_1 + C_2\ (R_1 + R_2)}{C_1\ R_1\ (1-K) + C_2\ (R_1 + R_2)} \tag{2.151}$$

Evidently, DAG is $3Q_p$ at the resonant frequency and is maximum at this frequency for the choice $R_1 = R_2 = R$ and $C_1 = C_2 = C$ and $K = 3 - \frac{1}{Q_p}$. On the other hand, by choosing unequal resistor and capacitor values, DAG can be reduced. Defining $GSP = K\, S_K^Q$, we have from the denominator of (2.150),

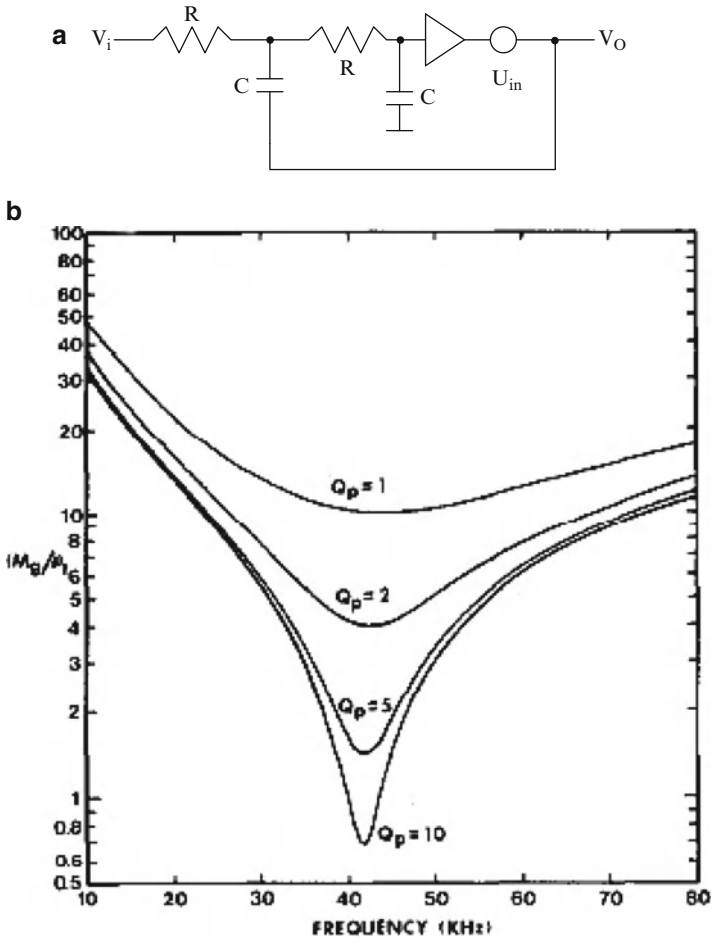


Fig. 2.43 (**a**) Sallen–Key active RC filter modeling input referred distortion, (**b**) plots of input signal versus frequency for the Sallen–Key active RC filter with Q as a parameter (pole-frequency 10 KHz $R_1 = R_2$ and $C_1 = C_2$ using 741 opamp). ((**b**) Adapted from [2.71] ©IEEE 1978)

$$GSP = \frac{K^2 C_1 R_1}{C_1 R_1 (1-K) + C_2 (R_1 + R_2)} \tag{2.152}$$

Thus, DAG and GSP are related as

$$DAG_{MAX} = GSP\left(\frac{C_1 R_1 + C_2 (R_1 + R_2)}{K^2 C_1 R_1}\right) \tag{2.153}$$

As an illustration, for $R_1 = R_2 = R$, $C_1 = C_2 = C$, we have $GSP = 9Q_p$ and $DAG = 3Q_p$. This can also be observed by noting that the GSP is the same as the noise transfer function. If distortion is also input referred, it is the same as the GSP.

It can be seen that Billam's technique [2.69] does not consider the nonidealities of the opamp. Allen [2.70, 2.71] has suggested taking the bandwidth of the amplifier into account, since due to the finite gain and bandwidth of the opamp, the differential input voltage at the opamp input terminals is finite and if it exceeds a particular threshold value δ, distortion sets in. As such, for a given input M_g, Allen suggests evaluating the resulting δ expressed as M_g/δ which reaches a minimum at a particular frequency. That minimum is less than δ. Note that the differential input voltage of the opamp is $V_o s/B$. We consider the Sallen–Key filter of Fig. 2.43a once again and evaluate the magnitude of M_g/δ as

$$\frac{M_g}{\delta} = \sqrt{\left(1 - \omega_n^2 + \frac{B_n}{3\,Q_p - 1}\right)^2 + \left(3\,\omega_n + \frac{B_n\,Q_p}{3\,Q_p - 1}\left(\omega_n - \frac{1}{\omega_n}\right)^2\right)^2} \qquad (2.154)$$

where $\omega_n = \frac{\omega}{\omega_p}$ and $B_n = \frac{B}{\omega_p}$

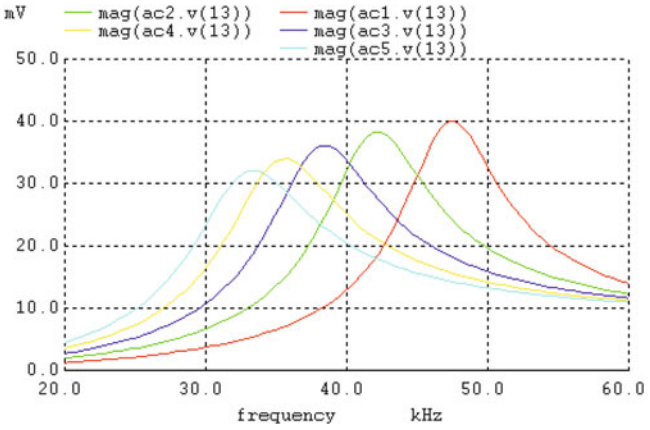
Typical curves for different pole-Qs are as shown in Fig. 2.43b for an example considering $f_p = 50$ KHz. Thus for a pole-Q of 10, the input voltage must be less than 140 mV assuming $\delta = 100$ mV for a typical bipolar opamp μA741 so that SID cannot set in. In a similar manner, the SID for other single-amplifier biquads can be carried out. Beyond this threshold value, the active filters will exhibit jump resonance. The reader is referred to Borys [2.72, 2.73, 2.74] for an explanation of the relationship between various distortion measures.

Example 2.14 Determine the level at which SID may set in for the single amplifier band-pass filter tunable using a resistor (see Fig. E.2.5b) using SPICE.

The input voltage maximum at the opamp inverting input can be found from the frequency responses plotted in Fig. 2.43b. If it exceeds a certain level, slew-induced distortion sets in.

```
*SA Bandpass distortion Allen's method

vin 1 0 ac 1 v

R11 1 12 15900
R12 12 0 200
C11 12 13 1000 pf
C12 12 14 1000pf
R16 13 14 31800
E11 0 15 13 0 100000
R14 15 16 1 k
C13 16 0 15.9 uf
E12 14 0 16 0 1

.control
destroy all
let ii = 0
while ii < 5
```

```
alter R12 = 200 + 100 * ii
ac lin 100 20k 60 k
let ii = ii + 1

plot mag(ac1.v(13)) mag(ac2.v(13)) mag(ac3.v(13)) mag(ac4.v(13)) mag(ac5.v
(13))
end
.endc
```



2.13 Problems

P.2.1. A first-order all-pass filter can be obtained by using the circuit of Fig. P.2.1. Analyze the circuit and compare it with the first-order all-pass filters using the opamp of Fig. 2.8a, b. Show that the circuit of Fig. P.2.1b realizes a second-order all-pass transfer function. Discuss the limitations of the circuit.

P.2.2. A bridged-T RC network is shown in Fig. P.2.2a. Derive the transfer function of this circuit and discuss its utility as a notch filter. The circuit

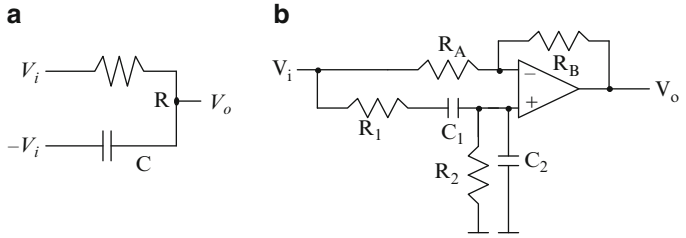


Fig. P.2.1 (**a**) (**b**)

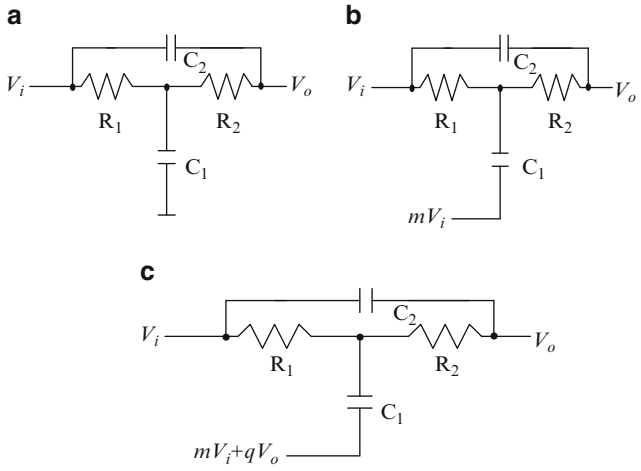


Fig. P.2.2

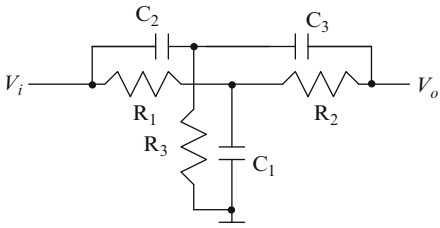


Fig. P.2.3

can be modified to realize a notch or all-pass transfer function using the configuration of Fig. P.2.2b. Analyze the circuit and determine the conditions for realizing notch and all-pass transfer functions. Discuss the limitations of this circuit. Positive feedback can be given to enhance the pole-Q using the modification as shown in Fig. P.2.2c. Derive the transfer function and establish the relationship between the pole-Q and the amount of positive feedback. Suggest a circuit for realizing $mV_i + qV_o$.

P.2.3. A parallel-T RC network is illustrated in Fig. P.2.3. Derive the transfer function of the circuit. This is a third-order network. Find the condition for pole-zero cancellation so that a second-order notch transfer function can be realized.

P.2.4. Hilberman [2.75] has shown that input and ground can be complements in an active RC filter. Using this concept, show that an all-pass filter can be easily obtained from the Tow–Thomas biquad. Compare the circuit with the all-pass filter realized using the feedforward technique in a Tow–Thomas biquad (Fig. P.2.4).

P.2.5. Second-order active RC filters can be built around the GIC. Two such circuits, Fig. P.2.5a due to Mikhael and Bhattacharya [2.76] and Fig. P.2.5b

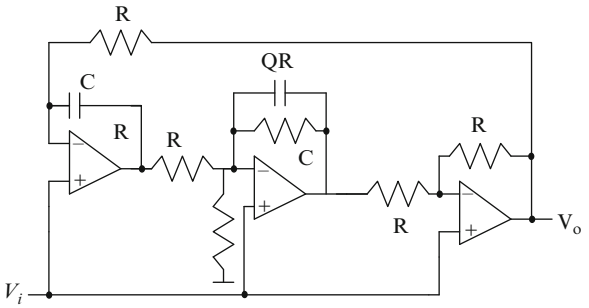


Fig. P.2.4 (Adapted from [2.75] ©IEEE 1973)

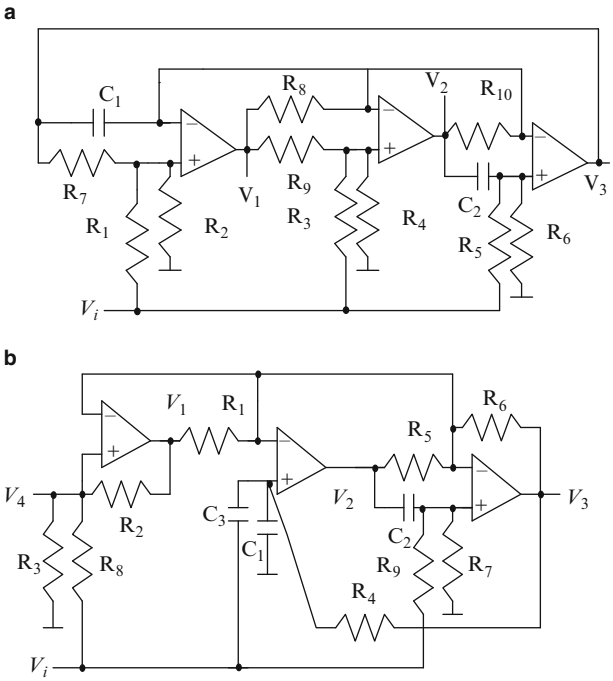


Fig. P.2.5 (Adapted from [2.14] ©IEEE 1984)

Padukone, Mulawka, and Ghausi [2.77] are shown below. Derive the transfer functions of both these circuits together with design equations and analyze the sensitivity of these filters due to opamp finite bandwidth.

P.2.6. A biquad due to Wilson, Bedri, and Bowron [2.78] based on two first-order all-pass filters is presented in Fig. P.2.6. Derive the transfer function of the

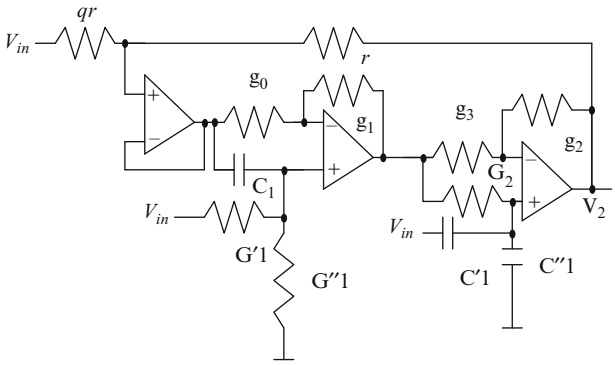


Fig. P.2.6 (Adapted from [2.14] ©IEEE 1984)

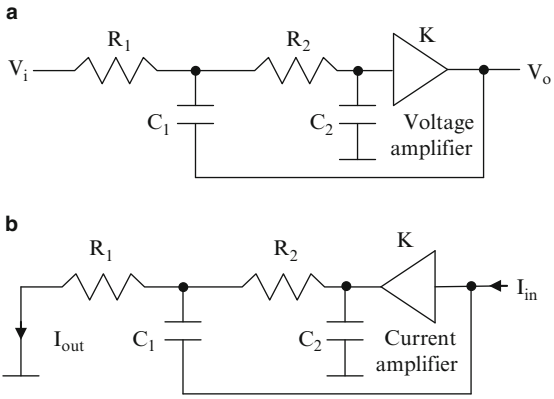


Fig. P.2.10 (**a**) (**b**)

circuit together with the design equations and analyze the effect of opamp finite bandwidth on performance.

P.2.7. Analyze the effect of finite opamp bandwidth on the pole-frequency and pole-Q of the active RC filter of Fig. 2.11b. Discuss the condition for instability.

P.2.8. Analyze the active R filters of Fig. 2.27 considering a two-pole model of the opamp. Discuss the stability of these circuits.

P.2.9. Derive the expressions for peak magnitude of the general second-order transfer function given in Appendix B.

P.2.10. A current-input current-output circuit can be obtained from the voltage-input voltage-output type active RC filter using voltage amplifiers (see, e.g., Fig. P.2.10a) by using the *adjoint technique*. In this technique, the output voltage terminal is fed the input current, the input voltage terminal is grounded, and the output current is tapped at this terminal as shown in Fig. P.2.10b. Discuss in which other cases the technique is applicable.

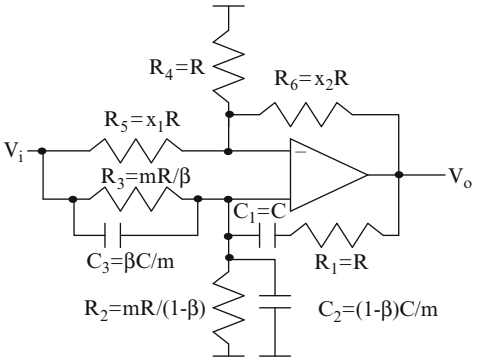


Fig. P.2.12 (Adapted from [2.79] ©IEEE 1973)

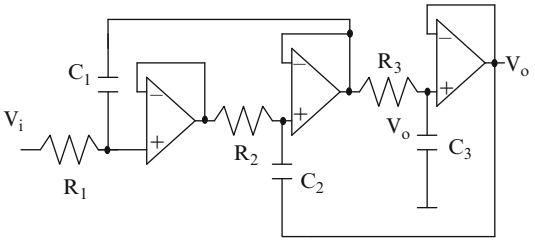


Fig. P.2.13

P.2.11. Derive expressions for the output noise of Tow–Thomas biquad of Fig. 2.18a. Assume that all opamps are identical.

P.2.12. An all-pass network can be realized using the circuit [2.79] of Fig. P.2.12. Derive the design equations and compare with the Steffen all-pass circuit of Fig. 2.13. Choose m for obtaining the minimum GSP. Examine the effect of the opamp finite bandwidth.

P.2.13. A high-order active RC filter due to Bach [2.80] using only unity gain buffers is shown in Fig. P.2.13. Derive the transfer function of this circuit and analyze the effect of finite bandwidth of the opamp. Suggest a design procedure. Derive a high-pass filter from this circuit and the design equations.

P.2.14. Denoting the pole of a second-order filter as p, with a denominator of the transfer function given as $s^2 + s\frac{\omega_p}{Q_p} + \omega_p^2$, show that $\Delta p/p$ in terms of variations in pole-Q and pole-frequency is given by $\frac{dp}{p} = \frac{d\omega_p}{\omega_p} - j\frac{dQ/Q}{\sqrt{4Q_p^2 - 1}}$ [2.81]. This means that it is important to reduce $\frac{d\omega_p}{\omega_p}$ which is $2Q_p$ times more than $\frac{dQ_p}{Q_p}$. Show also that $\frac{d|T(s)|}{|T(s)|} = \frac{dQ_p}{Q_p} + j2Q_p\frac{d\omega_p}{\omega_p}$ and also that $\frac{d|T(s)|}{|T(s)|} = 2Q_p\frac{dp}{p}$ at the frequency$\omega = \omega_p$.

P.2.15. Considering single-pole and two-pole models for the opamps, evaluate the bandwidth of both the amplifiers [2.82] of Fig. P.2.15a, b. Discuss the stability and improvement in bandwidth.

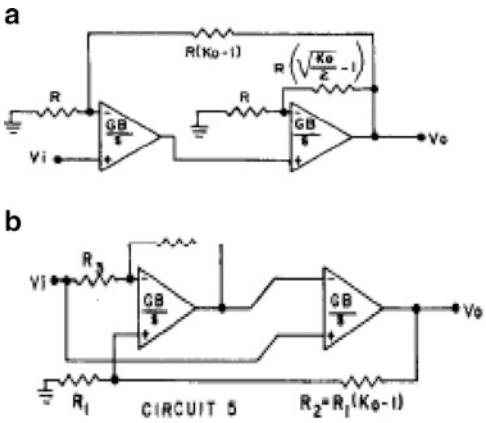


Fig. P.2.15 (**a**) (**b**) (Adapted from [2.82] ©IEEE 1977)

P.2.16. Analyze the performance of integrators using the compensated amplifiers of Fig. P.2.16a–e using two and three opamps [2.83].

P.2.17. Analyze the finite gain amplifiers shown [2.84] in Fig. P.2.17a, b and derive conditions to obtain the flat gain response.

P.2.18. Derive the expression for input impedance of the single-amplifier circuit [2.85, 2.87] of Fig. P.2.18. Analyze the nature of the input impedance. Considering the nonideal frequency response of the opamp, derive the input impedance and compare it with the results using an ideal opamp.

P.2.19. Repeat the problem for the circuit [2.86, 2.87] of Fig. P.2.19. Compare the results with those of Fig. P.2.18.

P.2.20. Derive the input impedance of the circuit [2.88] of Fig. P.2.20. Derive conditions under which a grounded FDNR in series with a capacitor can be realized.

P.2.21. Derive the transfer function of the active distributed network [2.89] of Fig. P.2.21a derived from Sallen–Key and multiple feedback type active RC filters. Using SPICE, simulate the frequency response and discuss the design procedure to realize a given specification. Note that a uniform distributed RC network can be modeled as a π network with irrational impedances as shown in Fig. P.2.21b.

Note that $Y = \frac{\sqrt{sc/r}}{\sinh \sqrt{src\,d^2}}$ and a shunt admittance of $(P-1)Y$ where $P = \cosh \sqrt{src\,d^2}$.

P.2.22. Analyze the positive impedance converter or active transformer [2.90] of Fig. P.2.22 and derive an expression for input impedance when the load impedance is Z_L.

P.2.23. Show that the circuit of Fig. P.2.25 realizes a floating inductance [2.90]. Discuss the behavior with nonideal opamps.

P.2.24. Derive the transfer function of the circuit [2.90] of Fig. P.2.24 and discuss its possible application.

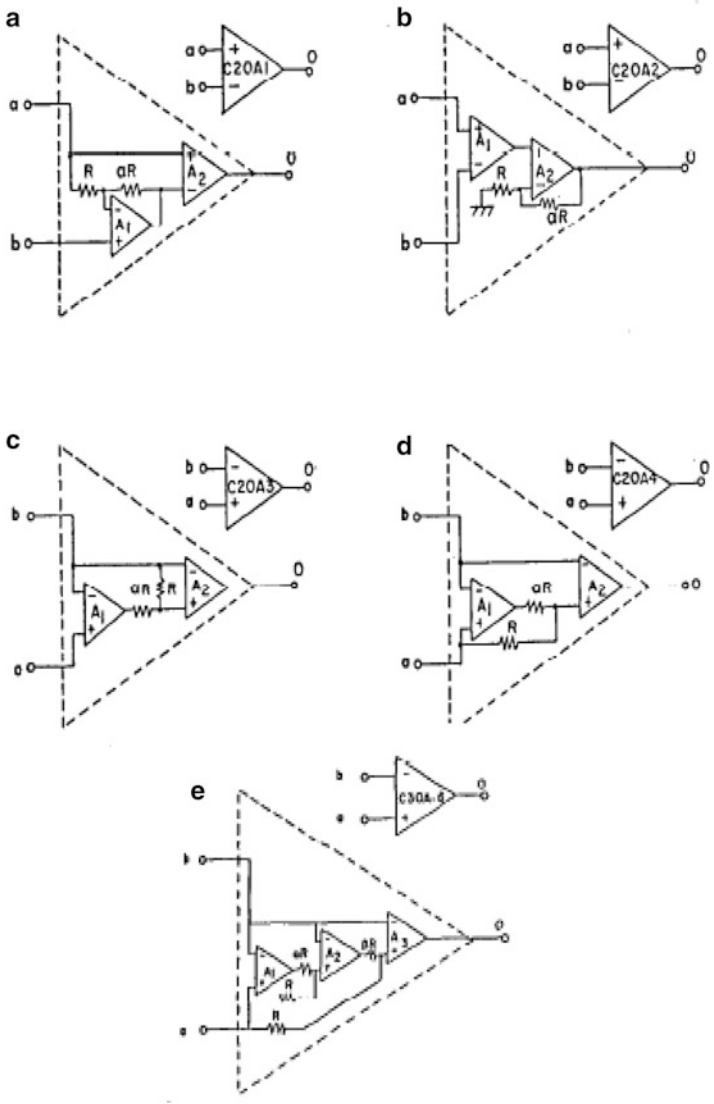


Fig. P.2.16 (Adapted from [2.83] ©IEEE 1987)

P.2.25. Derive the transfer functions of the 2 two-amplifier based filters [2.91] of Fig. P.2.26 and analyze their sensitivity to passive components and gains k1 and k2.

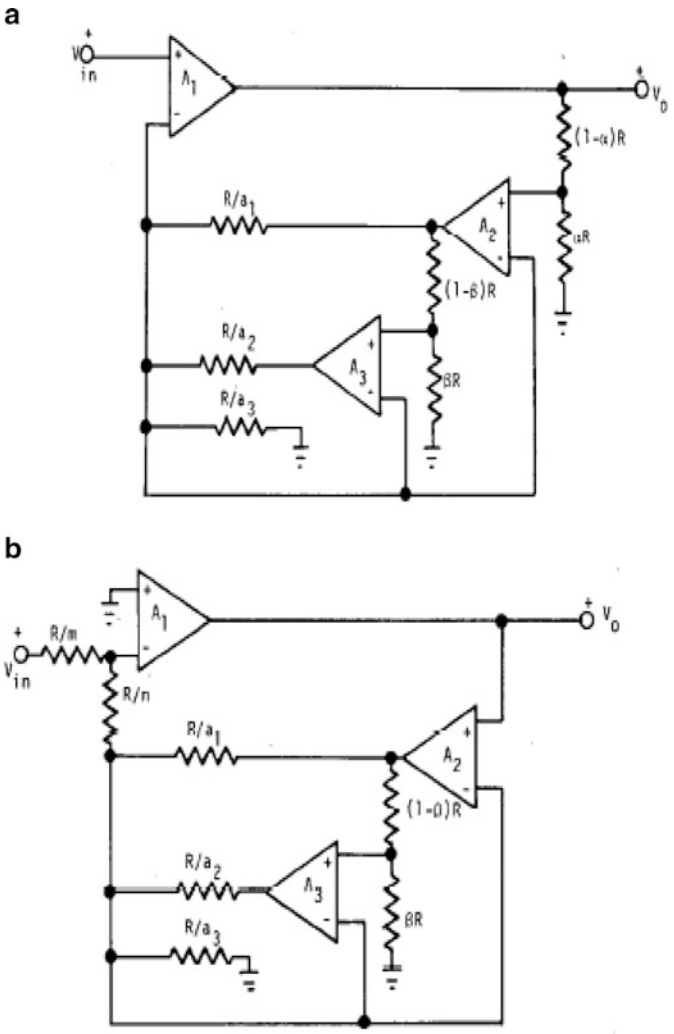


Fig. P.2.17 (**a**) (**b**) (Adapted from [2.84] ©IEEE 1980)

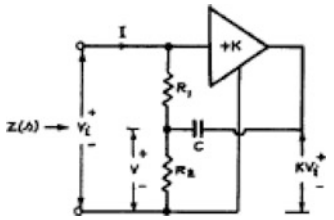


Fig. P.2.18 (Adapted from [2.87] ©IEEE 1970)

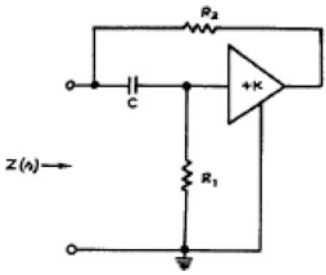


Fig. P.2.19 (Adapted from [2.87] ©IEEE 1970)

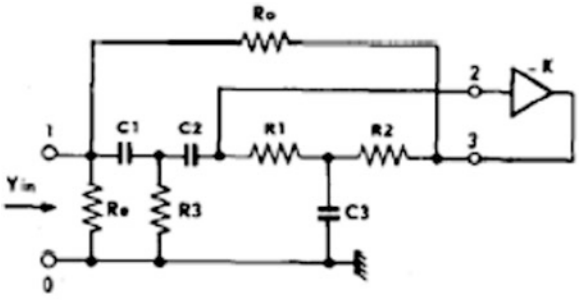


Fig. P.2.20 (Adapted from [2.88] ©IEEE 1974)

P.2.26. Derive the transfer function of the second-order filter [2.92] of Fig. P.2.26 using first-order all-pass networks. Compare with Tarmy–Ghausi modified by the Moschytz realization (Fig. 2.25a).

P.2.27. Analyze the two-amplifier-based active RC filters [2.93] of Fig. P.2.27a, b. Derive expressions for pole-frequency and pole-Q sensitivities.

P.2.28. Derive the transfer functions corresponding to both outputs of the active R filter of Fig. P.2.28 [2.94]. Derive conditions for realizing low-pass, band-pass, high-pass, notch, and all-pass transfer functions.

P.2.29. Derive the transfer functions of the transadmittance filters [2.95] of Fig. P.2.29a, b. Convert them into voltage-mode filters and discuss their utility.

P.2.30. A current conveyor is presented in Fig. P.2.30. This has the property that $V_x = V_y$, $I_z = I_x$, and $I_y = 0$. The input y is buffered and is available at the *x* terminal with a series resistance of Rx. The input current is mirrored and is available at the output terminal. The output terminal has finite output resistance and output capacitance to ground. Derive (a) an integrator, (b) a voltage amplifier, and (c) a current amplifier and obtain their transfer functions. Determine the bandwidth in cases (b) and (c) (Fig. P.2.30).

P.2.31. A second-order filter using a current conveyor CCII is shown in Fig. P.2.31. Derive its transfer function and sensitivity of pole-*Q* and pole-frequency to finite voltage transfer gain between the *y* and *x* terminals, finite current gain between the *x* and *z* terminals, and finite *Rx* and finite *Ro* and *Co* at the *z* terminal.

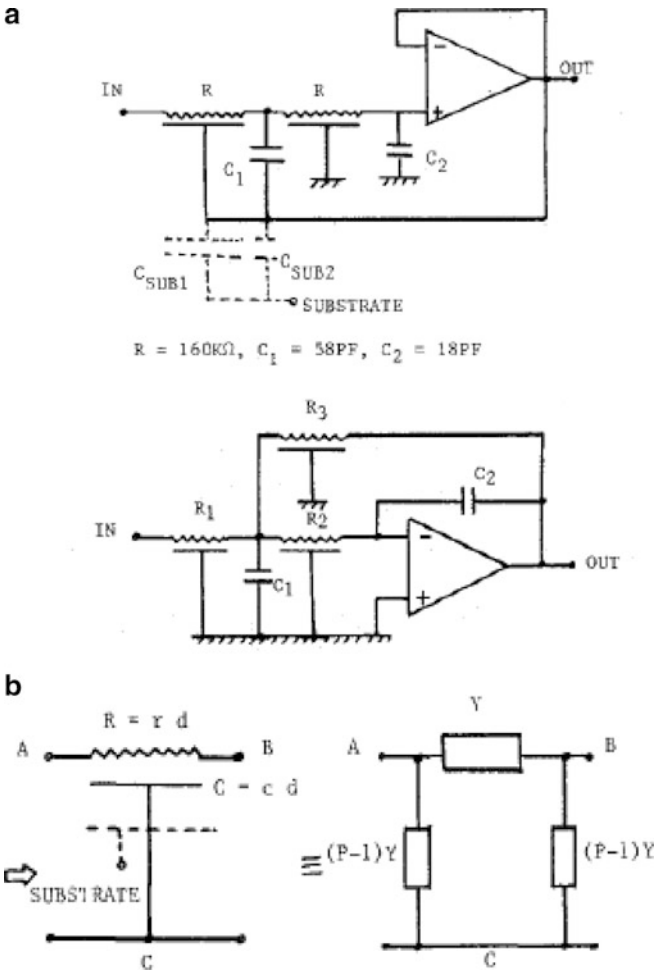


Fig. P.2.21 (**a**) (**b**) (Adapted from [2.89] ©IEEE 1987)

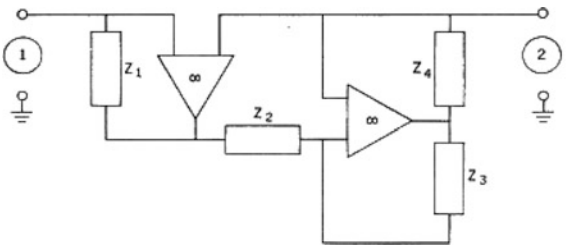


Fig. P.2.22 (Adapted from [2.90] ©IEEE 1971)

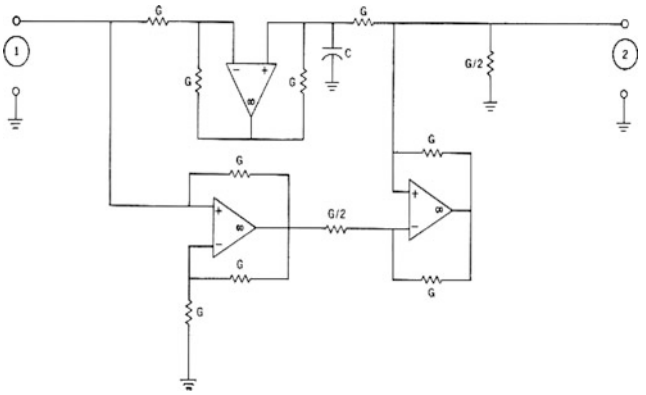


Fig. P.2.23 (Adapted from [2.90] ©IEEE 1971)

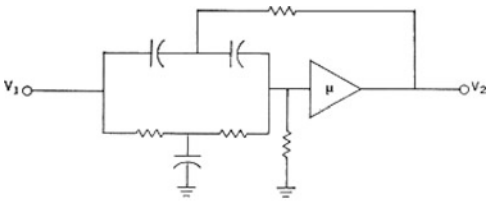


Fig. P.2.24 (Adapted from [2.90] ©IEEE 1971)

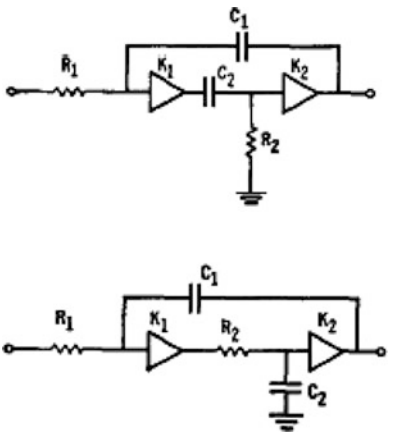


Fig. P.2.25 (Adapted from [2.91] ©IEEE 1971)

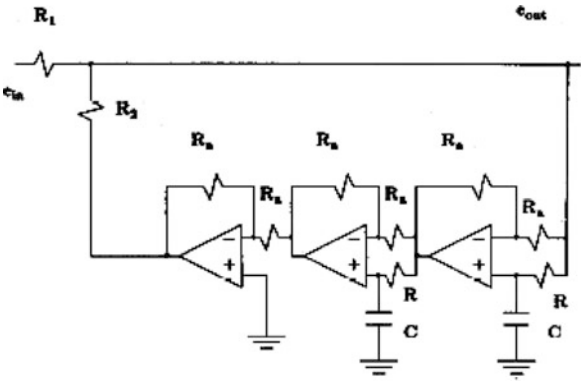


Fig. P.2.26 (Adapted from [2.92] ©IEEE 1968)

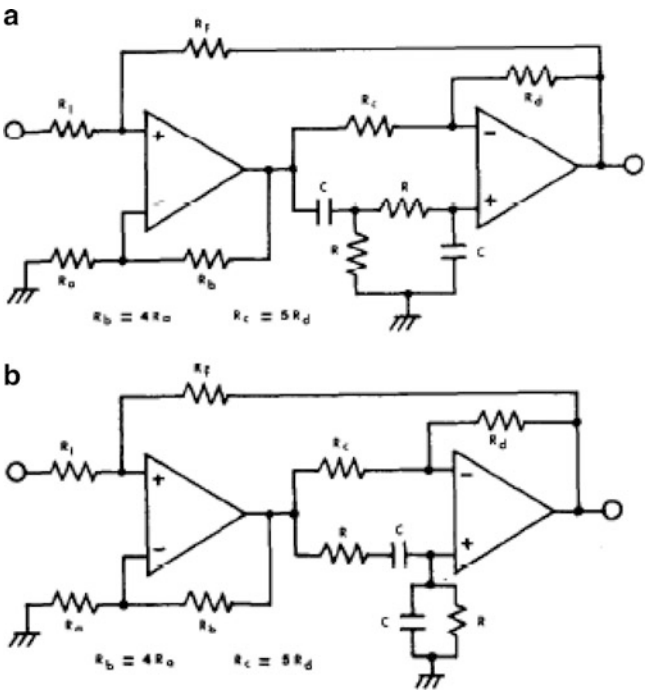


Fig. P.2.27 (**a**) (**b**) (Adapted from [2.93] ©IEEE 1978)

P.2.32. Derive the current-output–current-input transfer function of the circuit [2.96] of Fig. P.2.32. Analyze the effect of nonidealities of CCII.

P.2.33. Construct a state variable voltage mode and current mode biquad based on the Tow–Thomas biquad using a second-generation current conveyor. Derive the transfer functions and analyze the effect of nonidealities.

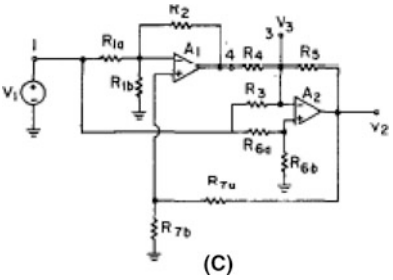


Fig. P.2.28 (Adapted from [2.94] ©IEEE 1977)

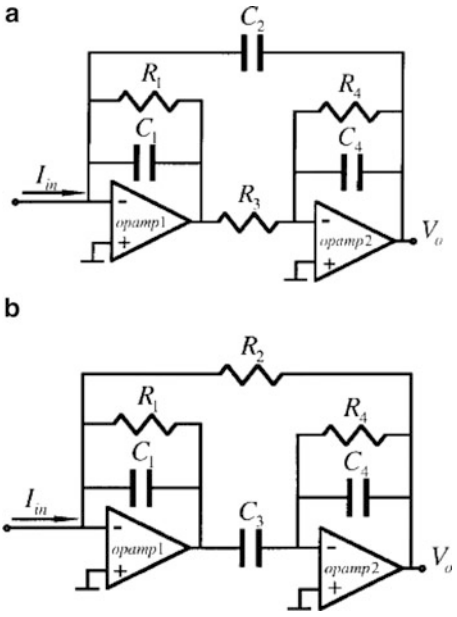


Fig. P.2.29 (Adapted from [2.95] ©IEEE 1997)

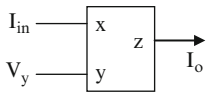


Fig. P.2.30

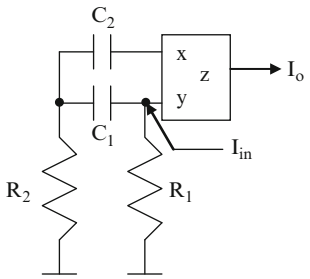


Fig. P.2.31

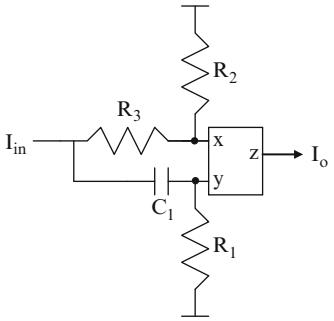


Fig. P.2.32 (Adapted from [2.96] ©IEEE 1990)

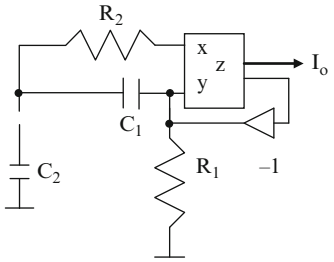


Fig. P.2.35 (Adapted from [2.97] ©IEEE 1987)

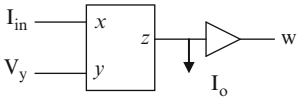


Fig. P.2.36

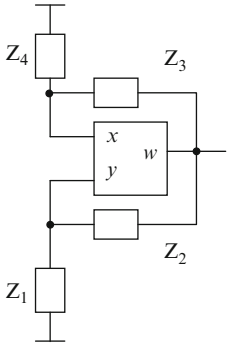


Fig. P.2.38 (Adapted from [2.98] ©IEEE 1996)

P.2.34. Derive a CCII-based biquad exactly identical to a KHN active RC biquad. (It should realize high-pass, low-pass, band-pass, and notch transfer functions.)

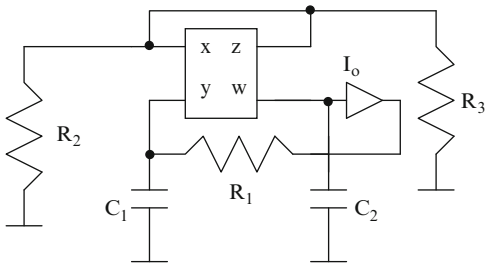


Fig. P.2.39 (Adapted from [2.99] ©IEEE 1999)

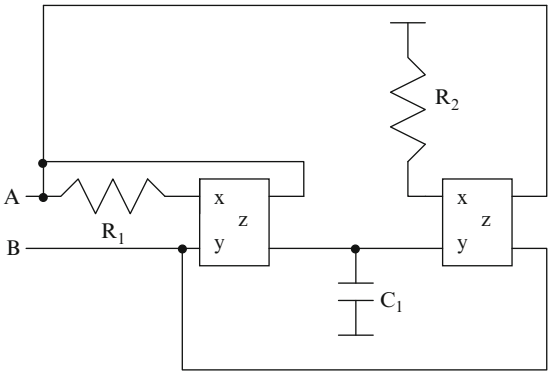


Fig. P.2.40 (Adapted from [2.100] ©IEE 1998)

P.2.35. Analyze the circuit of Fig. P.2.35 [2.97] and derive the condition for oscillations. This uses a first-generation current conveyor denoted as CCI which can be considered as a CCII with another current output that feeds back to the y terminal; that is, $V_x = V_y$, $I_z = I_x$, and $I_y = -I_z$.

P.2.36. A current conveyor CCII can be augmented with a buffer connected to the z terminal y to provide a voltage output at the w terminal. This device is known as CFOA. Derive the transfer function of a finite gain-inverting amplifier using CFOA and evaluate its performance as compared with an opamp-based finite gain-inverting amplifier. Also consider the current mirror pole (between the x and z terminals) in your evaluation (Fig. P.2.36).

P.2.37. Discuss the stability of an integrator using CFOA considering the current mirror pole and other parasitics R_x, R_t, and C_t. Note that x, y, and w correspond to inverting input, noninverting input, and output of the CFOA, respectively.

P.2.38. Derive the expressions for frequency of oscillation and condition for oscillation for the CFOA-based oscillator [2.98] of Fig. P.2.38 by choosing proper impedances for various Z_is.

P.2.39. A FTFN (four-terminal floating nullor) [2.103] is a useful active element. It is described as $V_x = V_y$, $I_x = I_y = 0$, and $I_w = -I_z$. An oscillator using FTFN [2.99] is shown in Fig. P.2.39. Derive expressions for the frequency

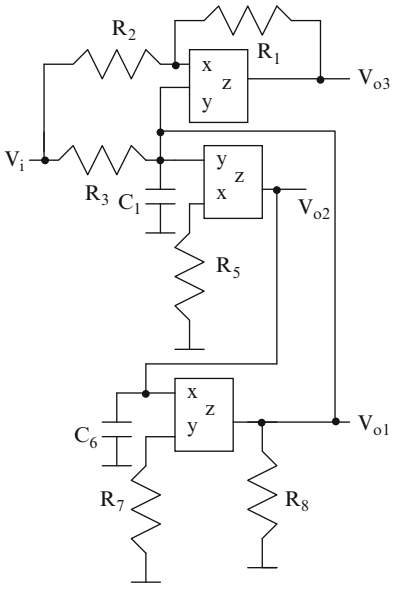


Fig. P.2.41 (Adapted from [2.101] ©IEE 1990)

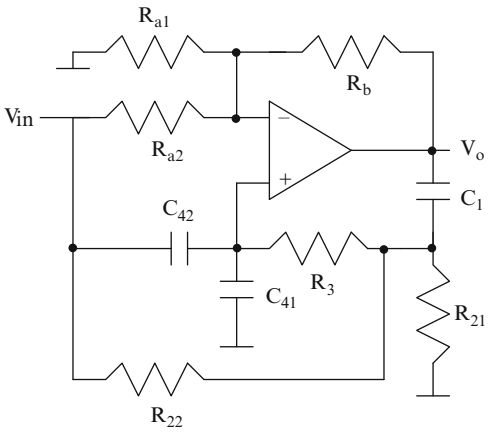


Fig. P.2.42 (Adapted from [2.102] ©IEEE 1980)

of oscillation and condition for oscillation. Analyze the circuit with resistor R_1 connected between the y and z terminals of the FTFN.

P.2.40. Derive the expression for the input impedance of the floating impedance simulator [2.100] of Fig. P.2.40 considering the nonidealities of the current conveyors.

P.2.41. A multifunction biquad using current conveyors due to Singh and Senani [2.101] is presented in Fig. P.2.41. Derive all the transfer functions.

P.2.42. The adjoint concept can be used to derive current mode circuits using current amplifiers. Derive a current-mode biquad from the active RC filter of Fig. P.2.42 due to Sedra, Ghorab, and Martin [2.102] and the Friend–Deliyannis biquad of Fig. 2.11a.

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Chapter 3
OTA-C Filters

In this chapter we consider the design of active filters using operational transconductance amplifiers (OTAs). The symbol of the OTA is presented in Fig. 3.1a. The output current of the OTA can be expressed as

$$I_o = G_m (V_1 - V_2) \tag{3.1}$$

Note that several current outputs may exist, which have the same relationship as that shown in (3.1), but possibly with sign inversion as well, as shown in Fig. 3.1b. The OTA, in practice, has finite frequency-dependent G_m, which is modeled by a single-pole model or a pole-zero or two-pole model [3.1]:

$$\begin{aligned} G_m &= G_{mo} \frac{1}{\left(1 + \frac{s}{\omega_{p1}}\right)}, \; G_m = G_{mo} \frac{\left(1 + \frac{s}{\omega_{z1}}\right)}{\left(1 + \frac{s}{\omega_{p1}}\right)}, \\ G_m &= G_{mo} \frac{1}{\left(1 + \frac{s}{\omega_{p1}}\right)\left(1 + \frac{s}{\omega_{p2}}\right)} \end{aligned} \tag{3.2}$$

where ω_{p1}, ω_{p2}, and ω_{z1} are the first and second poles and zero, respectively, and G_{mo} is the dc transconductance. The OTA also has finite output resistance and capacitance at each output terminal, and input resistance and capacitance at each input terminal as shown in Fig. 3.1c, which needs to be taken into account in the design of filters using OTAs.

It is useful to distinguish between an OTA and a transconductance (G_m). An OTA is basically an operational amplifier (opamp) without a low-impedance output stage (so that it can drive only a small capacitive load as is needed in switched capacitor or OTA-capacitor [OTA-C] filters). It operates with virtually a short at its input (i.e., with minute input signals) and its transconductance value is irrelevant as long as its voltage gain is high. It thus can be treated as a voltage-mode device. On the other hand, a transconductor is a voltage-controlled current source

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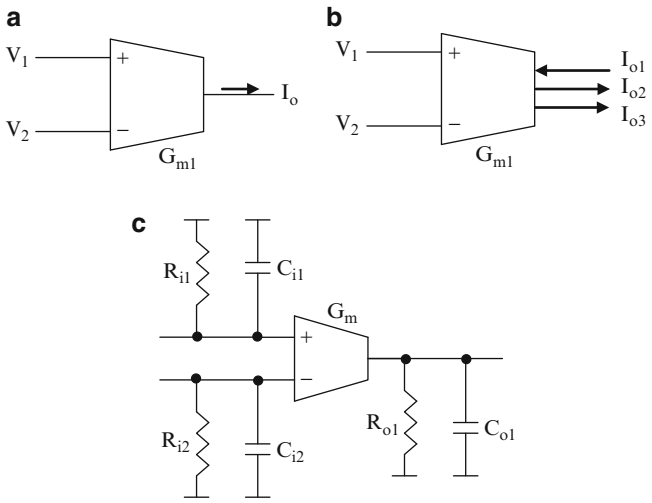


Fig. 3.1 (**a**) Symbol of single current output OTA, (**b**) symbol of multiple current output OTA, and (**c**) nonideal OTA model showing finite input and output impedances

and can handle linearly large input signals and deliver an output current. However, in the literature, the term *OTA-C filter* is used extensively where the authors actually mean G_m-C filter [3.2].

In practice, balanced output devices are used so that fully differential circuits can be built.

3.1 OTA-C Integrators

The basic building block in a G_m−C filter is an integrator shown in Fig. 3.2a. The transfer function of this integrator is given by

$$\frac{V_o}{V_1 - V_2} = \frac{G_m}{sC} \tag{3.3a}$$

The pole-frequency or unity-gain frequency of the integrator is

$$\omega_o = \frac{G_m}{C} \tag{3.3b}$$

An integrator with differential input and differential output is shown in Fig. 3.2b. The output current of this integrator is $I_o = 2\,V_i\,G_m$, which flows through the integrating capacitor C. Thus, the differential output voltage developed is $\dfrac{2\,V_i\,G_m}{sC}$. On the other hand, the circuit of Fig. 3.2c, which needs four times the capacitance of the circuit of Fig. 3.2b, realizes the same transfer function. In addition, the circuit

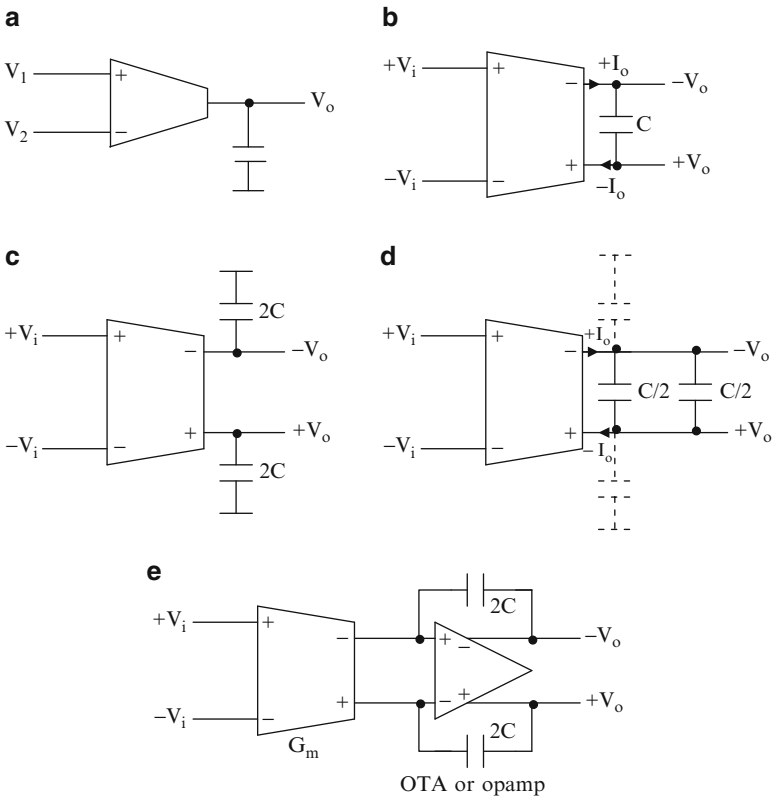


Fig. 3.2 (**a**) Single-ended OTA-C integrator, (**b–d**) fully differential integrators, (**e**) G_m–Opamp integrator (**b-e** Adapted from [3.2] ©1994 IEEE)

of Fig. 3.2c is not affected by the bottom-plate parasitics of the capacitor $2C$, whereas the circuit of Fig. 3.2b is sensitive to bottom-plate parasitics. This sensitivity can be reduced by careful balancing of the parasitics by using two capacitors in place of a single capacitor, as shown in Fig. 3.2d, whereby the bottom-plate parasitics are shown in broken lines.

The parasitic output capacitance of the transconductor can be forced to near zero ground potential by augmenting with an OTA-based integrator as shown in Fig. 3.2e. The advantage is that the transconductor is easier to design since its output swing is very small. Moreover, the transconductor need not have a very high output resistance since the output terminal is at a virtual ground. The integrator *dc* gain is product of *dc* gains of the OTA and transconductor, which is easier to be made large and easier to push the dominant pole frequency to low enough values, avoiding the phase lead it would otherwise produce. It may be noted, however, that the need of both transconductor and OTA in the G_m-OTA-C integrator can mean significant power dissipation, despite that the power dissipation of the individual elements can be low due to relaxed performance requirements.

3.2 First-Order OTA-C Filters

3.2.1 *First-Order OTA-C Filters Using OTAs with Single-Current Output*

As in the case of opamps, several structures are possible that can realize resistances, amplifiers, lossless and lossy integrators, differentiators, and first-order all-pass filters [3.3]. These are considered next.

The circuit of Fig. 3.3a realizes a grounded resistance of value $1/G_{m1}$, whereas the circuit of Fig. 3.3b realizes a floating resistance of value $1/G_m$ when $G_{m1} = G_{m2} = G_m$, thus necessitating matching transconductances. Note that in the case when V_A is a source, the OTA g_{m2} can be removed.

The circuit of Fig. 3.4a realizes an amplifier with gain G_{m1}/G_{m2}. Note that the feedback-connected OTA 2 realizes a resistance of value $1/G_{m2}$ as explained before. Note that the difference of two inputs can be amplified very easily. The circuit of a lossy integrator is presented in Fig. 3.4b. The derivation is quite simple: In Fig. 3.4b, the input difference voltage $(V_1 - V_2)$ is converted into a current $G_m(V_1 - V_2)$ that flows through the capacitor C shunted by a resistor realized using OTA G_{m2}, realizing the transfer function

$$V_o = \frac{G_{m1}\,(V_1 - V_2)}{sC + G_{m2}} \tag{3.4}$$

Note, however, that a differentiator can not be realized easily using an OTA, whereas a lossy differentiator can be realized using the circuit of Fig. 3.4c. This circuit has the transfer function given by

$$\frac{V_o}{V_i} = \frac{sC}{sC + G_{m2}} \tag{3.5}$$

A lossless differentiator [3.4] can be obtained by using an integrator in a feedback system as shown in Fig. 3.4d. This circuit evidently needs more

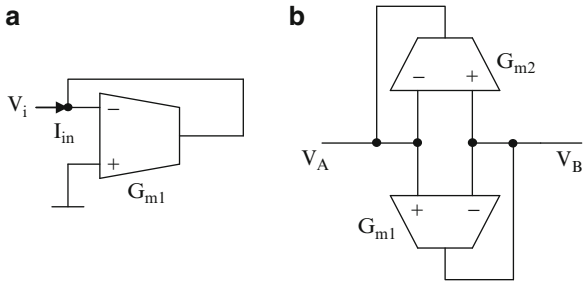


Fig. 3.3 OTA-based realization of grounded resistor (**a**) and floating resistor (**b**)

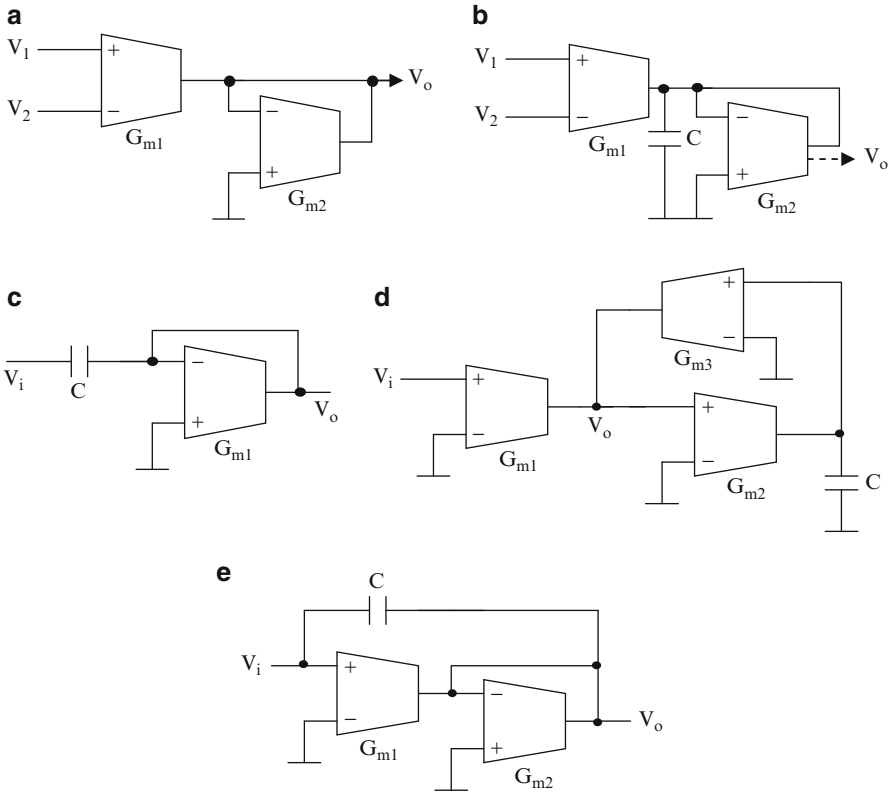


Fig. 3.4 (**a**) OTA-based differential amplifier, (**b**) lossy integrator, (**c**) first-order high-pass filter, (**d**) lossless differentiator based on integrator, and (**e**) filter for realizing finite zeroes ((**c**) Adapted from [3.3] ©IEEE, (**e**) Adapted from [3.3] ©IEEE)

OTAs. In this circuit, G_{m2} and C form a noninverting integrator and G_{m1}, G_{m3} realize the equation:

$$V_i\ G_{m1} + V_o\ \frac{G_{m2}\ G_{m3}}{sC} = 0 \tag{3.6a}$$

so that

$$\frac{V_o}{V_i} = -\frac{G_{m1}\ sC}{G_{m2}\ G_{m3}} \tag{3.6b}$$

The circuit of Fig. 3.4e realizes finite zeroes [3.3] and has the transfer function given by

$$\frac{V_o}{V_i} = \frac{sC + G_{m1}}{sC + G_{m2}} \tag{3.7}$$

Note, however, that it needs a floating capacitor and V_i needs to be a source with low output impedance.

A first-order all-pass filter can be obtained from Fig. 3.4e by interchanging the input terminals of the OTA G_{m1}:

$$\frac{V_o}{V_i} = \frac{sC - G_{m1}}{sC + G_{m2}} \tag{3.8}$$

Matching of OTA transconductances G_{m1} and G_{m2} will evidently be needed.

3.2.2 *First-Order Filters Using OTAs with Current Input and Current Output*

Recently, there has been interest in using OTAs to realize current-mode filters. In these the inputs and outputs are currents. The advantage is that the power supply voltage can be reduced and the desired dynamic range can be obtained in the current outputs. It is very easy to mirror the current outputs of either polarity in multiple output OTAs. For example, the circuit of Fig. 3.4b can use an OTA with two outputs so that a current transfer function can be obtained (as shown by dotted lines), whereas the input is a voltage. On the other hand, by deleting the OTA G_{m1} and feeding an input current as shown in Fig. 3.5a, a current-input current-output lossy integrator can be obtained. A lossy integrator can be obtained using the circuit of Fig. 3.5b.

A general current-input current-output circuit described by Sun and Fidler [3.5] is shown in Fig. 3.5c. This circuit can realize I_{o1} as a first-order low-pass and I_{o2} as a first-order low-pass or high-pass transfer function:

$$I_{o1} = \frac{G_{m1}\left(I_{in1} - I_{in2}\,\frac{G_{m2}}{G_{m3}}\right)}{sC + \frac{G_{m1}\,G_{m2}}{G_{m3}}},\quad I_{o2} = \frac{G_{m2}\,(G_{m1}\,I_{in1} + I_{in2}\,sC)}{G_{m3}\left(sC + \frac{G_{m1}\,G_{m2}}{G_{m3}}\right)} \tag{3.9}$$

Note that R_3 is implemented using an OTA G_{m3} connected as a resistor. Note also that an all-pass transfer function can be realized under the conditions $I_{in1} = -I_{in2}$ and $G_{m2} = G_{m3}$. This circuit uses three OTAs and two extra current outputs and needs matching OTAs and matching input currents.

We consider next another circuit proposed by Wu and El-Masry [3.6], shown in Fig. 3.5d, for which the transfer function can be derived as

$$I_o = \frac{I_{in2}\;G_{m2} + I_{in1}\left(\frac{G_{m2}}{G_{m1}}\right)sC}{sC + G_{m1}} \tag{3.10}$$

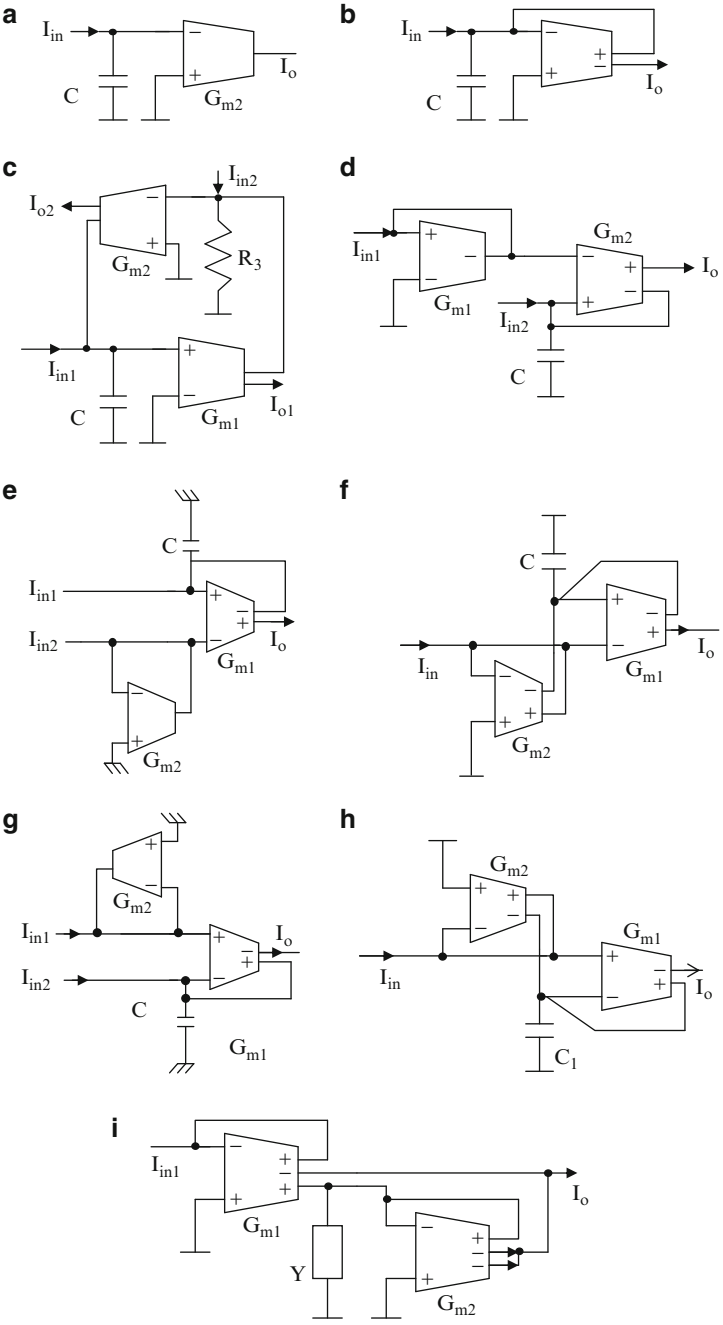


Fig. 3.5 Current-mode circuits using OTAs: (**a**) lossless integrator, (**b**) lossy integrator, (**c**) first-order filter due to Sun and Fidler (Adapted from [3.5] ©IEEE), (**d**) first-order filter due to Wu and El-Masry (Adapted from [3.6] ©IEEE), (**e**, **f**) all-pass filters due to Kamath, Ananda Mohan, and Prabhu with two inputs (Adapted from [3.7] ©Birkhauser), (**g**, **h**) with one input, and (**i**) Al-Hashimi, Dudek, and Moniri first-order all-pass filter (Adapted from [3.8] ©IEE)

Evidently, when $I_{in2} = 0$, a high-pass transfer function is realized, and when $I_{in1} = 0$, a low-pass transfer function is realized. Note, however, that when G_{m1} is negative, that is, when the input OTA is connected as a positive resistor, then an all-pass transfer function is obtained under the condition $G_{m1} = G_{m2}$. Thus, matching of G_ms is needed.

Two alternative first-order all-pass filters [3.7] are presented in Fig. 3.4e, g. For the circuit of Fig. 3.4e, the transfer function realized is

$$I_o = \frac{I_{in1}\ G_{m2} - I_{in2}\ sC}{G_{m2}\left(1 + \frac{sC}{G_{m1}}\right)} \tag{3.11a}$$

Note that when $I_{in1} = 0$, an inverting high-pass transfer function is realized, and when $I_{in2} = 0$, a low-pass transfer function is realized. When $I_{in1} = I_{in2}$ and $G_{m1} = G_{m2}$, a first-order all-pass transfer function is realized. In this case, the circuit can be simplified as shown in Fig. 3.5f. On the other hand, for the circuit of Fig. 3.5g, we have

$$I_o = \frac{I_{in1}\ sC - I_{in2}\ G_{m2}}{G_{m2}\left(1 + \frac{sC}{g_{m1}}\right)} \tag{3.11b}$$

This circuit also can realize an inverting low-pass transfer function when $I_{in1} = 0$, a noninverting high-pass transfer function when $I_{in2} = 0$, and when $I_{in1} = I_{in2}$ and $G_{m1} = G_{m2}$, a first-order all-pass transfer function is realized. In this case too, the circuit can be simplified, as shown in Fig. 3.5h.

We next consider another first-order all-pass configuration due to Al-Hashimi, Dudek, and Moniri [3.8] shown in Fig. 3.5i. The circuit realizes a transfer function given by

$$\frac{I_o}{I_{in}} = \frac{Y - G_{m2}}{Y + G_{m2}} \tag{3.12}$$

where $Y = sC$. Interestingly, the transfer function is independent of G_{m1} value since G_{m1} is used as current mirror with two outputs and the all-pass transfer function is realized as $1 - \dfrac{2\,G_{m2}}{G_{m2} + sC}$.

The multiplier 2 is realized by summing two equal outputs of the OTA G_{m2}.

3.3 Voltage-Mode Second-Order OTA-C Filters

Sanchez-Sinencio, Geiger, and Nevaraz-Lozano [3.9] have described voltage-mode OTA-C filters based on a two-integrator loop. The circuit shown in Fig. 3.6a has the transfer function given by

$$V_{o2} = \frac{1}{D_1(s)}\left(K_1\ K_2\ V_1 + sK_2\ V_2 + B_o\ K_2\ V_3 + s^2\ V_4 + sB_1\ V_5\right) \tag{3.13a}$$

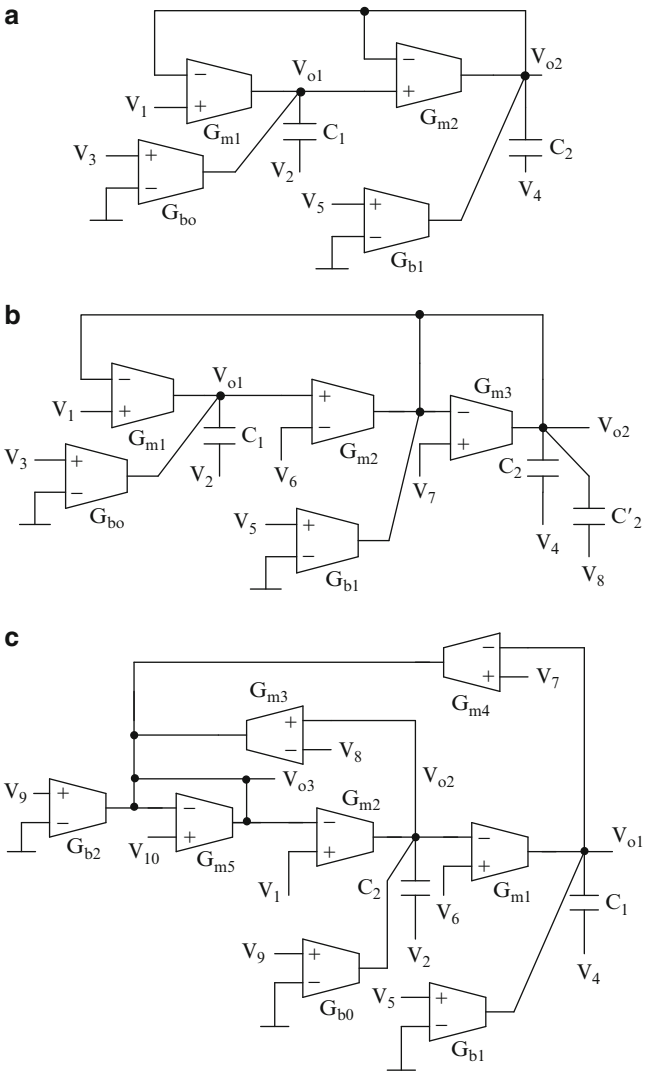


Fig. 3.6 OTA-C filters based on two-integrator loop (**a**)–(**c**) per Sanchez-Sinencio, Geiger, and Nevarez-Lozano (Adapted from [3.9] ©IEEE1988)

where

$$D_1(s) = s^2 + K_2 s + K_1 K_2 \tag{3.13b}$$

and $K_1 = \frac{G_{m1}}{C_1}, K_2 = \frac{G_{m2}}{C_2}, B_0 = \frac{G_{bo}}{C_1}, B_1 = \frac{G_{b1}}{C_2}$.

Evidently, the circuit has low pole frequency and pole-Q sensitivities. All positive gain low-pass, bandpass, and high-pass transfer functions can be realized by feeding only the inputs V_1 or V_3, V_5 or V_2, and V_4, respectively. A notch transfer function can be obtained using both the inputs V_4 and V_3 or V_1 and $V_5 = V_2 = 0$. Independent

control of pole-frequency and pole-Q is not feasible since the damping and integration functions are combined in one integrator using G_{m2} and capacitor C_2.

Another voltage-mode biquad is presented in Fig. 3.6(b). The transfer function of this eight-input circuit is as follows.

$$V_{o2} = \frac{1}{D_1(s)} \begin{pmatrix} K_1\ K_2\ V_1 + sK_2\ V_2 + B_o\ K_2\ V_3 + s^2\ B_2\ V_4 + s\ B_1 V_5 \\ -\ sK_2 V_6 + sA_1\ K_2\ V_7 + s^2\ B_3\ V_8 \end{pmatrix} \quad (3.14a)$$

where

$$D_2(s) = s^2 + A_1\ K_2\, s + K_1\ K_2 \quad (3.14b)$$

and

$$K_1 = \frac{G_{m1}}{C_1}, K_2 = \frac{G_{m2}}{C_2 + C'_2}, B_0 = \frac{G_{bo}}{C_1}, B_1 = \frac{G_{b1}}{C_2 + C'_2}, A_1\ K_2 = \frac{G_{m3}}{C_2 + C'_2},$$
$$B_2 = \frac{C_2}{C_2 + C'_2} \text{ and } B_3 = \frac{C'_2}{C_2 + C'_2}$$

Due to the presence of a negative s term in the numerator, the circuit can realize an all-pass filter also. Note that several options for realizing LP-, BP-, and HP-type transfer functions are available. In this case, A_1K_2 or (OTA G_{m3}) can be used to independently control the pole-Q.

We next consider another biquad shown in Fig. 3.6(c) which uses 10 voltage inputs. The transfer function of this circuit can be derived as

$$V_{o2} = \frac{1}{D_2(s)} \times \begin{pmatrix} +s^2\ V_2 + sK_2\ V_1 + sB_o\ V_3 + sA_o\ K_2\ V_4 + B_1\ A_o\ K_2\ V_5 \\ +K_1\ K_2\ V_6\ A_o + sA_1\ K_2\ V_8 - sA_o\ K_2\ V_7 - sB_2\ K_2\ V_9 - sK_2\ V_{10} \end{pmatrix} \quad (3.15a)$$

where

$$D_2(s) = s^2 + A_1\ K_2\, s + A_o\ K_1\ K_2 \quad (3.15b)$$

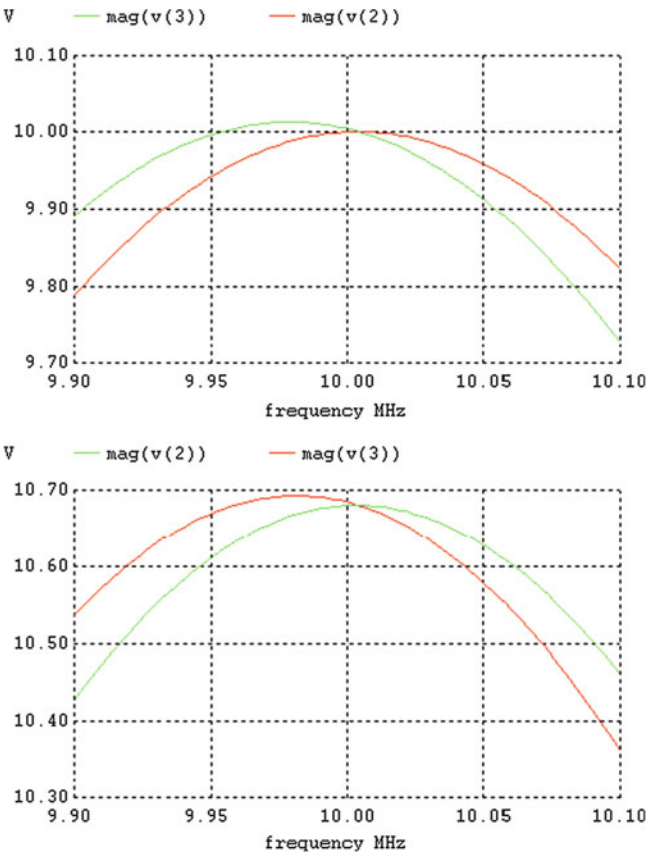
and

$$K_1 = \frac{G_{m1}}{C_1}, K_2 = \frac{G_{m2}}{C_2}, B_0 = \frac{G_{bo}}{C_2}, B_1 = \frac{G_{b1}}{C_1}, B_2 = \frac{G_{b2}}{G_{m5}}, A_o = \frac{G_{m4}}{G_{m5}}, A_1 = \frac{G_{m3}}{G_{m5}}.$$

Note that damping is realized through G_{m3}. Several choices of inputs are feasible to realize the various desired transfer functions. All the above circuits used OTAs with one current output. However, allowing additional current outputs for the OTAs, the hardware can be reduced considerably.

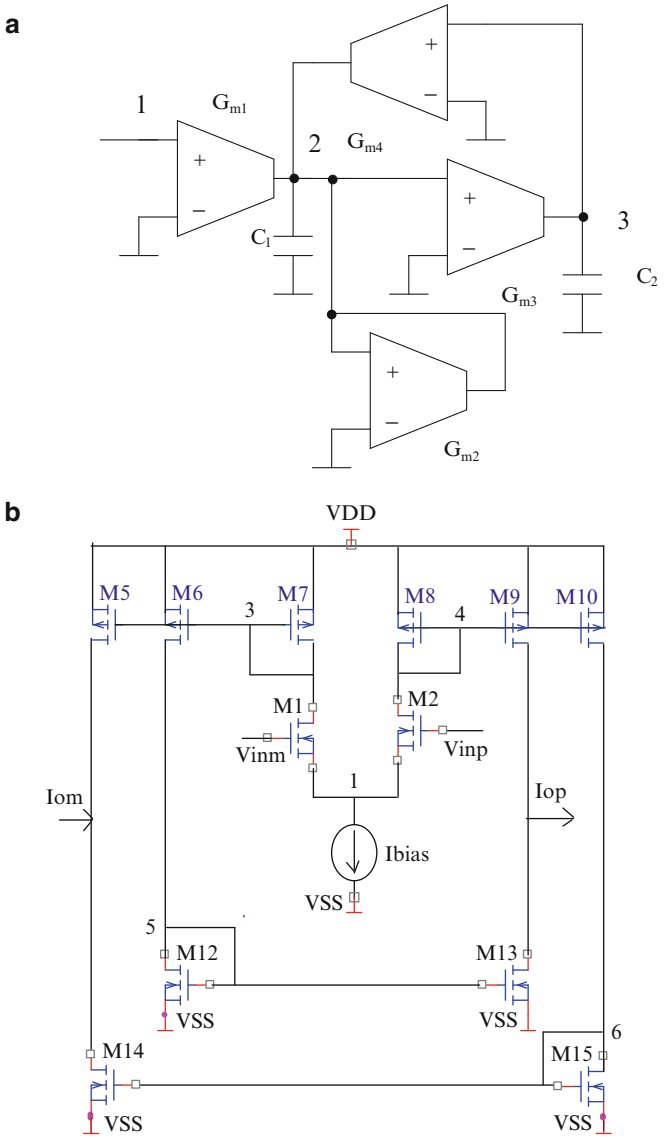
Example 3.1 Using PSPICE, simulate the OTA-C filter of Fig. E.3.1. Study the effect of finite output resistances of the OTAs considering typical output resistance of OTA is 1M Ohms. The effect is that the mid-band gain has increased.

```
*. OTA C two integrator loop
gm1 2 0 1 0 628.57umho
gm3 3 0 0 2 628.57umho
gm4 2 0 3 0 628.57umho
gm2 2 0 0 2 62.857umho
C1 2 0 10pf
C2 3 0 10pf
*R1 2 0 333k
*R2 3 0 1000k
vin 1 0 ac 1v
.ac lin 100 9900K 10100k
Ro1 2 0 1000K
Ro2 3 0 3000K
```



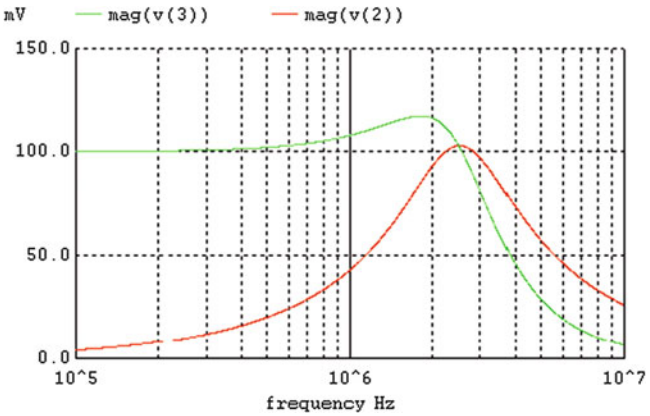
With R_o of 1 Meg Ohm for each OTA.

Example 3.2 Using PSPICE, simulate the OTA-C filter of Fig. E.3.2 using the Tsukutani, Sumi, and Fukui [3.19] CMOS OTA which uses all transistors of the same dimensions (L = 2 um,W = 4 um) and equal cpacitors of value 10 pf (see Fig. E.3.2b) (Adapted from [3.19]© Frequenz2006). The bias currents (100 μA) have been chosen to realize a G_m value (155 μS). Note that the OTA has dual current ouputs.



```
*Two integrator loop using Tsukutani, Sumi and Fukui [3.19] CMOS OTAs
Vin 1 0 ac 0.1v
C1 2 0 10pf
C2 3 0 10pf
x1 vdd vss Ibias1 1 0 2 NC1 doota
Ibias1 Ibias1 vss DC 100u
x2 vdd vss Ibias2 0 2 2 NC2 doota
Ibias2 Ibias2 vss DC 100u
x3 vdd vss Ibias3 0 2 3 NC3 doota
Ibias3 Ibias3 vss DC 100u
x4 vdd vss Ibias4 3 0 2 NC4 doota
Ibias4 Ibias4 vss DC 100u
R1 Nc1 0 100K
R2 NC2 0 100K
R3 NC3 0 100K
R4 NC4 0 100K
vdd vdd 0 DC 2
vss vss 0 DC -2
.AC DEC 1000 100K 10000K
.subckt doota vdd vss Ibias vinp vinm iop iom
.PARAM ln=2um,wn=4um
.PARAM lp=2um, wp=4um
M1 3 vinm Ibias vss CMOSN w={wn} l={ln}
M2 4 vinp Ibias vss CMOSN w={wn} l={ln}
M5 iom 3 vdd vdd CMOSP w={wp} l={lp}
M6 5 3 vdd vdd CMOSP w={wp} l={lp}
M7 3 3 vdd vdd CMOSP w={wp} l={lp}
M8 4 4 vdd vdd CMOSP w={wp} l={lp}
M9 iop 4 vdd vdd CMOSP w={wp} l={lp}
M10 6 4 vdd vdd CMOSP w={wp} l={lp}
M12 5 5 vss vss CMOSN w={wn} l={ln}
M13 iop 5 vss vss CMOSN w={wn} l={ln}
M14 iom 6 vss vss CMOSN w={wn} l={ln}
M15 6 6 vss vss CMOSN w={wn} l={ln}
.ends DOOTA
.MODEL CMOSN NMOS ( LEVEL = 3 PHI=0.700000 TOX=9.6000E-09
+ XJ=0.200000U TPG=1 VTO=0.6684 DELTA=1.0700E+00 LD=4.2030E-08
+ KP=1.7748E-04 UO=493.4 THETA=1.8120E-01 RSH=1.6680E+01
+ GAMMA=0.5382 NSUB=1.1290E+17 NFS=7.1500E+11 VMAX=2.7900E
  +05
+ ETA=1.8690E-02 KAPPA=1.6100E-01 CGDO=4.0920E-10 CGSO= 4.0920E
  -10
+ CGBO=3.7765E-10 CJ=5.9000E-04 MJ=0.76700 CJSW=2.0000E-11
+ MJSW=0.71000 PB=0.990000)
.MODEL CMOSP PMOS ( LEVEL = 3 PHI=0.700000 TOX=9.6000E-09
```

```
+ XJ=0.200000U TPG=-1 VTO=-0.9352 DELTA=1.2380E-02 LD=5.2440E-
  08
+ KP=4.4927E-05 UO=124.9 THETA=5.7490E-02 RSH=1.1660E+00
+ GAMMA=0.4551 NSUB=8.0710E+16 NFS=5.9080E+11 VMAX=2.2960E
  +05
+ ETA=2.1930E-02 KAPPA=9.3660E+00 CGDO=2.1260E-10 CGSO= 2.1260E
  -10
+ CGBO=3.6890E-10 CJ=9.3400E-04 MJ=0.48300 CJSW=2.5100E-10
+ MJSW=0.21200 PB=0.930000)
.end
```



Chang [3.10] has described a voltage-mode biquad shown in Fig. 3.7a using three OTAs, one of which has dual current outputs. The transfer functions of this circuit are:

$$\left(\frac{V_{o1}}{V_i}\right)D(s) = s^2\ C_1\ C_2\, G_{m1} + G_{m1}\ G_{m2}\ G_{m3},$$
$$\left(\frac{V_{o2}}{V_i}\right)D(s) = G_{m1}\ G_{m2}\ G_{m3},\ \left(\frac{V_{o3}}{V_i}\right)D(s) = s\, C_2\, G_{m1}\ G_{m2} \tag{3.16a}$$

where

$$D(s) = s^2\ C_1\ C_2\, G_{m1} + s\, C_2\, G_{m2}\ G_{m3} + G_{m1}\ G_{m2}\ G_{m3} \tag{3.16b}$$

Note that pole-Q can be controlled by G_{m1} independently. A floating inductance can be identified between terminals A and B. The circuit is thus a series resonator formed by $R = 1/G_{m1}$, $L = C_1/(G_{m2}G_{m3})$, and capacitor C_2.

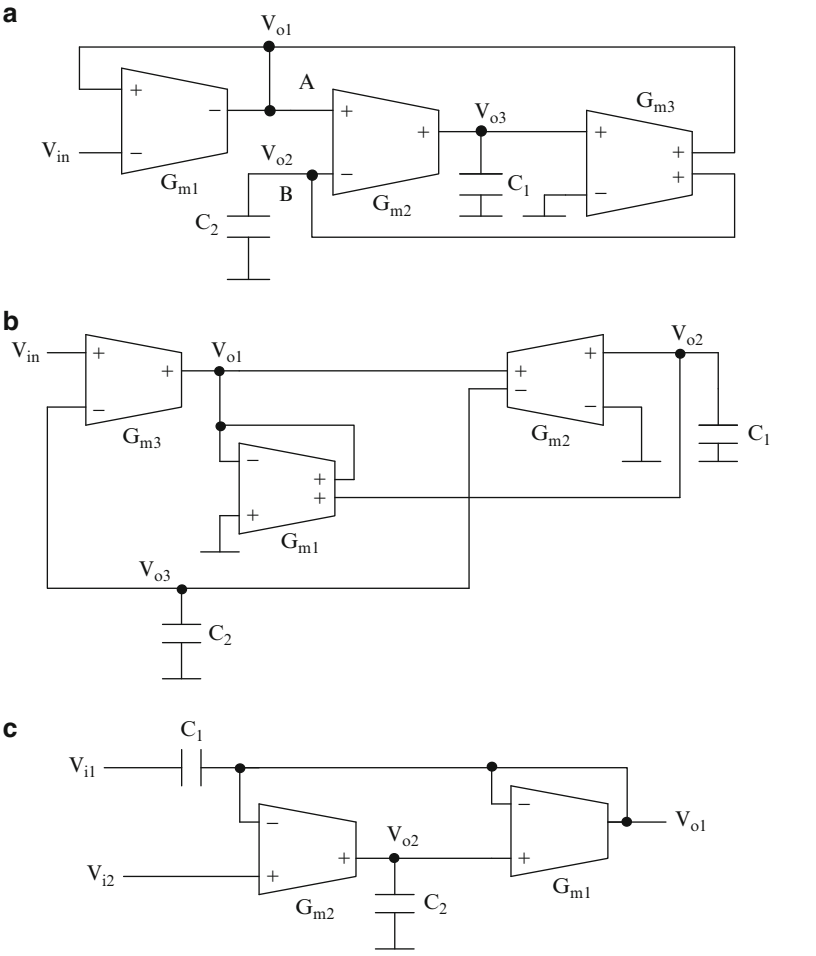


Fig. 3.7 Voltage-mode OTA-C filters due to Chang (Adapted from [3.10] ©IEEE 1999)

Chang [3.10] has described another voltage-mode OTA-C biquad presented in Fig. 3.7b. This circuit realizes LP, BP, and HP transfer functions:

$$\left(\frac{V_{o1}}{V_i}\right)D(s) = s^2\ C_1\ C_2\, G_{m3},$$
$$\left(\frac{V_{o2}}{V_i}\right)D(s) = -sG_{m1}\ G_{m3}\ C_2,\ \left(\frac{V_{o3}}{V_i}\right)D(s) = G_{m1}\ G_{m2}\ G_{m3} \tag{3.17a}$$

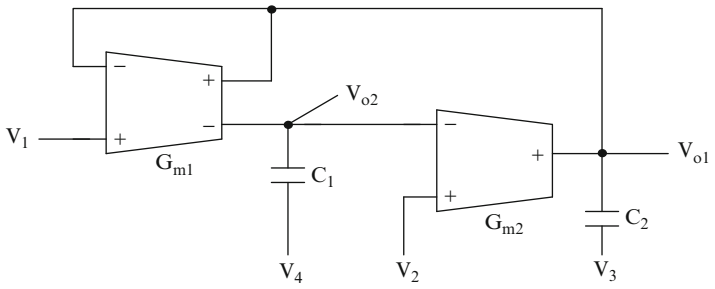


Fig. 3.8 Voltage-mode OTA-C filters due to Horng (Adapted from [3.11]© Taylor and Francis 2004)

where

$$D(s) = s^2\ C_1\ C_2\, G_{m1} + s\, C_2\, G_{m1}\ G_{m2} + G_{m1}\ G_{m2}\ G_{m3} \tag{3.17b}$$

Note that pole-Q cannot be independently controlled. The HP transfer function is realized by subtracting from the input the low-pass ouput signal and adding the inverted band-pass ouput signal.

Another voltage mode biquad due to Chang [3.10] which uses only two OTAs and needs two input voltages is presented in Fig. 3.7c. This circuit can realize notch, HP, BP, and LP transfer functions:

$$V_{o1} = \frac{V_{i2}\, G_{m1}\ G_{m2} + V_{i1}\, s^2\ C_1\ C_2}{s^2\ C_1\ C_2 + s\, C_2\, G_{m1} + G_{m1}\ G_{m2}} \tag{3.18a}$$

and

$$V_{o2} = \frac{-V_{i1}\, s\, C_1\ G_{m2} + V_{i2}(s\, C_1\ G_{m2} + G_{m1}\ G_{m2})}{s^2\ C_1\ C_2 + s\, C_2\, G_{m1} + G_{m1}\ G_{m2}} \tag{3.18b}$$

A unilateral floating inductance exists between terminals V_{i2} and V_{o1} and a resistor exists between V_{o1} and ground.

A voltage mode circuit due to Horng [3.11] is presented in Fig. 3.8. This circuit has two voltage transfer functions:

$$V_{01} = \frac{s^2\ C_1\ C_2\ V_3 + s\, C_1\,(G_{m1}\ V_1 + G_{m2}\ V_2 - G_{m2}\ V_4) + G_{m1}\ G_{m2}\ V_1}{s^2\ C_1\ C_2 + s\, C_1\ G_{m1} + G_{m1}\ G_{m2}} \tag{3.19a}$$

$$V_{02} = \frac{s^2\ C_1\ C_2\ V_4 + s\, G_{m1}\,(C_1\ V_4 + C_2\ V_3 - C_2\ V_1) + G_{m1}\ G_{m2}\ V_2}{s^2\ C_1\ C_2 + s\, C_1\ G_{m1} + G_{m1}\ G_{m2}} \tag{3.19b}$$

It can be seen from (3.19) that various voltage transfer functions can be obtained at V_{o1} or V_{o2}. The circuit is basically a two-integrator loop. Since the damping

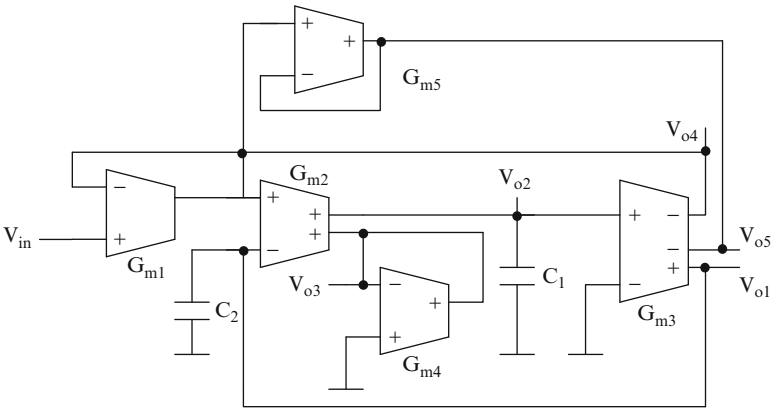


Fig. 3.9 Voltage-mode OTA-C filters due to Horng with single input (Adapted from [3.12] ©Taylor & Francis 2002)

resistor is used as a part of the second integrator, there is no degree of freedom to control the pole-Q independent of frequency. This may be observed from the denominator of (3.19), since G_{ml} affects both pole-Q and pole-frequency.

Another voltage mode circuit due to Horng [3.12] is presented in Fig. 3.9. This circuit realizes the five transfer functions given below:

$$\begin{aligned}
&\frac{V_{o1}}{V_{in}} = \frac{G_{m1}\ G_{m2}\ G_{m3}}{D(s)}, \frac{V_{o2}}{V_{in}} = \frac{s\,C_2\ G_{m1}\ G_{m2}}{D(s)},\\
&\frac{V_{o3}}{V_{in}} = \frac{s^2\ C_1\ C_2\ G_{m1}\ \frac{G_{m2}}{G_{m4}}}{D(s)}, \frac{V_{o4}}{V_{in}} = \frac{s^2\ C_1\ C_2\ G_{m1} + G_{m1}\ G_{m2}\ G_{m3}}{D(s)},\\
&\frac{V_{o5}}{V_{in}} = \frac{s^2\ C_1\ C_2\ G_{m1} - s\,C_{m2}\ G_{m2}\ G_{m3}\ \frac{G_{m1}}{G_{m5}} + G_{m1}\ G_{m2}\ G_{m3}}{D(s)}
\end{aligned} \tag{3.20a}$$

where

$$D(s) = s^2\ C_1\ C_2\ G_{m1} + s\,C_2\ G_{m2}\ G_{m3} + G_{m1}\ G_{m2}\ G_{m3} \tag{3.20b}$$

Note that this circuit is basically same as Chang's biquad of Fig. 3.7a except that the polarity of the output terminals of OTA G_{m3} and input terminals of OTA G_{m1} are changed. The additional OTA G_{m5} is used to realize the notch transfer function and a high-pass transfer function is obtained using G_{m4} to convert the mirrored output current of G_{m2} to a voltage V_{o3}.

Chang [3.13] has described a voltage-mode universal OTA-C filter using multiple-output OTAs presented in Fig. 3.10. The transfer function of this biquad is given by

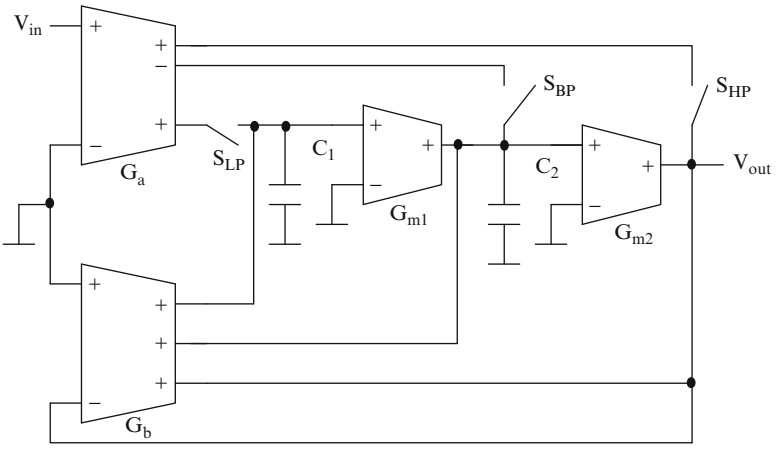


Fig. 3.10 Voltage-mode universal OTA-C filter due to Chang (Adapted from [3.13]©IEEE 2006)

$$\frac{V_o}{V_{in}} = \left(\frac{G_{ma}}{G_{mb}}\right) \frac{S_{HP}\ s^2\ C_1\ C_2 - S_{BP}\ s C_1\ G_{m2} + S_{LP}\ G_{m1}\ G_{m2}}{s^2\ C_1\ C_2 + s C_1\ G_{m2} + G_{m1}\ G_{m2}} \tag{3.21}$$

Note that S_{HP}, S_{LP}, and S_{BP} are switches that when selected appropriately will realize the numerator coefficients of all generally required second-order transfer functions. Note that the feedback is through multiple-output OTA G_b whereas the feedforward is through OTA G_a. This configuration can be used to realize a high-order transfer function as shown later. Chang [3.13] has also observed that the circuit can be designed with fixed capacitors and different G_ms or fixed G_ms and different capacitors.

Sun [3.14] has described two general OTA-C voltage-mode biquads based on the Nawrocki and Klein biquad [3.15] shown in Fig. 3.11a, b. Note that in the original biquad of Nawrocki and Klein [3.15], the input terminals V_{i4}, V_{i7}, and V_{i8} in Fig. 3.11a were connected to ground. The modified circuit of Fig. 3.11a [3.14] uses additional input OTAs whereas the circuit of Fig. 3.11b uses additional output OTAs and is also fed input current. Both are based on the two-integrator loop and use grounded capacitors. The transfer functions of the circuit of Fig. 3.11a are:

$$\begin{aligned} D(s)\,V_{o1} = {} & G_{mao}\,(G_{mb2}\ C_2\,s + G_{m2}\ G_{mb1})\,V_{i1} - G_{ma1}\ G_{mb0}\ G_{m2}\ V_{i2} \\ & - G_{ma2}\ G_{mb0}\ C_2\,s\,V_{i3} + G_{mbo}\,(G_{mb2}\ C_2\,s + G_{m2}\ G_{mb1})\,V_{i4} \\ & - G_{mbo}\ V_{i5}\ G_{mb1}\ G_{m2} - G_{mbo}\,s\,V_{i6}\ G_{mb2}\ C_2 \setminus \\ & + G_{mbo}\ G_{m1}\ G_{m2}\ V_{i7} + G_{mbo}\ G_{m2}\ C_2\,s\,V_{i8} \end{aligned} \tag{3.22a}$$

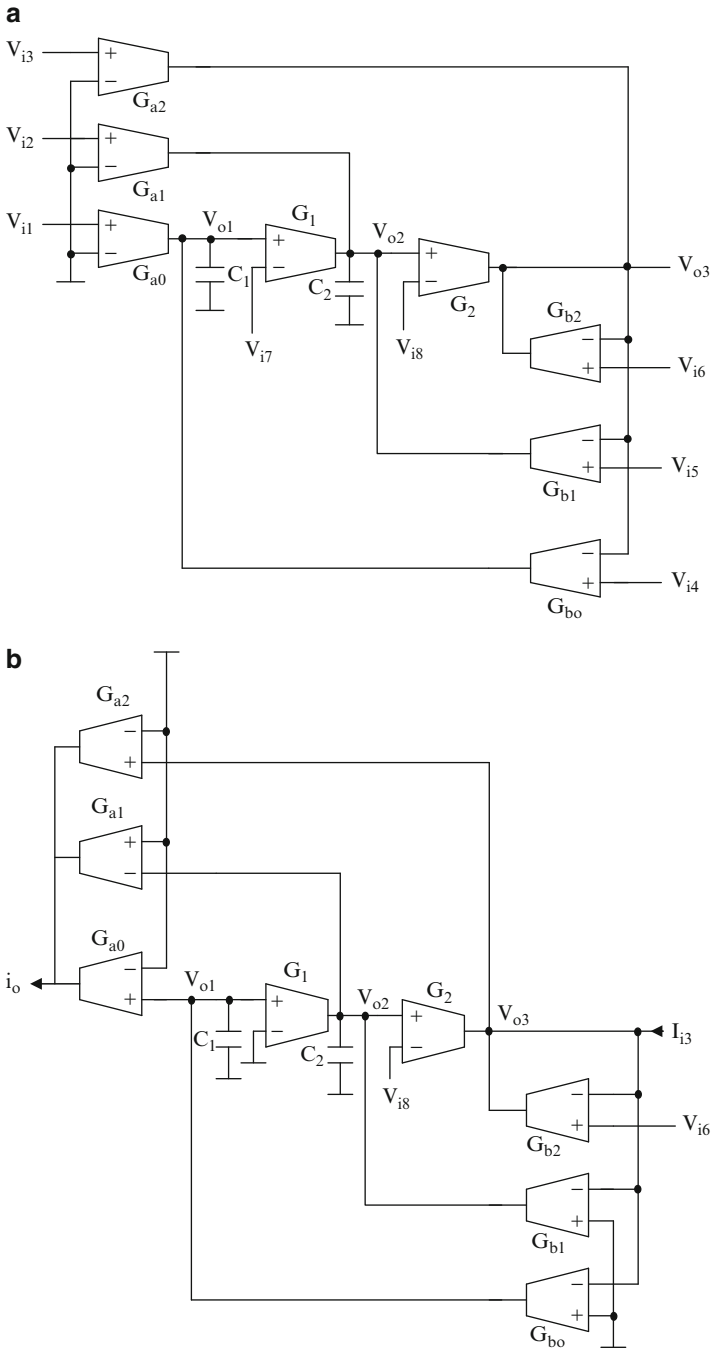


Fig. 3.11 Modified OTA-C biquads due to Sun based on the Nawrocki and Klein OTA-C biquad: (**a**) with input distribution and (**b**) with output summation (Adapted from [3.14] ©IEE 1998)

$$D(s)\,V_{o2} = G_{ao}\,G_{b2}\,G_1\,V_{i1} + G_{a1}\,G_{b2}\,C_1\,s\,V_{i2} - G_{a2}\,(G_{b1}\,C_1\,s + G_1\,G_{bo})\,V_{i3} + G_{bo}\,V_{i4}\,G_{b2}\,G_1 + G_{b1}\,s\,G_{b2}\,C_1\,V_{i5} - G_{b2}\,(G_{b1}\,C_1\,s + G_1\,G_{bo})\,V_{i6} - G_{b2}\,G_1\,C_1\,s\,V_{i7} + G_2\,(s\,G_{b1}\,C_1 + G_1\,G_{bo})\,V_{i8} \tag{3.22b}$$

$$D(s)\,V_{o3} = G_{ao}\,G_1\,G_2\,V_{i1} + G_{a1}\,G_2\,C_1\,s\,V_{i2} + G_{a2}\,C_1\,C_2\,s^2\,V_{i3} + G_{bo}\,G_1\,G_2\,V_{i4} + G_{b1}\,G_2\,C_1\,s\,V_{i5} + G_{b2}\,V_{i6}\,C_1\,C_2\,s^2 - G_1\,G_2\,C_1\,s\,V_{i7} - G_2\,C_1\,C_2\,s^2\,V_{i8} \tag{3.22c}$$

where

$$D(s) = G_{b2}\,C_1\,C_2\,s^2 + G_{b1}\,G_2\,C_1\,s + G_{bo}\,G_1\,G_2 \tag{3.22d}$$

Note that the circuit of Fig. 3.11a can realize LP, BP, and HP transfer functions directly by appropriate choice of inputs. The output V_{o3} realizes for V_{i1} to V_{i8} respectively LP, BP, HP, LP, BP, HP, BP, and HP transfer functions. The circuit can be reduced to a five-OTA circuit by tying certain voltage inputs together. As an illustration, for $V_{i4} = V_{i6} = V_i$, the circuit realizes LP, BP, and BS transfer functions. Similarly, for the case $V_{i4} = -V_{i5} = V_{i6} = V_{in}$, V_{o3} is an all-pass transfer function whereas V_{o1} and V_{o2} are LP and BP transfer functions, respectively.

The circuit of Fig. 3.11b realizes current transfer functions given as

$$I_o = \frac{(-V_{i8}\,G_{m2} + V_{i6}\,G_{mb2} + i_{i3})(G_{a2}\,C_1\,C_2\,s^2 + (G_{a1}\,G_{b1}\,C_1 - G_{ao}\,G_{bo}\,C_2)s + G_{a1}\,G_{bo}\,G_1)}{G_{b2}\,C_1\,C_2\,s^2 + G_{b1}\,G_2\,C_1\,s + G_{bo}\,G_1\,G_2} \tag{3.23}$$

Thus arbitrary biquadratic transfer functions can be obtained.

3.4 Current-Mode Second-Order OTA-C Filters

We next consider some current-mode biquads described in the literature. The current-mode universal biquad due to Al-Hashimi, Dudek, Moniri, and Living [3.16] is shown in Fig. 3.12a which is also based on a two-integrator-loop. The pole-frequency and pole-Q can be independently controlled. The realized current transfer function is given by

$$\frac{I_{out}}{I_{in}} = \frac{s^2\,S_1 \pm S_2\left(\frac{s\,G_{m2}}{C_1}\right) + (S_3 + S_4)\,\frac{G_{m2}\,G_{m3}}{C_1\,C_2}}{\frac{s^2}{R\,G_{m1}} + s\left(\frac{G_{m2}}{C_1}\right) + \frac{G_{m1}\,G_{m2}}{C_1\,C_2}} \tag{3.24}$$

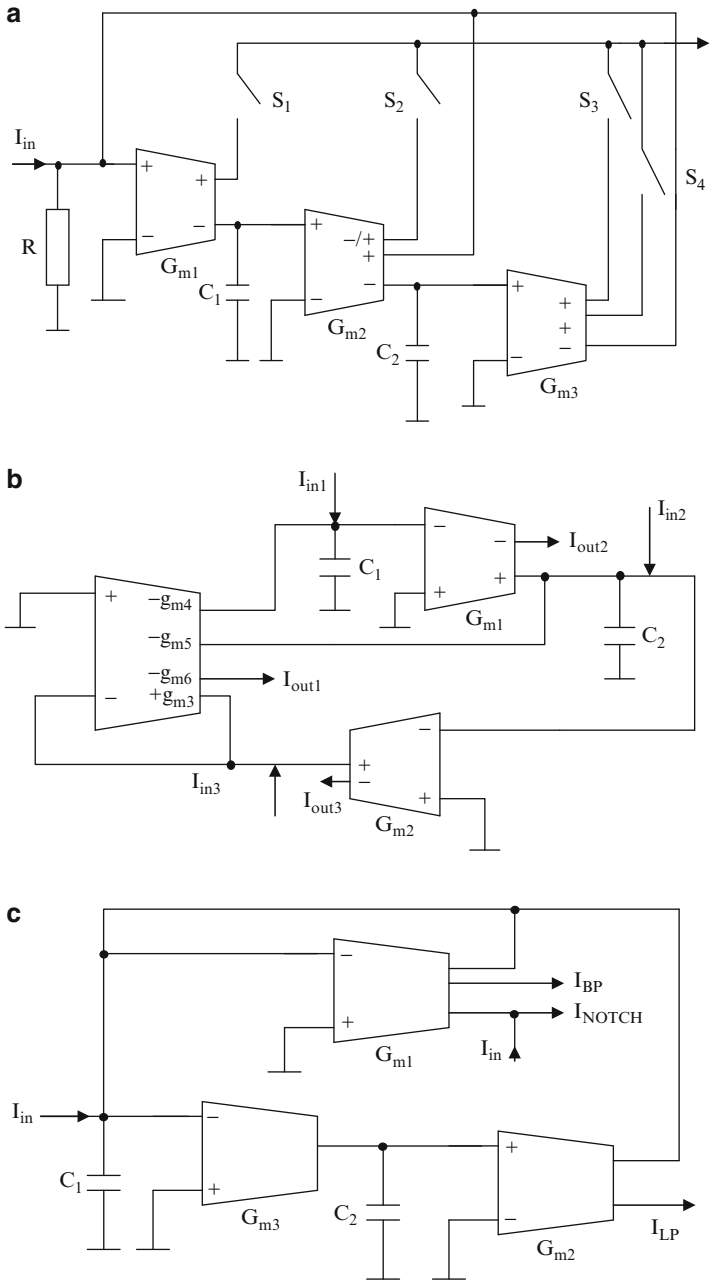


Fig. 3.12 Current-mode OTA-C biquads (**a**) due to Al-Hashimi, Dudek, Moniri, and Living (Adapted from [3.16]©IEE1998), (**b**) due to Abuelmaatti and Bentrcia (Adapted from [3.17] ©IEE 2004), and (**c**) due to Chang, Al-Hashimi, and Ross (Adapted from [3.18]©IET 2004)

Note that a low-pass transfer function of gain 1 or 2 can be realized by closing either one or both of the switches S_3 and S_4. All generally required transfer functions can be realized by an appropriate choice of switches S_1, S_2, S_3, and S_4. Note that R needs to be realized by another OTA simulating a resistor.

Abu elmaa'tti and Bentrcia [3.17] have suggested a current mode biquad configuration shown in Fig. 3.12b which is also based on a two-integrator loop. The three current transfer functions realized are as follows.

$$I_{out1} = \frac{1}{D}\frac{G_{m6}}{G_{m3}}\left(s^2\ C_1\ C_2\ I_{in3} - s\,C_1\ G_{m2}\ I_{in2} + G_{m1}\ G_{m2}\ I_{in1}\right) \tag{3.25a}$$

$$I_{out2} = -\frac{1}{D}\frac{G_{m1}}{G_{m3}}\left(\left(s(C_2\ G_{m3} + G_{m2}\ G_{m5})\,I_{in1} - s\,C_2\ G_{m4}\ I_{in3} + G_{m2}\ G_{m4}\ I_{in2}\right)\right) \tag{3.25b}$$

$$I_{out3} = \frac{1}{D}\left((G_{m1}\ G_{m2}\ I_{in1} - s\,C_1\ G_{m2}\ I_{in2} - \frac{1}{G_{m3}}(G_{m1}\ G_{m2}\ G_{m4} + s\,C_1\ G_{m2}\ G_{m5})\,I_{in3}\right) \tag{3.25c}$$

where

$$D = \frac{g_{m1}\ g_{m2}\ g_{m4}}{g_{m3}} + s\,C_1\ \frac{g_{m2}\ g_{m5}}{g_{m3}} + s^2\ C_1\ C_2 \tag{3.25d}$$

Note that the pole-Q can be controlled independently by G_{m5}. Note that even though different current terminals are labeled by different G_{mi} values, the G_m is same.

Chang, Al-Hashimi, and Ross [3.18] have proposed a current-mode OTA-C filter shown in Fig. 3.12c. This is also based on the two-integrator loop. It can realize low-pass, notch, and band-pass transfer functions. A high-pass transfer function can be obtained by joining NH and LP terminals. An all-pass transfer function can be obtained by joining BP and NH terminals. The circuit has independent control of pole-Q and pole-frequency. The transfer functions of this circuit are:

$$\begin{aligned}
&\left(\frac{I_{BP}}{I_{in}}\right)D(s) = -s\,C_2\ G_1,\ \frac{I_{Notch}}{I_{in}} = s^2\ C_1\ C_2 + G_2\ G_3,\\
&\left(\frac{I_{LP}}{I_{in}}\right)D(s) = -\,G_2\ G_3,\ \left(\frac{I_{AP}}{I_{in}}\right)D(s) = s^2\ C_1\ C_2 - s\,C_2\ G_1 + G_2\ G_3,\\
&\left(\frac{I_{HP}}{I_{in}}\right)D(s) = s^2\ C_1\ C_2
\end{aligned} \tag{3.26a}$$

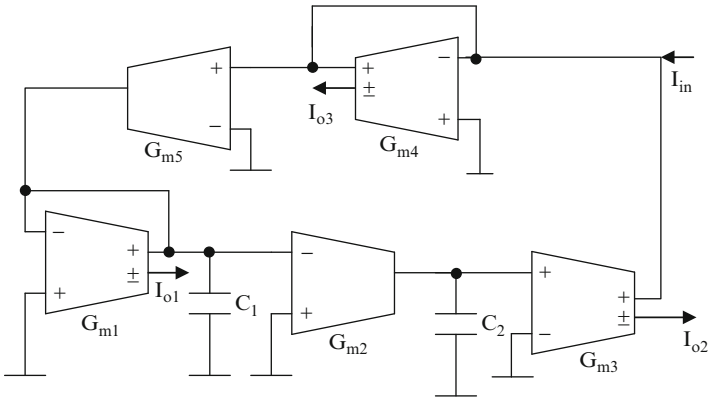


Fig. 3.13 Current-mode OTA-C biquad due to Tsukutani, Sumi, and Fukui (Adapted from [3.19] ©Frequenz 2006)

where

$$D(s) = s^2\ C_1\ C_2 + sC_2\ G_1 + G_2\ G_3 \tag{3.26b}$$

Tsukutani, Sumi, and Fukui [3.19] have described an OTA-C filter based on a two-integrator loop, which is presented in Fig. 3.13. In this circuit, a current multiplier has been used in the feedback formed by OTAs G_{m4} and G_{m5}. The transfer functions of this circuit are:

$$\begin{aligned} &\left(\frac{I_{o1}}{I_{in}}\right)D(s) = \pm\frac{G_{m1}\ G_{m5}}{C_1\ G_{m4}}s,\ \left(\frac{I_{o2}}{I_{in}}\right)D(s) = \pm\frac{G_{m2}\ G_{m3}\ G_{m5}}{C_1\ C_2\ G_{m4}}, \\ &\frac{I_{o3}}{I_{in}}D(s) = \pm s\left(s + \frac{G_{m1}}{C_1}\right) \end{aligned} \tag{3.27a}$$

where

$$D(s) = s^2 + s\frac{g_{m1}}{C_1} + \frac{g_{m2}\ g_{m3}\ g_{m5}}{C_1\ C_2\ g_{m4}} \tag{3.27b}$$

Note that although (3.27a) realizes band-pass and low-pass current transfer functions, the high-pass, all-pass, and notch transfer functions are obtained as (a) $I_{HP} = I_{o1} - I_{o3}$, $G_{m5} = G_{m4}$, (b) $I_{BS} = I_{o1} + I_{o2} - I_{o3}$ under the condition $G_{m5} = G_{m4}$ and (c) $I_{AP} = I_{o1} + I_{o2} - I_{o3}$ under the condition $G_{m5} = 2G_{m4}$.

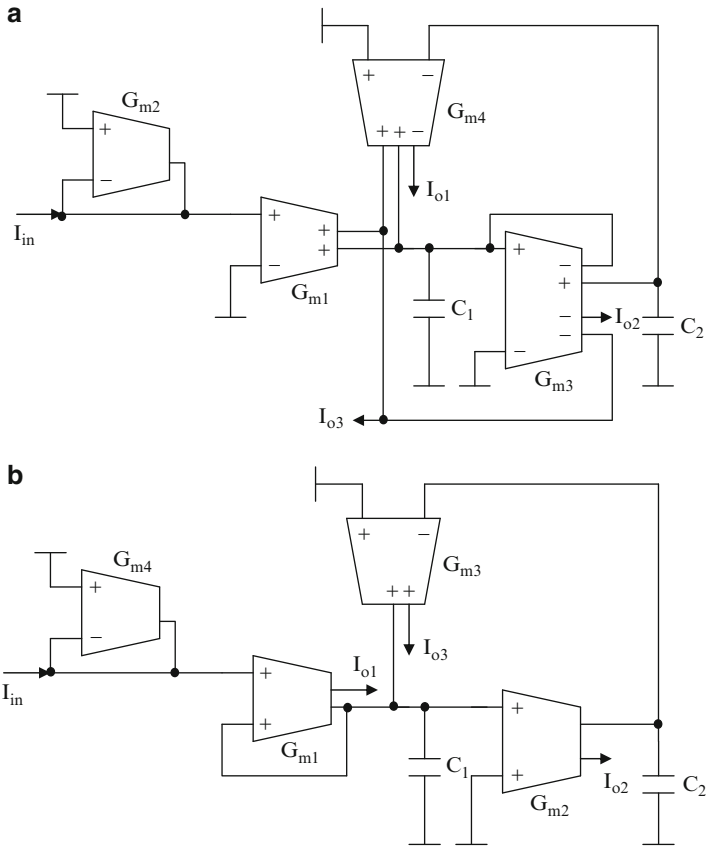


Fig. 3.14 Current-mode OTA-C biquads due to Bhaskar, Singh, Sharma, and Senani (Adapted from [3.20] ©IEICE 2005)

Bhaskar, Singh, Sharma, and Senani [3.20] have proposed two universal filter realizations using OTAs. These are presented in Fig. 3.14a, b. In the circuit of Fig. 3.14a, OTA G_{m2} converts the input current to voltage which is again converted into two currents by OTA G_{m1}. Note that G_{m3}, G_{m4}, and capacitor C_2 realize a grounded inductance, with which capacitor C_1 forms a LC tank circuit. However, damping is provided by G_{m3} thus not letting independent control of pole-frequency and pole-Q. Note that LP, HP, and BP transfer functions are realized. The transfer functions of the circuit of Fig. 3.14a are as follows.

$$\frac{I_{o1}}{I_{in}} = \left(\frac{G_{m1}}{G_{m2}}\right)\left(\frac{\frac{G_{m3}\,G_{m4}}{C_1\,C_2}}{D(s)}\right),\quad \frac{I_{o2}}{I_{in}} = -\left(\frac{G_{m1}}{G_{m2}}\right)\left(\frac{s\left(\frac{G_{m3}}{C_1}\right)}{D(s)}\right),$$
$$\frac{I_{o3}}{I_{in}} = \left(\frac{G_{m1}}{G_{m2}}\right)\left(\frac{s^2}{D(s)}\right) \tag{3.28a}$$

where

$$D(s) = s^2 + s\left(\frac{G_{m3}}{C_1}\right) + \frac{G_{m3}\ G_{m4}}{C_1\ C_2} \tag{3.28b}$$

Consider next the circuit of Fig. 3.14b whose transfer functions can be derived as follows.

$$\begin{aligned} &\frac{I_{o3}}{I_{in}} = -\left(\frac{G_{m1}}{G_{m4}}\right)\left(\frac{\frac{G_{m2}\ G_{m3}}{C_1\ C_2}}{D(s)}\right),\ \frac{I_{o2}}{I_{in}} = \left(\frac{G_{m1}}{G_{m4}}\right)\left(\frac{s\left(\frac{G_{m2}}{C_1}\right)}{D(s)}\right), \\ &\frac{I_{o1}}{I_{in}} = \left(\frac{G_{m1}}{G_{m4}}\right)\left(\frac{s^2 + \frac{G_{m2}\ G_{m3}}{C_1\ C_2}}{D(s)}\right) \end{aligned} \tag{3.29a}$$

where

$$D(s) = s^2 + s\left(\frac{G_{m1}}{C_1}\right) + \frac{G_{m2}\ G_{m3}}{C_1\ C_2} \tag{3.29b}$$

In this circuit, OTA G_{m4} converts the input current to voltage. The OTA G_{m1} acts as a source resistance feeding the tank circuit formed by capacitor C_1 and lossless grounded inductance realized by OTAs G_{m3}, G_{m4}, and capacitor C_2. The OTA G_{m1} converts the difference between input voltage and the voltage across the LC tank (a band-pass transfer function) to current output yielding a notch transfer function.

Chunhua, Ling, and Tao [3.21] have suggested a universal filter configuration presented in Fig. 3.15 using four OTAs. The various transfer functions of this circuit can be derived as

$$\begin{aligned} &\left(\frac{I_{o1}}{I_{in}}\right)D(s) = \left(\frac{G_b}{G_a}\right)s^2\ C_1\ C_2, \\ &\left(\frac{I_{o2}}{I_{in}}\right)D(s) = \left(\frac{G_b}{G_a}\right)s\,C_2\ G_{m1}, \\ &\left(\frac{I_{o3}}{I_{in}}\right)D(s) = G_{m1}\ G_{m2}\left(\frac{G_b}{G_a}\right), \\ &\left(\frac{I_{o4}}{I_{in}}\right)D(s) = \left(\frac{G_b}{G_a}\right)s^2\ C_1\ C_2 + G_{m1}\ G_{m2}, \\ &\left(\frac{I_{o5}}{I_{in}}\right)D(s) = \left(\frac{G_b}{G_a}\right)\left(s^2\ C_1\ C_2 - s\,C_2\ G_{m1} + G_{m1}\ G_{m2}\right) \end{aligned} \tag{3.30a}$$

where

$$D(s) = s^2\ C_1\ C_2 + s\,C_2\ G_{m1}\left(\frac{G_b}{G_a}\right) + G_{m1}\ G_{m2} \tag{3.30b}$$

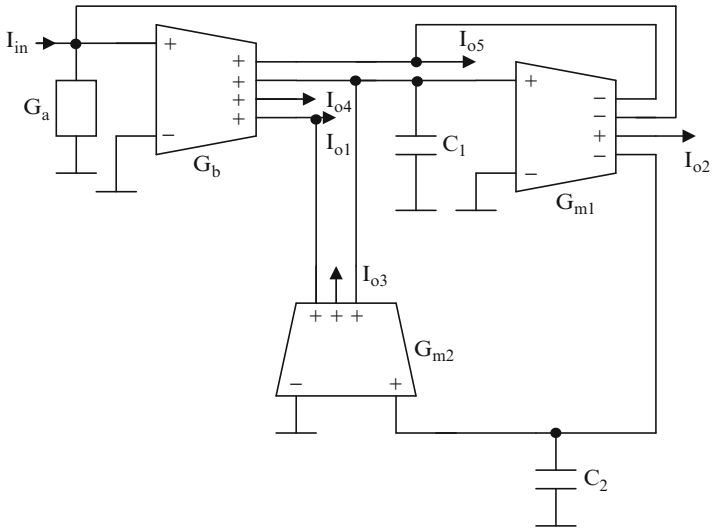


Fig. 3.15 Current mode OTA-C biquad due to Chunhua, Ling, and Tao (Adapted from [3.21] ©AEU 2008)

Evidently, the circuit has independent control of pole-Q using (G_b/G_a). This circuit (also based on a two-integrator loop) evidently needs OTAs with several current outputs.

Biolek, Biolkova, and Kolka [3.22] have described a current-mode OTA-C biquad based on KHN active RC biquad which is presented in Fig. 3.16. Note that the circuit needs two input currents. The transfer functions of this circuit are given as

$$\frac{I_{HP}}{I_{in}} = \frac{s^2}{\Delta},\ \frac{I_{BP}}{I_{in}} = \frac{s\,\omega_p / Q_p}{\Delta},\ \frac{I_{LP}}{I_{in}} = \frac{\omega_p^2}{\Delta} \tag{3.31a}$$

where

$$\Delta = s^2 + s\left(\frac{G_{m1}}{C_1}\right) + \frac{G_{m1}\ G_{m2}}{C_1\ C_2} \tag{3.31b}$$

Note that the circuit realizes basic low-pass and bandpass current transfer functions from which others are obtained as

$$\begin{aligned} &\frac{I_{HP}}{I_{in}} = \frac{s^2}{\Delta} = \frac{I_{in} - I_{LP} - I_{BP}}{I_{in}},\ \frac{I_{BR}}{I_{in}} = \frac{s^2 + \frac{G_{m1}\ G_{m2}}{C_1\ C_2}}{\Delta} = \frac{I_{in} - I_{BP}}{I_{in}}, \\ &\frac{I_{BP}}{I_{in}} = \frac{s\left(\frac{G_{m1}}{C_1}\right)}{\Delta},\ \frac{I_{AP}}{I_{in}} = \frac{s^2 - s\left(\frac{G_{m1}}{C_1}\right) + \frac{G_{m1}\ G_{m2}}{C_1\ C_2}}{\Delta} = \frac{I_{in} - 2I_{BP}}{I_{in}},\ \frac{I_{LP}}{I_{in}} = \frac{\frac{G_{m1}\ G_{m2}}{C_1\ C_2}}{\Delta} \end{aligned} \tag{3.32}$$

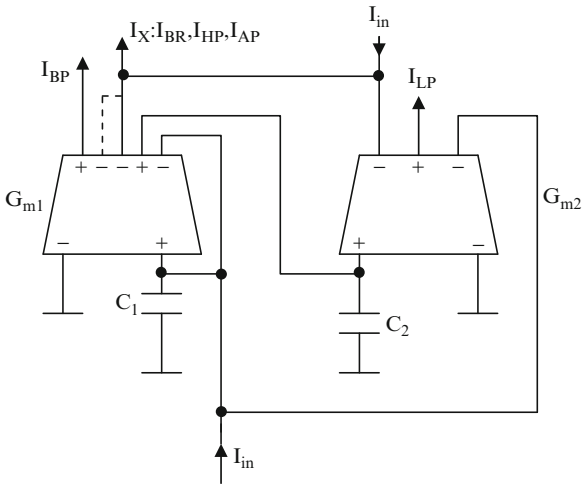


Fig. 3.16 Current-mode OTA-C biquad due to Biolek, Biolkova, and Kolka (Adapted from [3.22] ©WASET2007)

Chang [3.10] has proposed two current-mode biquads shown in Fig. 3.17a, b whose transfer functions are given, respectively, by

$$\begin{aligned}\left(\frac{I_{out}}{I_{in}}\right)D(s) &= s^2\ C_1\ C_2\ I_3 - sC_1\ G_2\ I_2 + G_1\ G_2\ I_1,\\ \left(\frac{I_{o1}}{I_{in}}\right)D(s) &= sC_2\ G_1\ I_1 + G_1\ G_2\ I_2,\\ \left(\frac{I_{o2}}{I_{in}}\right)D(s) &= -sC_1\ G_2\ I_2 + G_1\ G_2\ I_1 - G_1\ G_2\ I_2\end{aligned} \tag{3.33a}$$

where

$$D(s) = s^2\ C_1\ C_2 + sC_1\ G_2 + G_1\ G_2 \tag{3.33b}$$

Chang and Pai [3.23] have described a current-mode biquad using only two OTAs with multiple current outputs and with three current inputs. The transfer functions of this circuit, shown in Fig. 3.18, are as follows.

$$\begin{aligned}I_{out1}\,D(s) &= s^2\ C_1\ C_2\ I_{in3} + sC_1\ G_2\ (I_{in3} - I_{in2}) + G_1\ G_2\ (I_{in3} - I_{in1}),\\ I_{out2}\,D(s) &= -sG_1\ C_2\ I_{in1} - G_1\ G_2\ (I_{in1} - I_{in2}),\\ I_{out3} &= -sC_1\ G_2\ I_{in2} + G_1\ G_2\ I_{in1}\end{aligned} \tag{3.34a}$$

where

$$D(s) = s^2\ C_1\ C_2 + sC_1\ G_2 + G_1\ G_2 \tag{3.34b}$$

Note that at I_{out1}, an all-pass transfer function is realized using $I_{in2} = 2I_{in3}, I_{in1} = 0$, $I_{in3} = I_{in}$. The HP, LP, and BP realizations need, respectively, (a) $I_{in1} = I_{in2} = I_{in3}$, (b) $I_{in3} = I_{in2} = 0$, and (c) $I_{in3} = I_{in1} = 0$. A notch realization needs $I_{in3} = I_{in2}, I_{in1} = 0$.

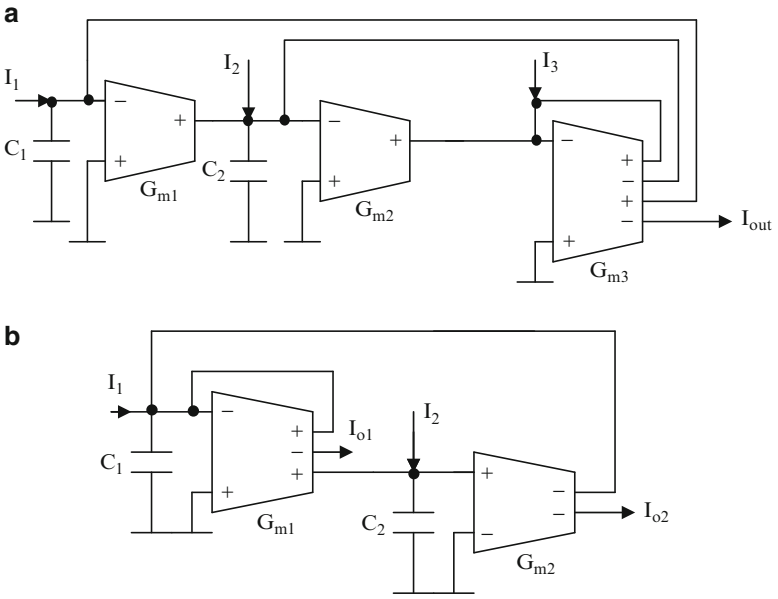


Fig. 3.17 (**a**) and (**b**) Current-mode OTA C biquads due to Chang (Adapted from [3.10] ©IEEE 1999)

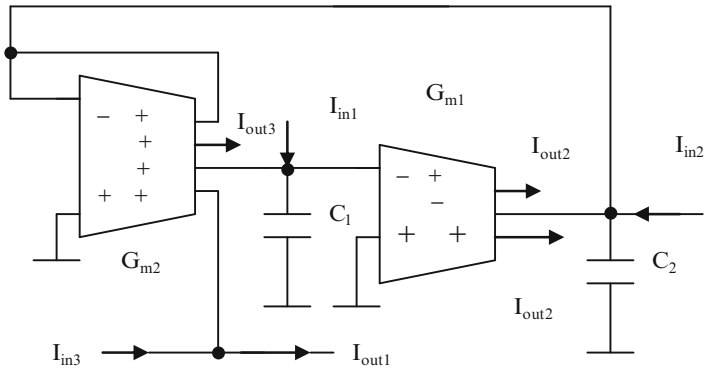


Fig. 3.18 Current-mode OTA C biquads due to Chang and Pai (Adapted from [3.23]©IEEE 2000)

Wu and El-Masry [3.6] have described two current-mode biquads as shown in Fig. 3.19a, b. The transfer functions of these two biquads are, respectively:

$$\begin{aligned} I_{out1}\,D(s) &= \frac{G_{m1}\,G_{m3}}{C_1\,C_2}\,I_1 + I_2\,s\frac{G_{m3}}{C_2}, \\ I_{out2}\,D(s) &= \frac{G_{m1}\,G_{m2}}{C_1\,C_2}\,I_1 + I_2\,\frac{G_{m2}\,G_{m4}}{C_2\,C_3} + I_3\,s^2\,\frac{G_{m2}}{G_{m3}} \end{aligned} \tag{3.35a}$$

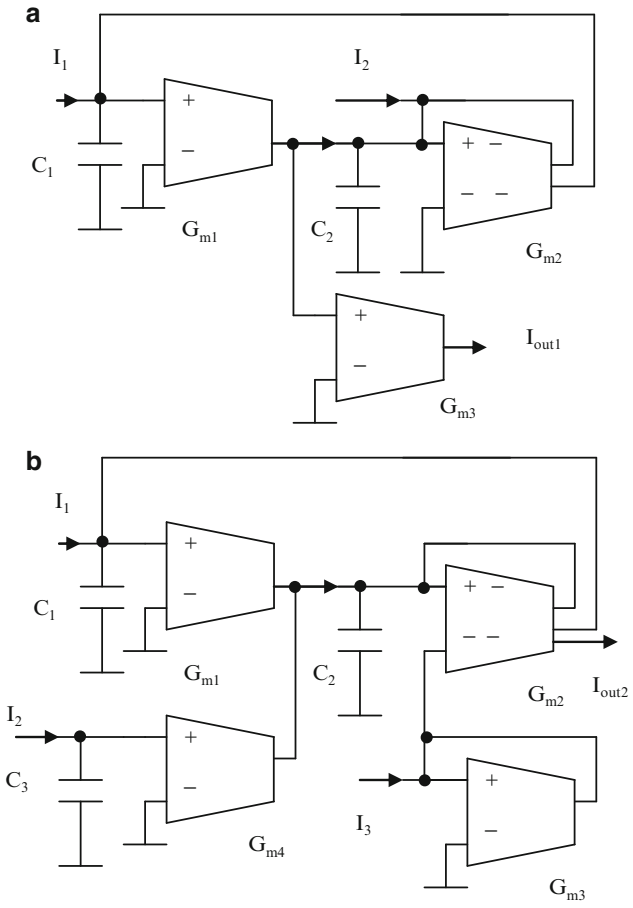


Fig. 3.19 Current-mode OTA C biquads due to Wu and El-Masry (Adapted from [3.6]©IEEE 1998)

where

$$D(s) = s^2 + s\frac{G_{m2}}{C_2} + \frac{G_{m1}\ G_{m2}}{C_1\ C_2} \tag{3.35b}$$

By removing the feedback around G_{m2}, infinite pole-Q can be realized. The circuit (b) is same as that of (a) except for additional feedforward voltage and current inputs using additional OTAs.

Sun and Fidler [3.5] have exhaustively studied the two-integrator loop-based current-mode OTA-C filters. They have suggested the four structures shown in Fig. 3.20a–d in which by having different choices, different filters can be obtained. All of these have been designed to have independent control of pole-Q and pole-frequency.

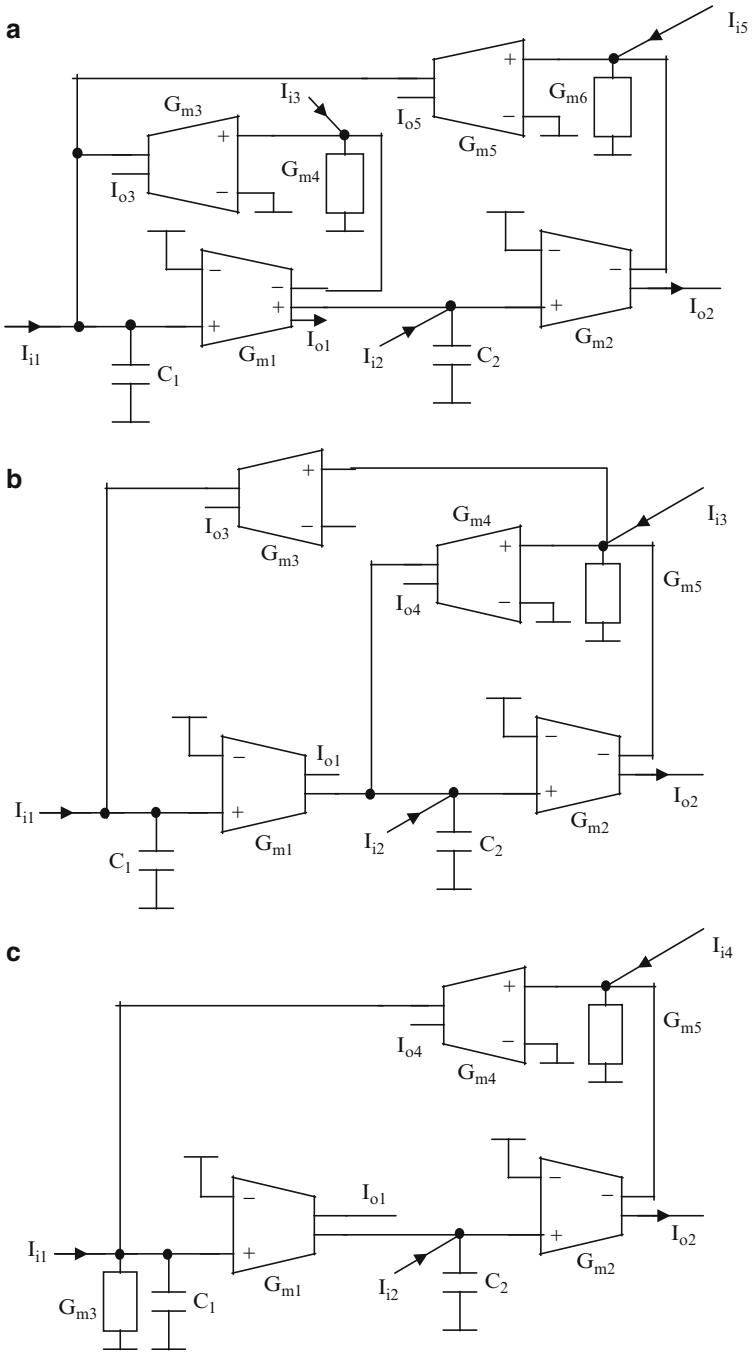


Fig. 3.20 (**a**)–(**d**) Current-mode biquads due to Sun and Fidler (Adapted from [3.5] ©IEEE 1996)

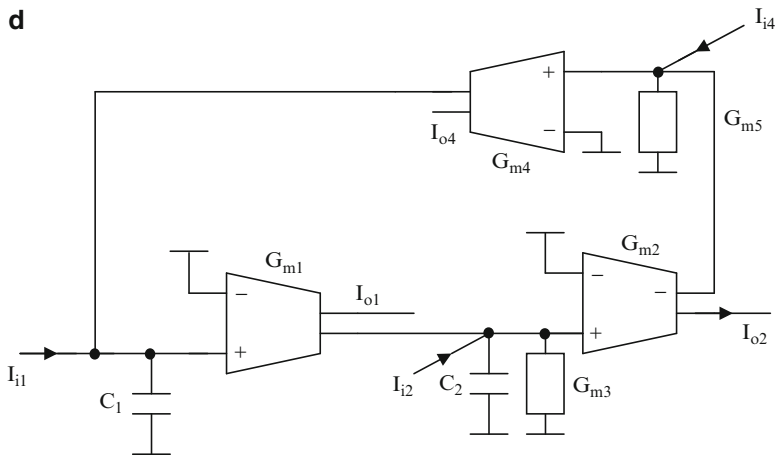


Fig. 3.20 (continued)

The transfer functions of these circuits are
Figure 3.20a:

$$D_1(s)\,I_{o1} = \tau_2\, s\, I_{i1} - k_{12}\, I_{i2} + k_{11}\, I_{i3}\, \tau_2\, s + k_{12}\, I_{i5}\, \tau_2\, s \tag{3.36a}$$

where $D_1(s) = s^2\ \tau_1\ \tau_2 + s\,\tau_2\ k_{11} + k_{12}$ and $k_{11} = \frac{G_{m3}}{G_{m4}}, k_{12} = \frac{G_{m5}}{G_{m6}}$.
Figure 3.20b:

$$D_2(s)\,I_{o1} = (\tau_2\, s + k_{22})\, I_{i1} - k_{12}\, I_{i2} + k_{12}\, \tau_2\, s\, I_{i34}$$

$$D_2(s)\,I_{o2} = I_{i1} + \tau_1\, s\, I_{i2} + (\tau_1\, s\, k_{22} + k_{12})\, I_{i34} \tag{3.36b}$$

where $D_2(s) = s^2\ \tau_1\ \tau_2 + s\,\tau_1\ k_{22} + k_{12}$ and $k_{22} = \frac{G_{m4}}{G_{m5}}, k_{12} = \frac{G_{m3}}{G_{m5}}$.
Figure 3.20c:

$$D_1(s)\,I_{o1} = \tau_2\, s\, I_{i1} - k_{12}\, I_{i2} + k_{12}\, I_{i4}\, \tau_2\, s \tag{3.36c}$$

where $k_{11} = \dfrac{G_{m3}}{G_{m1}}, k_{12} = \dfrac{G_{m4}}{G_{m5}}$
Figure 3.20d:

$$D_2(s)\,I_{o1} = (\tau_2\, s + k_{22})\, I_{i1} - k_{12}\, I_{i2} + k_{12}\, (\tau_2\, s + k_{22})\, I_{i4} \tag{3.36d}$$

where $k_{22} = \dfrac{G_{m3}}{G_{m2}}, k_{12} = \dfrac{G_{m4}}{G_{m5}}$. Note that in (3.35), $\tau_1 = \dfrac{C_1}{g_1}$ and $\tau_2 = \dfrac{C_2}{g_2}$.

The circuit of Fig. 3.20a needs six OTAs, has four current inputs, and realizes four current transfer functions at different output terminals of LP, HP, BP, and BS types. The circuit of Fig. 3.20b needs five OTAs, has three current inputs, and realizes current transfer functions of LP, HP, and BP types. The circuit of Fig. 3.20c on the other hand needs five OTAs, has three current inputs and realizes only current transfer functions of LP and BP types. Finally, the circuit of Fig. 3.20d needs five OTAs, has three current inputs and realizes LP and BP current transfer functions. Sun and Fidler have also suggested that the circuits can be simplified by choosing $k_{11} = 1$ or $k_{12} = 1$ or both $k_{11} = k_{12} = 1$ in the case of Fig. 3.20a (where $k_{11} = G_{m3}/G_{m4}$, $k_{12} = G_{m5}/G_{m6}$) and in the case of Fig. 3.20c, d $k_{12} = 1$ (where $k_{12} = G_{m4}/G_{m5}$).

A universal biquad filter circuit capable of providing all-pass/band-pass/high-pass/band-stop/low-pass filter function can be obtained by using the basic structure of Fig. 3.5g redrawn in Fig. 3.21a by replacing the admittance Y_p with a resistance realized using OTA G_{m4} and Y_n with a series network of grounded inductance L_1 (of value $C_2/G_{m2}G_{m3}$ simulated using OTAs G_{m2}, G_{m3}, and grounded capacitor C_2) in series with a capacitor C_1. The resulting universal biquad1 circuit due to Kamat, Ananda Mohan, and Prabhu [3.24] is presented in Fig. 3.21b.

The transfer function I_{AP1}/I_{in} for the circuit is given by

$$\frac{I_{AP1}}{I_{in}} = -\frac{N_1(s)}{D_1(s)} = -\frac{s^2 - s\left(\frac{g_{m2}g_{m3}}{g_{m4}C_2}\right) + \frac{g_{m2}g_{m3}}{C_1C_2}}{s^2 + s\left(\frac{g_{m2}g_{m3}}{g_{m1}C_2}\right) + \frac{g_{m2}g_{m3}}{C_1C_2}} \tag{3.37a}$$

Evidently under the condition $G_{m1} = G_{m4} = G_m$, (3.36a) becomes a second-order all-pass (AP1) current transfer function. The other node voltages and current transfer functions can be obtained as

$$\frac{V_{BS1}}{I_{in}} = \left(\frac{g_{m4} + g_{m1}}{g_{m1}\ g_{m4}}\right)\frac{\left(s^2 + \frac{g_{m2}g_{m3}}{C_1C_2}\right)}{D_1(s)},\ \frac{V_{HP1}}{I_{in}} = \left(\frac{g_{m4} + g_{m1}}{g_{m1}\ g_{m4}}\right)\frac{(s^2)}{D_1(s)}$$

$$\frac{I_{HP1}}{I_{in}} = \left(\frac{G_{m4} + G_{m1}}{G_{m1}\ G_{m4}}\right)\frac{G_{m3}\,s^2}{D_1(s)},\ \frac{V_{BP1}}{I_{in}} = \left(\frac{G_{m4} + G_{m1}}{G_{m1}\ G_{m4}}\right)\frac{s\left(\frac{G_{m3}}{C_2}\right)}{D_1(s)}, \tag{3.37b}$$

$$\frac{I_{BP1}}{I_{in}} = -\left(\frac{G_{m4} + G_{m1}}{G_{m1}\ G_{m4}}\right)\frac{\left(s\frac{G_{m2}\ G_{m3}}{C_2}\right)}{D_1(s)}$$

Thus an inverting all-pass, an inverting band-pass, and a noninverting high-pass current transfer functions and a noninverting notch and a noninverting high-pass voltage transfer functions are available. Note also that the band-stop current transfer

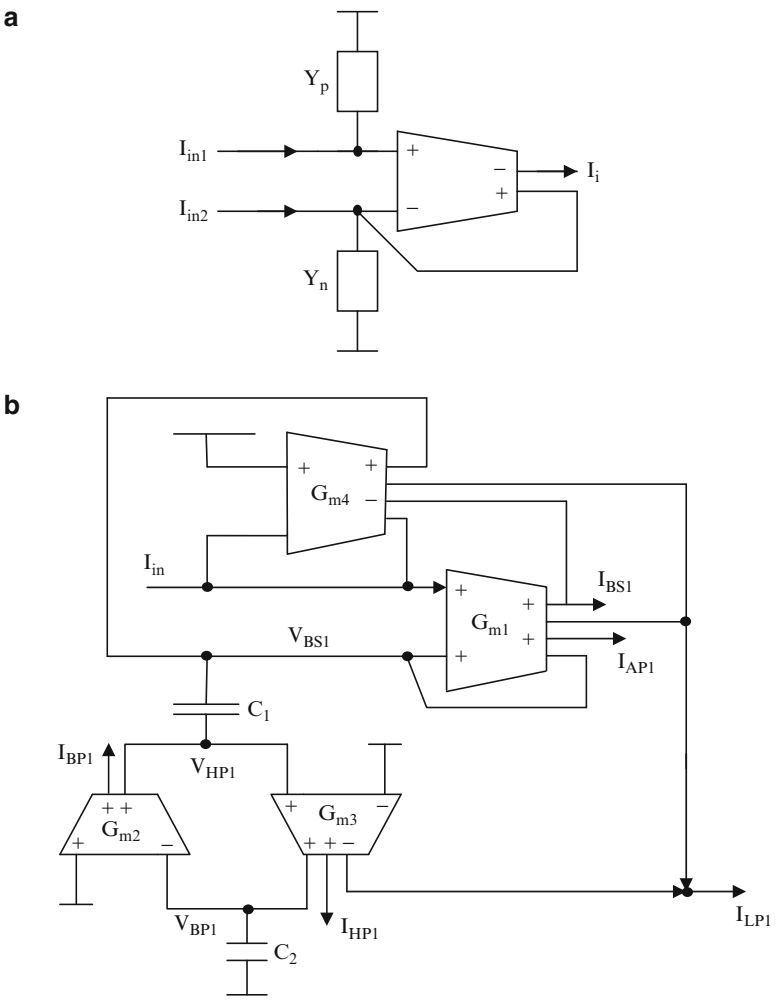


Fig. 3.21 (**a**) Basic configuration to derive universal biquads, (**b**) universal biquad1 (AP1/BP1/HP1/BS1/LP1) filter derived from the configuration of (**a**), (**c**) universal biquad2 (AP2/LP2/BP2/BS2/HP2) filter derived from the configuration of (**a**), (**d**) biquad3 (HPN3/HP3/LP3/BP3) filter (ILP3 when $G_{m1} = G_{m2} = G_{m3}$, $C_2 = C_3$ and I_{BP3} when $G_{m1} = G_{m3}$, $C_1 = C_3$), and (**e**) biquad4 (LPN4/LP4/HP4) (I_{HP4} and I_{NOTCH} when $I_{in2} = 0$) (Adapted from [3.24] Birkhauser ©2010)

function can be obtained as $I_{BS1} = I_{AP1} - I_{in}$. A low-pass transfer function can also be obtained as $I_{LP1} = I_{HP1} + I_{AP1} - I_{in}$ using $G_{m1} = G_{m4} = G_{m3}$. However, no independent control of pole-Q and pole-frequency is possible in the case of the LP transfer function. The resulting transfer functions are:

$$\frac{I_{BS1}}{I_{in}} = \frac{I_{AP1} - I_{in}}{I_{in}} = -\frac{2\left(s^2 + \frac{G_{m2}\ G_{m3}}{C_1\ C_2}\right)}{D_1(s)}, \frac{I_{LP1}}{I_{in}} = \frac{I_{AP1} - I_{in} + I_{HP1}}{I_{in}}$$

$$= -\frac{\left(\frac{2G_{m2}G_{m3}}{C_1C_2}\right)}{D_1(s)}$$

$$\frac{I_{BP1}}{I_{in}} = -\frac{-\left(\frac{G_{m4}+G_{m1}}{G_{m1}\ G_{m4}}\right)\left(\frac{s G_{m2}\ G_{m3}}{C_2}\right)}{D_1(s)}, \frac{I_{HP1}}{I_{in}} = \left(\frac{G_{m4}+G_{m1}}{G_{m1}\ G_{m4}}\right)\frac{G_{m3}\ s^2}{D_1(s)} \tag{3.38}$$

Note that all-pass transfer function is realized under the condition $G_{m1} = G_{m3} = G_{m4}$.

Another universal biquad filter circuit capable of providing all-pass/low-pass/band-pass/band-stop/high-pass filter function is realized using the basic structure of Fig. 3.21a by replacing the admittance Y_p with a resistance and Y_n with L_1 in parallel with C_1. The resulting universal biquad2 circuit is presented in Fig. 3.21c. Note that G_{m4} realizes Y_p and the grounded inductance L_1 is realized by OTAs G_{m2} and G_{m3} and capacitor C_2. The all-pass transfer function I_{AP2}/I_{in} of this circuit is given by

$$\frac{I_{AP2}}{I_{in}} = \frac{g_{m1}}{g_{m4}}\frac{N_2(s)}{D_2(s)} = \frac{g_{m1}}{g_{m4}}\frac{\left(s^2 - s\frac{g_{m4}}{C_1} + \frac{g_{m2}g_{m3}}{C_1C_2}\right)}{\left(s^2 + s\frac{g_{m1}}{C_1} + \frac{g_{m2}g_{m3}}{C_1C_2}\right)} \tag{3.39a}$$

under the matching condition $G_{m1} = G_{m4}$. The other node voltages and current transfer functions obtained in the circuit of Fig. 3.21c are as follows.

$$\frac{V_{BP2}}{I_{in}} = \frac{(G_{m1}+G_{m4})}{g_{m4}}\frac{\left(\frac{s}{C_1}\right)}{D_2(s)}, \frac{I_{BP2}}{I_{in}} = \frac{(G_{m1}+G_{m4})}{G_{m4}}\frac{s\left(\frac{G_{m2}}{C_1}\right)}{D_2(s)},$$

$$\frac{V_{LP2}}{I_{in}} = \frac{(G_{m1}+G_{m4})}{G_{m4}}\frac{\frac{G_{m2}}{C_1C_2}}{D_2(s)}, \frac{I_{LP2}}{I_{in}} = -\frac{(G_{m1}+G_{m4})}{G_{m4}}\frac{\frac{G_{m2}G_{m3}}{C_1C_2}}{D_2(s)} \tag{3.39b}$$

A notch transfer function can be obtained by adding the input current with the all-pass current output:

$$\frac{I_{BS2}}{I_{in}} = \frac{I_{in} + I_{AP2}}{I_{in}} = \frac{(G_{m1}+G_{m4})}{G_{m4}}\frac{\left(s^2 + \frac{G_{m2}G_{m3}}{C_1C_2}\right)}{D_2(s)} \tag{3.39c}$$

A high-pass transfer function can be realized by noting that $I_{HP2} = I_{in} + I_{AP2} + I_{LP2}$:

$$\frac{I_{HP2}}{I_{in}} = \frac{I_{AP2} + I_{LP2}}{I_{in}} + 1 = \frac{(G_{m1}+G_{m4})}{G_{m4}}\frac{s^2}{D_2(s)} \tag{3.39d}$$

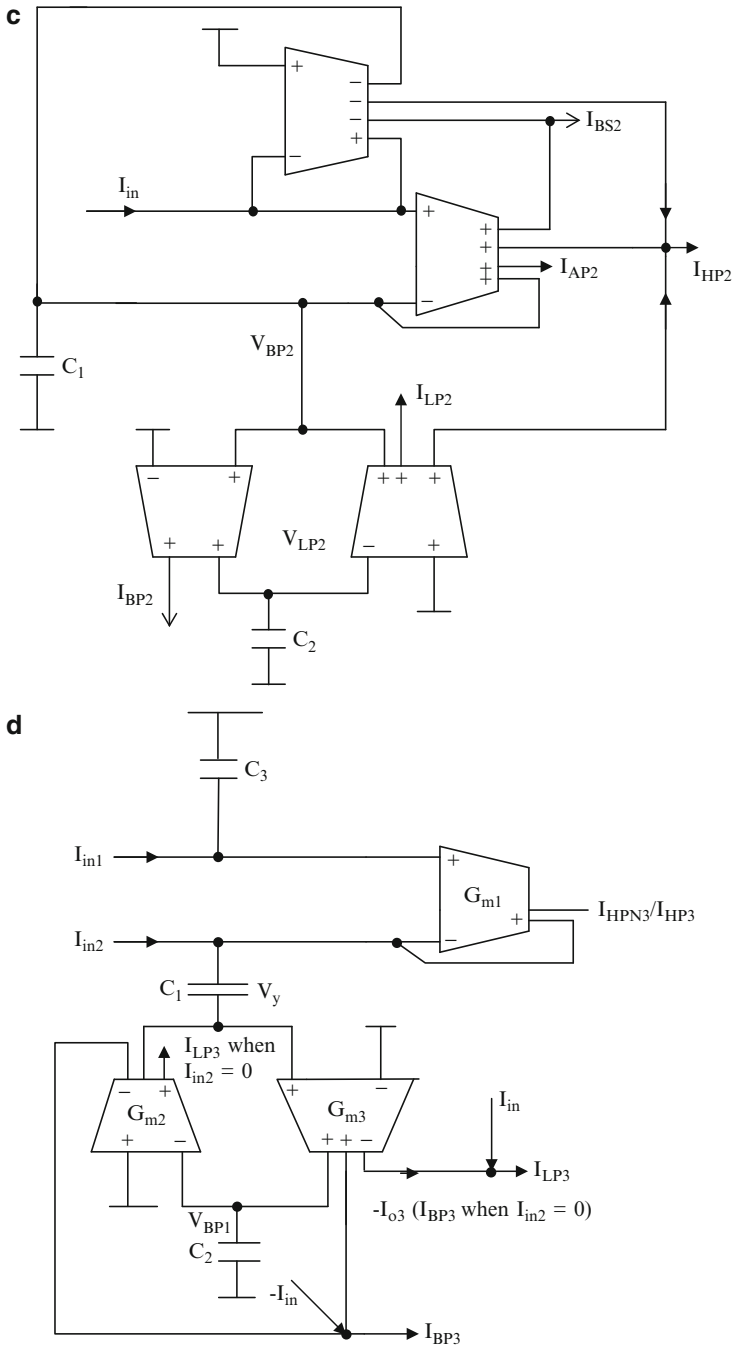


Fig. 3.21 (continued)

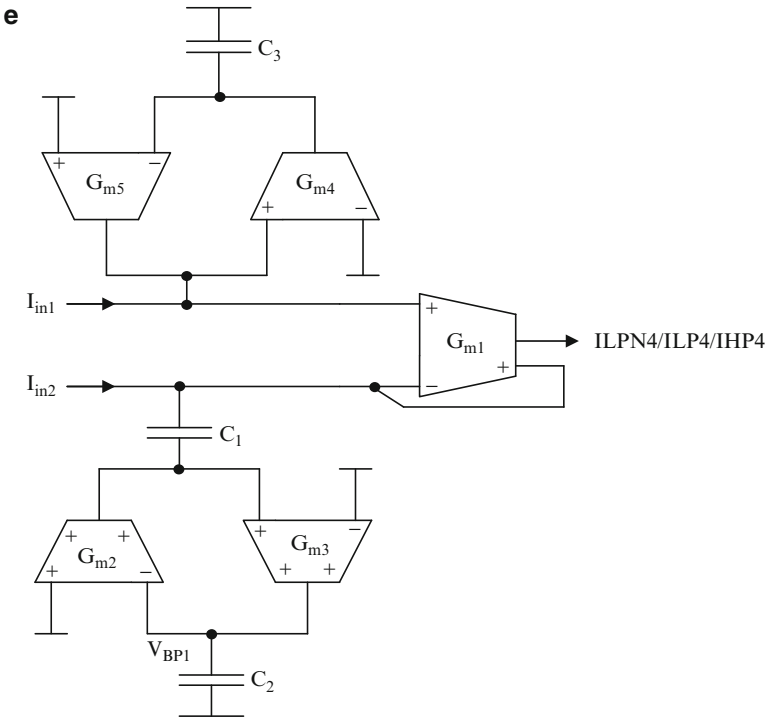


Fig. 3.21 (continued)

A circuit capable of providing a high-pass notch/high-pass filter function is realized using the basic structure of Fig. 3.21a by replacing the admittance Y_p with a grounded capacitor C_3 and Y_n with L_1 in series with C_1 with $I_{in1} = I_{in2} = I_{in}$. The resulting biquad3 filter circuit is presented in Fig. 3.21d. Here the grounded inductance L_1 is realized by OTAs G_{m2} and G_{m3} and capacitor C_2. The transfer function I_{HPN3}/I_{in} of this circuit is given by

$$\frac{I_{HPN3}}{I_{in}} = -\frac{N_3(s)}{D_3(s)} = -\left(\frac{s^2 + \dfrac{G_{m2}G_{m3}}{C_1C_2}\left(1 - \dfrac{C_1}{C_3}\right)}{s^2 + s\left(\dfrac{G_{m2}G_{m3}}{G_{m1}C_2}\right) + \left(\dfrac{G_{m2}G_{m3}}{C_1C_2}\right)}\right) \tag{3.40a}$$

Evidently the function I_{HPN3}/I_{in} is a high-pass notch since $\omega_n < \omega_p$. The circuit for the case $C_3 = 0$ is known in the literature, since component simulation of a series LC circuit in parallel with R is known to realize a notch transfer function. In this case, however, other transfer functions including I_{BP} and I_{LP} are available. In this case, I_{in1} at the noninverting input of OTA G_{m1} is not needed.

It is possible to realize a low-pass transfer function for which there is no independent control of pole-Q and pole-frequency:

$$\frac{I_{LP3}}{I_{in}} = \frac{I_{in} - I_{o3}}{I_{in}} = \frac{\dfrac{G_m^2}{C_1\ C_2}}{s^2 + s\left(\dfrac{G_m}{C_2}\right) + \dfrac{G_m^2}{C_1\ C_2}} \tag{3.40b}$$

under the condition $I_{in1} = I_{in2} = I_{in}$, $G_{m1} = G_{m2} = G_{m3}$, and $C_2 = C_3$. Under this condition, the notch frequency is related to pole frequency and pole-Q, since $C_1/C_2 = 1/{Q_p}^2$. Next, a band-pass transfer function can be obtained under the condition $G_{m1} = G_{m3}$, $C_1 = C_3$, as

$$\frac{I_{BP3}}{I_{in}} = \frac{I_{o1} - I_{o2} - I_{in}}{I_{in}} = \frac{s\dfrac{G_{m1}}{C_1}}{s^2 + s\left(\dfrac{G_{m2}}{C_2}\right) + \dfrac{G_{m1}\ G_{m2}}{C_1\ C_2}} \tag{3.40c}$$

A high-pass transfer function is realized at the I_{HP3} output. Note that independent control of pole frequency and pole-Q is not possible.

Alternatively, with $I_{in2} = 0$, the circuit of Fig. 3.21d can also realize a I_{LP3} at the IHPN3 output given by

$$\frac{I_{HPN3(LP3)}}{I_{in}} = \left(\frac{\left(\dfrac{G_{m2}G_{m3}}{C_2C_3}\right)}{D_3\,(s)}\right) \tag{3.41a}$$

The circuit also can realize band-pass and low-pass transfer functions at the output of OTAs G_{m3} and G_{m2}, respectively:

$$\frac{I_{03}}{I_{in}} = \left(\frac{s\left(\dfrac{G_{m3}}{C_3}\right)}{D_3\,(s)}\right) \tag{3.41b}$$

$$\frac{I_{02}}{I_{in}} = -\left(\frac{\left(\dfrac{G_{m2}G_{m3}}{C_2C_3}\right)}{D_3\,(s)}\right) \tag{3.41c}$$

A low-pass notch filter circuit (LPN) can be realized by using the basic structure of Fig. 3.21a by replacing the admittance Y_p with a grounded inductor L_1 and Y_n with C_1 in series with grounded inductor L_2 with $I_{in1} = I_{in2} = I_{in}$. The resulting

circuit is presented in Fig. 3.21e wherein the grounded inductance L_1 is realized by OTAs G_{m4} and G_{m5} and capacitor C_3. The grounded inductance L_2 is realized by OTAs G_{m2} and G_{m3} and capacitor C_2. The transfer function of this circuit is given by

$$\frac{I_{LPN4}}{I_{in}} = -\left(1 - \frac{G_{m2}G_{m3}C_3}{G_{m4}G_{m5}C_2}\right)\frac{N_4(s)}{D_4(s)}$$
$$= -\left(1 - \frac{G_{m2}G_{m3}C_3}{G_{m4}G_{m5}C_2}\right)\left(\frac{s^2 + \dfrac{G_{m2}G_{m3}}{C_1C_2\left(1 - \dfrac{G_{m2}G_{m3}C_3}{G_{m4}G_{m5}C_2}\right)}}{s^2 + s\left(\dfrac{G_{m2}G_{m3}}{G_{m1}C_2}\right) + \left(\dfrac{G_{m2}G_{m3}}{C_1C_2}\right)}\right) \tag{3.42a}$$

Evidently the circuit implements low-pass notch, as $\omega_n > \omega_p$. The notch and pole frequencies ω_n, ω_p and the pole-Q Q_p can be independently tuned. For optimal design/low spread, we may use $G_{m4} = G_{m5}$ and $G_{m2} = G_{m3}$. The sensitivity of the pole-frequency and pole-Q can be seen to be low with respect to all G_m and capacitor values. Under the condition $G_{m2}G_{m3} = G_{m4}G_{m5}$ and $C_2 = C_3$, I_{o1}/I_{in} will implement a low-pass biquad LP4 and with $I_{in2} = 0$, the circuit of Fig. 3.21e will realize a noninverting high-pass biquad.

$$\frac{I_{LP4}}{I_{in}} = -\left(\frac{\dfrac{G_{m2}G_{m3}}{C_1C_2}}{D_4(s)}\right), \quad \frac{I_{HP4}}{I_{in}} = \left(\frac{G_{m2}G_{m3}C_3}{G_{m4}G_{m5}C_2}\right)\left(\frac{s^2}{D_4(s)}\right) \tag{3.42b}$$

Bhaskar, Sharma, Singh, and Senani [3.25] have described five OTA-C biquads that can work in dual-mode as VIVO or CICO biquads. These are presented in Fig. 3.22a–e. All of these need only four OTAs and some with dual ouputs. All realize three voltage transfer functions and three current transfer functions. The current-mode ciruit is obtained by using a resistor (simulated using OTA) as an input current to voltage converter to realize the same voltage transfer functions. All these filters are based on two-integrator loops and use one OTA-based additional amplifier to realize the finite Q by damping the lossless two-integrator loop. The circuit of Fig. 3.22c needs only three OTAs for the pole-forming loop.

The voltage mode and current-mode transfer functions of these circuits of Fig. 3.22a–e are presented next:

Figure 3.22a:

$$\left(\frac{V_{o1}}{V_i}\right)D_1(s) = -s^2\left(\frac{G_{m4}}{G_{m3}}\right),$$
$$\left(\frac{V_{o2}}{V_i}\right)D_1(s) = s\left(\frac{G_{m1}\,G_{m4}}{C_1\;G_{m3}}\right), \quad \left(\frac{V_{o3}}{V_i}\right)D_1(s) = \left(\frac{G_{m1}\;G_{m2}\;G_{m4}}{C_1\;C_2\;G_{m3}}\right) \tag{3.43a}$$

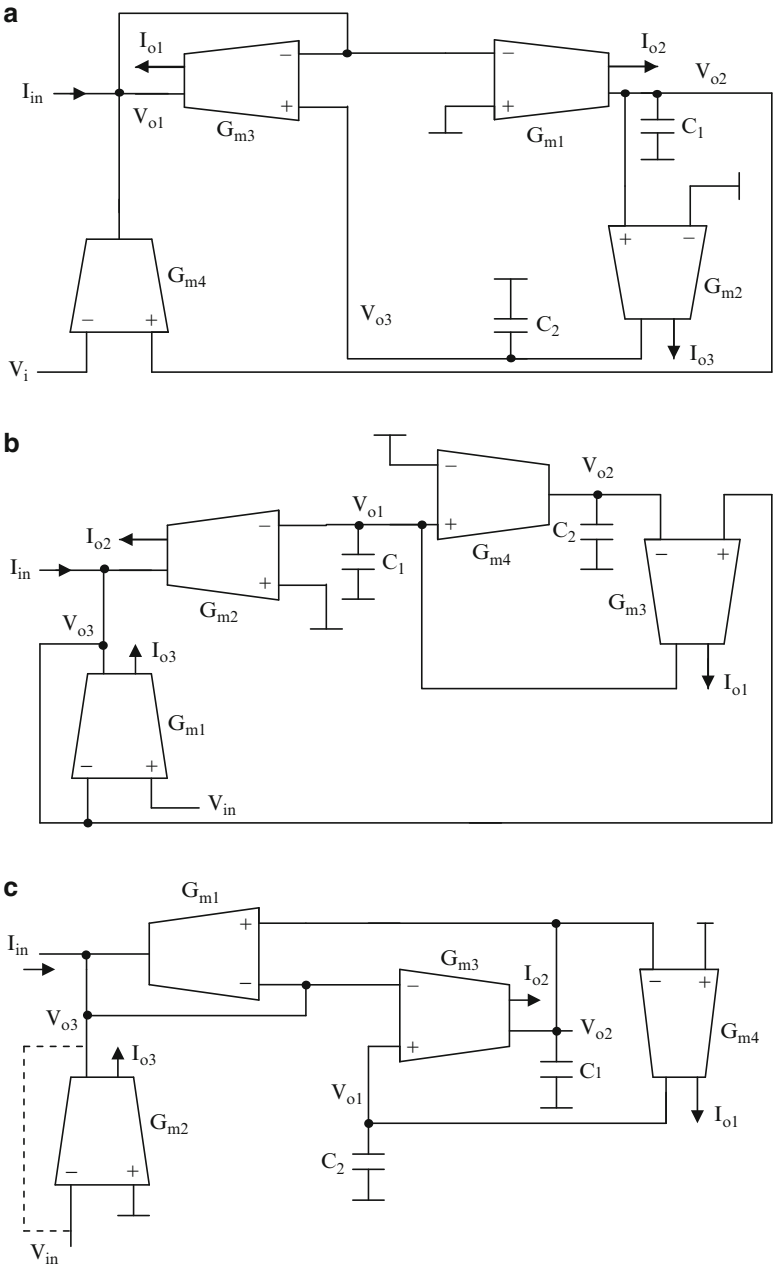


Fig. 3.22 (**a**)–(**e**) Current-mode OTA-C biquads due to Bhaskar, Sharma, Singh, and Senani (Adapted from [3.25]©Frequenz 2006)

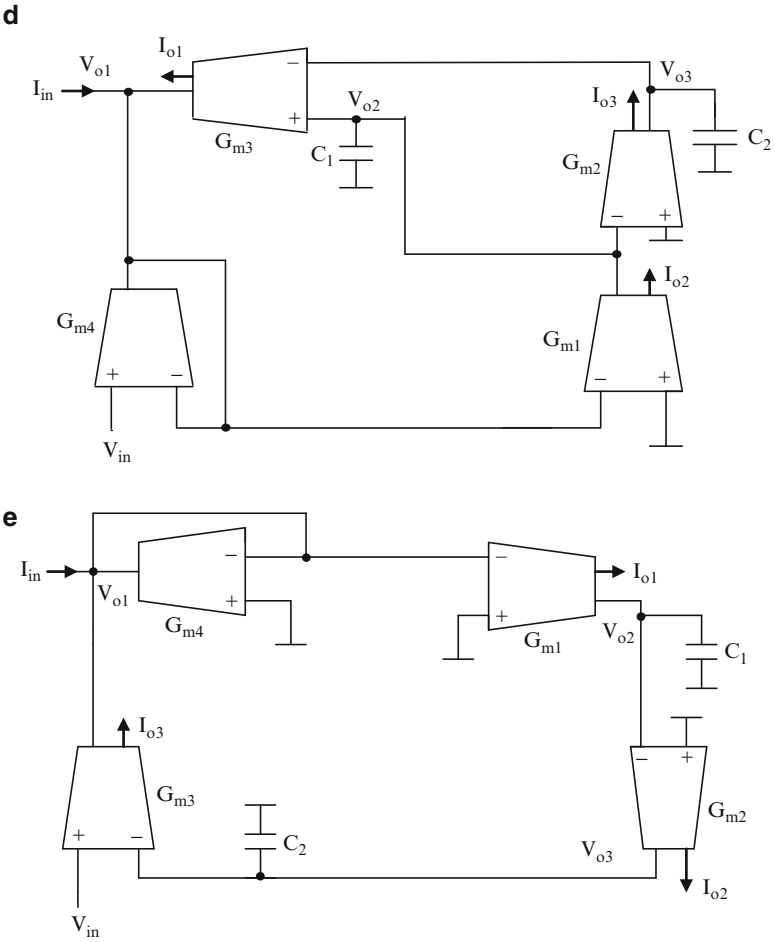


Fig. 3.22 (continued)

where

$$D_1(s) = s^2 + s\left(\frac{G_{m1}\,G_{m4}}{C_1\,G_{m3}}\right) + \frac{G_{m1}\,G_{m2}}{C_1\,C_2} \tag{3.43b}$$

Figure 3.22b:

$$\left(\frac{V_{o1}}{V_i}\right) D_2(s) = s\left(\frac{G_{m3}}{C_1}\right),\ \left(\frac{V_{o2}}{V_i}\right) D_2(s) = \left(\frac{G_{m3}\,G_{m4}}{C_1\,C_2}\right),$$
$$\left(\frac{V_{o3}}{V_i}\right) D_2(s) = s^2 + \frac{G_{m3}\,G_{m4}}{C_1\,C_2} \tag{3.43c}$$

where

$$D_2(s) = s^2 + s\left(\frac{G_{m2}\ G_{m3}}{C_1\ G_{m1}}\right) + \frac{G_{m3}\ G_{m4}}{C_1\ C_2} \tag{3.43d}$$

Figure 3.22c:

$$\left(\frac{V_{o3}}{V_i}\right) D_3(s) = -\frac{G_{m2}}{G_{m1}}\left(s^2 + \frac{G_{m3}\ G_{m4}}{C_1\ C_2}\right),$$
$$\left(\frac{V_{o2}}{V_i}\right) D_3(s) = s\left(\frac{G_{m2}\ G_{m3}}{C_1\ G_{m1}}\right),\ \left(\frac{V_{o1}}{V_i}\right) D_3(s) = -\left(\frac{G_{m2}\ G_{m3}\ G_{m4}}{C_1\ C_2\ G_{m1}}\right) \tag{3.43e}$$

where

$$D_3(s) = s^2 + s\left(\frac{G_{m3}}{C_1}\right) + \frac{G_{m3}\ G_{m4}}{C_1\ C_2} \tag{3.43f}$$

Figure 3.22d:

$$\left(\frac{V_{o1}}{V_i}\right) D_4(s) = s^2,\ \left(\frac{V_{o2}}{V_i}\right) D_4(s) = -s\left(\frac{G_{m1}}{C_1}\right),$$
$$\left(\frac{V_{o3}}{V_i}\right) D_4(s) = \left(\frac{G_{m1}\ G_{m2}}{C_1\ C_2}\right) \tag{3.43g}$$

where

$$D_4(s) = s^2 + s\left(\frac{G_{m1}\ G_{m3}}{C_1\ G_{m4}}\right) + \frac{G_{m1}\ G_{m2}\ G_{m3}}{C_1\ C_2\ G_{m4}} \tag{3.43h}$$

Figure 3.22e:

$$\left(\frac{V_{o1}}{V_i}\right) D_5(s) = s^2\left(\frac{G_{m3}}{G_{m4}}\right),\ \left(\frac{V_{o2}}{V_i}\right) D_5(s)$$
$$= -s\left(\frac{G_{m1}\ G_{m3}}{C_1\ G_{m4}}\right),\ \left(\frac{V_{o3}}{V_i}\right) D_5(s) = \left(\frac{G_{m1}\ G_{m2}\ G_{m3}}{C_1\ C_2\ G_{m4}}\right) \tag{3.43i}$$

where

$$D_5(s) = s^2 + s\left(\frac{G_{m1}}{C_1}\right) + \frac{G_{m1}\ G_{m2}\ G_{m3}}{C_1\ C_2\ G_{m4}} \tag{3.43j}$$

The respective current-mode transfer functions are:
Figure 3.22a:

$$\left(\frac{I_{o1}}{I_{in}}\right) D_1(s) = -\left(s^2 + \frac{G_{m1}\ G_{m2}}{C_1\ C_2}\right),\ \left(\frac{I_{o2}}{I_{in}}\right) D_1(s) = s^2\left(\frac{G_{m1}}{G_{m3}}\right),\ \left(\frac{I_{o3}}{I_{in}}\right) D_1(s) = -s\left(\frac{G_{m1}\ G_{m2}}{C_1\ G_{m3}}\right) \tag{3.44a}$$

$I_{o4} = I_{o1} - I_{o2}$ and $G_{m1} = G_{m3}$ low-pass, $I_{o5} = I_{o1} - I_{o3}$ and $G_{m2} = G_{m4}$ all-pass
Figure 3.22b:

$$\left(\frac{I_{o3}}{I_{in}}\right) D_2(s) = -\left(s^2 + \frac{G_{m3}\ G_{m4}}{C_1\ C_2}\right),\ \left(\frac{I_{o1}}{I_{in}}\right) D_2(s) = s^2\left(\frac{G_{m3}}{G_{m1}}\right),\ \left(\frac{I_{o2}}{I_{in}}\right) D_2(s) = -s\left(\frac{G_{m2}\ G_{m3}}{C_1\ G_{m1}}\right) \tag{3.44b}$$

$I_{o4} = I_{o1} + I_{o3}$ and $G_{m1} = G_{m3}$ low-pass, $I_{o5} = I_{o3} - I_{o2}$ and $G_{m2} = G_{m4}$ all-pass
Figure 3.22c:

$$\left(\frac{I_{o3}}{I_{in}}\right) D_3(s) = -\left(s^2 + \frac{G_{m3}\ G_{m4}}{C_1\ C_2}\right)\frac{G_{m2}}{G_{m1} + G_{m2}},\ \left(\frac{I_{o2}}{I_{in}}\right) D_3(s) = -s^2\left(\frac{G_{m3}}{G_{m1}\ + G_{m2}}\right),\ \left(\frac{I_{o1}}{I_{in}}\right) D_3(s) = s\left(\frac{G_{m3}\, G_{m4}}{C_1\,(G_{m1}\ + G_{m2})}\right) \tag{3.44c}$$

$I_{o4} = I_{o2} + I_{o3}$ and $G_{m2} = G_{m3}$ low-pass, $I_{o5} = I_{o1} + I_{o3}$ and $G_{m1} = G_{m2} = 2G_{m4}$, all-pass
Figure 3.22d:

$$\left(\frac{I_{o1}}{I_{in}}\right) D_1(s) = -\left(s\frac{G_{m1}\ G_{m3}}{C_1\ G_{m4}} + \frac{G_{m1}\ G_{m2}\ G_{m3}}{C_1\ C_2\ G_{m4}}\right),\ \left(\frac{I_{o2}}{I_{in}}\right) D_4(s) = -s^2\left(\frac{G_{m1}}{G_{m4}}\right),\ \left(\frac{I_{o3}}{I_{in}}\right) D_4(s) = \left(\frac{sG_{m1}\ G_{m2}}{C_1\ G_{m4}}\right) \tag{3.44d}$$

$I_{o4} = I_{o1} + I_{o3}$ and $G_{m2} = G_{m3}$ low-pass, $I_{o5} = I_{o2} + I_{o4}$ and $G_{m1} = G_{m4}$, $G_{m2} = G_{m3}$, notch and $I_{o6} = I_{o2} + I_{o3} + I_{o4}$ and $G_{m1} = G_{m4}$, $G_{m2} = G_{m3}$ all-pass,

Figure 3.21e:

$$\left(\frac{I_{o3}}{I_{in}}\right) D_1(s) = -\left(\frac{G_{m1}\ G_{m2}\ G_{m3}}{C_1\ C_2\ G_{m4}}\right),$$
$$\left(\frac{I_{o1}}{I_{in}}\right) D_1(s) = -s^2\left(\frac{G_{m1}}{G_{m4}}\right), \left(\frac{I_{o2}}{I_{in}}\right) D_5(s) = s\left(\frac{G_{m1}\ G_{m2}}{C_1\ G_{m4}}\right) \tag{3.44e}$$

Note that $I_{o4} = I_{o1} + I_{o3}$ notch and $I_{o5} = I_{o1} + I_{o2} + I_{o3}$ are all-pass transfer functions.

3.5 OTA-C Filters Using First-Order All-Pass Sections

3.5.1 OTA-C Filters Derived from Tarmy–Ghausi Active RC Filter

The active RC filter due to Moschytz [3.26] which is a modification of the Tarmy and Ghausi proposal [3.27] based on the block diagram of Fig. 3.23 was discussed in Chap. 2 (see Fig. 2.25a). This basically consists of two first-order all-pass filters in a negative feedback loop. The pole-Q of this circuit denoted as Q_p can be shown to be

$$Q_p = \frac{1 + A_2}{2(1 - A_2)} \tag{3.45a}$$

The sensitivity of Q_p to A_2 can be derived as

$$S_{A_2}^{Q_p} = Q_p - \frac{1}{4\,Q_p} \tag{3.45b}$$

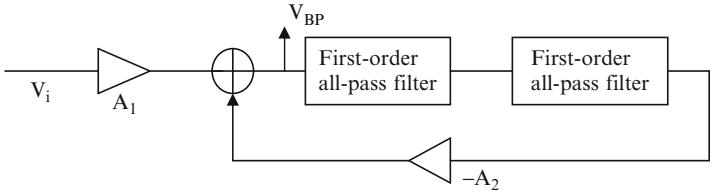


Fig. 3.23 Moschytz's modified Tarmy–Ghausi configuration

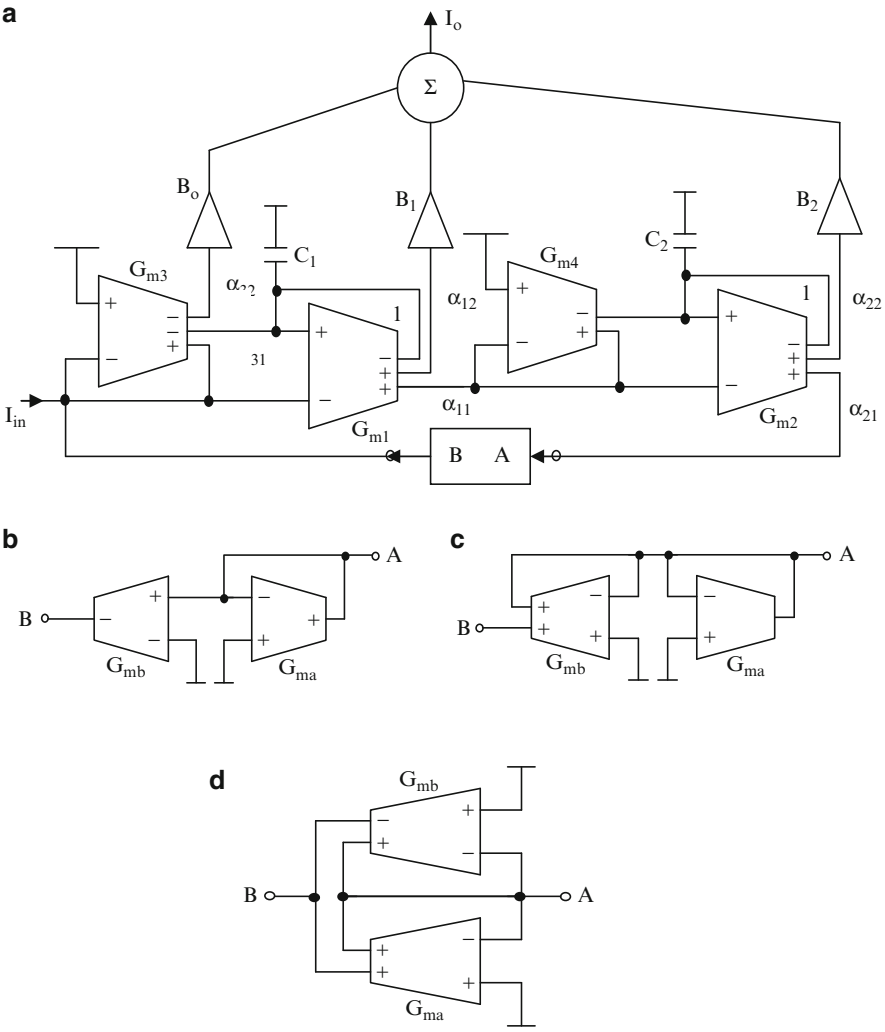


Fig. 3.24 (**a**) OTA-C filter based on Moschytz's modified Tarmy–Ghausi active RC filter and (**b**)–(**d**) three subcircuits that are used between terminals *A* and *B* in (**a**) (Adapted from [3.32] ©IET 2010)

Interestingly, there are two methods suggested in the literature [3.28, 3.29, 3.30, 3.31] for implementing A_2 to reduce the pole-Q sensitivity. In these, A_2 is expressed as $P/(P + Q)$ and $(P - Q)/(P + Q)$. These are considered next.

The OTA-C implementation of universal current-mode filter structure based on the Tarmy–Ghausi (TG) configuration [3.32] is given in Fig. 3.24a. The feedback factor A_2 can be realized in three ways as shown in Fig. 3.24b–d. The circuit denoted as TG0 uses two OTAs G_{ma} and G_{mb} to realize feedback factor $A_2 = G_{mb}/G_{ma}$ as shown in Fig. 3.24b. The OTA G_{ma} is used as an OTA simulated resistor and the OTA G_{mb} acts as a V-to-I converter. In Fig. 3.24a, the feed-forward path consists of two

first-order all-pass circuits. The OTAs G_{m1}, G_{m3} and capacitor C_1 realize one first-order all-pass section and the OTAs G_{m2}, G_{m4} and capacitor C_2 realize another second first-order all-pass section. The overall transfer function of the circuit TG0, under the matching condition $G_{m1} = G_{m3} = G_{m2} = G_{m4} = G_m$ and $C_1 = C_2 = C$, is given by

$$\frac{I_{out}}{I_{in}} = \left\{ \frac{G_{ma}}{(G_{ma}+G_{mb})} \frac{s^2(B_o - B_1 + B_2) + 2s\frac{G_m}{C}(B_o - B_2) + \left(\frac{G_m}{C}\right)^2 (B_o + B_1 + B_2)}{s^2 + 2s\frac{G_m}{C}\frac{(G_{ma}-G_{mb})}{(G_{ma}+G_{mb})} + \left(\frac{G_m}{C}\right)^2} \right\} \tag{3.46a}$$

The circuit has independent control of the Q-factor and pole-frequency ω_p. Evidently the pole-Q_p and Q_p-sensitivity of this circuit (TG0) can be obtained from (3.45a) by noting that $A_2 = G_{mb}/G_{ma}$ as

$$Q_p = \frac{1}{2}\frac{(G_{ma}+G_{mb})}{(G_{ma}-G_{mb})} = \frac{1}{2}\frac{\left(1+\frac{G_{mb}}{G_{ma}}\right)}{\left(1-\frac{G_{mb}}{G_{ma}}\right)} \tag{3.46b}$$

and from (3.45b),

$$S^{Q_p}_{\frac{g_{mb}}{g_{ma}}} = Q_p - \frac{1}{4Q_p} \tag{3.46c}$$

For high Q_p realizations, the sensitivity of Q_p with respect to A_2 has the same order of Q_p.

The use of the feedback circuit as shown in Fig. 3.24c in the structure of Fig. 3.24a, significantly reduces the Q_p sensitivity. In this case, the two OTAs G_{ma} and G_{mb} realizing resistors are connected in parallel. The feedback factor A_2 can easily be seen to be

$$A_2 = \frac{G_{mb}}{G_{ma}+G_{mb}} \tag{3.47a}$$

The overall transfer function of TG1, under the matching condition $G_{m1} = G_{m3} = G_{m2} = G_{m4} = G_m$ and $C_1 = C_2 = C$ is given by

$$\frac{I_{out}}{I_{in}} = \frac{(G_{ma}+G_{mb})}{(G_{ma}+2G_{mb})} \times \frac{s^2(B_o - B_1 + B_2) + 2s\frac{G_m}{C}(B_o - B_2) + \left(\frac{G_m}{C}\right)^2 (B_o + B_1 + B_2)}{s^2 + 2s\frac{G_m}{C}\frac{G_{ma}}{(G_{ma}+2G_{mb})} + \left(\frac{G_m}{C}\right)^2} \tag{3.47b}$$

The pole-Q and Q_p sensitivity of TG1 circuit are given as

$$Q_p = \frac{1}{2} + \frac{g_{mb}}{g_{ma}},\ S^{Q_p}_{\frac{g_{mb}}{g_{ma}}} = 1 - \frac{1}{2\,Q_p} \tag{3.47c}$$

The third modified Tarmy–Ghausi biquad circuit TG2 uses the feedback circuit of Fig. 3.24d and realizes

$$A_2 = \frac{g_{mb} - g_{ma}}{g_{mb} + g_{ma}} \tag{3.48a}$$

using two OTAs in a novel manner to reduce the Q_p-sensitivity. The two OTA simulated resistors G_{ma} and G_{mb} in Fig. 3.24d are connected in parallel as in Fig. 3.24c, but the mirrored output current of OTA G_{ma} is subtracted from that of G_{mb} to obtain the feedback current I_f. The overall transfer function of TG2 can be shown to be

$$\frac{I_{out}}{I_{in}} = \frac{(G_{mb} + G_{ma})}{2G_{mb}} \frac{s^2(B_o - B_1 + B_2) + 2s\frac{G_m}{C}(B_o - B_2) + \left(\frac{G_m}{C}\right)^2 (B_o + B_1 + B_2)}{s^2 + 2s\frac{G_m}{C}\frac{G_{ma}}{G_{mb}} + \left(\frac{G_m}{C}\right)^2} \tag{3.48b}$$

The pole-Q and Q_p-sensitivity of TG2 circuit can be seen to be

$$Q_p = \frac{1}{2}\frac{G_{mb}}{G_{ma}},\ S^{Q_p}_{\left(\frac{G_{mb}}{G_{ma}}\right)} = 1 \tag{3.48c}$$

It is possible to realize a universal OTA-C biquad using the basic configuration of Fig. 3.24b using a general synthesis procedure for obtaining the various component values to realize general biquadratic functions. This is possible by invoking an analogy between direct form digital filter structure [3.33] and Tarmy–Ghausi *circuit arrangement* by recognizing that in the place of the delay operator "z^{-1}", using bilinear transformation, one obtains a first-order all-pass network in the s-domain. Thus, the Tarmy–Ghausi biquad can be considered to be based on a second-order direct-form digital filter of Fig. 3.25a with no middle feedback loop (i.e., $A_1 = 0$). Thus we consider the architecture of Fig. 3.25b to realize a general second-order filter whose transfer function is given by

$$\frac{I_{out}}{I_{in}} = \frac{B_0 + B_1\ z^{-1} + B_2\ z^{-2}}{1 + A_2\ z^{-2}} \tag{3.49a}$$

Note that CM in Fig. 3.25b is a current mirror with two outputs. The corresponding analog transfer function is as follows.

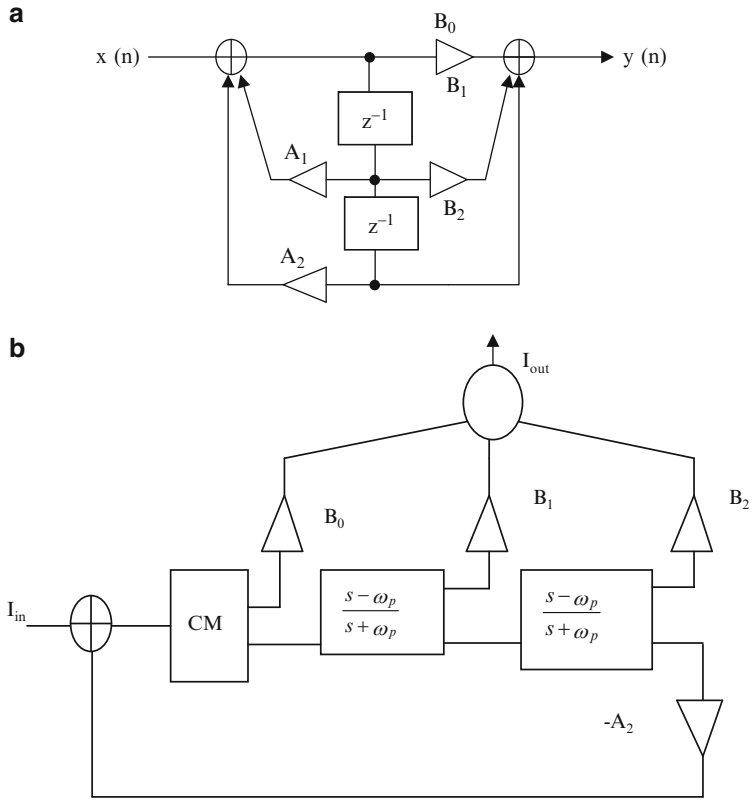


Fig. 3.25 (**a**) Direct form II realization of second-order digital filter and (**b**) equivalent general current-mode second-order analog filter realization using first-order all-pass sections based on Tarmy–Ghausi circuit arrangement

$$\frac{I_{out}}{I_{in}} = \left\{ \frac{s^2(B_o - B_1 + B_2) + 2s\omega_p(B_o - B_2) + {\omega_p}^2(B_o + B_1 + B_2)}{(1 + A_2)\left\{ s^2 + 2s\omega_p \dfrac{(1 - A_2)}{(1 + A_2)} + {\omega_p}^2 \right\}} \right\} \tag{3.49b}$$

Note that (3.48b) is a universal second-order transfer function, since any filter type can be derived from the expression. However, it is easy to synthesize the desired A_2, B_0, B_1, and B_2 values by observing (3.49a). The numerators of second-order digital transfer functions corresponding to the use of bilinear transformation on s-domain prototype for low-pass, band-pass, high-pass, notch, and all-pass transfer functions are:

$$\text{LP}: \ (1 + 2z^{-1} + z^{-2}) \qquad B_0 = 1,\ B_1 = 2,\ B_2 = 1$$

$$\text{BP}: \ (1 - z^{-2}) \qquad B_0 = 1,\ B_1 = 0,\ B_2 = -1$$

Table 3.1 Different filter realizations using basic Tarmy–Ghausi circuit arrangement with feedforward factors

B_o	B_1	B_2	Filter type	Transfer function
1	2	1	LP	$\frac{4}{(1+A_2)}\frac{{\omega_p}^2}{D(s)}$
1	−2	1	HP	$\frac{4}{(1+A_2)}\frac{s^2}{D(s)}$
1	0	−1	BP+	$\frac{4}{(1+A_2)}\frac{s\omega_p}{D(s)}$
−1	0	1	BP-	$-\frac{4}{(1+A_2)}\frac{s\omega_p}{D(s)}$
1	0	1	BS	$\frac{2}{(1+A_2)}\frac{\left(s^2+{\omega_p}^2\right)}{D(s)}$
β_1	−1	β_1	HPN1	$\left(\frac{2\beta_1+1}{1+A_2}\right)\left\{s^2+\left(\frac{2\beta_1-1}{2\beta_1+1}\right){\omega_p}^2\right\}\Big/D(s).$ $\omega_n\langle\omega_p$, Condition to be satisfied :$\beta_1\rangle 0.5$
β_1	1	β_1	LPN1	$\left(\frac{2\beta_1-1}{1+A_2}\right)\left\{s^2+\left(\frac{2\beta_1+1}{2\beta_1-1}\right){\omega_p}^2\right\}\Big/D(s).$ $\omega_n\rangle\omega_p$, Condition to be satisfied:$\beta_1\rangle 0.5$
A_2	0	1	AP	$\left(s^2-2s\omega_p\left(\frac{1-A_2}{1+A_2}\right)+{\omega_P}^2\right)\Big/D(s).$
1	0	β	AE	$\left(\frac{1+\beta}{1+A_2}\right)\left(\left(s^2+2s\omega_p\frac{(1-\beta)}{(1+\beta)}+{\omega_P}^2\right)\Big/D(s).\right)$

Note that $D(s)=s^2+2s\omega_p\frac{(1-A_2)}{(1+A_2)}+{\omega_p}^2$

Adapted from [3.32] ©IET 2010

$$\text{HP}: \ (1-2z^{-1}+z^{-2}) \qquad B_0=1,\ B_1=-2,\ B_2=1$$

$$\text{Notch}: \ (1+\alpha z^{-1}+z^{-2}) \qquad B_0=1,\ B_1=\ \alpha,\ B_2=1$$

$$\text{All - pass}: \ (A_2+z^{-2}) \qquad B_0=A_2,\ B_1=0,\ B_2=1$$

Note that $|\alpha| < 2$ and thus α can be positive or negative. The corresponding s-domain transfer functions for these various cases are presented in Table 3.1. From this table, it is evident that all second-order filter types such as low-pass (LP), high-pass (HP), band-pass (BP), symmetric notch (BS), low-pass notch (LPN), high-pass

notch (HPN), all-pass (AP), and amplitude equalizer (AE) can be derived using the circuit arrangement given in Fig. 3.25b. The band-pass and symmetric band-stop realizations are simple as they need unity coefficients for feedforward inputs, whereas all the other biquad filter types such as LP, HP, LPN, HPN, AP, and AE require at least one nonunity gain feedforward coefficient. Note that in some cases, a multiplier of 2 will be needed. Note that current mirrors with appropriate ratioed devices can be used at the OTA output to realize these desired gain constants.

3.5.2 *Second-Order All-Pass OTA-C Filter Realization Derived from Mitra–Hirano and Gray–Markel Structures*

The second-order all-pass filter realization using basic Tarmy–Ghausi circuit arrangement of Fig. 3.25a requires the feedforward coefficients $B_0 = A_2$ in addition to $B_2 = 1$, which needs matching of the appropriate additional OTAs in the feedforward path with those in the pole-forming loop. Therefore, it is of interest to derive novel circuits that may possibly need a single scaling factor A_2 which acts as both a feedback factor as well as a feedforward factor. It is also of interest to explore other second-order all-pass digital filter structures using two z^{-1} delay blocks, which is equivalent to two first-order all-pass sections in the s-domain that also share the scaling factors in the numerator and denominator of the transfer function.

Mitra and Hirano [3.34] have presented Type 2 and Type 3 second-order all-pass digital filters. However, their direct adaptation to OTA-C filters can take advantage of a property that the pole frequency ω_p of the second-order OTA-C filter is controlled by the pole-frequency of the two identical first-order all-pass filters and only the pole-Q needs to be controlled. However, due to the particular structure of the denominator of the transfer function (viz., $1 + A_1z^{-1} + A_1A_2z^{-2}$), both the multipliers are needed, not enabling any simplification if we choose a Type 2 all-pass digital filter. On the other hand, if we choose the Type 3 structure of Fig. 3.26a, the denominator of the transfer function is $(1 + A_1z^{-1} + A_2z^{-2})$, thus providing the option of choosing $A_1 = 0$. The corresponding OTA-C filter is shown in Fig. 3.26b. This filter uses a single scaling factor A_2 given by $A_2 = g_{mb}/(g_{ma} + g_{mb})$. The denominator of the transfer function of the filter of Fig. 3.26b is same as that of Fig. 3.24a using the subcircuit of Fig. 3.24c and hence the pole-Q and its sensitivity are described by (3.47c).

Consider next the second-order all-pass digital filter realization, given in Fig. 3.27a, based on the Gray–Markel lattice structure [3.35] using two one-multiplier lattice sections connected in a nested direct-form II structure. As has been seen in the case of the Mitra–Hirano all-pass filter, the pole-frequency in the OTA-C version can be controlled by the pole-frequency of the first-order all-pass filters but only the pole-Q needs to be controllable. The OTA-C filter derived from Fig. 3.27a is presented in Fig. 3.27b. Note that $K_1 = G_{mb}/(G_{ma} + G_{mb})$. The pole-$Q$

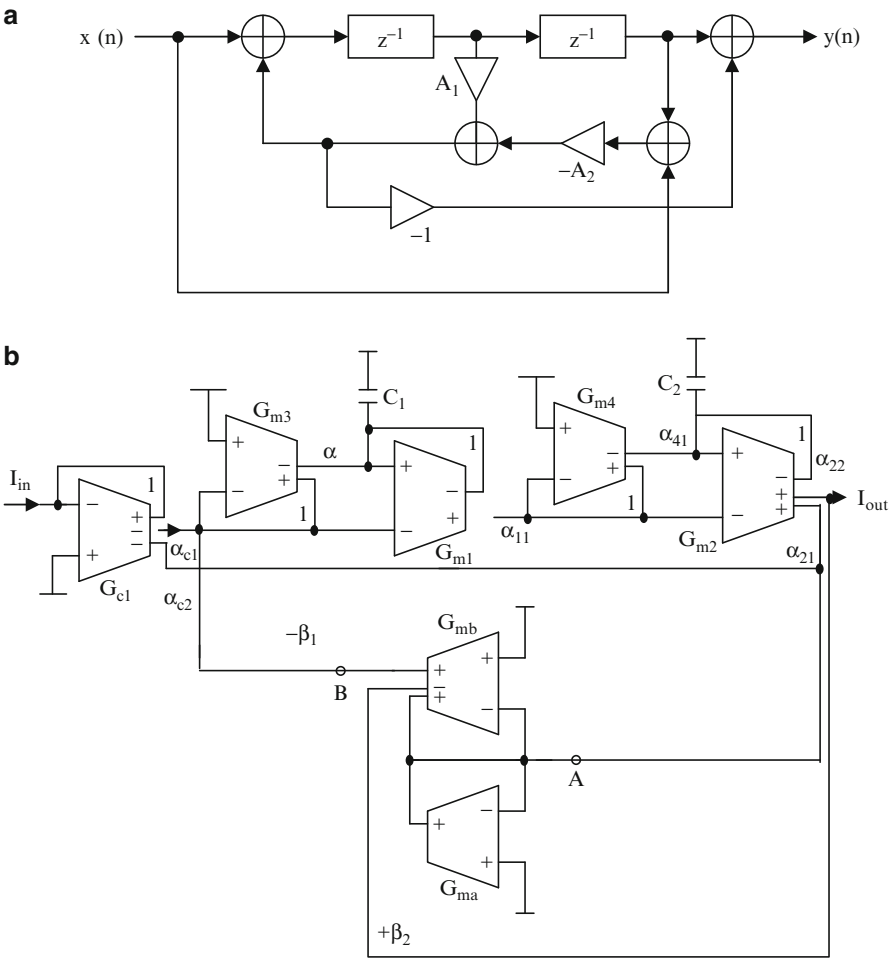


Fig. 3.26 (**a**) Mitra and Hirano Type 2 second-order digital all-pass filter structure (Adapted from [3.34]©IEEE 1974), and (**b**) second-order OTA-C all-pass filter derived from (**a**) choosing $A_1 = 0$ (Adapted from [3.32]©IET 2010)

realized and the pole-Q sensitivity are described in this case as well by (3.47c). It may be mentioned that essentially the Gray and Markel filter of Fig. 3.27a uses two all-pass filters of transfer functions z^{-1} and $\dfrac{A_1 + z^{-1}}{1 + A_1\, z^{-1}}$ and the use of bilinear transformation yields first-order all-pass filters of different pole frequencies which is of no advantage in OTA-C filters. As such identical first-order OTA-C all-pass filters have been used. Hence, the architecture is of interest in the way the numerator of the second-order all-pass filter is realized sharing the multiplier used in the realization of the denominator.

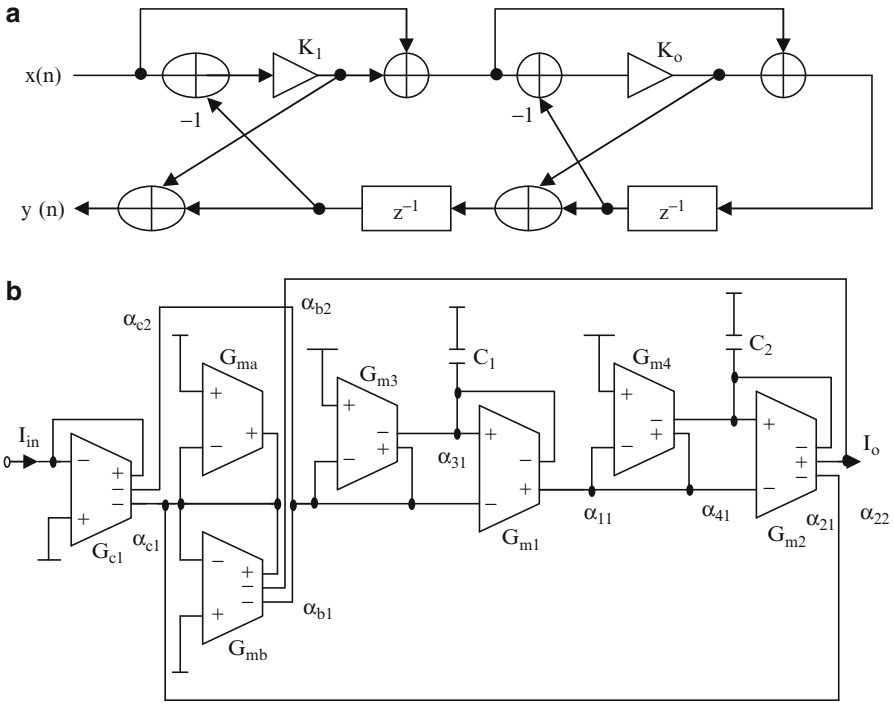


Fig. 3.27 (**a**) Gray and Markel second-order all-pass digital filter structure (Adapted from [3.35] ©IEEE 1973) and (**b**) OTA-C second-order all-pass filter derived from (**a**) (Adapted from [3.32] ©IET 2010)

3.6 High-Order OTA-C Filters

High-order OTA-C filters can be realized using a cascade technique in which the previously considered first- and second-order biquads can be used appropriately by taking into account the loading considerations. High input impedance will be required to facilitate such cascading of voltage-mode OTA-C filters. Current-input current-ouput type OT-C filters also can be easily cascaded. On the other hand, high-order filters can be realized based on operational or component simulation of LC ladders or multiple-loop feedback techniques. These are considered next.

3.6.1 Inductance Simulation Using OTAs

A circuit for floating inductance simulation [3.36] is presented in Fig. 3.28a. The principle of operation is as follows. The input voltage $(V_A - V_B)$ is converted into a current of value $G_{m1}(V_A - V_B)$ and integrated on a capacitor C to develop a voltage

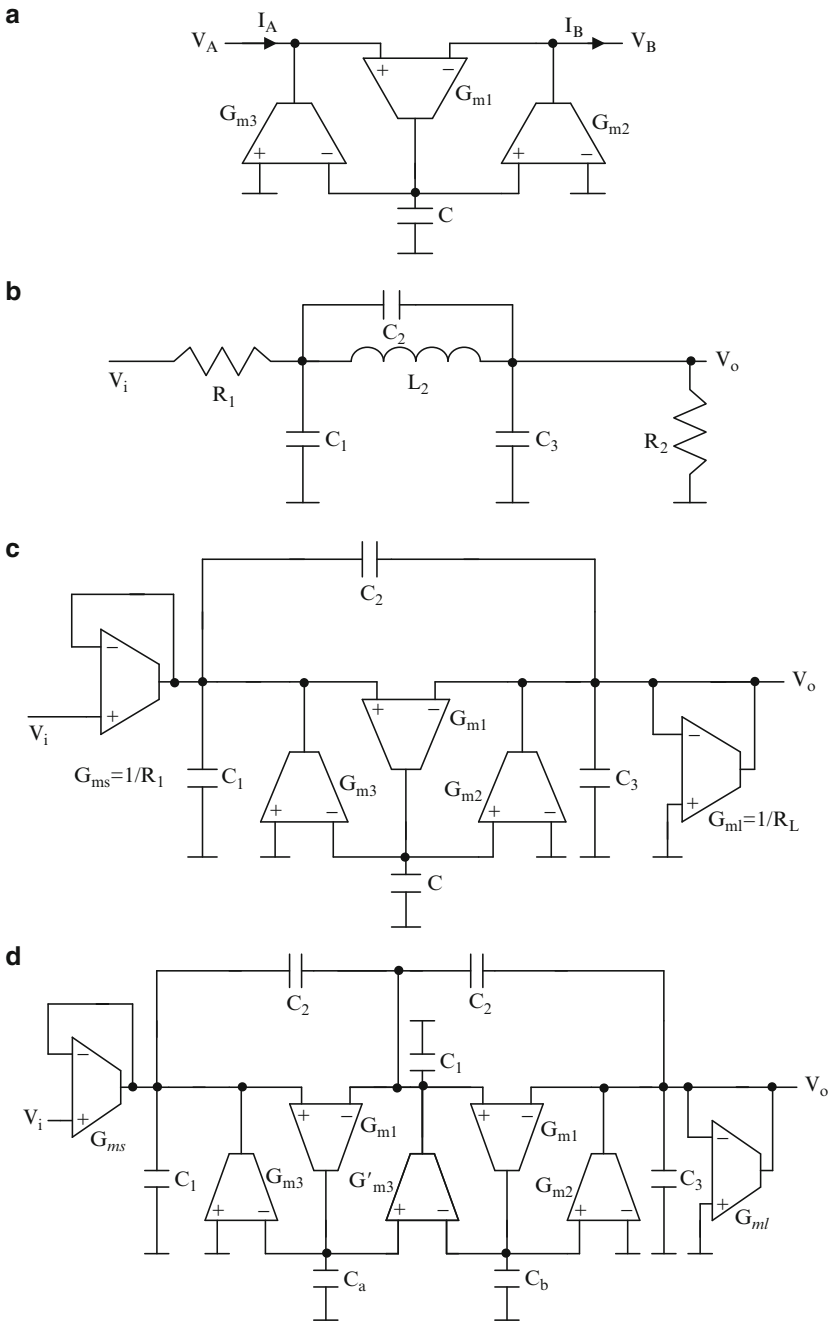


Fig. 3.28 (**a**) OTA-based floating lossless inductance, (**b**) third-order prototype elliptic low-pass filter, (**c**) OTA-C filter derived from (**b** using (**a**), (**d**) fifth-order OTA-C filter derived from a RLC prototype, (**e**) floating resonator simulation using OTAs (Adapted from [3.36] ©IEEE 1991), (**f**) equivalent ciruit of (**e**), (**g**) floating FDNR simulation using OTA (Adapted from [3.37] ©IEE 1998) and (**h**) third-order low-pass filter using FDNRs

$G_{m1}(V_A - V_B)/(sC)$. This voltage is converted into two currents I_A and I_B using two OTAs G_{m2} and G_{m3}. These currents evidently are $I_A = -I_B = \frac{g_{m1}\, g_{m2}\,(V_A - V_B)}{sC}$. Effectively, thus an inductance of value $\frac{C}{g_{m1}\, g_{m2}}$ is realized. If one desires a grounded inductance, it can be easily obtained by grounding terminal B. In this case, OTA G_{m2} is not needed and hence can be deleted. Note that the parasitic capacitances at the outputs of the OTAs affect the realized impedance. Specifically, considering the output resistance and capacitance to ground of OTA G_{m1}, the output capacitance C_p adds to the existing capacitance C and thus the inductance value changes to $\frac{(C + C_p)}{g_{m1}\, g_{m2}}$. The effect of finite R_o is to introduce a resistance of value $\frac{1}{R_o\, g_{m1}\, g_{m2}}$ in series with the realized inductance. The output parasitics of the OTAs G_{m2} and G_{m3} and input parasitics of OTA G_{m1} will be directly across the ports A and B to ground and these need to be controlled by proper layout or can be absorbed if resistance and capacitance exist to ground at these nodes in the circuit.

3.6.2 *Voltage-Mode OTA-C Filters Derived from RLC Ladder Filters Using Component Simulation*

The OTA-based floating inductance of Fig. 3.28a can be used to obtain voltage-mode OTA-C filters from prototype RLC ladder filters. As an illustration, a prototype elliptic low-pass ladder filter is presented in Fig. 3.28b. The corresponding OTA-C filter obtained by substituting the floating inductance of Fig. 3.28a in place of the inductance L and OTA-C based resistances for the terminating resistances R_1 and R_2 is shown in Fig. 3.28c. Note that these circuits invariably have parasitic capacitances at various nodes (inputs and outputs of the OTAs) and these can be absorbed in the shunt capacitances in the case of low-pass filters as mentioned before. In the case of high-order filters, the adjacent OTAs can be shared between floating inductances, by lifting the (previously) grounded input of the OTAs to feed another input from the neighboring OTA. As an illustration an OTA-C filter based on a fifth-order low-pass filter is presented in Fig. 3.28d, in which the OTA G'_{m3} is shared between adjacent floating inductances.

The implementation of Fig. 3.28c uses a floating capacitor. It is preferable to use circuits with grounded capacitors. Interestingly, the floating capacitors can be realized using the grounded inductance simulation circuit by replacing the grounded capacitor with a grounded inductance. This inductance can be simulated using OTAs and grounded capacitors. Instead of separately using a floating capacitor and floating inductance in parallel, the simulation of the floating tank circuit can be done using the circuit of Fig. 3.28e. The resulting equivalent circuit of the floating tank circuit is shown in Fig. 3.28f.

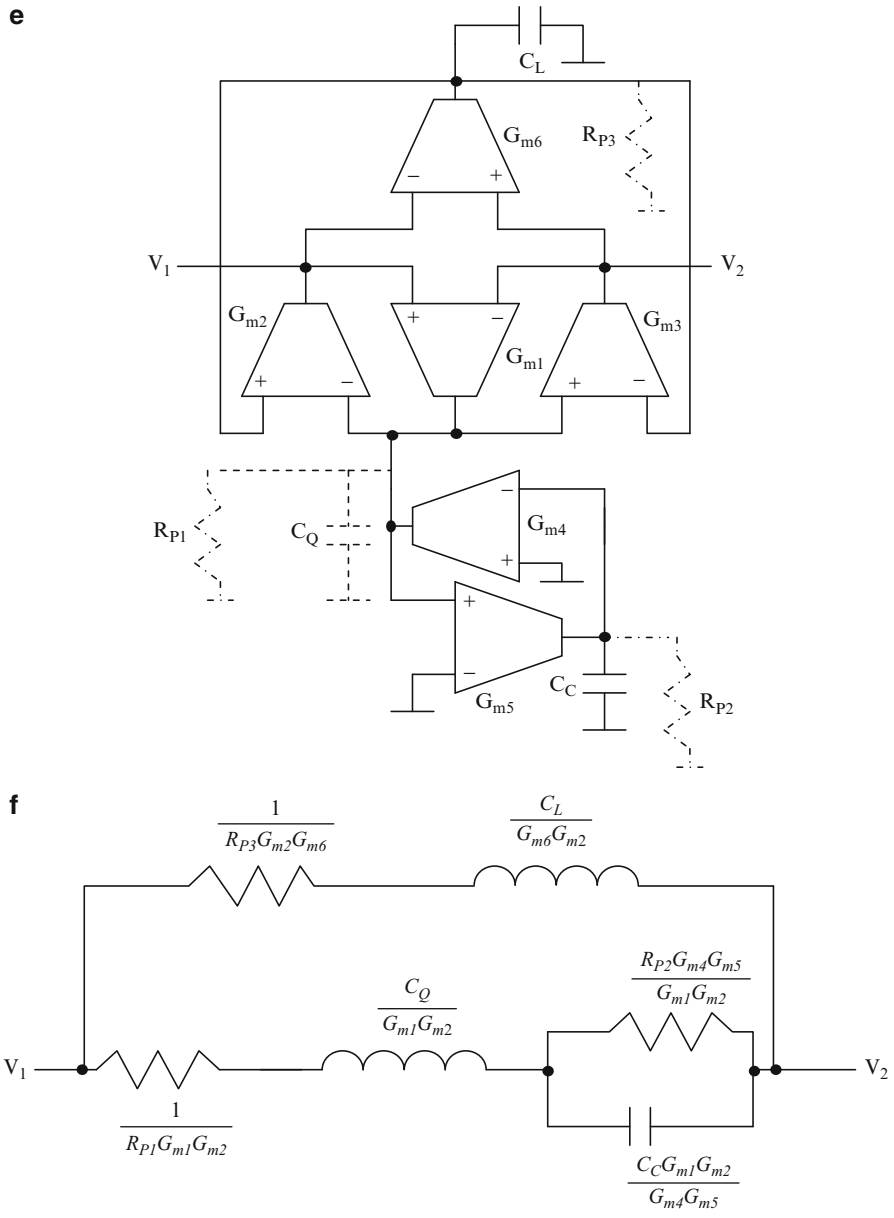


Fig. 3.28 (continued)

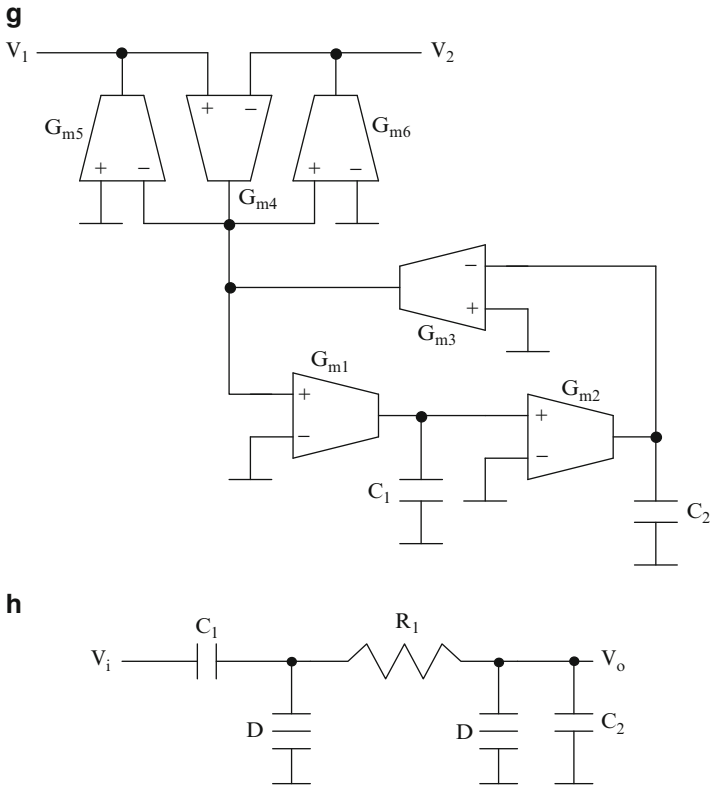


Fig. 3.28 (continued)

Sun [3.37] has described realization of FDNR (frequency dependent negative resistance) simulation based on OTAs and grounded capacitors. This circuit, shown in Fig. 3.28g, once again is based on the inductance simulation scheme of Fig. 3.28a in which in place of the grounded capacitance, an impedance of value $\frac{s^2\, G_{m1}\, G_{m2}}{C_1\, C_2}$ realized using three OTAs and two grounded capacitors is employed. The value of the realized FDNR is $\frac{G_{m1}\, G_{m2}}{-\omega^2\, C_1\, C_2\, G_{m4}\, G_{m5}}$. A grounded FDNR can be obtained by grounding the terminal V_2 and deleting the OTA G_{m6}. A third-order low-pass filter using two such grounded super-capacitances is shown in Fig. 3.28h. Note, however, the circuit is quite complicated compared to the OTA-C filter of Fig. 3.28c without capacitor C_2.

3.6.3 Table-Based Linear Transformation Type OTA-C Filters Based on Ladder Filters

Hwang, Liu, Wu, and Wu [3.39] have described a table-based substitution method for obtaining OTA-C filters from LC filters. This is based on a technique known as linear transformation which was described for active RC filters by Dimopoulos and Constantinides [3.38]. In this technique, the given RLC prototype is first divided into sections comprising shunt and series arms. The ith two-port sections are usually described by port voltage V_i and port currents I_i. These are transformed into new variables x_i and y_i through multiplication by a matrix:

$$\begin{bmatrix} x_{1i} \\ y_{1i} \end{bmatrix} = \begin{bmatrix} \alpha_{1i} & \beta_{i1} \\ \gamma_{i1} & \delta_{1i} \end{bmatrix} \begin{bmatrix} V_{i1} \\ I_{i1} \end{bmatrix} \tag{3.50a}$$

In a similar manner, the other port voltage and current also can be defined as

$$\begin{bmatrix} x_{2i} \\ y_{2i} \end{bmatrix} = \begin{bmatrix} \alpha_{2i} & \beta_{2i} \\ \gamma_{2i} & \delta_{2i} \end{bmatrix} \begin{bmatrix} V_{2i} \\ I_{2i} \end{bmatrix} = \Im_{2i} \begin{bmatrix} V_{2i} \\ I_{2i} \end{bmatrix} \tag{3.50b}$$

It is easy to see that x_1, y_1, x_2, and y_2 can be related through the ABCD matrix of the network relating V_{1i}, I_{1i}, V_{2i}, and I_{2i} as

$$\begin{bmatrix} x_{1i} \\ y_{1i} \end{bmatrix} = \begin{bmatrix} \alpha_{1i} & \beta_{1i} \\ \gamma_{1i} & \delta_{1i} \end{bmatrix} \begin{bmatrix} A_1 & B_1 \\ C_1 & D_1 \end{bmatrix} \Im_{2i}^{-1} \begin{bmatrix} x_{2i} \\ y_{2i} \end{bmatrix} = \begin{bmatrix} a_i & b_i \\ c_i & d_i \end{bmatrix} \begin{bmatrix} x_{2i} \\ y_{2i} \end{bmatrix} \tag{3.50c}$$

where

$$a_i = \frac{1}{\Delta_i}\left[\alpha_{1i}\left(\delta_{2i}\, A_i - \gamma_{2i}\, B_i\right) + \beta_{1i}\left(\delta_{2i}\, C_i - \gamma_{2i}\, D_i\right)\right]$$

$$b_i = \frac{1}{\Delta_i}\left[\alpha_{1i}\left(\alpha_{2i}\, B_i - \beta_{2i}\, A_i\right) + \beta_{1i}\left(\alpha_{2i}\, D_i - \beta_{2i}\, C_i\right)\right]$$

$$c_i = \frac{1}{\Delta_i}\left[\gamma_{1i}\left(\delta_{2i}\, A_i - \gamma_{2i}\, B_i\right) + \delta_{1i}\left(\delta_{2i}\, C_i - \gamma_{2i}\, D_i\right)\right]$$

$$a_i = \frac{1}{\Delta_i}\left[\gamma_{1i}\left(\alpha_{2i}\, B_i - \beta_{2i}\, A_i\right) + \delta_{1i}\left(\alpha_{2i}\, D_i - \beta_{2i}\, C_i\right)\right] \tag{3.50d}$$

where $\Delta_i = \alpha_{2i}\ \delta_{2i} - \beta_{2i}\ \gamma_{2i}$. Furthermore, $[y_{1i}\ \ y_{2i}]^T$ can be easily obtained from $[x_{1i}\ \ x_{2i}]^T$.

It may be noted that α and γ are dimensionless wheras β and δ have dimensions of impedance, making x and y have dimensions of voltages and consequently a, b, c, and d are dimensionless ratios.

Next, it is to be noted that the cascade connection of two ports imposes a constraint:

$$\begin{bmatrix} V_{12} \\ I_{12} \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & -1 \end{bmatrix} \begin{bmatrix} V_{21} \\ I_{21} \end{bmatrix} \tag{3.50e}$$

It is required to choose the transformation matrices appropriately so that simple structures can be obtained and the constraint can be seen to result in cross connection of two adjacent ports. Note also that the source and load terminations are described as

$$[1 \; R_s] \begin{bmatrix} V_{11} \\ I_{11} \end{bmatrix} = [1 \; R_s] \, \mathfrak{S}_{11}^{-1} \begin{bmatrix} x_{11} \\ y_{11} \end{bmatrix} = E \tag{3.50f}$$

and

$$[1 \; R_s] \, \mathfrak{S}_{2n}^{-1} \begin{bmatrix} x_{2n} \\ y_{2n} \end{bmatrix} = 0 \tag{3.50g}$$

The reader is urged to refer to [3.38] for a detailed discussion.

The application of this technique to OTA-C filters results in the equivalences of Fig. 3.29 which consist of the equivalent OTA-C subcircuits corresponding to the usually needed series and shunt arms in ladder filters. Starting with the prototype, after sectioning the circuit, look-up from these tables yields corresponding OTA-C sections. These need to be cross-connected to obtain the final circuit.

As an illustration, consider the third-order all-pole low-pass filter of Fig. 3.30a. The corresponding OTA-C filter is as shown in Fig. 3.30b. This circuit needs only four OTAs. On the other hand, the circuit obtained by substituting the floating inductance simulation circuit of Fig. 3.28a needs five OTAs. Consider next the third-order elliptic low-pass filter of Fig. 3.28b for which the corresponding table-based transformation using Fig. 3.29 yields the OTA-C filter of Fig. 3.30b. Evidently, this circuit needs only seven OTAs as against eight needed in the component simulation-based circuit of Fig. 3.28e.

It is possible to derive the circuits obtained by table-based transformation in an alternative way without involving the theory of linear transformation. This uses the observation that the series components of impedance Z need to be considered as fed with the voltage $(V_1 - V_2)$ and create a current I to be given to the adjacent sections on either side. Thus, a floating inductance L will develop the relationship $I_1 R = \dfrac{V_1 - V_2}{sL}$. In the case of the shunt arm of impedance Z_i, the input current I_{ini}, output current I_{outi}, and the impedance Z_i and the port voltage V_i are related for a shunt capacitor as $V_i = \dfrac{I_{ini} - I_{outi}}{sC}$. In the case of source E and a RC network

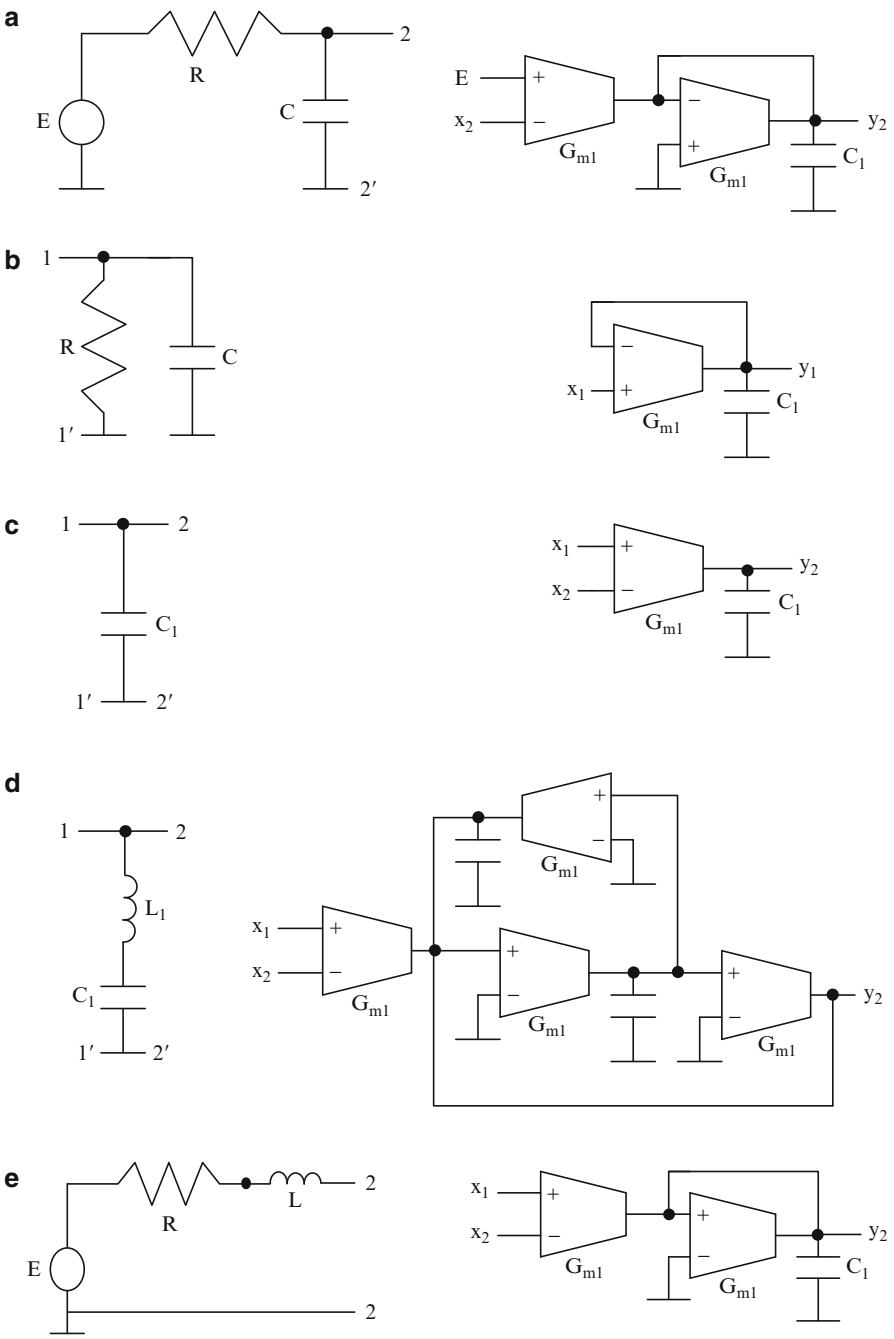


Fig. 3.29 Tables used in table-based simulation of ladde filters due to Hwang, Liu, Wu, and Wu (Adapted from [3.39]©IET 1994)

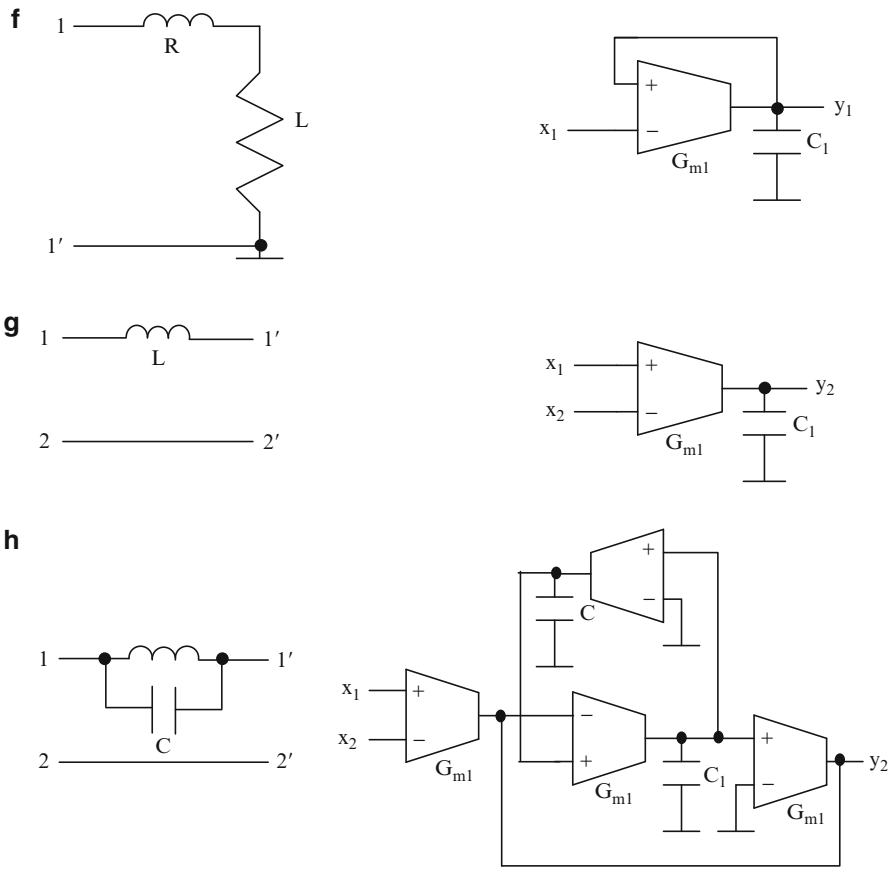


Fig. 3.29 (continued)

(see Fig. 3.29a), the output voltage is expressed in terms of E and current i fed by the next branch as

$$V_1 = \frac{E - iR}{1 + sCR} \tag{3.51}$$

In summary, the series arms convert differential voltages across the terminals to current whereas the shunt arms convert differential currents into voltage. The interesting point is that in the derivation of active RC filters from low-pass elliptic filters, we have modeled the circuit as an all-pole filter together with cross-connecting capacitors being used to realize the transmission zeroes. Thus the inductor currents are state variables (inverted, i.e., of opposite sign) and capacitor voltages are also state variables realized at the outputs of integrator blocks. On the other hand, in LT filters, the complete branch currents and node voltages are

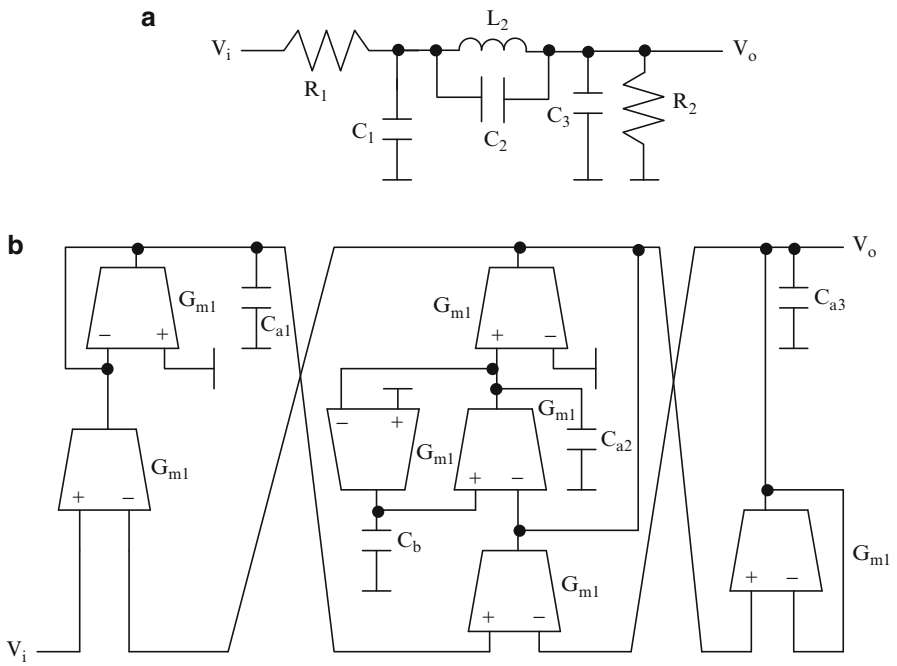


Fig. 3.30 (**a**) A prototype third-order elliptic low-pass RLC ladder filter, (**b**) OTA-C filter obtained by table-based simulation (Adapted from [3.39]©IEE 1994)

obtained. Another difference is that in the operational simulation of leap-frog ladder filters to obtain active RC filters, the node voltages realized are negatives of those in the prototype. On the other hand, in the case of table-based simulation, all the node voltages realized are the same as in the protype.

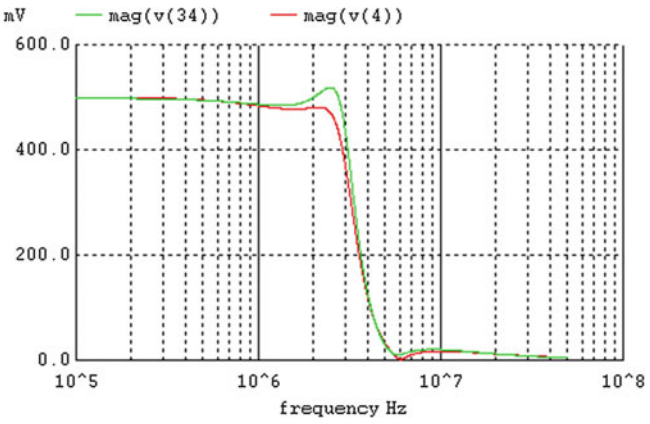
Note that circuit derivation may lead to complicated circuits in some cases. For instance, realization of a source series arm of R in series with C as needed in all-pole high-pass filters will be quite difficult.

Example 3.3 The third-order elliptic low-pass filter of Hwang, Liu, Wu, and Wu [3.39] is considered. WINSPICE simulation results using the OTA macromodel and Tsukutani CMOS OTA of Fig. E.3.2b are shown. Note that the OTAs have fixed transconductance of 157 μS. The circuit inductance and capacitance are first-impedance scaled accordingly and then frequency scaled. The effect of actual OTA nonidealities results in peaking in the frequency response. Dual ouput OTA is used, therefore the unused current ouputs are resistively terminated.

```
*Third order Elliptic OTA C filter of Hwang, Liu, Wu and Wu
G1 10 0 8 5 .000157S
G2 10 0 0 10 .000157S
C4 10 0 15.3436pf
C5 4 0 8.9084pf
```

```
G3 5 0 10 4 .000157S
C6 7 0 9.16408pf
C7 6 0 1.87910pf
G7 4 0 5 4 .000157S
G6 5 0 6 0 .000157S
G5 7 0 0 6 .000157S
G4 6 0 7 5 .000157S
vin1 8 0 ac 1v
.ac dec 100 1k 5000k
*Using Tsukutani OTA
C14 40 0 15.2356pf
C15 34 0 8.9084pf
C16 37 0 9.164090pf
c17 36 0 1.87910pf
x1 vdd vss Ibias1 8 35 40 NC1 doota
Ibias1 Ibias1 vss DC 100u
x2 vdd vss Ibias2 0 40 40 NC2 doota
Ibias2 Ibias2 vss DC 100u
x3 vdd vss Ibias3 40 34 35 NC3 doota
Ibias3 Ibias3 vss DC 100u
x4 vdd vss Ibias4 37 35 36 NC4 doota
Ibias4 Ibias4 vss DC 100u
x5 vdd vss Ibias5 0 36 37 NC5 doota
Ibias5 Ibias5 vss DC 100u
x6 vdd vss Ibias6 36 0 35 NC6 doota
Ibias6 Ibias6 vss DC 100u
x7 vdd vss Ibias7 35 34 34 NC7 doota
Ibias7 Ibias7 vss DC 100u
R11 Nc1 0 1000K
R12 NC2 0 1000K
R13 NC3 0 1000K
R14 NC4 0 1000K
R15 Nc1 0 1000K
R16 NC2 0 1000K
R17 NC3 0 1000K
vdd vdd 0 DC 2
vss vss 0 DC -2
.AC DEC 1000 100K 50000K
.subckt doota vdd vss Ibias vinp vinm iop iom
.PARAM ln=2um,wn=4um
.PARAM lp=2um, wp=4um
M1 3 vinm Ibias vss CMOSN w={wn} l={ln}
M2 4 vinp Ibias vss CMOSN w={wn} l={ln}
M5 iom 3 vdd vdd CMOSP w={wp} l={lp}
M6 5 3 vdd vdd CMOSP w={wp} l={lp}
```

```
M7 3 3 vdd vdd CMOSP w={wp} l={lp}
M8 4 4 vdd vdd CMOSP w={wp} l={lp}
M9 iop 4 vdd vdd CMOSP w={wp} l={lp}
M10 6 4 vdd vdd CMOSP w={wp} l={lp}
M12 5 5 vss vss CMOSN w={wn} l={ln}
M13 iop 5 vss vss CMOSN w={wn} l={ln}
M14 iom 6 vss vss CMOSN w={wn} l={ln}
M15 6 6 vss vss CMOSN w={wn} l={ln}
.ends DOOTA
.MODEL CMOSN NMOS ( LEVEL = 3 PHI=0.700000 TOX=9.6000E-09
+ XJ=0.200000U TPG=1 VTO=0.6684 DELTA=1.0700E+00 LD=
  4.2030E-08
+ KP=1.7748E-04 UO=493.4 THETA=1.8120E-01 RSH=1.6680E+01
+ GAMMA=0.5382 NSUB=1.1290E+17 NFS=7.1500E+11 VMAX=
  2.7900E+05
+ ETA=1.8690E-02 KAPPA=1.6100E-01 CGDO=4.0920E-10 CGSO=
  4.0920E-10
+ CGBO=3.7765E-10 CJ=5.9000E-04 MJ=0.76700 CJSW= 2.0000E-11
+ MJSW=0.71000 PB=0.990000)
.MODEL CMOSP PMOS ( LEVEL = 3 PHI=0.700000 TOX=9.6000E-09
+ XJ=0.200000U TPG=-1 VTO=-0.9352 DELTA=1.2380E-02 LD=
5.2440E-08
+ KP=4.4927E-05 UO=124.9 THETA=5.7490E-02 RSH=1.1660E+00
+ GAMMA=0.4551 NSUB=8.0710E+16 NFS=5.9080E+11 VMAX=
  2.2960E+05
+ ETA=2.1930E-02 KAPPA=9.3660E+00 CGDO=2.1260E-10 CGSO=
  2.1260E-10
+ CGBO=3.6890E-10 CJ=9.3400E-04 MJ=0.48300 CJSW= 2.5100E-10
+ MJSW=0.21200 PB=0.930000)
.end
```



3.6.4 Current-Mode OTA-C Filters Based on RLC Ladder Filters

Several current-mode techniques are available in the literature. All these generally avoid the use of floating capacitors in innovative ways. These are considered next.

3.6.4.1 Ramirez–Angulo and Sanchez–Sinencio Technique for Realizing Current-Mode Filters

We first consider the technique due to Ramirez–Angulo and Sanchez–Sinencio [3.40]. In this technique, first the equations at the various nodes in the prototype RLC low-pass filter shown in Fig. 3.31a can be written as follows.

$$V_1 = \left(\frac{V_s - V_1}{R_1} - I_2\right)\frac{1}{sC_1},\ I_2 = (V_1 - V_3)\frac{1}{sL_2},\ V_3 = (I_2 - I_4)\frac{1}{sC_3},$$
$$I_4 = (V_3 - V_5)\frac{1}{sL_4},\ V_5 = \left(I_4 - \frac{V_5}{R_2}\right)\frac{1}{sC_5} \tag{3.52}$$

A signal flow graph (SFG) realizing these equations is presented in Fig. 3.31b. From the SFG, the block diagram of Fig. 3.31c can be constructed easily. The voltages in the SFG can be considered to be scaled by a resistance to yield currents in the current-mode circuit. Note that the blocks shown $\frac{1}{sC_i}$ and $\frac{1}{sL_i}$ are OTA-C-based integrators of Fig. 3.31d with two current outputs. The transfer functions of these integrators are

$$\frac{I_{out}}{I_{in}} = \frac{G_m}{C'} \tag{3.53}$$

The current directions are as shown. It is thus very straightforward to plot the OTA-C filter from the block diagram. We can choose equal G_m s for all OTAs used in the integrators and then the capacitances will be related to those in the prototype through the relationship $C'_i = C_i G_m$ or $L_i G_m$. Of course, one can also choose equal capacitors and different G_m values as well.

It is possible to realize finite transmission zeroes, for example, needed in elliptic low-pass filters. As an illustration, a third-order low-pass filter with a pair of transmission zeroes is shown in Fig. 3.32a together with its simulation block diagram in Fig. 3.32b. The cross-coupling multiplier blocks C_2/C_1 and C_2/C_3 will

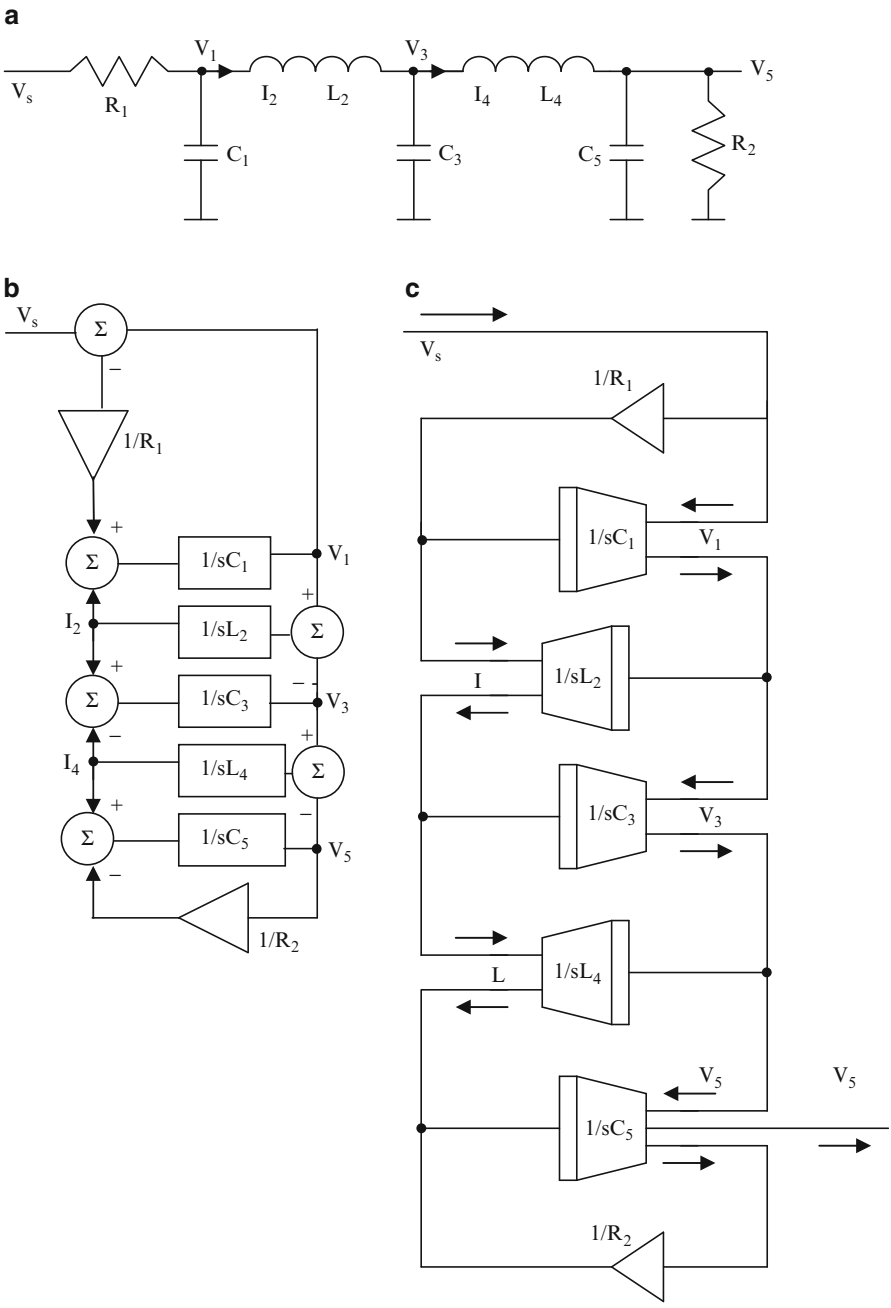


Fig. 3.31 (**a**) A protype fifth-order all-pole low-pass filter, (**b**) SFG describing (**a**), (**c**) block diagram of current-mode filter derived from (**b**), and (**d**) two blocks used in (**c**) (Adapted from [3.40]©IEEE1994)

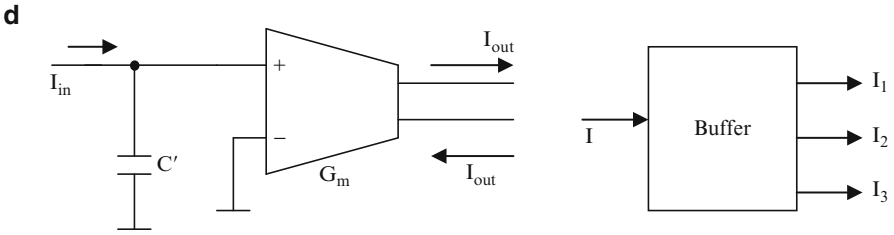


Fig. 3.31 (continued)

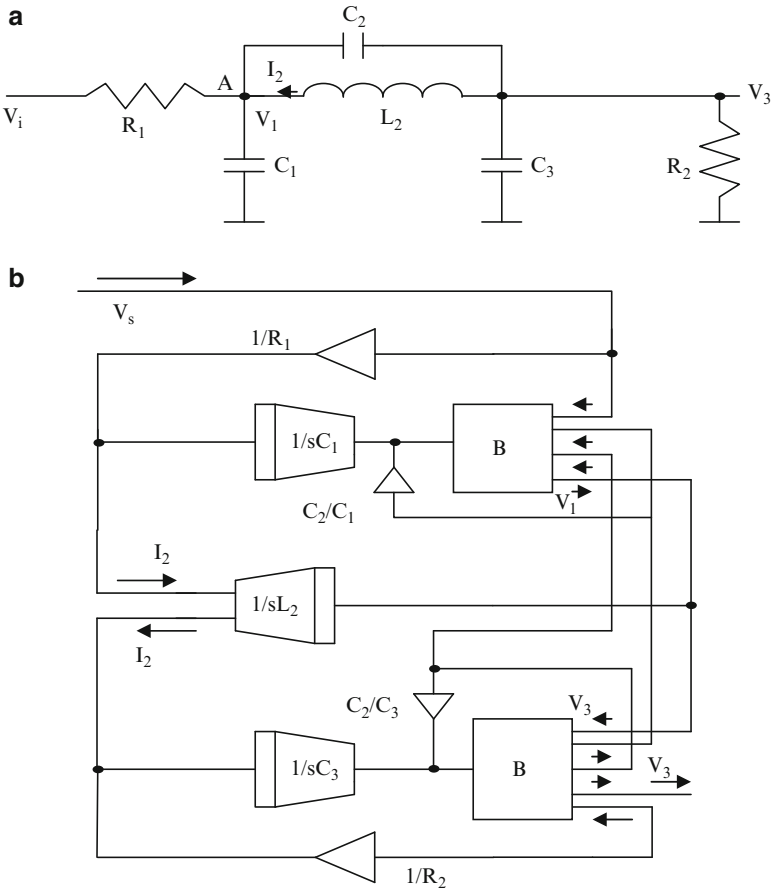


Fig. 3.32 (**a**) A prototype third-order elliptic low-pass filter and (**b**) a current-mode filter derived from (**b**) (Adapted from [3.40]©IEEE1994)

realize the transmission zeroes. This can be appreciated by writing the node equation at node A:

$$\frac{V_s - V_1}{R_1} + I_2 + (V_3 - V_1)sC_2 = V_1\, sC_1 \tag{3.54a}$$

which can be rewritten as

$$\left(\frac{V_s - V_1}{R_1} + I_2\right)\frac{1}{sC_1} + (V_3 - V_1)\frac{C_2}{C_1} = V_1 \tag{3.54b}$$

In the block diagram of Fig. 3.32b, the currents corresponding to V_3 and $-V_1$ are added by tying the current outputs and multiplying using a current mirror of gain C_2/C_1 and summed with the output current of the integrator block $(1/sC_1)$. Note that the block B is a single-input multiple-output current buffer (see Fig. 3.31d) which can be realized by an OTA connected as a resistor with multiple current outputs.

3.6.4.2 Wu and El-Masry Technique of Realizing Current-Mode OTA-C Filters

The second technique we consider next is due to Wu and El-Masry [3.6] which is based on coupled biquads. Wu and El-Masry have suggested two techniques based on mesh current simulation and branch current simulation. Consider the prototype general configuration of Fig. 3.33a redrawn for convenience from which using mesh current simulation, we wish to derive current-mode OTA-C filters. In each mesh, KVL (Kirchoff's voltage law) is applied. As an illustration, in the mesh with mesh current I_1, we have

$$I_{m1}\left(sL_2 + \frac{1}{sC_3} + R_1\right) - I_{in}\, R_1 - \frac{I_{m2}}{sC_3} = 0 \tag{3.55a}$$

which can be manipulated to yield

$$I_{m1}\, D(s) = I_{in}\left(\frac{sR_1}{L_2}\right) + \frac{I_{m2}}{L_2\, C_3} \tag{3.55b}$$

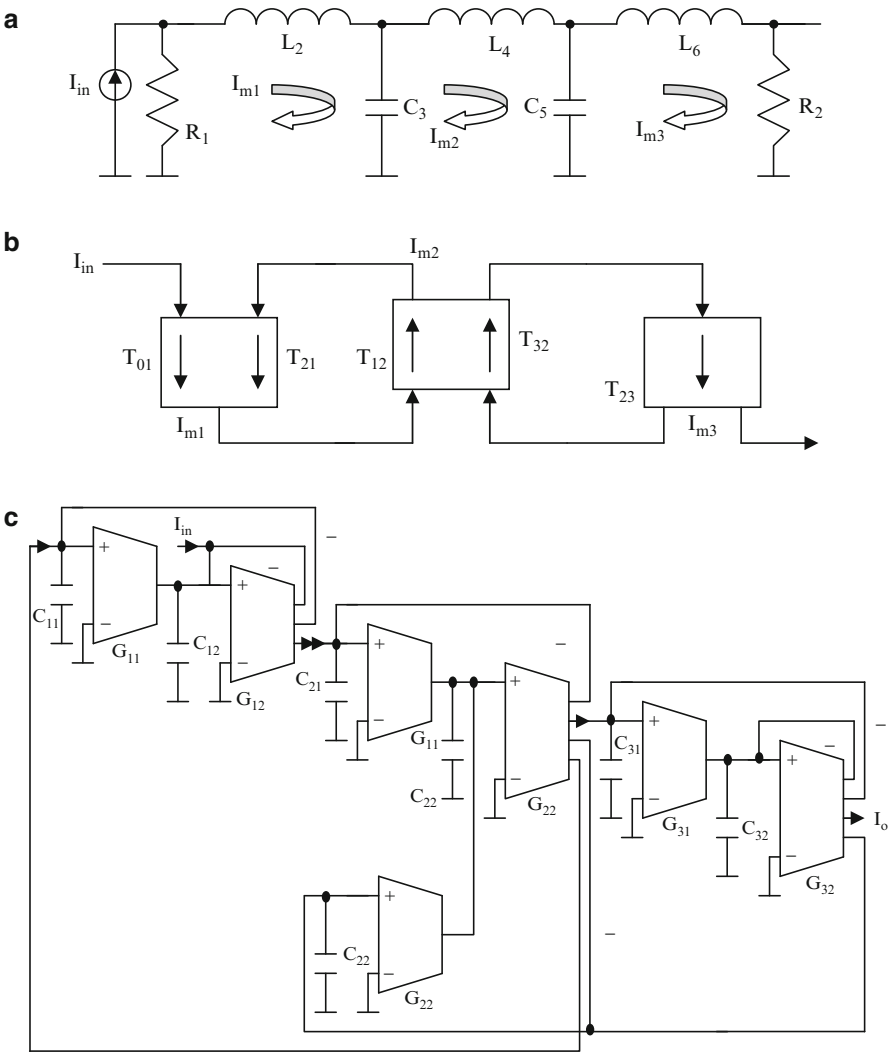


Fig. 3.33 (**a**) A protype RLC filter, (**b**) coupled biquad-based equivalent derived by mesh current simulation from (**a**), and (**c**) OTA-C filter derived from (**b**) ((**a**) and (**c**) adapted from [3.6] ©IEEE1998)

where $D(s) = \left(s^2 + \frac{sR_1}{L_2} + \frac{1}{L_2\,C_3}\right)$

This leads to the block diagram of Fig. 3.33b where there are two transfer functions from each mesh current to the neighboring mesh currents. The two transfer functions corresponding to (3.55a) can be seen in the first two equations

in (3.56) which share the same poles and have different numerators. The remaining transfer functions also are presented the first two equations in (3.56):

$$
\begin{aligned}
T_{01}D_1(s) &= \frac{I_1}{I_{in}}D_1(s) = s\left(\frac{R_1}{L_2}\right) \quad \text{when } i_2 = 0,\ D_1(s) = s^2 + s\frac{R_1}{L_2} + \frac{1}{L_2C_3} \\
T_{21}D_1(s) &= \frac{I_1}{I_2}D_1(s) = \frac{1}{L_2C_3} \quad \text{when } i_{in} = 0. \\
T_{12}D_2(s) &= \frac{I_2}{I_1}D_2(s) = \frac{1}{L_4C_3} \quad \text{when } i_3 = 0,\ D_2(S) = s^2 + \frac{1}{L_4C_{3,5}} \\
T_{32}D_2(s) &= \frac{I_2}{I_3}D_2(s) = \frac{1}{L_4C_5} \quad \text{when } i_1 = 0. \\
T_{23}D_3(s) &= \frac{I_3}{I_2}D_3(s) = \frac{1}{L_6C_5},\ D_3(s) = s^2 + s\frac{R_2}{L_6} + \frac{1}{L_6C_5}
\end{aligned}
\tag{3.56}
$$

where $C_{3,5}$ is the total capacitance of the second loop.

Thus, three current-mode biquads will be needed with low-pass and band-pass current transfer functions as shown in the block diagram of Fig. 3.33b. One of these biquads also needs to realize infinite pole-Q. Earlier we studied Wu and El-Masry [3.6] OTA-C biquads (see Fig. 3.19a, b) which can realize low-pass as well as band-pass transfer functions. Employing these, (3.56) can be easily realized as shown in Fig. 3.33c.

We next consider the realization of low-pass filters with transmission zeroes. Consider the third-order elliptic filter shown in Fig. 3.34a for which following the same procedure, we obtain the current-mode OTA-C filter of Fig. 3.34b. The various transfer functions are:

$$
\begin{aligned}
T_{01} &= \frac{I_1}{I_{in}} = \frac{s}{s + \frac{1}{R_1C_1}} \quad \text{when } i_2 = 0, \\
T_{21} &= \frac{I_1}{I_2} = \frac{\frac{1}{R_1C_1}}{s + \frac{1}{R_1C_1}} \quad \text{when } i_{in} = 0 \\
T_{12} &= \frac{I_2}{I_1} = K_1 = \frac{C_{22}}{C_1} \quad \text{when } I' = I_3 = 0, \\
T_{22} &= \frac{I_2}{I_2} = K_2 = \frac{C_{22}}{C_2} \quad \text{when } I_1 = I_3 = 0 \\
T_{32} &= \frac{I_2}{I_3} = K_3 = \frac{C_{22}}{C_3} \quad \text{when } i_1 = i_2 = 0 \\
\text{where } \frac{1}{C_{22}} &= \frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3} \text{ and note that } k_1 + k_2 + k_3 = 1. \\
T_{22} &= \frac{I'_2}{I_2} = \frac{\frac{1}{L_2C_2}}{s^2 + \frac{1}{L_2C_2}},\ T_{23} = \frac{I_3}{I_2} = \frac{\frac{1}{R_2C_3}}{s + \frac{1}{R_2C_3}}
\end{aligned}
\tag{3.57}
$$

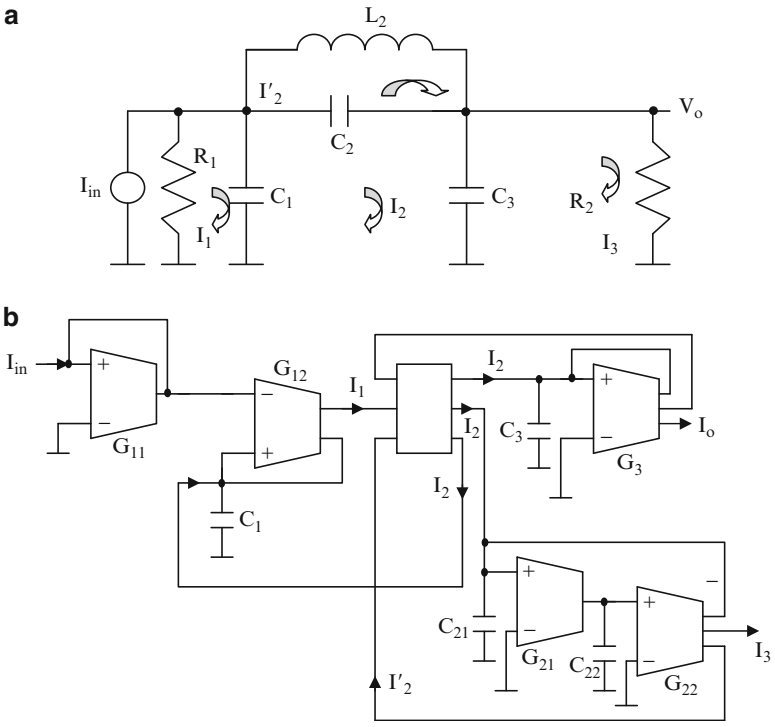


Fig. 3.34 (**a**) Third-order low-pass filter prototype with transmission zeroes, and (**b**) current-mode OTA-C filter derived from (**a**) based on mesh current simulation ((**b**) Adapted from [3.6] ©IEEE 1998)

The advantage of the structure is that T_{12}, T_{22}, T_{32} need simple current amplifiers since the mesh has only one type of circuit elements: capacitors.

We next consider the realization of a sixth-order band-pass filter shown in Fig. 3.35a. In this case, we employ the branch current simulation technique. The equations to be realized can be easily written as follows.

$$I_{in} - I_2 = \frac{V_1}{R_1},\ I_2 = \frac{V_1 - V_2}{sL_2 + \frac{1}{sC_2}},\ V_2 = \frac{(I_2 - I_4)}{sC_3 + \frac{1}{sL_3}},\ I_4 = \frac{V_2 - V_o}{sL_4 + \frac{1}{sC_4}},\ I_4\, R_2 = V_o \tag{3.58}$$

These transfer functions can be realized using three biquads as shown in the complete circuit of Fig. 3.35b. In the above synthesis, the voltages are considered

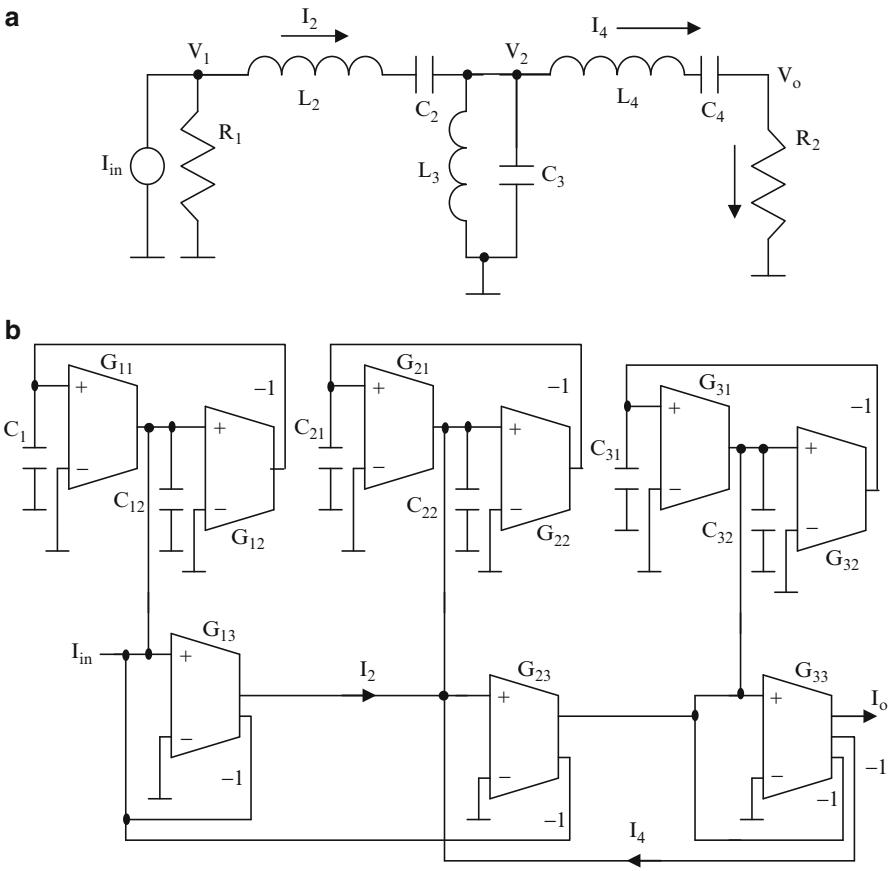


Fig. 3.35 (**a**) A prototype sixth-order band-pass filter, and (**b**) OTA-C filter derived from (**a**) using branch current siulation ((**b**) Adapted from [3.6] ©IEEE 1998)

as currents through a scaling resistance. On the other hand, different scaling factors can also be used to obtain different final filter circuits.

3.7 Multiple-Feedback-Type OTA-C Filters

Sun and Fidler [3.41] have suggested the realization of high-order filters using grounded capacitors and OTAs with one input connected to a grounded capacitor. The general configuration for a fourth-order filter is presented in Fig. 3.36a.

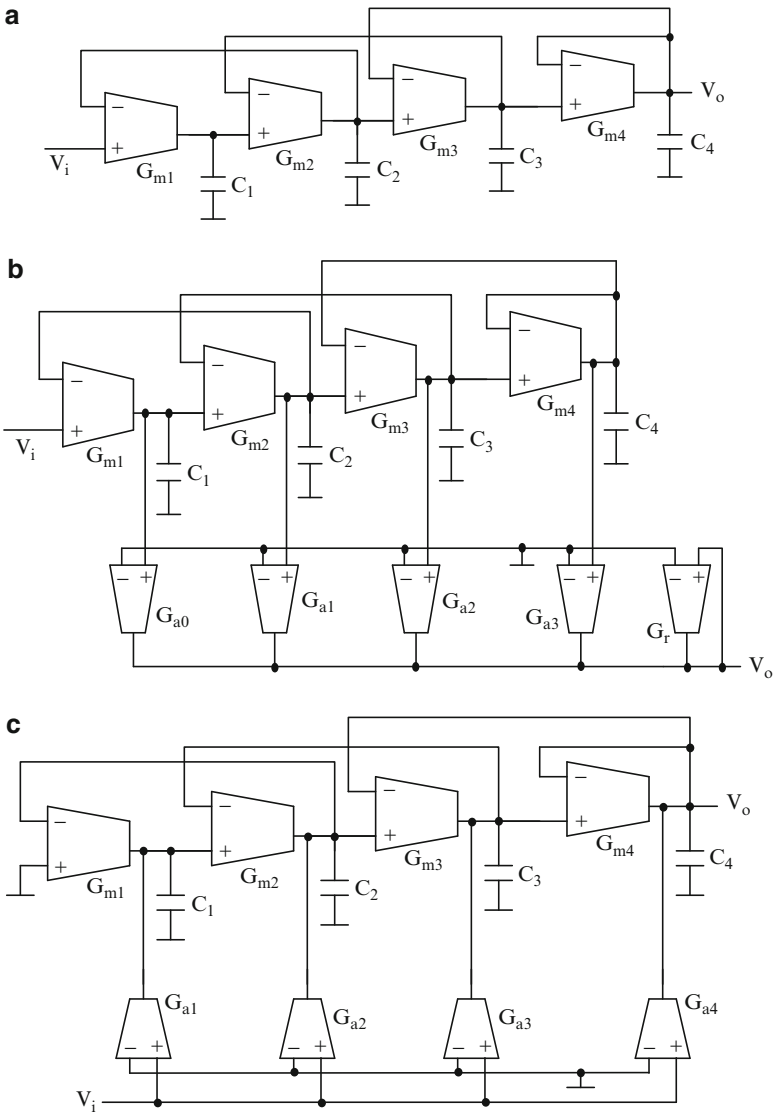


Fig. 3.36 (**a**) A multiple feedback all-pole OTA-C filter, (**b**) realization of transmission zeroes by output summation, and (**c**) realization of transmission zeroes by input distribution (Adapted from [3.41]©IEEE 1997)

Note that the inverting input of each OTA can be connected to the outputs of other OTAs to the right. Thus, several options are possible. Denoting the connection between the *i*th OTA input to the other outputs by a function f_{ij} (i.e., with $j > i$), the general transfer function can be written as

$$H(s) = 1/(s^4\tau_1\ \tau_2\ \tau_3\ \tau_4 + s^3(\tau_1\ \tau_2\ \tau_3 f_{44} + \tau_4\ \tau_1\ \tau_2 f_{33} + \tau_3\ \tau_4\ \tau_1 f_{22} + \tau_2\ \tau_3\ \tau_4 f_{11}) + s^2(\tau_1\ \tau_2(f_{33}f_{44} + f_{34}) + \tau_1\ \tau_3 f_{22} f_{44} + \tau_1\ \tau_4(f_{22}f_{33} + f_{23}) + \tau_2\ \tau_3 f_{11} f_{44} + \tau_2\ \tau_4 f_{33} f_{11} + \tau_3\ \tau_4(f_{11}f_{22} + f_{12})) + s(\tau_1(f_{22}f_{33}f_{44} + f_{22}f_{34} + f_{23}f_{44} + f_{24}) + \tau_2(f_{11}f_{33}f_{44} + f_{11}f_{34}) + \tau_3(f_{11}f_{22}f_{44} + f_{12}f_{44}) + \tau_4(f_{11}f_{22}f_{33} + f_{11}f_{23} + f_{12}f_{33} + f_{13})) + f_{11}f_{22}f_{33}f_{44} + f_{11}f_{22}f_{34} + f_{11}f_{44}f_{23} + f_{12}f_{33}f_{44} + f_{11}f_{24} + f_{13}f_{44} + f_{12}f_{34} + f_{14}) \tag{3.59a}$$

where we have defined $\tau_i = \frac{G_{mi}}{C_i}$. Of the 24 configurations possible, only 9 are suitable for realizing all-pole filters. One configuration yields a cascade of two second-order filters and three others do not give solutions for Butterworth and Chebychev approximations. The remaining structures degenerate to first-order filter cascaded by third-order filter or third-order filter cascaded by a first-order filter. As an illustration, the filter of Fig. 3.36a is defined by $f_{12} = 1, f_{23} = 1, f_{34} = 1, f_{44} = 1$ so that (3.59a) becomes

$$H(s) = 1\Big/(s^4\tau_1\ \tau_2\ \tau_3\ \tau_4 + s^3\ \tau_1\ \tau_2\ \tau_3 f_{44} + s^2(\tau_1\ \tau_2 f_{34} + \tau_1\ \tau_4 f_{23} + + \tau_3\ \tau_4 f_{12}) + s(\tau_1 f_{23} f_{44} + \tau_3 f_{12} f_{44})) + f_{12} f_{34}) = 1\Big/(s^4\tau_1\ \tau_2\ \tau_3\ \tau_4 + s^3\ \tau_1\ \tau_2\ \tau_3 + s^2(\tau_1\ \tau_2 + \tau_1\ \tau_4 + \tau_3\ \tau_4) + s(\tau_1 + \tau_3) + 1) \tag{3.59b}$$

Considering that a fourth-order Butterworth filter is desired with a denominator of transfer function given by

$$D(s) = s^4 + 2.61313\, s^3 + 3.41421\, s^2 + 2.61313\, s + 1$$

the various τ_i values can be found as

$\tau_1 = 1.53073$, $\tau_2 = 1.57716$, $\tau_3 = 1.08239$ and $\tau_4 = 0.382683$.

In some cases nonlinear equations need to be solved. The complete options for various f_{ij} are

(a) $f_{12} = f_{23} = f_{34} = f_{44} = 1$, (b) $f_{12} = f_{24} = f_{34} = f_{44} = 1$,
(c) $f_{13} = f_{22} = f_{34} = f_{44} = 1$, (d) $f_{13} = f_{23} = f_{34} = f_{44} = 1$,
(e) $f_{13} = f_{24} = f_{34} = f_{44} = 1$, (f) $f_{14} = f_{22} = f_{34} = f_{44} = 1$,
(g) $f_{14} = f_{23} = f_{33} = f_{44} = 1$, (h) $f_{14} = f_{23} = f_{34} = f_{44} = 1$,
(i) $f_{14} = f_{24} = f_{34} = f_{44} = 1$.

It is possible to realize the transmission zeroes of a high-order filter transfer function by using two techniques: output summation shown in Fig. 3.36b and input distribution shown in Fig. 3.36c using additional OTAs. Note, however, the synthesis is very cumbersome and hence is omitted here.

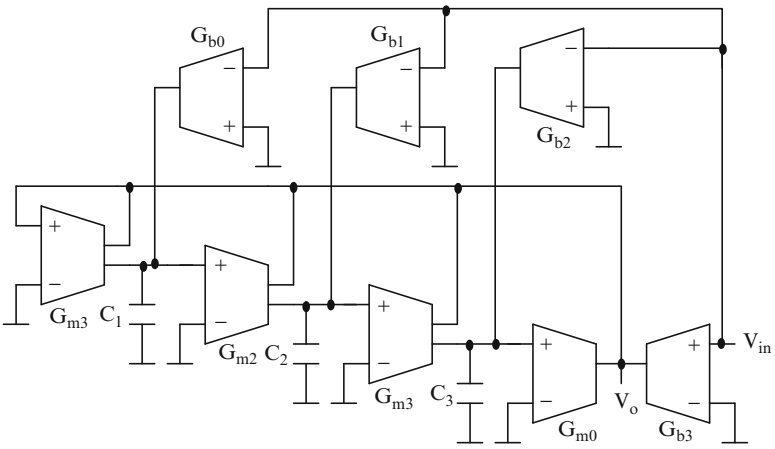


Fig. 3.37 A high-order voltage-mode OTA-C filter using dual ouput OTAs

3.8 Analytical Synthesis-Based OTA-C Filters

Chang, Al-Hashimi, Sun, and Ross [3.42] have described a high-order voltage-mode OTA-C filter realization using grounded capacitors and dual-output OTAs. A third-order filter derived using this procedure is presented in Fig. 3.37. This method needs an nth-order filter in general $(n + 2)$ OTAs and n capacitors. The OTAs $G_{bo} - G_{b3}$ realize the numerator coefficients, whereas the remaining OTAs and grounded capacitors realize the pole-forming loop. The transfer function of this third-order filter of Fig. 3.37 is given by

$$\frac{V_o}{V_{in}} = \frac{\begin{array}{c} s^3C_1C_2C_3g_{b3} + s^2(C_2C_3G_{bo}G_{m2} + C_1C_3G_{b1}G_{m1} + C_1C_2G_{b2}G_{mo}) \\ +s(C_3G_{m1}G_{m2}G_{b0} + C_1G_{b1}G_{m1}G_{mo}) + G_{bo}G_{m1}G_{m2}G_{mo} \end{array}}{s^3C_1C_2C_3g_{m3} + s^2C_2C_3G_{m3}G_{m2} + sC_3G_{m1}G_{m2}G_{m3} + G_{mo}G_{m1}G_{m2}G_{m3}} \tag{3.60}$$

Note that from a given denominator transfer function, the G_{m3}, G_{m2}, G_{m1}, and G_{mo} values can be calculated iteratively. Under the condition, $G_{bo} = G_{b1} = G_{b2} = 0$, a high-pass transfer function is realized at V_o whereas transfer functions with s^2 and s terms in the numerator are realized across capacitors C_1 and C_2. Note that by appropriate choice of signs of the transconductances of the OTAs G_{bo}, G_{b1}, and G_{b2}, negative terms can also be realized in the numerator.

A current-mode configuration for high-order OTA-C filters using grounded capacitors due to Chang and Al-Hashimi [3.43] is presented in Fig. 3.38 for the third-order case (for $n = 3$). Note that in this case, a front-end OTA with $(n + 1)$

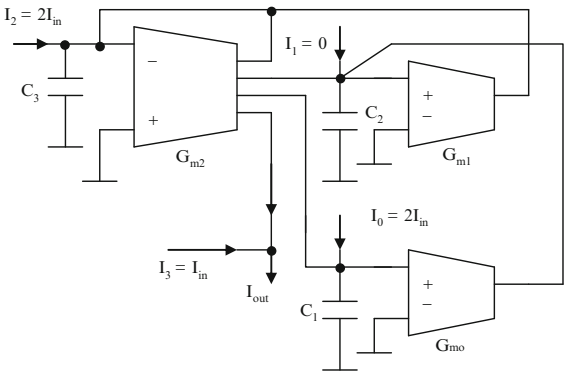


Fig. 3.38 A current-mode third-order OTA-C filter (Adapted from [3.43]©IEEE 2003)

outputs will be required together with $(n-1)$ OTAs and n grounded capacitors for realizing an nth-order filter. The transfer function of this circuit can be derived as

$$\frac{I_{out}}{I_{in}} = \frac{\left(\begin{array}{l} s^3C_1C_2C_3I_3 + s^2C_1C_2G_{m2}(I_3 - I_2) + sC_1G_{m1}G_{m2}(I_3 - I_1) \\ + G_{m1}G_{m2}G_{mo}(I_3 - I_0) \end{array}\right)}{s^3C_1C_2C_3 + s^2C_1C_2G_{m2} + sC_1G_{m1}G_{m2} + G_{m1}G_{m2}G_{m0}} \tag{3.61}$$

Note that in this case also, from a given denominator transfer function, the G_{m3}, G_{m2}, G_{m1}, and G_{mo} values can be calculated iteratively. For realizing a third all-pass transfer function given by

$$\frac{I_{out}}{I_{in}} = \frac{s^3a - s^2b + sc - d}{s^3a + s^2b + sc + d} \tag{3.62}$$

we need to choose $I_1 = 0$, $I_o = I_2 = 2I_{in}$, and $I_3 = I_{in}$.

The analytical synthesis technique can be extended to realize band-elimination filters also. An architecture due to Tu, Chang, Ross, and Swamy [3.44] is presented in Fig. 3.39a. As an illustration, a third-order elliptic filter can be realized using this circuit needing four OTAs and three grounded capacitors. Three of these need dual-current outputs. The transfer function of this filter can be derived considering all capacitors as unity, as

$$\frac{I_o}{I_{in}} = \frac{G_{m2}(s^2C_2C_3 + G_{m3}G_{m4})}{s^3C_1C_2C_3 + s^2G_{m1}C_2C_3 + sC_3G_{m2}G_{m3} + G_{m2}G_{m3}G_{m4}} \tag{3.63}$$

Evidently, a third-order elliptic transfer function can be realized. The transmission zeroes are controlled by G_{m3} and G_{m4} whereas the poles are also dependent on these transconductances, in addition to G_{m1} and G_{m2}. Tu, Chang, Ross, and Swamy [3.44] have expressed the desired transfer function as

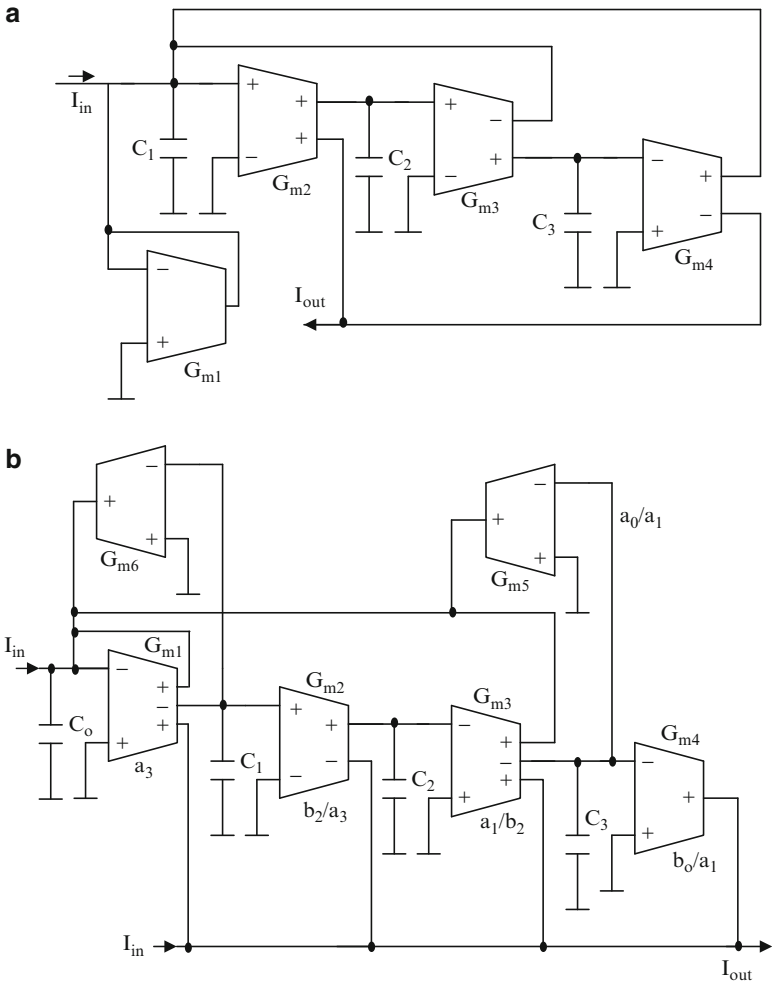


Fig. 3.39 (**a**) A OTA-C current-mode third-elliptic filter, and (**b**) a fourth-order elliptic current-mode OTA-C filter (Adapted from [3.44]©IEEE 2007)

$$\frac{I_o}{I_{in}} = \frac{s^2 b_2 + b_o}{s^3 a_3 + s^2 a_2 + s a_1 + a_o} \tag{3.64}$$

so that the various G_m values (considering $C_1 = C_2 = C_3 = 1$) will be

$$a_o = b_o, G_{m1} = \frac{a_2}{a_3},\ G_{m2} = \frac{b_2}{a_3},\ G_{m3} = \frac{a_1}{b_2} \text{ and } G_{m4} = \frac{a_o}{a_1}.$$

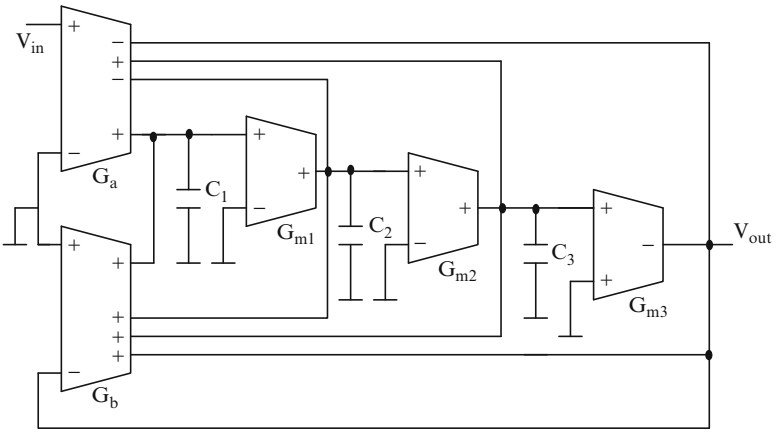


Fig. 3.40 Third-order voltage-mode OTA-C all-pass filter due to Chang, Hou, Chung, Horng, and Tu (Adapted from [3.45] ©IEEE2006)

Note that in the fourth-order case some simplification is feasible as shown in Fig. 3.39b. The transfer function of this circuit is given by

$$\frac{I_o}{I_{in}} = \frac{s^4 C_o C_1 C_2 C_3 + s^2 C_2 C_3 G_{m1}(G_{m6} - G_{m2}) + G_{m1} G_{m2} G_{m3}(G_{m5} - G_{m4})}{s^4 C_o C_1 C_2 C_3 + s^3 C_1 C_2 C_3 G_{m1} + s^2 C_2 C_3 G_{m1} G_{m6} + s C_3 G_{m1} G_{m2} G_{m3} + G_{m1} G_{m2} G_{m3} G_{m5}} \tag{3.65a}$$

The desired transfer function is

$$\frac{I_o}{I_{in}} = \frac{s^4 b_2 + s^2(a_2 - b_2) + (a_o - b_o)}{s^4 + s^3 a_3 + s^2 a_2 + s a_1 + a_o} \tag{3.65b}$$

The various G_m values are as shown in Fig. 3.39b.

Chang, Hou, Chung, Horng, and Tu [3.45] have described another technique of realizing voltage-mode high-order all-pass and band-reject-type OTA-C filters using grounded capacitors. A third-order all-pass filter is presented in Fig. 3.40. Note that in this case the denominator is realized by the multiple-output OTA G_b whereas the zeroes are realized by feeding currents into various internal nodes using the multiple-output OTA G_a. The transfer function of this circuit can be derived to be

$$\frac{V_o}{V_{in}} = -\frac{G_a}{G_b}\left(\frac{s^3 C_1 C_2 C_3 - s^2 C_1 C_2 G_{m3} + s C_1 G_{m2} G_{m3} - G_{m1} G_{m2} G_{m3}}{s^3 C_1 C_2 C_3 + s^2 C_1 C_2 G_{m3} + s C_1 G_{m2} G_{m3} + G_{m1} G_{m2} G_{m3}}\right) \tag{3.66}$$

Interestingly, some of the terms in the numerator can be made zero as needed for band-reject filters by not feeding the appropriate output of the OTA G_a to the internal nodes. Note that the gain can be scaled by using the ratio G_a/G_b. Note also that the poles and zeroes are realized by the same time constants avoiding the matching conditions needed. However, the inequality of various current outputs will lead to errors in the coefficients in the numerator and denominator.

3.9 Effect of OTA Nonidealities

In practice, the OTA nonidealities affect the performance of the OTA-C filters. We consider the effect of these nonidealities on typical biquads next. The sensitivity of the pole-frequency and pole-Q for the biquad of Fig. 3.21b can be seen to be low with respect to all G_m and capacitor values. Taking into the various input and output impedances of the OTAs, the denominator of the transfer function can be shown (after neglecting s^3 term and terms of the order of C_iC_j involving parasitics only) to be

$$\begin{aligned} &s^2(C_1C_2(G_{m1}+G_b+G_c)+G_{m1}(C_1C_a+C_2C_b))\\ &+s(G_{m2}G_{m3}(C_1+C_c)+G_{m1}(G_aC_1+G_bC_2))+G_{m2}G_{m3}(G_{m1}+G_c) \end{aligned} \tag{3.67}$$

where

$$\begin{aligned} &G_a=G_{i2}+G_{o3}, C_a=C_{i2}+C_{o3}, G_b=G_{i3}+G_{o2}, C_b=(C_{i3}+C_{o2}),\\ &G_c=G_{i1}+G_{o1}+G_{o4}, C_c=C_{i1}+C_{o1}+C_{o4}, G_d=G_{i1}+G_{i4}+G_{o4},\\ &C_d=C_{i1}+C_{i4}+C_{o4} \end{aligned} \tag{3.68}$$

It can be seen that the pole-frequency and pole-Q are slightly affected by the parasitic capacitances and output impedance of the various OTAs.

Taking into account the finite bandwidth of the OTA (using (3.2) with $\omega_{p2}=\omega_{z1}=\infty$), the realized denominator of the transfer function can be shown to be

$$\begin{aligned} &s^4C_1C_2\tau_2\tau_3G_{m1}+s^3g_{m1}C_1C_2(\tau_2+\tau_3)+s^2\{G_{m10}C_1C_2+G_{m20}G_{m30}C_1\tau_1\}\\ &+s(G_{m20}G_{m30}C_1)+(G_{m10}G_{m20}G_{m30}) \end{aligned} \tag{3.69}$$

where $\tau_i=1/\omega_{pi}$

Evidently, the pole-frequency and pole-Q are affected by the bandwidths of the OTAs:

$$\frac{\omega_p}{\omega'_p}=\sqrt{1+\frac{\tau_1\omega_p}{Q_p}},\ \frac{\omega_pQ_p}{\omega'_pQ'_p}=1-(\tau_2+\tau_3)\omega_pQ_p \tag{3.70}$$

where the primes indicate the perturbed values. Note that these results are obtained by neglecting the s^4 term in (3.69) and substituting $s^3 = -s{\omega_o}^2$ based on the well-known Akerberg–Mossberg approximation so that that the third-order system becomes a second-order one.

We next consider another OTA-C biquad of Fig. 3.21c. The sensitivity of the pole-frequency and pole-Q can be seen to be low with respect to all G_m and capacitor values. Taking into account the various input and output impedances of the OTAs, the denominator of the realized transfer function can be shown to be

$$D(s) = s^2(C_2(C'_b + C_1) + C_1C_a) + s(C_2G'_b + C_1G_a + C_2G_{m1} + C_aG_{m1}) + G_{m2}G_{m3} + G_{m1}G_a \tag{3.71}$$

where

$$G'_b = G_{i1} + G_{o4} + G_{o1} + G_{i2} + G_{03}, G_a = G_{i3} + G_{o2}, G_d = G_{i1} + G_{i4} + G_{o4},$$
$$C'_b = C_{i1} + C_{o4} + C_{o1} + C_{i2} + C_{o3}, C_a = C_{i3} + C_{o2}, C_d = C_{i1} + C_{i4} + C_{o4} \tag{3.72}$$

It can be seen that the pole-frequency and pole-Q are slightly affected by the parasitic capacitances and output impedance of the various OTAs.

Taking into account the finite bandwidth of the OTA, the realized fifth-order denominator of the transfer function can be seen to be

$$s^5\frac{\tau_1\tau_2\tau_3}{\omega_p^2} + s^4\frac{(\tau_1\tau_2 + \tau_2\tau_3 + \tau_3\tau_1)}{\omega_p^2} + s^3\left(\frac{\tau_1 + \tau_2 + \tau_3}{\omega_p^2} + \frac{\tau_2\tau_3}{\omega_pQ_p}\right) + s^2\left(\frac{1}{\omega_p^2} + \frac{(\tau_2 + \tau_3)}{\omega_pQ_p}\right) + s\left(\frac{1}{\omega_pQ_p} + \tau_1\right) + 1 \tag{3.73}$$

Evidently the pole-frequency and pole-Q are affected by the bandwidths of the OTAs:

$$\frac{{\omega_p}^2}{{\omega'_p}^2} = 1 + (\tau_2 + \tau_3)\frac{\omega_p}{Q_p} \tag{3.74a}$$

and

$$\frac{\omega_pQ_p}{\omega'_pQ'_p} = 1 - \omega_pQ_p(\tau_2 + \tau_3) - \tau_2\tau_3\omega_p^2 \tag{3.74b}$$

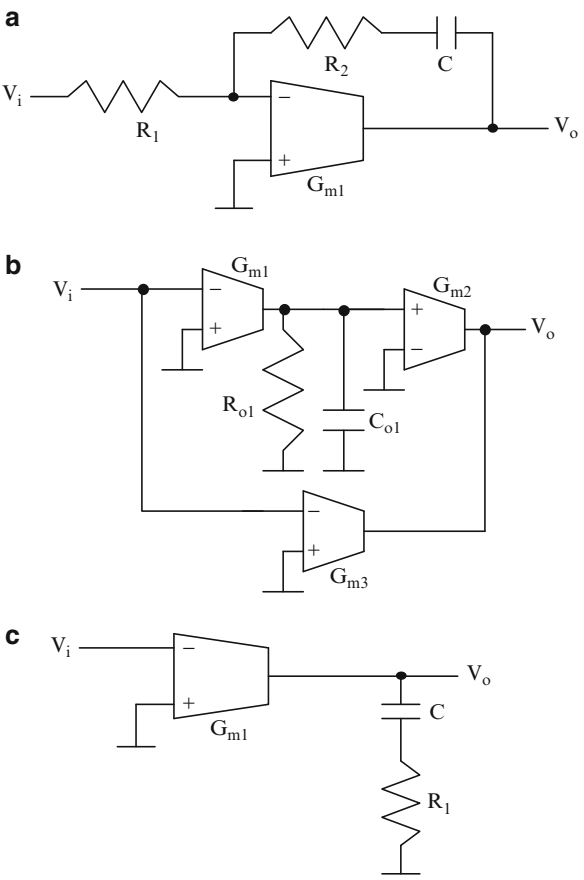


Fig. 3.41 Techniques for frequency compensation of OTA-based integrators: (**a**) using a resistor in series with integrating capacitor, (**b**) using a composite OTA employing feedforward, and (**c**) using a resistor in series with the integrating capacitor

Some techniques for compensating for the finite bandwidth of the OTA in integrators have been suggested. In one method [3.46], [3.2] shown in Fig. 3.41a, a resistance can be inserted in series with the integrating capacitor. The resulting transfer function considering the output capacitance and resistance of the OTA, can be derived as

$$\frac{V_o}{V_i} = -\frac{1 + sC\left(R_2 - \frac{1}{G_m}\right)}{\frac{1}{G_m R_o} + sC\left(R_1 + \frac{R_1+R_2}{G_m R_o} + \frac{1}{G_m} + \frac{C_o}{CG_m}\right) + s^2 \frac{CC_o(R_1+R_2)}{G_m}} \tag{3.75a}$$

Note that the first term in the denominator is very small thus simplifying (3.75a) as

$$\frac{V_o}{V_i} = -\frac{1 + sC\left(R_2 - \frac{1}{G_m}\right)}{sCR_1\left(1 + \frac{R_1+R_2}{R_1 G_m R_o} + \frac{1}{R_1 G_m} + \frac{C_o}{R_1 CG_m} + s\frac{C_o(R_1+R_2)}{R_1 G_m}\right)} \tag{3.75b}$$

Evidently under the condition, the "s" terms in the numerator and denominator in (3.75b) are equal, an ideal integrator can be realized. This yields R_2 as the solution of the quadratic equation

$$R_2^2 + R_2\left(\frac{1+G_mR_1}{G_o} + R_1 - \frac{1}{G_m}\right) - \left(\frac{1}{G_m}\left(\frac{1+G_mR_1}{G_o} + R_1 + \frac{C_o}{CG_o}\right) + \frac{C_oR_1}{CG_o}\right) = 0 \tag{3.76}$$

Several authors [3.47, 3.48, 3.49] have suggested the use of composite OTAs using feedforward compensation in place of the OTA of Fig. 3.41a as shown in Fig. 3.41b. In this case, in place of G_m in (3.75a), we need to substitute

$$G_m = G_{m3} + \frac{G_{m1}G_{m2}}{G_{o1} + sC_{01}} \tag{3.77}$$

where $R_{o1}(= 1/g_{o1})$ and C_{o1} are the output resistance and output capacitance of the transconductance block realizing G_{m1}. Note also that the output impedance of the G_{m2} block and G_{m3} block are already considered in the output resistance and capacitance in Fig. 3.41a. The resulting transfer function of the integrator can be derived as

$$\frac{V_o}{V_i} = -\frac{-G_{m4}\left(1+sC\left(R_2 - \frac{1}{G_{m4}} + \frac{G_{m3}\tau}{G_{m4}C}\right) + s^2\frac{C\tau}{G_{m4}}(R_2G_{m3}-1)\right)}{2s^3\tau CC_o(R_1+R_2) + s^2\left(\tau C\left(1+2G_o(R_1+R_2)+\frac{2C_o}{C}\right) + 2CC_o(R_1+R_2) + G_{m3}CR_1\tau\right)}$$

$$+ s\left(2G_o\tau + C\left(1+2G_o(R_1+R_2)+\frac{2C_o}{C}\right) + CR_1G_{m4}\right) + 2G_o \tag{3.78}$$

where $g_{m4} = g_{m3} + g_{m1}g_{m2}R_{o1}$. The value of R_2 needed for phase cancellation can be derived as

$$R_2^2 + \frac{R_2}{2CG_o}(y + 2G_o(z-\tau) - 2C_o) + \left(\frac{yz-x}{2C^2G_o}\right) = 0 \tag{3.79}$$

where

$$x = \tau C\left(1 + 2G_oR_1 + \frac{2C_o}{C}\right) + 2CC_oR_1 + G_{m3}CR_1\tau \tag{3.80a}$$

$$y = 2G_o\tau + C\left(1 + 2G_oR_1 + \frac{2C_o}{C}\right) + CR_1G_{m4} \tag{3.80b}$$

and

$$z = \frac{G_{m3}\tau - C}{G_{m4}} \tag{3.80c}$$

Another technique of passive compensation of the intrinsic phase lag of the OTA [3.2] is presented in Fig. 3.41c. The realized transfer function is obtained as

$$\frac{V_o}{V_i} = -\frac{G_m(1 + sCR_1)}{sC\left(1 + \frac{s}{\omega_t}\right)} \tag{3.81}$$

Thus the condition for compensation is $\omega_t = \frac{1}{CR_1}$. Note, however, that this technique does not compensate the effect of the finite output resistance and capacitance of the OTA.

3.10 OTA-C Oscillators

Several OTA-C oscillators have been proposed in the literature. These can be considered to be derived from OTA-C filters by removing the damping in a two-integrator loop or by adding positive feedback through the use of a negative resistance realized using OTAs. These are considered next.

The OTA-C oscillator of Fig. 3.42a realizes poles defined by the equation

$$s^2(C_1C_2 + C_2C_3 + C_1C_3) + sC_1(G_{m1} - G_{m2}) + G_{m1}G_{m2} = 0 \tag{3.82a}$$

Evidently, C_2 or C_3 can be zero leading to two oscillator structures described by Abuelmaa'tti [3.50]. The condition for oscillation is $G_{m1} = G_{m2}$. We next consider an oscillator due to Senani and Amitkumar [3.51] shown in Fig. 3.42b which is obtained from a Wien bridge oscillator. The OTAs G_{m1} and G_{m3} realize resistors. The OTA G_{m2} and the resistor R_o realize a voltage amplifier. The realized poles are given by

$$s^2C_1C_2 + s(C_2(G_{m1} + G_{m3} - G_{m2}G_{m3}R_o) + C_1G_{m3}) + G_{m1}G_{m3} = 0 \tag{3.82b}$$

Note that R_o needs to be realized using another OTA. The condition for oscillation can be derived for $G_{m1} = G_{m3}$ and $C_1 = C_2$ as $G_{m2}R_o = 3$. Consider another oscillator due to Senani [3.52], shown in Fig. 3.42c whose poles are given by

$$s^2C_1C_2 + s(C_1G_{m3} - C_2G_{m2}) + G_{m1}G_{m3} = 0 \tag{3.82c}$$

Senani, Tripathi, Bhaskar and Banerjee [3.53] have described five more oscillators. The oscillator of Fig. 3.42d realizes poles given by

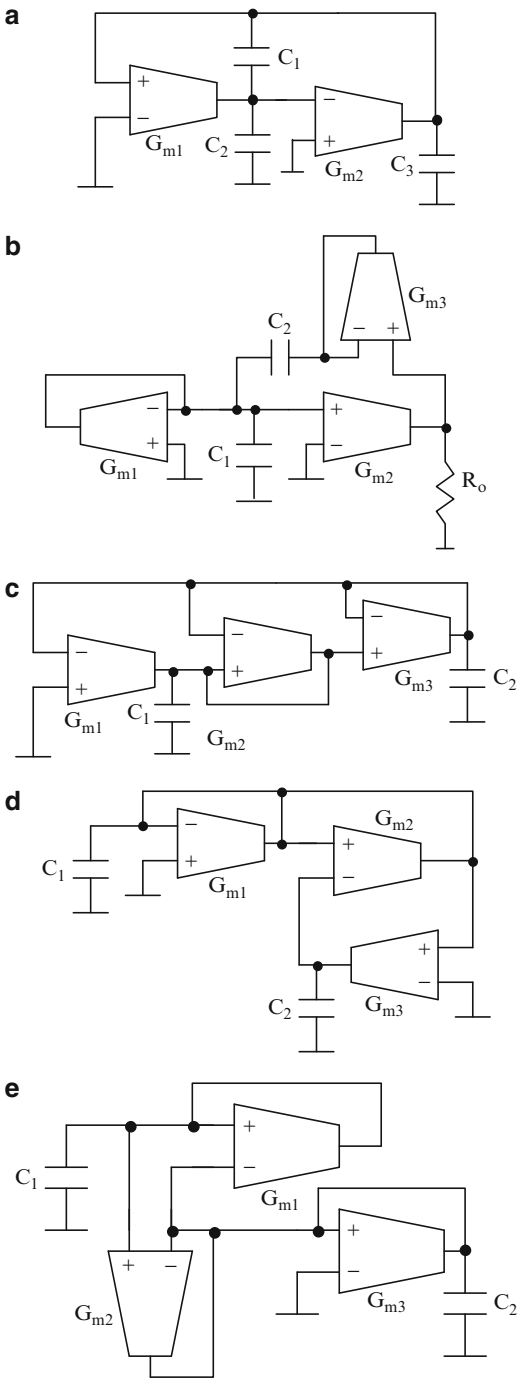


Fig. 3.42 OTA-C oscillators: (**a**) due to Abuelmaatti [3.50], (**b**) due to Senani and AmitKumar [3.51], (**c**) Senani [3.52], (**d**)–(**h**) Senani, Tripathi, Bhaskar and Banerjee [3.53], and (**i**) Linares-Barranco, Rodriguez-Vazquez, Sanchez-Sinencio and Huertas [3.54] ((**a**) Adapted from [3.50] ©IET1989, (**b**) adapted from [3.51] ©IET 1989, (**c**) adapted from [3.52] ©IET 1989, (**d**)-(**h**) adapted from [3.53] ©IET 1990)

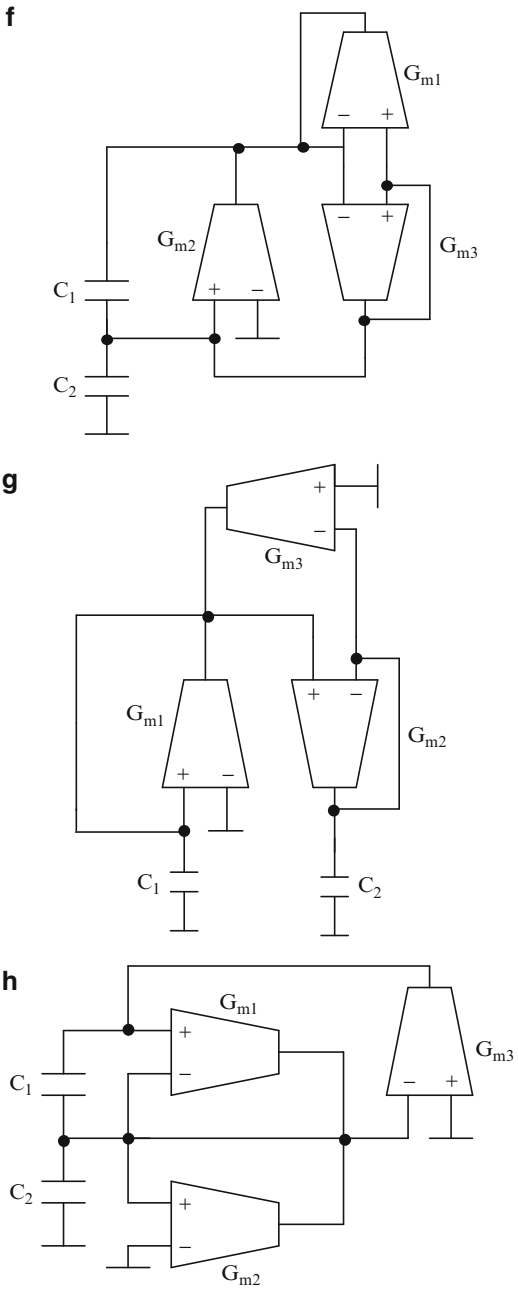


Fig. 3.42 (continued)

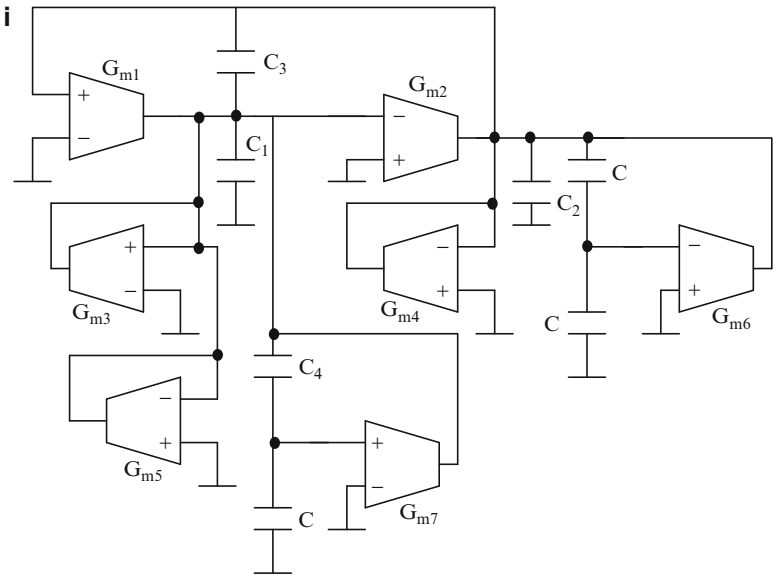


Fig. 3.42 (continued)

$$s^2C_1C_2 + sC_2(G_{m1} - G_{m2}) + G_{m2}G_{m3} = 0 \tag{3.82d}$$

The oscillator of Fig. 3.42e realizes poles given by

$$s^2C_1C_2 + s(C_1(G_{m2} - G_{m3}) - C_2G_{m1}) + G_{m1}G_{m3} = 0 \tag{3.82e}$$

The circuit of Fig. 3.42f realizes poles given by

$$s^2C_1C_2 + s(C_2G_{m1} - C_1G_{m2}) + G_{m2}G_{m3} = 0 \tag{3.82f}$$

On the other hand, the circuit of Fig. 3.42g realizes poles given by

$$s^2C_1C_2 + s(C_1G_{m2} - C_2G_{m1}) + G_{m2}(G_{m3} - G_{m1}) = 0 \tag{3.82g}$$

In another OTA-C oscillator shown in Fig. 3.42h, we have the poles given by

$$s^2C_1C_2 + sC_1(G_{m3} - G_{m2}) + G_{m1}G_{m3} = 0 \tag{3.82h}$$

Linares-Barranco, Rodriguez-Vazquez, Sanchez-Sinencio, and Huertas [3.54] have described five OTA-C oscillators that can be derived from the general circuit of Fig. 3.42i. The realized poles are given by

$$s^2\big((C_1+C_3+(1-\alpha)C_4)(C_2+(1-\beta)C_6)+C_3(C_1+(1-\alpha)C_4)\big)$$
$$+s\begin{pmatrix}C_3(G_{m2}-G_{m1})-(C_3+C_2+(1-\beta)C_6)(G_{m3}-G_{m5}+\alpha G_{m7})\\+(\beta G_{m6}+G_{m4})(C_3+C_1+(1-\alpha)C_4)\end{pmatrix}$$
$$+G_{m1}G_{m2}+(G_{m5}-G_{m3}-\alpha G_{m7})(\beta G_{m6}+G_{m4})=0 \tag{3.83}$$

The various cases are:

(a) $G_{m3}=G_{m4}=G_{m5}=G_{m6}=G_{m7}=0$ and $C_4=C_5=C_6=C_7=0$
(b) $G_{m4}=G_{m5}=G_{m6}=G_{m7}=0$ and $C_4=C_5=C_6=C_7=C_3=0$
(c) $G_{m5}=G_{m6}=G_{m7}=0$ and $C_4=C_5=C_6=C_7=C_3=0$
(d) $G_{m4}=G_{m6}=G_{m7}=0$ and $C_4=C_5=C_6=C_7=C_3=0$
(e) $G_{m3}=G_{m4}=G_{m5}=0$ and $C_1=C_2=C_3=0$

The condition for oscillation and frequency of oscillation can be determined easily from (3.83).

The basic principle of all these oscillators is that the poles be defined by an equation of the form $s^2 + bs + c = 0$ where the value of b shall be such as to cancel the positive terms that may arise because of the finite input and output resistances of the OTAs. Even though the two lossless integrators in a negative feedback loop can realize ideally a sinusoidal oscillator, the parasitics may shift the poles to the left half of the complex plane. Hence a degree of freedom shall exist to bring them onto the imaginary axis of the complex frequency plane.

In practice, oscillators need to have an amplitude control loop or have native amplitude limiting by exploiting the nonlinear behavior of OTAs. The reader is referred to [3.55, 3.56, 3.57] for information on these designs.

3.11 Derivation of Voltage-Mode OTA-C Filters from Active RC Filters and Current-Mode OTA-C Filters from Voltage-Mode OTA-C Filters

It is possible to derive voltage-mode OTA-C filters from active RC filters by using the nodal voltage simulation technique [2.41]. As an illustration, consider the voltage-mode Sallen–Key second-order high-pass active RC filter of Fig. 3.43a. The node voltages can be written at nodes x and y as

$$(V_i-V_x)sC_1+(V_o-V_x)sC_2+\frac{(V_o-V_x)}{R_1}=0 \tag{3.84a}$$

$$(V_x-V_o)sC_2=\frac{V_o}{R_2} \tag{3.84b}$$

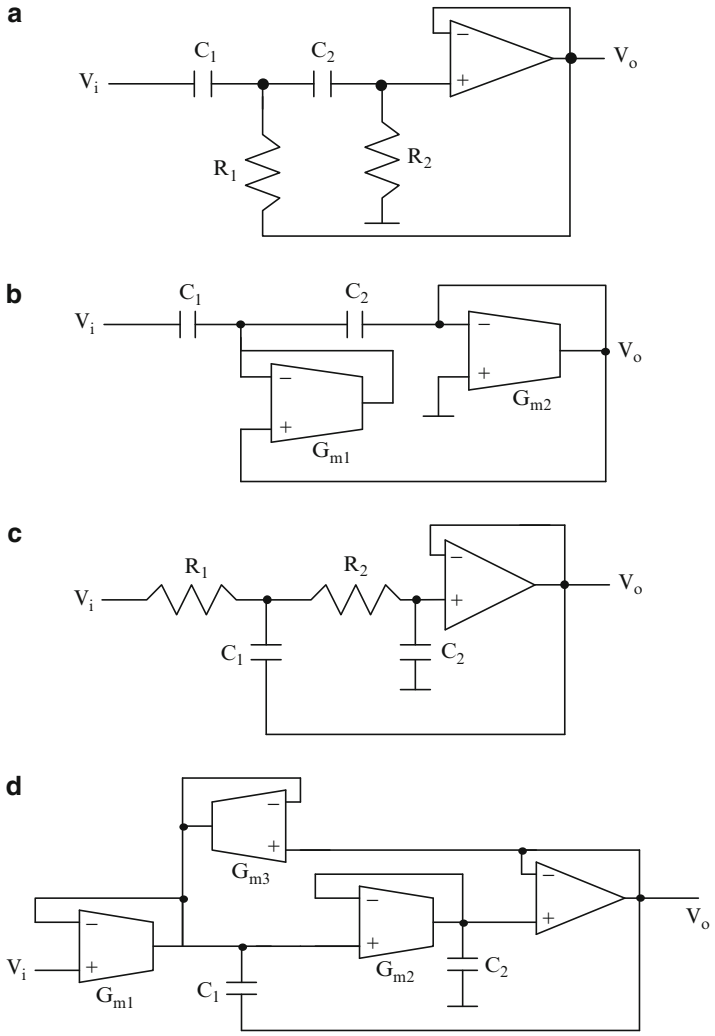


Fig. 3.43 (**a**) Sallen and Key second-order low-pass filter, (**b**) OTA-C filter derived from (**a**), (**c**) Sallen and Key high-pass filter, and (**d**) OTA-C filter derived from (**c**) ((**b**) and (**d**) Adapted from [3.4] ©IEEE 1985)

The circuit of Fig. 3.43b implements exactly these equations. Note that $G_{m1} = 1/R_1$ and $G_{m2} = 1/R_2$. However, the matters may not be that simple in the case of other active RC filters. As an illustration, consider the Sallen–Key second-order low-pass active RC filter of Fig. 3.43c. Proceeding in a similar manner, the circuit of Fig. 3.43d can be obtained wherein a buffer opamp will be needed to provide the needed isolation. The reader is urged to derive in a similar manner, OTA-C filters from other active RC filters. In some cases, the number of capacitors

needed may be more as well as the number of OTAs. In addition, some matching requirements on OTAs and capacitors may be present.

It is possible to derive current-mode OTA-C filters from active RC filters directly using Ahmed, Awad, and Soliman's technique [3.58]. As an illustration, consider the KHN active RC biquad presented in Fig. 3.44a. The equations at various nodes can be written easily as follows.

$$\begin{aligned} sC_1V_{BP} &= -G_1V_{HP},\ sC_2V_{LP} = -G_2V_{BP},\ G_3(V_i - V_{notch}) \\ &= G_4(V_{notch} - V_{BP}),\ G_5(V_{LP} - V_{notch}) = G_6(V_{notch} - V_{HP}) \end{aligned} \tag{3.85}$$

The first step is to substitute in place of various node voltages V_i, node currents I_i yielding the following equations.

$$\begin{aligned} C_1I_{BP} &= -\frac{G_1I_{HP}}{s},\ C_2I_{LP} = \frac{-G_2I_{BP}}{s},\ G_3(I_i - I_{notch}) \\ &= G_4(I_{notch} - I_{BP}),\ G_5(I_{LP} - I_{notch}) = G_6(I_{notch} - I_{HP}) \end{aligned} \tag{3.86}$$

Defining $\hat{C}_1 = \frac{CG}{G_1}, \hat{C}_2 = \frac{CG}{G_2}, \hat{G}_1 = \frac{CG}{C_1}, \hat{G}_2 = \frac{CG}{C_2}, \hat{G}_3 = \frac{G^2}{G_3}, \hat{G}_4 = \frac{G^2}{G_4}, \hat{G}_5 = \frac{G^2}{G_5}$ and $\hat{G}_6 = \frac{G^2}{G_6}$, (3.86) can be rewritten as

$$\begin{aligned} \frac{1}{\hat{G}_1}I_{BP} &= -\frac{1}{s\hat{C}_1}I_{HP},\ \frac{1}{\hat{G}_2}I_{LP} = -\frac{1}{s\hat{C}_2}I_{BP}, \\ \frac{1}{\hat{G}_4}I_{notch} &= -\frac{1}{\hat{G}_3}(I_i - I_{notch}) + \frac{1}{\hat{G}_4}I_{BP}, \\ \frac{1}{\hat{G}_6}I_{HP} &= -\frac{1}{\hat{G}_5}(I_{notch} - I_{LP}) + \frac{1}{\hat{G}_6}I_{notch} \end{aligned} \tag{3.87}$$

These equations can be easily realized using OTAs with multiple current outputs. Note that the OTAs realize the currents $(I_{BP} - I_{notch}), I_{BP}, (I_{HP} - I_{notch}), I_{LP}$ from which other currents are obtained by adding the appropriate mirrored output currents as shown in Fig. 3.44b. As an illustration, $I_{LP} - I_{\text{notch}}$ needed in (3.87) is obtained as

$$I_{LP} - I_{notch} = I_{BP} - I_{notch} - I_{BP} + I_{LP} \tag{3.88}$$

Evidently, the filter needs two grounded capacitors and same number of OTAs as in the original active RC filter but OTAs have several current outputs. It may be noted that the KHN biquad can be designed using $G_5 = G_6$ in which case the circuit can be simplified as shown in Fig. 3.44c. Note that from (3.86), under the condition $G_5 = \mathrm{G}_6$, we have

$$2I_{notch}\frac{(G_3 + G_4)}{2} = G_3I_i + G_4I_{BP},\ I_{HP} = 2I_{notch} - I_{LP} \tag{3.89a}$$

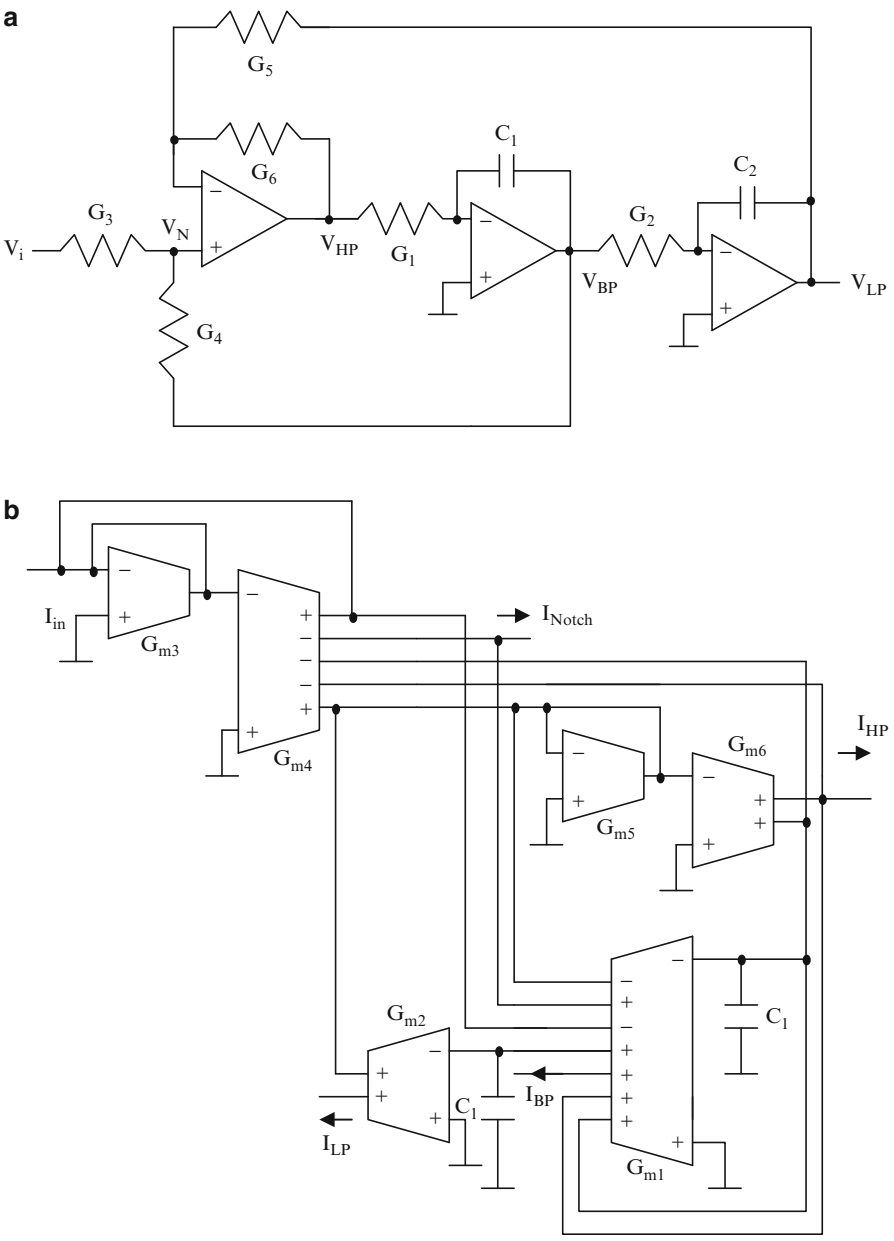


Fig. 3.44 (**a**) KHN active RC biquad, (**b**) current-mode OTA-C filter derived from (**a**), and (**c**) simplification of (**b**) when $G_5 = G_6$ (Adapted from [3.58] ©Birkhauser 2006)

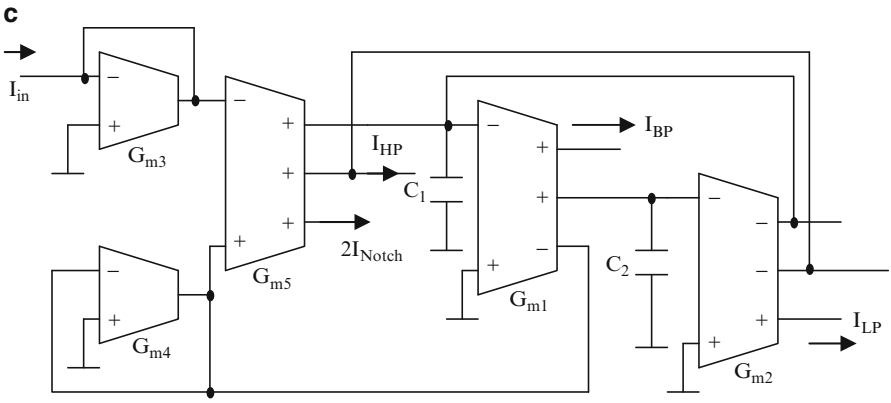


Fig. 3.44 (continued)

Defining $\hat{G}_3 = \frac{G^2}{G_3}$, $\hat{G}_4 = \frac{G^2}{G_4}$, $\hat{G}_5 = \frac{2G^2}{G_3+G_4}$, (3.87) reduces to

$$2I_{notch}\frac{1}{\hat{G}_5} = \frac{1}{\hat{G}_3}I_i + \frac{1}{\hat{G}_4}I_{BP} \tag{3.89b}$$

The reader is urged to apply the technique to the Friend's biquad which may lead to the need for more capacitors.

It is possible to generate current-mode OTA-C filters from voltage-mode OTA-C filters using the transposition principle [3.59, 3.60, 3.61]. In this method, the voltage input is grounded and the output current flowing to ground at this terminal is tapped. The input current is fed at the output voltage terminal. Furthermore, all the OTAs are reversed in the sense that the out terminal will be the new input voltage terminal of the OTA with the other input of the OTA grounded. The input voltage terminal will be the OTA output current terminal. As an illustration, consider the differentiator of Fig. 3.4d redrawn in Fig. 3.45a. The new current-mode filter is as shown in Fig. 3.45b. Next consider the voltage-mode first-order all-pass filter of Fig. 3.45c and its transpose current-mode filter derived as shown in Fig. 3.45d. As another example, a voltage-mode OTA-C biquad and its current-mode version are shown in Fig. 3.45e, f, respectively. The technique can be applied to oscillators as well. Consider the two OTA-C oscillators of Abuelmaa'tti [3.50] of Fig. 3.45g, h of which one can be derived from another.

3.12 Distortion in OTA-C Filters

Transconductors generally have higher bandwidth than operational amplifiers and can be tuned electronically and lead to simple circuitry. The transconductance of the OTA is the transconductance of the driver transistors and can be varied by bias

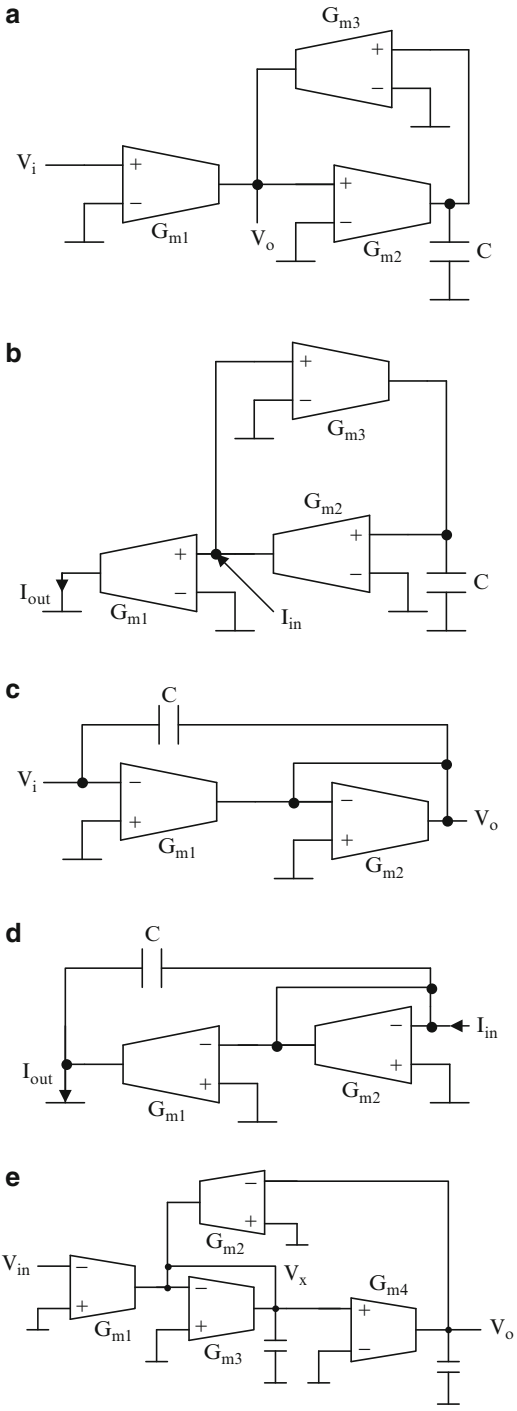


Fig. 3.45 (**a**) Voltage-mode OTA-C differentiator, (**b**) current-mode differentiator derived from (**a**), (**c**) voltage-mode first-order all-pass filter, (**d**) current-mode OTA-C first-order all-pass filter derived from (**c**), (**e**) voltage-mode two-integrator loop OTA-C biquad, (**f**) current-mode filter obtained from (**e**), (**g**) OTA-C oscillator, and (**h**) another OTA-C oscillator obtained by transposition ((**a**)–(**g**) Adapted from [3.64]©Birkhauser 2003)

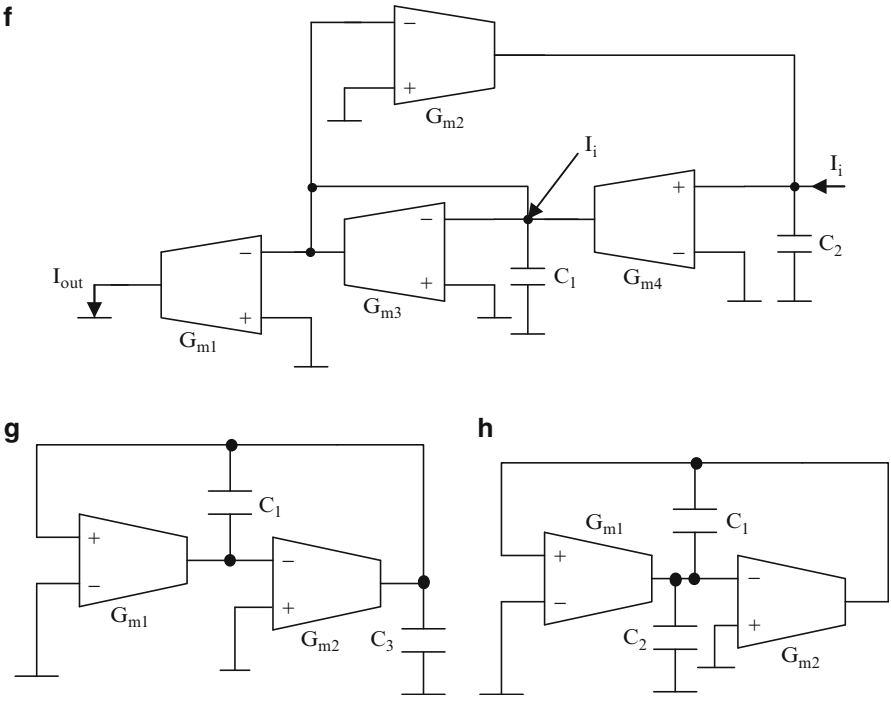


Fig. 3.45 (continued)

current. The advantage of using the differential structure shown in Fig. 3.46a is that the linearity of the output signal is improved due to the absence of even-order distortion. There is a tradeoff between linearity and speed in the design of the OTA. Gain, noise, and speed are affected, for example, by using emitter/source degeneration and the linearity is improved. Transconductances can operate at very high frequencies but distortion of the output signal can be considerably high.

Theoretically, the transconductance remains constant irrespective of the input voltage. However, in practice, this is true only for small input voltages. In other words, the output current is not linearly dependent on the input voltage. This will result in output distortion and amplitude-dependent transconductance. Thus, the input voltage must be kept small enough so that the transconductor exhibits linear V-I conversion.

The transconductance typically can be expressed as

$$G_m = G_m\sqrt{1-\left(\frac{G_m|V_{in}|}{2I_{BIAS}}\right)^2} \tag{3.90}$$

where $|V_{in}|$ is the amplitude of the input signal, and G_m the small-signal transconductance equals $\sqrt{k'I_{BIAS}\left(\frac{W}{L}\right)}$. Hence when V_{in} is much smaller than $2I_{BIAS}/G_m$, the

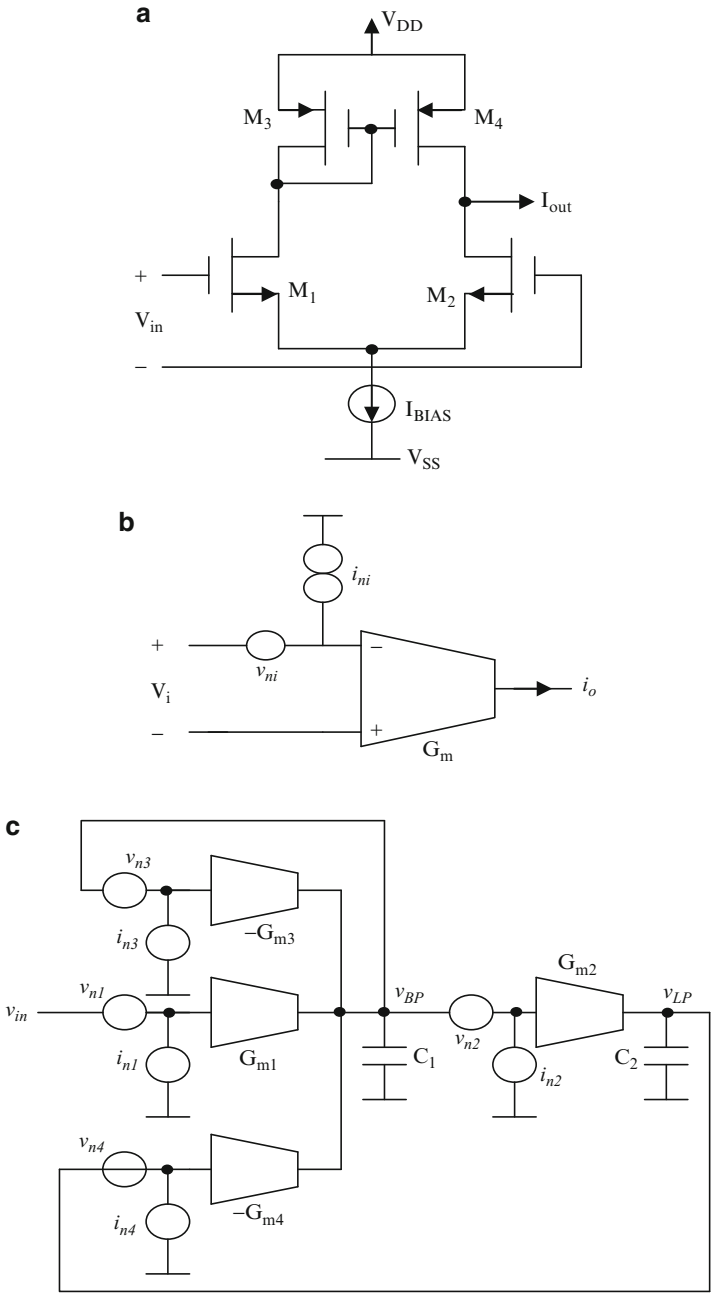


Fig. 3.46 (**a**) A simple CMOS OTA, (**b**) noise model of the OTA, (**c**) voltage-mode biquad used for noise analysis. and (**d**) a current-mode OTA-C biquad used for noise analysis ((**c**) and (**d**) Adapted from [3.62] ©IEEE1998)

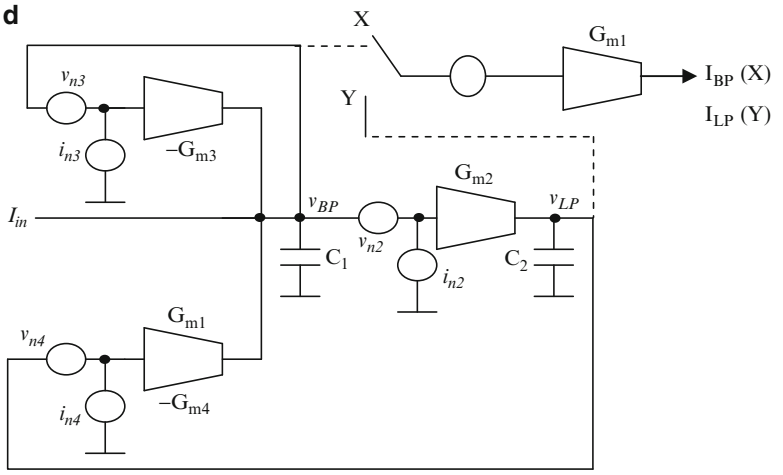


Fig. 3.46 (continued)

transcondutance gain is independent of $|V_{in}|$. Under these conditions, the third harmonic distortion can be found as

$$HD_3 = \frac{k'\left(\frac{W}{L}\right)|V_{in}|^2}{32I_{BIAS}} \cong \frac{\lambda^2}{32} \tag{3.91a}$$

where $\lambda = \frac{I_{out}}{I_{BIAS}}$ and I_{out} is the amplitude of the output current. Thus it can be seen that λ plays an important role in deciding the distortion in the output current of the OTA. In addition to bias current, the supply voltage also plays a role in the linearity of the circuits. When the supply voltage is small, the signal may get clipped and distorted. In biquads, however, the relation of bias current to output current is the main cause of distortion.

In the case of OTAs realized using bipolar transistors, for small input signals, $G = G_m = \frac{2I_{BIAS}}{V_T}$ and the third harmonic distortion is given by

$$HD_3 = \frac{\left(\frac{|V_{in}|}{2V_T}\right)^2}{12} \cong \frac{\lambda^2}{32} \tag{3.91b}$$

3.13 Noise Analysis of OTA-C Biquads

Transconductors have inherent noise that can be modeled as a noise voltage source in series with the input terminal and a noise current source to ground to the input terminal as shown in Fig. 3.46b. The noise can be expressed as

$$v_n^2 = \frac{8}{3}\left(1 + \frac{G_{m3}}{G_{m1}}\right)\frac{kT\Delta\omega}{\pi G_{m1}} \tag{3.92}$$

where G_{m1} is the transconductance of the driver transistor and G_{m3} that of the load transistor (see Fig. 3.46a), k is Boltzmann's constant, and T is absolute temperature.

The total noise of the OTA of transconductance G_m can be expressed as voltage and current noise given by

$$v_n^2 = \gamma_v \frac{kT\Delta\omega}{\pi G_m} \tag{3.93a}$$

and

$$i_n^2 = \gamma_i \frac{kTG_m\Delta\omega}{\pi} \tag{3.93b}$$

where γ_v and γ_i are voltage and current noise factors, respectively, and are usually greater than unity. For the circuit of Fig. 3.46a, $\gamma_i = 0$ and $\gamma_v = \frac{8}{3}\left(1 + \frac{G_{m3}}{G_{m1}}\right)$. Moreover, γ_v is always larger than γ_i.

It is useful to derive the total noise first of a second-order OTA-C voltage mode filter [3.62] shown in Fig. 3.46c wherein all the relevant voltage and current sources are shown. Routine analysis yields the transfer functions at the band-pass and low-pass outputs as

$$V_{BP} = \frac{-sC_2(I_{n2} + I_{n3} + v_{n3}G_{m3} + v_{n4}G_{m4} + v_{n1}G_{m1} - v_iG_{m1}) + i_{n4}G_{m4} + v_{n2}G_{m2}G_{m4}}{s^2C_1C_2 + sC_2G_{m3} + G_{m2}G_{m4}} \tag{3.94a}$$

and

$$V_{LP} = \frac{\left(\begin{array}{l} sC_1v_{n2}G_{m2} + v_{n3}G_{m2}G_{m3} + v_{n4}G_{m2}G_{m4} + v_{n1}G_{m1}G_{m2} + v_{n2}G_{m2}G_{m3} \\ -v_{in}G_{m1}G_{m2} + i_{n4}(sC_1 + G_{m3}) + (i_{n2} + i_{n3})G_{m2} \end{array}\right)}{s^2C_1C_2 + sC_2G_{m3} + G_{m2}G_{m4}} \tag{3.94b}$$

Assuming that the contribution of the noise current sources is negligible compared to noise voltage sources, it is first necessary to find the squared magnitude of the various transfer functions of the noise sources v_{n1},v_{n2},v_{n3}, and v_{n4} to the output. These can be seen to be low-pass and band-pass types only. The integrals of the low-pass and band-pass transfer functions already have been derived in Chap. 2 and turn out to be $Q_p\pi\omega_p/2$ (see (2.136a) and (2.136b)). Using these together with the expressions for the spectral density of noise voltage sources of OTAs given in (3.93), we obtain the total noise as

$$v_{n,BP}^2 = kT\frac{G_{m4}}{2C_2}\left(\frac{\gamma_2}{G_{m2}} + \frac{C_2}{G_{m2}G_{m4}C_1}(\gamma_3 G_{m3} + \gamma_4 G_{m4} + \gamma_1 G_{m1}\right) \tag{3.95a}$$

and

$$v_{n,LP}^2 = kT\frac{G_{m4}}{2C_2}\left(\frac{\gamma_2 C_1}{G_{m4}C_2} + \frac{G_{m3}^2}{G_{m4}^2}\left(\frac{\gamma_2}{G_{m2}} + \frac{\gamma_3}{G_{m3}}\right) + \frac{\gamma_4}{G_{m4}} + \frac{\gamma_1 G_{m1}}{G_{m4}^2}\right) \tag{3.95b}$$

For the choice of components $C_1 = C_2$, $G_{m2} = G_{m4}$, $G_{m3}/G_{m4} = 1/Q$, we have from (3.95),

$$v_{n,BP}^2 = \frac{kT}{2C_2}\gamma_{vBP} = \frac{kT}{2C_2}\left(\gamma_2 + \left(\frac{\gamma_3}{Q} + \gamma_4 + \frac{\gamma_1 G_{m1}}{G_{m4}}\right)\right) \tag{3.96a}$$

and

$$v_{n,LP}^2 = \frac{kT}{2C_2}\gamma_{vLP} = \frac{kT}{2C_2}\left(\gamma_2 + \frac{1}{Q^2}(\gamma_2 + \gamma_3 Q) + \gamma_4 + \frac{\gamma_1 G_{m1}}{G_{m4}}\right) \tag{3.96b}$$

It is thus evident that the total noise is inversely proportional to the integrator capacitance. If the assumption $C_1 = C_2$ is not used, in place of C_2 in (3.96), we will have $\sqrt{C_1 C_2}$.

We next examine the power dissipation of the OTA-C filters. Considering the OTA-C filter of Fig. 3.46c, the power dissipation can be written as the sum of the dc power dissipation of all four OTAs. The low distortion requirement stipulates that λ_i defined earlier, that is, the ratio of I_{dc} to the maximum output current I_{out}, shall be very small. The power dissipation thus can be expressed as

$$PD = \sum_{i=1}^{4} V_{DD}\frac{|I_i|_{\max}}{\lambda_i} = \frac{V_{DD}}{\lambda_i}\sum_{i=1}^{4}|I_i|_{\max} \tag{3.97}$$

These maxima $|I_i|_{\max}$ occur approximately at the pole-frequency for high pole-Q designs. Denoting $|V_{in}|$ as the amplitude of the input signal, these are, respectively, as follows.

$$|I_1|_{\max} = |V_{in}|G_{m1} \tag{3.98a}$$

$$|I_2|_{\max} = |V_{in}|\frac{G_{m1}G_{m2}}{G_{m3}} \tag{3.98b}$$

$$|I_3|_{\max} = |V_{in}|G_{m1} \tag{3.98c}$$

$$|I_4|_{\max} = |V_{in}|G_{m1} \quad \text{if} \quad Q < \frac{1}{\sqrt{2}} \tag{3.98d}$$

$$|I_4|_{\max} = |V_{in}| \frac{G_{m1} Q}{\sqrt{1 - \frac{1}{4Q^2}}} \quad \text{if} \quad Q > \frac{1}{\sqrt{2}} \tag{3.98e}$$

Thus the total power dissipation can be obtained as

$$PD == \frac{V_{DD}}{\lambda_i} V_{in} G_{m1} \left(3 + \frac{G_{m2}}{G_{m3}}\right) \quad \text{if} \quad Q < \frac{1}{\sqrt{2}} \tag{3.99a}$$

and

$$PD == \frac{V_{DD}}{\lambda_i} V_{in} G_{m1} \left(2 + \frac{G_{m2}}{G_{m3}} + \frac{Q}{\sqrt{1 - \frac{1}{4Q^2}}}\right) \quad \text{if} \quad Q > \frac{1}{\sqrt{2}} \tag{3.99b}$$

We finally consider the dynamic range of the OTA-C filter. The minimum signal level that the filter can handle is decided by the biquad noise, whereas the maximum signal level is decided by the acceptable *THD* (third harmonic distortion):

$$DR_{n\%THD} = \frac{|\text{signal}|^2_{\text{n\%THD}}/2}{\text{noise}^2} \tag{3.100a}$$

where $|\text{signal}|^2_{\text{n\%THD}}$ is the magnitude of the output signal when its *THD* reaches *n%*. Hence for low-pass output, *DR* can be obtained as

$$DR = \frac{|v_{LP}|^2/2}{v^2_{LP,n}} \tag{3.100b}$$

It is interesting that a relationship between speed (implying capability to realize high pole-frequencies), power dissipation, and dynamic range can be found from (3.96b), (3.99b), and (3.100b) as

$$PD^2 = \frac{DRkTV^2_{\text{sup}}\gamma_{vLP}}{\lambda^2} \left(3 + \frac{G_{m2}}{G_{m3}}\right)^2 \frac{G^2_{m4}}{\sqrt{C_1 C_2}} \tag{3.101}$$

Note that the pole-frequency is implicit in C_1, C_2, and G_{m4} values and that PD^2 can also be expressed in terms of *DR* and γ_{vBP}.

The analysis of the current-mode filter of Fig. 3.46d can be carried out in a similar manner. Note that in this case, the OTA G_{m1} is not present. In addition, the node voltages are converted into currents using the OTA G_{m4}. This is a wideband device and hence the noise needs to be integrated over the frequency band of interest. Detailed analysis shows that the voltage-mode filter is superior to the current-mode filter. The reader is referred to [3.62] for more information.

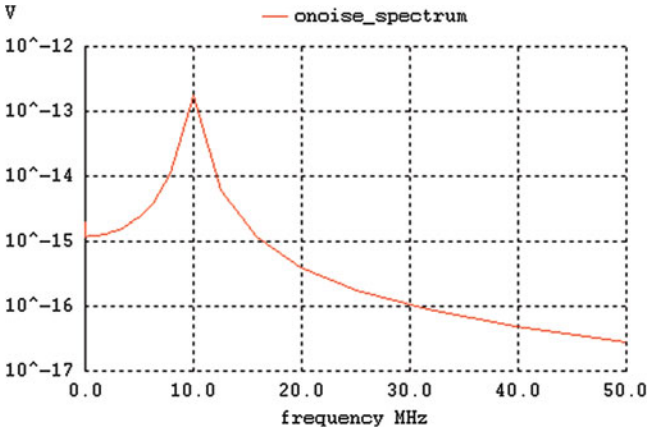
Example 3.3 Analyze the noise of the OTA-C biquad of Fig. E.3.1 with $C_1 = C_2 = 10$ pf and $C_1 = C_2 = 50$ pf and appropriate G_m values to realize the same pole frequency and pole-Q.

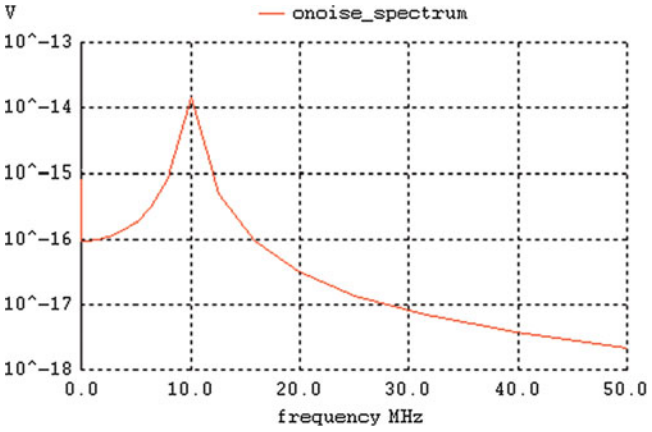
```
*OTA C two integrator loop noise analysis
gm1 2 0 11 0 628.57umho
gm3 3 0 0 31 628.57umho
gm4 2 0 41 0 628.57umho
gm2 2 0 0 21 62.857umho
C1 2 0 10pf
C2 3 0 10pf
*gm1 2 0 11 0 3142.85umho
*gm3 3 0 0 31 3142.85umho
*gm4 2 0 41 0 3142.85umho
*gm2 2 0 0 21 314.285umho
*C1 2 0 50pf
*C2 3 0 50pf
Xnoise1 1 11 0 Noisesources
Xnoise2 2 31 0 Noisesources
xnoise3 3 41 0 Noisesources
xnoise4 2 21 0 noisesources
.subckt noisesources in out grnd
V1 58 0 dc 0.1
V2 60 0 dc 0.1
D1 58 59 DIODE
R30 59 0 726.4
D2 60 61 DIODE
R31 61 0 726.4
E1 in out 59 61 1
V17 62 0 0
R32 62 0 73.6
FN1 out 0 V17 1
.ends noisesources
vin 1 0 ac 0
.noise v(3) vin dec 10 0.5 50000000 1
.MODEL DIODE D(AF=1.0,IS=0.001F,KF=1.667E-9)
```

The results with 10pF capacitors and the noise spectrum are as follows:

```
onoise_total = 2.914011e-07
onoise_total_d:xnoise1:d1 = 2.879963e-15
onoise_total_d:xnoise1:d1_1overf = 2.877193e-15
onoise_total_d:xnoise1:d1_id = 2.770007e-18
onoise_total_d:xnoise1:d1_rs = 0.000000e+00
onoise_total_d:xnoise1:d2 = 2.879963e-15
onoise_total_d:xnoise1:d2_1overf = 2.877193e-15
onoise_total_d:xnoise1:d2_id = 2.770007e-18
```

onoise_total_d:xnoise1:d2_rs = 0.000000e+00
onoise_total_d:xnoise2:d1 = 1.425000e-15
onoise_total_d:xnoise2:d1_1overf = 1.422244e-15
onoise_total_d:xnoise2:d1_id = 2.756068e-18
onoise_total_d:xnoise2:d1_rs = 0.000000e+00
onoise_total_d:xnoise2:d2 = 1.425000e-15
onoise_total_d:xnoise2:d2_1overf = 1.422244e-15
onoise_total_d:xnoise2:d2_id = 2.756068e-18
onoise_total_d:xnoise2:d2_rs = 0.000000e+00
onoise_total_d:xnoise3:d1 = 2.879963e-15
onoise_total_d:xnoise3:d1_1overf = 2.877193e-15
onoise_total_d:xnoise3:d1_id = 2.770007e-18
onoise_total_d:xnoise3:d1_rs = 0.000000e+00
onoise_total_d:xnoise3:d2 = 2.879963e-15
onoise_total_d:xnoise3:d2_1overf = 2.877193e-15
onoise_total_d:xnoise3:d2_id = 2.770007e-18
onoise_total_d:xnoise3:d2_rs = 0.000000e+00





3.14 Problems

P.3.1. It is possible to compensate the finite frequency dependent G_m of an OTA by using partial positive feedback using another OTA [3.63] as shown in Fig. P.3.1. Analyze the circuit and determine the condition for phase compensation.

P.3.2. Analyze the oscillators shown in Fig. 3.42 taking into account the finite output impedance of the OTAs. Derive the condition for oscillation and frequency of oscillation.

P.3.3. The table-based simulation technique of Hwang, Liu, Wu, and Wu [3.39] does not include floating capacitor simulation. Suggest solutions for realizing an OTA-C filter from the prototype ladder filter of Fig. P.3.3.

P.3.4. Analyze the effect of OTA output resistance and capacitance on the performance of OTA-C filters of Fig. 3.6a–c.

P.3.5. Derive a voltage-mode OTA-C filter from Friend's biquad of Fig. 2.11a and discuss the limitations/advantages.

P.3.6. Suggest methods of scaling the OTA-C filter of Fig. 3.6a for optimal dynamic range.

P.3.7. Derive a current-mode OTA-C fiter from Friend's active RC biquad of Fig. 2.11a using the technique of Ahmed, Awad, and Soliman [3.58].

P.3.8. Analyze the sensitivities of a fourth-order OTA-C filter realized using the technique of Fig. 3.36a.

P.3.9. Analyze the effect of mismatch of current mirrors used to obtain multiple output currents on the performance of the OTA-C filter of Fig. 3.16.

P.3.10. Analyze the effect of finite output resistance and output capacitance of the OTAs on the performance of the first-order circuits of Fig. 3.4.

P.3.11. Analyze the effect of nonideal OTA on the performance of the first-order all-pass filters of Fig. 3.5c–j. Use SPICE to verify your results.

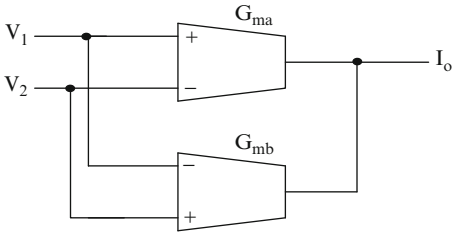


Fig. P.3.1

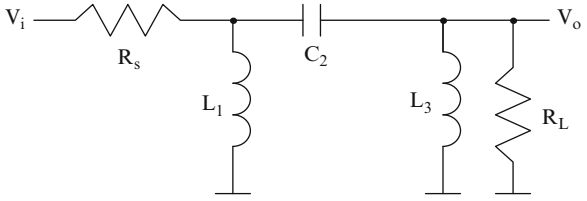


Fig. P.3.3

P.3.12. Analyze the effect of the frequency response of OTA on the pole-frequency and pole-Q of the OTA-C filter of Fig. 3.16.
P.3.13. Derive an OTA-C filter from the third-order elliptic filter prototype low-pass filter showing all component values. Analyze the effect of parasitics of all OTAs using SPICE.
P.3.14. Using SPICE, compare the OTA-C filter of Fig. 3.30b with that of Fig. 3.28d.
P.3.15. Derive OTA-C filters not needing buffers from the circuit of Fig. 3.43d.
P.3.16. Derive an OTA-C filter from Bach's active RC filter of Fig. P.2.13 using the nodal voltage simulation technique.
P.3.17. Derive a voltage-mode OTA-C filter from the KHN active RC biquad using the nodal voltage simulation technique. Compare with the current-mode filter of Fig. 3.44b.
P.3.18. Derive the various voltage and current transfer functions of the OTA-C filter of Fig. 3.21b. Show how band-stop, low-pass, and high-pass current transfer functions can be obtained.
P.3.19. Derive all the voltage and current transfer functions of the OTA-C biquad of Fig. 3.21c.
P.3.20. Derive the voltage and current transfer functions of the circuit of Fig. 3.21d under the condition $I_{in1} = I_{in2} = I_{in}$, $G_{m1} = G_{m2} = G_{m3}$, $C_2 = C_3$. Also derive the various transfer functions with $I_{in2} = 0$ and discuss their utility.
P.3.21. Show that low-pass, noninverting high-pass current transfer functions are available from the circuit of Fig. 3.21e.
P.3.22. Derive the various transfer functions of the circuit of Fig. 3.22a–e and compare them.

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Chapter 4
Switched Capacitor Filters

The main limitation of active resistor–capacitor (RC) filters or operational transconductance amplifier (OTA)-capacitor (OTA-C) filters is that the performance is dependent on the component values thereby needing some techniques for automated tuning. This has spurred research into alternative technologies wherein the tuning requirements are not present. One such technique is the switched-capacitor technique which was invented before OTA-C filters were popularized. In this chapter, we study the topic of switched capacitor (SC) filter design in a systematic manner.

4.1 Basic Concept of Switched-Capacitor Resistor

The realization of a resistor using an SC [4.1, 4.2, 4.3] is shown in Fig. 4.1a. This circuit uses two metal-oxide semiconductor (MOS) switches and a MOS capacitor. The switches are driven by a two-phase, nonoverlapping clock, as shown in Fig. 4.1b. In phase 1, the capacitor C_1 is connected to the voltage source v_1 by closing the switch S_1. Thus, the capacitor C_1 charges to the voltage v_1 and has the charge C_1v_1. In phase 2, the switch S_2 is turned on and switch S_1 is turned off. Thus, the capacitor has the charge C_1v_2. In effect, the charge that has been transferred is $(C_1v_1-C_1v_2)$ in a time interval T. Noting that current i is defined as

$$i = \frac{\textit{incremental}\ \text{charge}\ \textit{flown}}{\textit{time}} = \frac{dq}{dt} \tag{4.1}$$

we have

$$i = \frac{C_1\,(v_1 - v_2)}{T} = \frac{(v_1 - v_2)}{\left(\frac{T}{C_1}\right)} = \frac{(v_1 - v_2)}{R} \tag{4.2}$$

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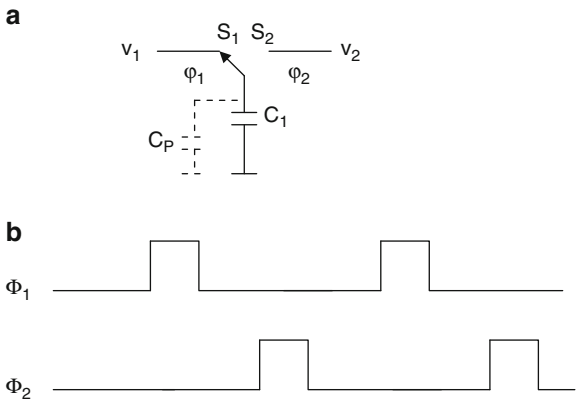


Fig. 4.1 (**a**) Resistor realization using a switched capacitor and (**b**) switching waveforms used in (a)

Thus an effective resistance of T/C_1 is realized. This quickly leads to the observation that resistance can be tuned by changing the sampling frequency $f_s = 1/T$. In addition, note that a very small value of capacitance C_1 can realize a very large resistance. For example, a 0.01-pF capacitor with a sampling frequency of 1 MHz can realize a resistance of value 100 MΩ.

Now, consider the circuit of Fig. 4.2a; by replacing the resistor R_1 with an *SC*, we obtain the *SC* low-pass filter shown in Fig. 4.2b. The time constant τ needed in the *RC* circuit is R_1C_2, which corresponds to

$$\tau = R_1\ C_2 = \left(\frac{T}{C_1}\right) C_2 = T\left(\frac{C_2}{C_1}\right) \tag{4.3}$$

It is very interesting to note that the time constant is controlled by the *ratio of capacitors* and a controllable parameter *clock period T*. The ratios are controlled by the mask design accurately delineating the areas of capacitors C_1 and C_2. Thus the pole frequency of filters using this technique can be controlled by ratios of capacitors, an attractive proposition.

The grounded capacitors used in Figs. 4.1a and 4.2b have parasitic capacitance of top plates C_{p1} and C_{p2}, as shown in Fig. 4.2c, which increases the value of C_1 to $(C_1 + C_{p1})$ and C_2 to $(C_2 + C_{p2})$, thus changing the realized time constant. The parasitic at the bottom plate of the capacitor is nonlinear and generally high (of value 20–30% of the capacitance value C_1). Since the bottom plate of the capacitance C_1 is connected to ground, this parasitic capacitance does not contribute to any errors.

In a similar manner, an inverting SC integrator can be obtained by replacing the resistor in an active RC integrator with an SC. The resulting circuit is shown in Fig. 4.3a. Note that the parasitic capacitance across C_1 changes the time constant of the integrator from $T(C_2/C_1)$ to $T(C_2/(C_2 + C_{p1}))$. It is therefore necessary to have techniques where the circuits can be made *parasitic-insensitive* or *stray-insensitive*. This is possible by using the circuit shown in Fig. 4.3b [4.4]. Note that in this circuit,

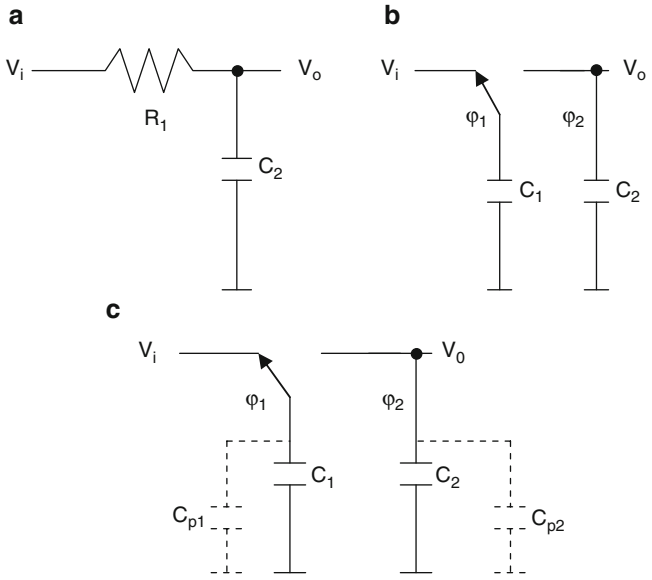


Fig. 4.2 (**a**) First-order RC low-pass filter, (**b**) circuit obtained using a switched-capacitor in place of resistor R, and (**c**) actual realized circuit including parasitic capacitances

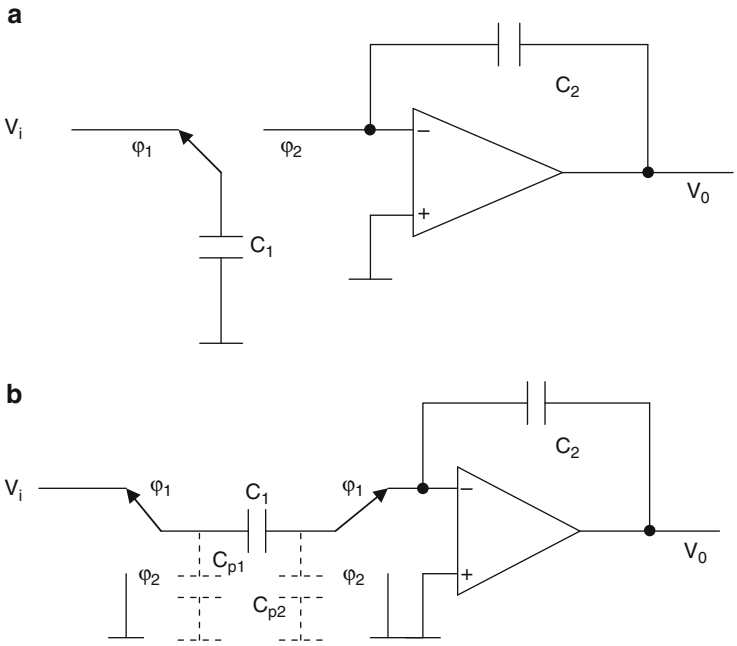


Fig. 4.3 SC integrators: (**a**) a parasitic-sensitive inverting integrator, and (**b**) a stray-insensitive inverting integrator

the parasitic capacitances are also shown. In phase 1, the capacitor C_1 charges to the input voltage and transfers the charge to the capacitor C_2, which still has the charge obtained in previous such operations. In phase 2, the capacitor C_1 is discharged since both terminals are grounded. The parasitic capacitance C_{p1} is charged to input and discharged to ground, thus not transferring any input-dependent charge to capacitor C_1. On the other hand, the parasitic capacitance C_{p2} is charged to *virtual ground* considering that the opamp has high gain and is discharged to ground, thus not causing any charge transfer to C_2. The circuit is therefore parasitic-insensitive.

SC circuits can be analyzed by writing a charge conservation equation at various nodes in the network in each phase. However, it is convenient and efficient to use the z-domain equivalent circuits as described by Laker [4.5]. We consider this technique in the next section so that it can be used as a tool to derive the transfer functions of complex SC networks.

4.2 Analysis of SC Filters

4.2.1 Laker's z-Domain Equivalent Circuit Method

In SC circuits, either terminal of a capacitor may be connected in either phase 1 or phase 2 to some other capacitors, voltage sources, ground or virtual ground, or positive or negative input of opamps [4.5]. Thus, charge transfer takes place between various capacitors during either phase. Consider a capacitor in the SC network shown in Fig. 4.4a. Charge flows through terminal 1 in both phases of the clock and leaves from terminal 2. Since the capacitor is bilateral, similarly, charge enters the capacitor at terminal 2 and leaves from terminal 1. There is a time delay between the present phase and the next phase. We denote the two phases as "even" and "odd" for convenience and the suffix "*e*" stands for *even* phase and "*o*" stands for *odd* phase. With these basic ideas in mind, we can write the following four equations at both terminals 1 and 2 in each phase.

$$\Delta Q_{1e}(z) = C(V_{1e} - V_{2e}) - C(V_{1o} - V_{2o})\, z^{-\frac{1}{2}} \tag{4.4a}$$

$$\Delta Q_{1o}(z) = C(V_{1o} - V_{2o}) - C(V_{1e} - V_{2e})\, z^{-\frac{1}{2}} \tag{4.4b}$$

$$\Delta Q_{2e}(z) = C(V_{2e} - V_{1e}) - C(V_{2o} - V_{1o})\, z^{-\frac{1}{2}} \tag{4.4c}$$

$$\Delta Q_{2o}(z) = C(V_{2o} - V_{1o}) - C(V_{2e} - V_{1e})\, z^{-\frac{1}{2}} \tag{4.4d}$$

where ΔQ is the incremental charge flowing into the terminal during the phase under consideration. Note that all the z transforms of variables appear in (4.4). Equations (4.4a, 4.4b, 4.4c, 4.4d) mean that the incremental charge flow into any

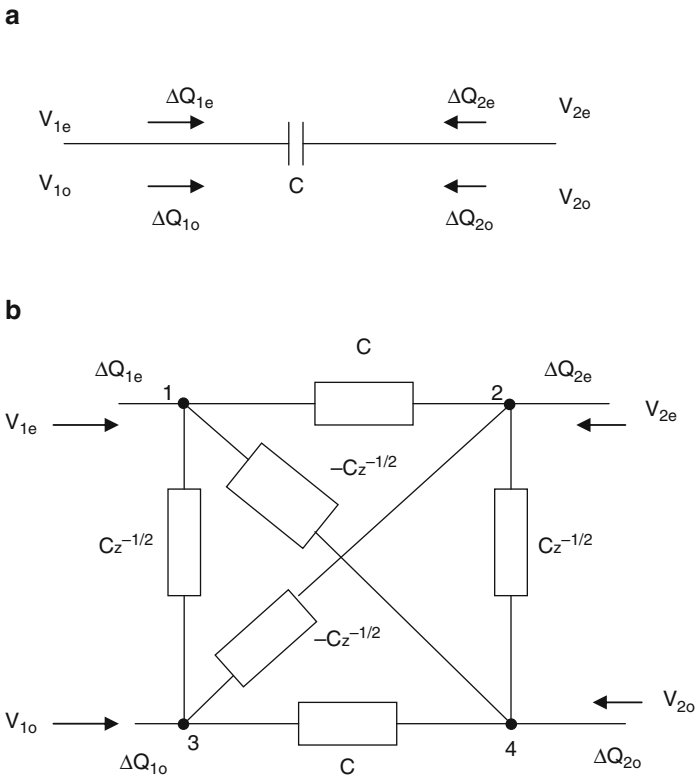


Fig. 4.4 (**a**) A capacitor in an SC circuit and (**b**) its z-domain equivalent circuit

terminal is given by (present charge – previous charge) and the term $z^{-1/2}$ indicates the timing relationship "*previous*" to "*present*," implying a delay of a half-cycle.

Laker [4.5] has observed ingeniously that the four equations can be completely represented by the equivalent circuit given in Fig. 4.4b. These four equations are basically charge-to-voltage relationships and hence the voltage differences need to be multiplied by capacitances. Note that each node in the original circuit becomes two nodes labeled "even" and "odd" by the suffixes e and o, respectively. However, the term $Cz^{-1/2}$ is not just a capacitor but has a delay in addition. Although the equivalent circuit looks bewildering, in practical circuits, the use of the equivalent circuit considerably simplifies the analysis. Note that the opamp in SC circuits is considered as two opamps: one in the even phase and one in the odd phase.

As an illustration, consider the SC integrator shown in Fig. 4.5a. Substituting Laker's z-domain equivalent circuit for both the capacitors and using two opamps, the interconnection in the original circuit can be transferred to the equivalent circuit. Thus, the circuit of Fig. 4.5b is obtained. Fortunately, much simplification can be made by noting the following. The connection of any component between

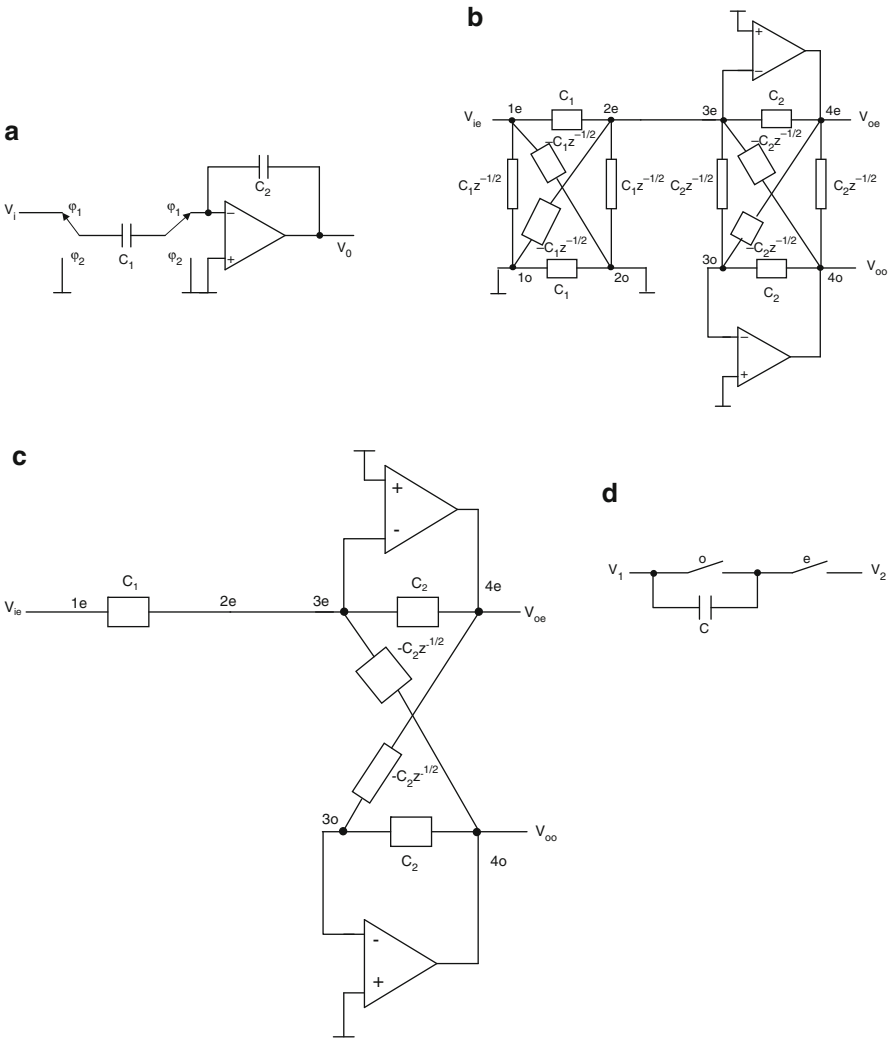


Fig. 4.5 (**a**) An SC integrator, (**b**) a z-domain equivalent circuit, (**c**) a simplified version of (b), and (**d**) a series-switched capacitor

virtual grounds of two opamps or two output terminals of two opamps does not contribute to the circuit. Hence, these can be deleted. Similarly, a component between ground and virtual ground or source to ground also does not serve any purpose. With these simplifications, we get the much simpler circuit of Fig. 4.5c. This circuit can be analyzed easily by writing two charge conservation equations (CCEs) at nodes 3e and 3o:

$$V_{ie}\, C_1 + V_{oe}\, C_2 - V_{oo}\, C_2\, z^{-1/2} = 0 \tag{4.5a}$$

and

$$V_{oo}\, C_2 - V_{oe}\, C_2\, z^{-1/2} = 0 \tag{4.5b}$$

Solving these two equations, we obtain the transfer function of the circuit as

$$\frac{V_{oe}}{V_{ie}} = -\frac{C_1}{C_2\,(1 - z^{-1})} \tag{4.6a}$$

$$V_{oo} = V_{oe}\, z^{-1/2} \tag{4.6b}$$

This corresponds to a *stray-insensitive inverting integrator*. Note that Eq. 4.6b means that the output in the odd phase is a "half-cycle delayed version of the output in the even phase." In other words, we can say that "the output is held over a clock period." This is since the charge transfer takes place to the integrating capacitor in only one phase. We also note that V_{io} has no effect since the input is disconnected from the circuit in the odd phase. In general, note that there are four transfer functions possible for a two-phase SC circuit: v_{oe}/v_{ie}, v_{oo}/v_{ie}, v_{oe}/v_{io}, and v_{oo}/v_{io}. It is convenient to ensure that charge transfer takes place in only one phase so that circuits can be cascaded without needing an interface in between. In addition, the opamp will have enough time to settle, that is, to enable the capacitors to charge to the final signal voltage value.

If we wish to consider the output in the odd phase, we have seen from Eqs. 4.6a and 4.6b that

$$\frac{V_{oo}}{V_{ie}} = -\frac{C_1\, z^{-1/2}}{C_2\,(1 - z^{-1})} \tag{4.6c}$$

This corresponds to a lossless discrete integrator (LDI) type [4.6, 4.7] using LDI type of $s \rightarrow z$ transformation given as $s \rightarrow \dfrac{1 - z^{-1}}{T\, z^{-1/2}}$. On the other hand, if we choose Eq. 4.6a itself, it corresponds to the backward Euler transformation [4.7]; that is, $s \rightarrow \dfrac{1 - z^{-1}}{T}$. This SC branch comprising C_1 and the associated four switches in Fig. 4.5a is known as a *series-switched capacitor*, and in the original form was presented as shown in Fig. 4.5d [4.2]. Intuitively, the capacitor is discharged in one phase so that it loses its "memory," making it a resistor causing charge transfer only in one phase. In this form, however, the branch will be affected by the parasitic capacitances and thus not used in practice.

4.3 First-Order SC Circuits

Armed with the equivalent circuit, we can quickly derive the transfer functions of SC circuits. Some first-order SC circuits are presented in Fig. 4.6a–d. SCs can facilitate some tricks to simplify the hardware.

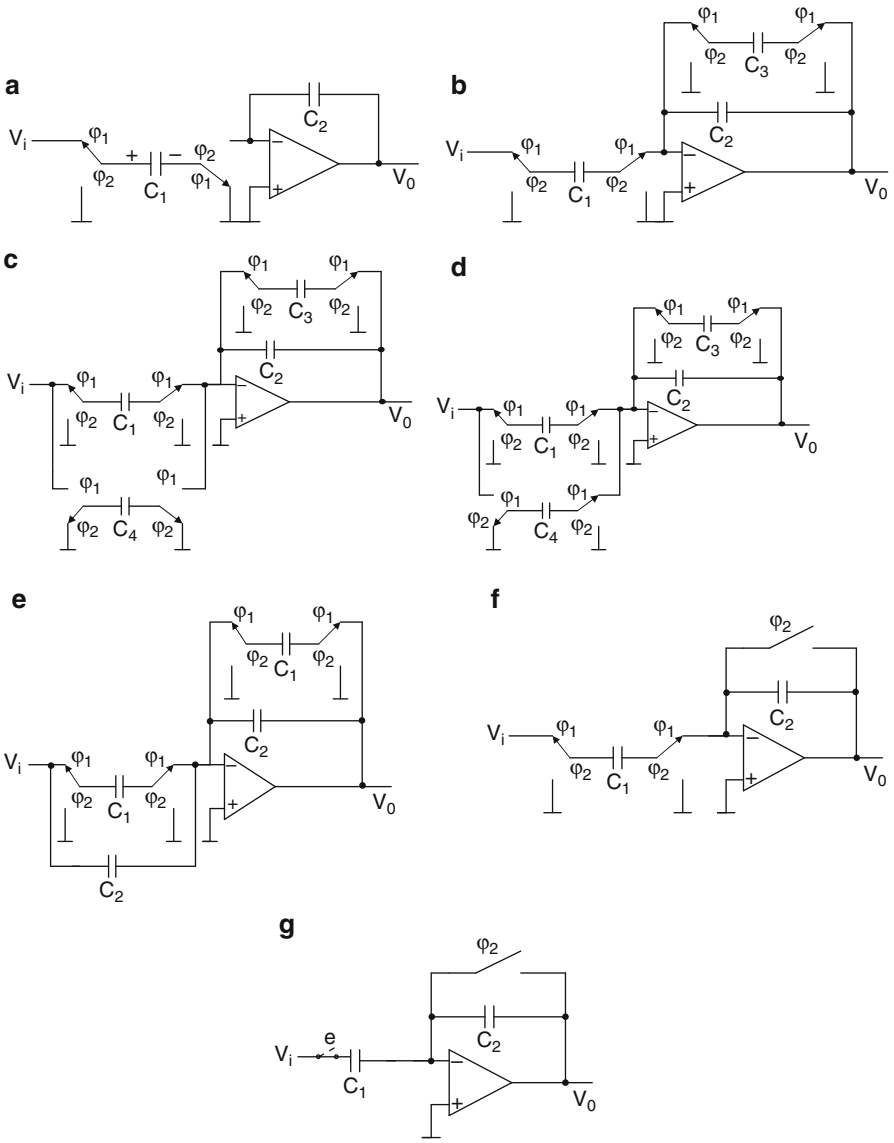


Fig. 4.6 SC building blocks: (**a**) a noninverting integrator, (**b**) a lossy inverting integrator, (**c**) a bilinear integrator (Adapted from [4.8] © IEE 1980), (**d**) a first-order circuit with output held over a clock period (Adapted from [4.9] © IEE 1982), (**e**),(**f**) SC amplifiers(Adapted from [4.10] © IEEE 1983), (**g**) an SC differentiator, (**h**) an SC differentiator using fully differential output opamp (Adapted from [4.11] © IEEE 1992), (**i**) an integrator with input and feedback capacitors multiplexed (Adapted from [4.12] © IEEE 1984), and (**j**) an all-pass filter (Adapted from [4.12] © IEEE 1984)

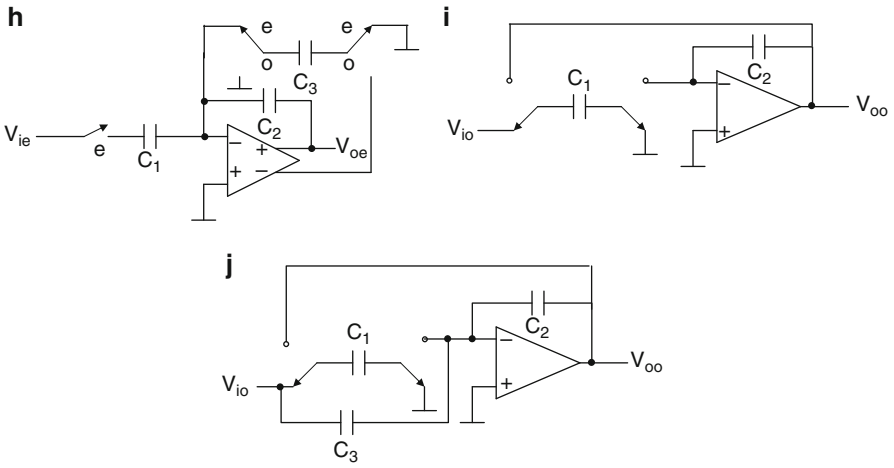


Fig. 4.6 (continued)

A noninverting integrator [4.1] can be obtained by simple change of the input SC, as shown in Fig. 4.6a. This circuit also is stray-insensitive. Note that in this circuit, the capacitor C_1 is charged to the input voltage in phase ϕ_1. Consider that V_{in} is positive, for illustration; the capacitor terminals assume the polarity as shown. Hence, in the other phase, when the input is grounded, the capacitor looks as though it has negative voltage in series which is transferred to C_2. Thus a noninverting integrator can be realized by just interchanging the controlling phases of the input switches. The circuit of Fig. 4.6a thus saves one opamp additionally needed to realize a noninverting integrator from an inverting integrator.

A lossy integrator is presented in Fig. 4.6b, which is easily obtained by shunting the integrating capacitor with a resistance simulated using an SC. The transfer function of the lossy integrator is given by

$$\frac{V_{oe}}{V_{ie}} = -\frac{C_1}{C_2\,(1 - z^{-1}) + C_3} \tag{4.7}$$

The circuit evidently is stray-insensitive and has output held over a clock period.

The circuit of Fig. 4.6c [4.8] realizes a transfer function given by

$$V_{oe} = -\frac{C_1\,V_{ie} + C_4\,V_{io}\,z^{-1/2}}{C_2\,(1 - z^{-1}) + C_3} \tag{4.8a}$$

Hence a bilinear integrator is realized under the condition $V_{io} = V_{ie}z^{-1/2}$ and $C_1 = C_4$, with a transfer function given as

$$\frac{V_{oe}}{V_{ie}} = -\frac{C_1\,(1 + z^{-1})}{C_2\,(1 - z^{-1}) + C_3} \tag{4.8b}$$

Evidently, when $C_3 = 0$, a lossless integrator is realized. This means that the circuit realizes the bilinear transformation $s \rightarrow \frac{2}{T}\left(\frac{1-z^{-1}}{1+z^{-1}}\right)$. However, the realization of an exact bilinear lossy integrator is not possible. The reader is urged to verify this. Note that the output in the other phase can be shown to be

$$\frac{V_{oo}}{V_{ie}} = -z^{-1/2}\,\frac{C_4\,(C_{12}+C_3)+C_1\,C_2}{C_2\,(C_2\,(1-z^{-1})+C_3)} \tag{4.8c}$$

It will often be required to realize a general first-order transfer function with output held over a clock period, which is feasible using the circuit shown in Fig. 4.6d. The transfer function of this circuit [4.9], which uses a noninverting and inverting SC in the feedforward path, is given by

$$\frac{V_{oe}}{V_{ie}} = -\frac{C_1 - C_4\,z^{-1}}{C_2\,(1-z^{-1})+C_3} \tag{4.9}$$

As an illustration, for realizing a first-order, digital, all-pass filter transfer function

$$\frac{V_{oe}}{V_{ie}} = -\frac{a-z^{-1}}{1-a\,z^{-1}} \tag{4.10}$$

we have

$$a = \frac{C_1}{C_4} = \frac{C_2}{C_2+C_3} \tag{4.11}$$

The gain of the all-pass filter is $\frac{C_4}{C_2+C_3}$. Note that in the case $C_1 = C_4$, a first-order high-pass filter is realized.

Yet another interesting circuit shown in Fig. 4.6e is used to realize an amplifier [4.10]. Note that other simpler circuits for realizing amplifiers are feasible (see Fig. 4.6f). But this circuit has the problem that it cannot work at very high frequencies since the opamp acts as a buffer in one clock phase and its output will be at ground potential. The opamp output needs to make the transition from signal level to ground and ground to the new input signal value. Such a problem does not exist for the amplifier shown in Fig. 4.6e.

An SC differentiator is presented in Fig. 4.6g. This circuit realizes a transfer function given by

$$\frac{V_{oe}}{V_{ie}} = -\frac{C_1\,(1-z^{-1})}{C_2} \tag{4.12}$$

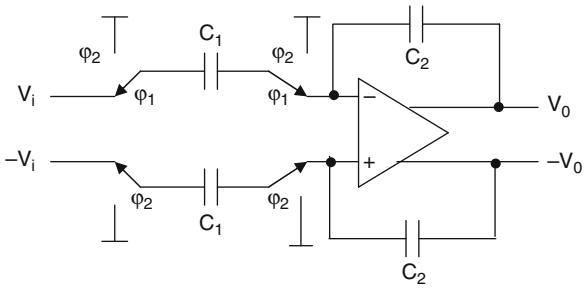


Fig. 4.7 A fully differential SC integrator

Note that this circuit has the same limitation that the opamp needs to "slew" fast from ground level to the signal value. The output exists only in the even phase.

An alternative SC differentiator [4.11] using a fully differential configuration of the opamp is shown in Fig. 4.6h. Note that the memory of the capacitor C_2 can be destroyed by connecting capacitor C_3 since the z-domain equivalent feedback will be $C_2(1-z^{-1}) + C_3 z^{-1} = C_2$ when $C_2 = C_3$. The output is held over a clock period for an input that also is held over a clock period.

It is possible to reduce the component count in certain SC building blocks by multiplexing the switched capacitors. As an illustration, a damped integrator is shown in Fig. 4.6i that uses only two capacitors. The transfer function of this circuit, known as a *direct transfer integrator* [4.12, 4.13], can be derived as

$$\frac{V_{oo}}{V_{io}} = \frac{C_1\ z^{-1}}{(C_1 + C_2) - C_2\ z^{-1}} \tag{4.13a}$$

$$V_{oe} = V_{oo}\ z^{-1/2} \tag{4.13b}$$

under the condition $V_{ie} = V_{io}\ z^{-1/2}$.

The modified circuit of Fig. 4.6j realizes a first-order all-pass transfer function given by

$$\frac{V_{oo}}{V_{io}} = \frac{(C_1 + C_3)\, z^{-1} - C_3}{(C_1 + C_2) - C_2\ z^{-1}} \tag{4.14}$$

under the condition $C_2 = C_3$.

Just in the case of active *RC* circuits, fully differential SC circuits are recommended to have better performance. A typical fully differential *SC* integrator corresponding to Fig. 4.6a is presented in Fig. 4.7.

Second-order SC filters are the most important building blocks and these use the first-order blocks described in Figs. 4.5a and 4.6. We consider these in detail in the next section.

4.4 Stray-Insensitive SC Biquads

4.4.1 Fliescher–Laker SC Biquad

Perhaps the most popular SC biquad is from Fleischer and Laker [4.14], shown in Fig. 4.8a. This circuit is based on the two-integrator loop. Note that earlier simplified versions of this biquad were presented by other authors [4.15, 4.16]. The switched/unswitched capacitors A, B, and F form a lossy noninverting integrator. The switched/unswitched capacitors C and D form a lossless inverting integrator. The switched capacitor branches G, H, I, and J are feedforward capacitors. Note that among the capacitors E and F, only one is sufficient to provide damping. We also observe that the output can be taken at opamp 1 with the output denoted T' or at opamp 2 with the output denoted T. It is interesting to note that all charge transfer takes place only in the even phase, that is, ϕ_1. Evidently, the outputs are held over a clock period. As a first step, we use Laker's equivalent circuit method to obtain the z-domain equivalent circuit shown in Fig. 4.8b.

By writing the charge conservation equations at the virtual ground input of the opamps in the z-domain equivalent circuit, the transfer functions T and T' can be found as follows.

$$\frac{V_o(z)}{V_i(z)} = T = \frac{-DI + z^{-1}(DI + DJ - AG) + (AH - DJ)z^{-2}}{D(B+F) + z^{-1}(AC + AE - 2BD - FD) + (BD - AE)z^{-2}} \tag{4.15a}$$

and

$$\frac{V'_o(z)}{V_i(z)} = T' = \frac{\begin{pmatrix} -G(B+F) + I(C+E) + z^{-1}(GB + HB + FH \\ -CJ - IE - EJ) + (EJ - HB)z^{-2} \end{pmatrix}}{D(B+F) + z^{-1}(AC + AE - 2BD - FD) + (BD - AE)z^{-2}} \tag{4.15b}$$

Note that in these two transfer functions, one can choose $E = 0$ or $F = 0$. It can be seen from the numerators of Eqs. 4.15a and 4.15b that the numerator is decided by G, H, I, and J, the feedforward capacitors. Moreover, in the case of the T circuit, the numerator is independent of the capacitors E, C, F, and B. The design of the circuit can be carried out by matching Eqs. 4.15a and 4.15b with the desired z-domain transfer function. We next illustrate the elegant design procedure described by Laker and Fleischer [4.14].

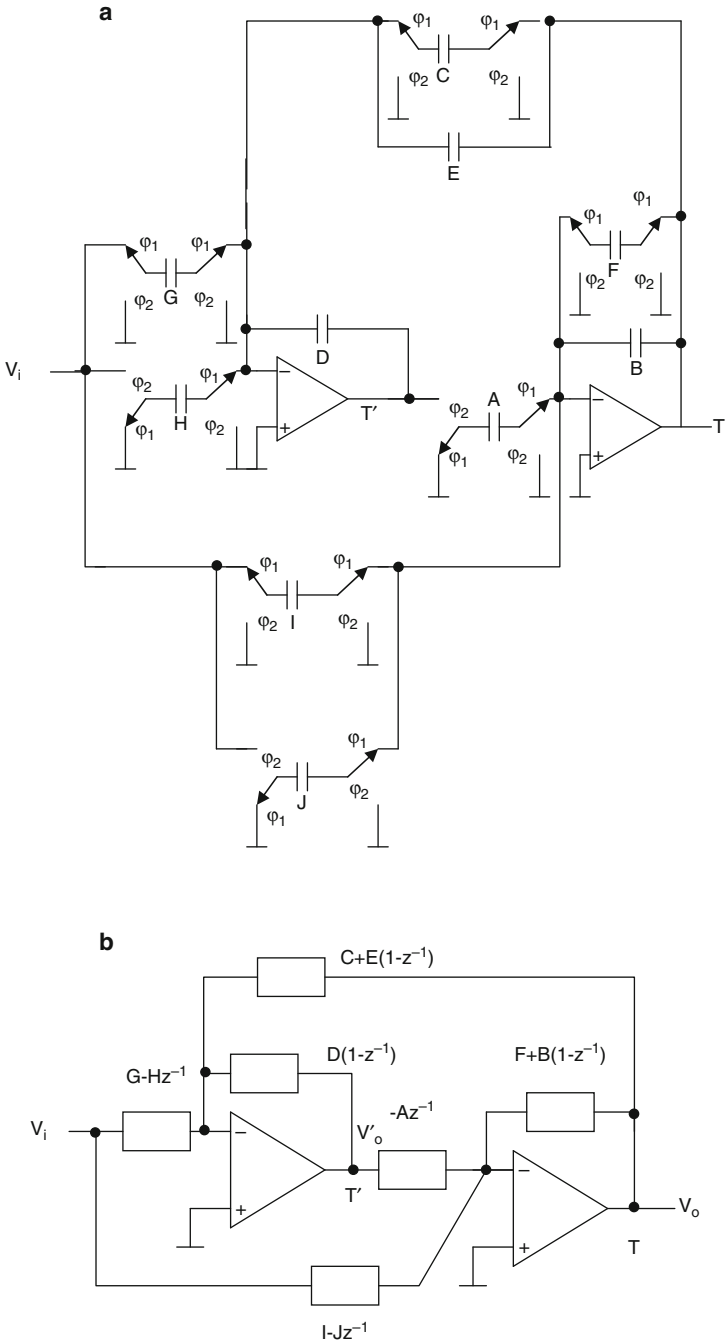


Fig. 4.8 (**a**) Fleisher–Laker SC biquad, and (**b**) z-domain equivalent circuit of (**a**) (**a** Adapted from [4.17] © IEEE1989, **b** Adapted from [4.20] © IEEE1986)

4.4.2 Design Procedure

(a) First choose $A = B = D = 1$ since there are only two parameters to be realized by the denominator: the pole-Q and pole frequency. The simplified transfer functions are:

$$\frac{V_o(z)}{V_i(z)} = T = \frac{-I + z^{-1}(I + J - G) + (H - J)z^{-2}}{(1 + F) + z^{-1}(C + E - 2 - F) + (1 - E)z^{-2}} \tag{4.16a}$$

and

$$\frac{V'_o(z)}{V_i(z)} = T' = \frac{\left(-G(1 + F) + I(C + E) + z^{-1}(G + H + FH - CJ - IE - EJ) + (EJ - H)z^{-2}\right)}{(1 + F) + z^{-1}(C + E - 2 - F) + (1 - E)z^{-2}} \tag{4.16b}$$

Thus, C and F for the F circuit ($E = 0$) or C and E for the E circuit ($F = 0$) can decide the denominator. However, the scaling step described later will bring the final A, B, and D values to the correct values.

(b) Determine the values of all the other capacitors. While doing so, it will be advantageous to go for choices such as $I = 0$ and avoid choices that involve matching of capacitors, for example, $J - I = 0$. This is often feasible since four degrees of freedom G, H, I, and J exist whereas only three are needed to decide the numerator.

(c) The next step is to substitute the various values of capacitors obtained in Eqs. 4.16a and 4.16b. Then scale the various capacitances in the circuit so as to have optimal dynamic range. This involves calculating the maxima of the transfer functions at the T and T' outputs and equalizing them. Interestingly, closed-form expressions for the maxima of a second-order digital transfer function are available (see Appendix A). Using these formulae, the maximum of T', in the case where T is the desired output, can be determined. The maximum of T is known since the given specification of the filter decides this maximum value. In a similar manner, if T' is the desired output, maxima of both T and T' can be determined. We denote next $\mu = T_{\max}/T'_{\max}$. Note that μ can be greater or less than 1. Our aim is to see that $T'_{\max}$ is brought to $\mu T'_{\max}$. This is made possible by dividing all the capacitors associated with the T' (i.e., capacitors A and D) by μ. In other words, they become A/μ and D/μ. Thus, when D is scaled to D/μ, the output $T'_{\max}$ has changed to $\mu\, T'_{\max}$. This, however, changes the output T to μT. To keep T at the old value decided by the specification, we need to maintain the loop gain constant. This is achieved by scaling A to A/μ. On the other hand, if we wish to scale $T_{\max}$ to the desired value when $T'_{\max}$ is the desired output, we need to scale B, F, C, and E.

(d) At this stage, some equivalences can be used to reduce two capacitors to one, thus saving area. Specifically if $G = H$ (or $I = J$), instead of using two capacitors of value G, one unswitched capacitor can be used, thereby saving the associated switches as well. This point can be appreciated by observing the z-domain

equivalent circuit of Fig. 4.8b. Under this condition, the branch ($G-Hz^{-1}$) becomes $G(1-z^{-1})$, thus enabling the use of a single unswitched capacitor.

(e) The next step is to scale the circuit for minimum total capacitance. After the previous step outlined in (d), the capacitor values associated with each opamp are grouped as ABFIJ and CDEGH so all the capacitors in each group are connected to the same virtual ground node (inverting input of the opamp). Denoting the smallest capacitance in each group as C_u, the unit capacitor, all the other capacitors can be expressed in terms of this smallest capacitor. This enables computing the total capacitance in both the groups in terms of C_u. Next, summing these total capacitances in both groups, the total capacitance needed for the complete biquad can be obtained. The capacitor spread needed also will be evident at this stage.

(f) The last step is to combine the switches. It can be seen from Fig. 4.8a that all the switches connected to the node N do the same function-transferring charge to the feedback capacitors in ϕ_1 and getting grounded in ϕ_2. Thus, these can be combined to reduce the number of switches. This is important to save on the area as well as other problems associated with the switches discussed later.

This completes the design of the SC biquad. Several options are available: (1) output can be taken at T or T', (2) E or F can be zero, or (3) only three among G, H, I, and J will be needed – therefore, computer-aided design packages are available that can explore the full design space and give an optimal design.

4.4.3 Capacitor Spread Evaluation

It is interesting to note that since the circuit in Fig. 4.8a is based on a two-integrator loop, the pole frequency and pole-Q sensitivities tend to be low [4.18]. However, it is required to estimate these so that among the various design choices, the better options can be chosen. The *SC* circuits are sampled-data systems, thus the sensitivity analysis needs to be carried out in the z-domain [4.17]. However, the analysis in the s-domain will lead to practical insights since specifications are often given in the s-domain and designers tend to use the bilinear $s \rightarrow z$ transformation to get the required digital transfer function. We use the inverse bilinear $s \rightarrow z$ transformation on the sampled-data transfer function to obtain two parameters, δ and Q, where $\delta = f_s/\omega_p$, with f_s as the clock frequency and ω_p corresponding to the prewarped pole frequency. Considering a general second-order denominator of the transfer function

$$D(z) = az^2 - bz + c \tag{4.17a}$$

using the relationship

$$s = \frac{2}{T}\left(\frac{1 - z^{-1}}{1 + z^{-1}}\right) \tag{4.17b}$$

with $T = 1/f_s$ as the clock period, we have the corresponding second-order analog transfer function as

$$D(s) = s^2 + s4f_s\left(\frac{a-c}{a+b+c}\right) + 4f_s^2\left(\frac{a-b+c}{a+b+c}\right) \tag{4.18}$$

Thus the two parameters δ and Q can be obtained as

$$\frac{1}{4\,\delta^2} = \left(\frac{a-b+c}{a+b+c}\right) \tag{4.19a}$$

and

$$\frac{1}{4\delta Q} = \left(\frac{a-c}{a+b+c}\right) \tag{4.19b}$$

It may be noted that in high pole-Q designs, the choice of equal time constants for the integrators yields optimal dynamic range. This implies that for the Fleischer–Laker biquad, the choice $A/B = C/D$ is appropriate. Next, without loss of generality, we consider $B = D = 1$. Thus, from the denominator of Eq. 4.15 and using Eq. 4.19 we have

$$\frac{\delta}{Q} = \frac{DF + AE}{AC} \tag{4.20a}$$

and

$$\frac{4\,\delta^2 - 2\frac{\delta}{Q} + 1}{4} = \frac{DB - AE}{AC} \tag{4.20b}$$

From Eq. 4.20, for the E and F circuits, the corresponding A and C values can be obtained as

E circuit ($F = 0$)

$$A = C = \frac{2}{\sqrt{4\,\delta^2 + 2\frac{\delta}{Q} + 1}},\quad E = \frac{2\dfrac{\delta}{Q}}{\sqrt{4\,\delta^2 + 2\frac{\delta}{Q} + 1}} \tag{4.21a}$$

F circuit ($E = 0$)

$$A = C = \frac{2}{\sqrt{4\,\delta^2 - 2\frac{\delta}{Q} + 1}},\quad F = \frac{4\dfrac{\delta}{Q}}{4\,\delta^2 - 2\frac{\delta}{Q} + 1} \tag{4.21b}$$

It is important to note the absence of square root in the expression for F in Eq. 4.21b. For high pole-Qs, (4.21) can be approximated as

E circuit ($F = 0$)

$$A = C = \frac{2}{\sqrt{4\,\delta^2 + 1}}, \quad E = \frac{2\dfrac{\delta}{Q}}{\sqrt{4\,\delta^2 + 1}} \tag{4.22a}$$

F circuit ($E = 0$)

$$A = C = \frac{2}{\sqrt{4\,\delta^2 + 1}}, \quad F = \frac{4\dfrac{\delta}{Q}}{4\,\delta^2 + 1} \tag{4.22b}$$

It can be seen that A and C values needed are the same for both the E and F circuits. However, for $\delta > \frac{\sqrt{3}}{2}$, we see that $E > F$, and for $\delta < \frac{\sqrt{3}}{2}$, we see that $E < F$.

4.4.4 Sensitivity Evaluation

It is relevant to examine the pole frequency and pole-Q sensitivities of both E- and F-type SC biquads. From Eq. 4.19a and the denominator of Eqs. 4.15a, 4.15b, we can express δ as

$$\delta = \sqrt{\frac{4DB + 2DF - 2AE - AC}{4AC}} \tag{4.23}$$

Thus, from Eqs. 4.20a and 4.23, the following sensitivity expressions can be obtained in terms of δ and Q.

F circuit:

$$S_A^\delta = S_C^\delta = -S_D^\delta = -\frac{1}{8\,\delta^2} - \frac{1}{2}, S_B^\delta = \frac{1}{8\,\delta^2} + \frac{1}{2} - \frac{1}{4\delta Q}, S_F^\delta = \frac{1}{4\delta Q} \tag{4.24a}$$

$$S_D^{\delta/Q} = S_F^{\delta/Q} = -S_A^{\delta/Q} = -S_C^{\delta/Q} = 1 \tag{4.24b}$$

E circuit:

$$\begin{aligned} S_A^\delta &= -\frac{1}{8\,\delta^2} - \frac{1}{2} - \frac{1}{4\delta Q}, S_C^\delta = -\frac{1}{8\,\delta^2} - \frac{1}{2}, S_B^\delta = S_D^\delta \\ &= \frac{1}{8\,\delta^2} + \frac{1}{2} + \frac{1}{4\delta Q}, S_E^\delta = -\frac{1}{4\delta Q} \end{aligned} \tag{4.24c}$$

$$S_D^{\delta/Q} = 0 = S_A^{\delta/Q}, S_E^{\delta/Q} = 1 = -S_C^{\delta/Q} \tag{4.24d}$$

4.5 Multiplexed Single-Amplifier SC Filters

4.5.1 Parasitic Compensated SC Biquads

The Fleischer–Laker biquad of Fig. 4.8a needs two opamps. It may be noted that both opamps in this biquad update the capacitors B and D in the even phase. In the odd phase there is no charge transfer and hence the opamps are idle. Interestingly, this fact can be used to multiplex the opamp in both phases, thus enabling the realization of the single-amplifier SC biquad seen in Fig. 4.9b [4.19, 4.20]. The z-domain equivalent circuit of Fig. 4.8b can be redrawn by changing the branch $-Az^{-1}$ to $-Az^{-1/2}$ and to compensate this, the branch C + E(1 − z^{-1}) becomes $Cz^{-1/2} + E(z^{-1/2} - z^{-3/2})$, as shown in Fig. 4.9a. This branch is realized as $Pz^{-1/2} - Qz^{-3/2}$ where $P = C + E$ and $Q = E$ to simplify the hardware. In addition, the input branch $(G - Hz^{-1})$ also needs to be changed to $(Gz^{-1/2} - Hz^{-3/2})$. This new z-domain equivalent circuit needs to be realized next.

The realization of the $z^{-1/2}$ term is possible using the fundamental parallel switched capacitor of Fig. 4.1a. But this circuit suffers from the parasitic capacitance of the top plate of the capacitor C_1. Thus, it is first required to obtain switched capacitors that are not affected by parasitic capacitances and realize the various $\Delta Q(z) - V(z)$ relationships of the form $C_i z^{-1/2}$, $C_i z^{-1}$, and $C_i z^{-3/2}$. Interestingly, these can be realized in a *parasitic-compensated* manner. This means that under matching conditions of capacitor values and identical layout of the circuit branches, the nonideal parasitics do not affect the performance to a first order.

The realization of the branch $Pz^{-1/2}$ is possible by first charging the series network of capacitors $2P$ and $2P + C_{P1} + C_{P2}$ to the input voltage in the even phase (see Fig. 4.9b) so that across $2P + C_{P1} + C_{P2}$ we have a voltage $\dfrac{2P}{4P + C_{P1} + C_{P2}}$ in the even phase. In the odd phase, the charge on the capacitor $2P + C_{P2}$ given as $\dfrac{2P(2P + C_{P2})}{4P + C_{P1} + C_{P2}} z^{-1/2}$ is available for integration by the feedback circuit. Under the matching condition $C_{P1} = C_{P2}$, we have the incremental charge voltage relationship given by $\dfrac{2P(2P + C_{P2})}{4P + C_{P1} + C_{P2}} z^{-1/2} = P z^{-1/2}$. In a similar manner, the branch realizing $Hz^{-3/2}$ transfers a charge given by $\dfrac{4H(4H + C_{P2})(4H + C_{P3})}{(8H + C_{P1} + C_{P2})(8H + C_{P2} + C_{P3})} z^{-3/2} = H z^{-3/2}$ under the matching condition $C_{P1} = C_{P2} = C_{P3}$. Note, however, that it is required to discharge the middle capacitor $4H$ using an additional clock phase ϕ_3 as shown in Fig. 4.9b and in the timing diagram in Fig. 4.9c. In a similar manner, $-Jz^{-1}$ also can be realized as shown. The remaining branches can be easily understood. It may be noted that the capacitors B and D have two switches [4.13] even though theoretically one switch to isolate the capacitor will do. This will help in reducing the clock feedthrough.

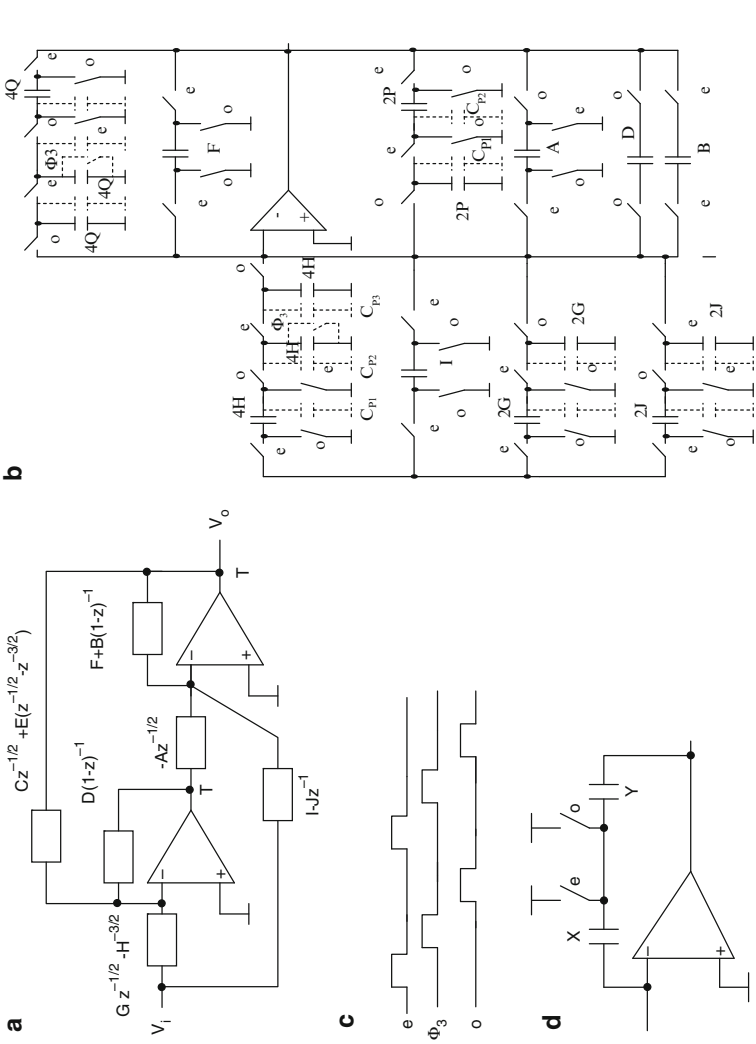


Fig. 4.9 (**a**) A modified z-domain equivalent circuit of a Fleischer–Laker biquad, (**b**) multiplexed single amplifier SC biquad based on (a), (**c**) switching waveforms, and (**d**) XY feedback (Adapted from [4.20] © IEEE 1986)

It may also be noted that during the interval between ϕ_1 and ϕ_2 (even and odd phases of the clock), the opamp feedback loop is open and hence the opamp tends to slew from its earlier output to ground thereby reducing the settling time to the new input. This can be avoided by a technique known as "*XY* feedback" which uses two dummy capacitors and two switches as shown in Fig. 4.9d. Note that the junction of capacitors *X* and *Y* is grounded during both phases, thus not affecting the charge transfer. On the other hand, during the interval between ϕ_1 and ϕ_2, the capacitors *X* and *Y* close the feedback loop and their charge is not going to affect the circuit operation. Other techniques involve no additional components but rely on the requirement that the interval between the nonoverlapping clock phases shall be less than the time required for the opamp's output to slew a small amount (e.g., a fraction of a volt). This, in turn, virtually eliminates the possibility of op-amp saturation during the nonoverlap period, at no extra cost to the SC multiplexed circuit.

The combination of *C* and *E* to one capacitor *P* will affect the sensitivity. The reader is urged to study the sensitivity of the pole-frequency and pole-*Q* to capacitors *P* and *Q*.

4.5.2 Multiplexed Single Opamp High-Order SC Filters

Roberts et al. [4.21] have described a technique for multiplexing an opamp to realize a high-order filter. This structure is stray-insensitive. For realizing an *N*th order filter, this structure needs $(2N + 1)$ clock phases and several switched capacitors. The block diagram and SC implementation of this structure are presented in Fig. 4.10a, b. The circuit uses a fully differential amplifier and hence the sign of the coefficients needed in filter realization, which may be positive or negative, can be easily realized. The z^{-1} blocks are realized by inverting switched-capacitor branches whereas the integrator function is realized by capacitors in the feedback path of opamps and switches. The block diagram can be best described by the well-known state–space description:

$$(z-1)X = AX + Bu \tag{4.25a}$$

$$Y = c^T X + du \tag{4.25b}$$

where $\boldsymbol{X}$ is the vector of state variables x_i.

Equation 4.25a updates the state variables x_i based on the input u_i and all the state variables x_i whereas (4.25b) is used to obtain the desired output y_i. The factor $1/(z-1)$ is realized by an integrator with transfer function $z^{-1}/(1-z^{-1})$.

The circuit has three stages of operation. In the computation stage, the *N* phases $\varphi_1, \varphi_2, \ldots, \varphi_N$ are used to compute the present state $x_i(k)$ for $i = 1$ to *N* using the weighted past state $x_j(k-1)$ for $j = 1, \ldots, N$ and the input $u(k-1)$. The *i*th state

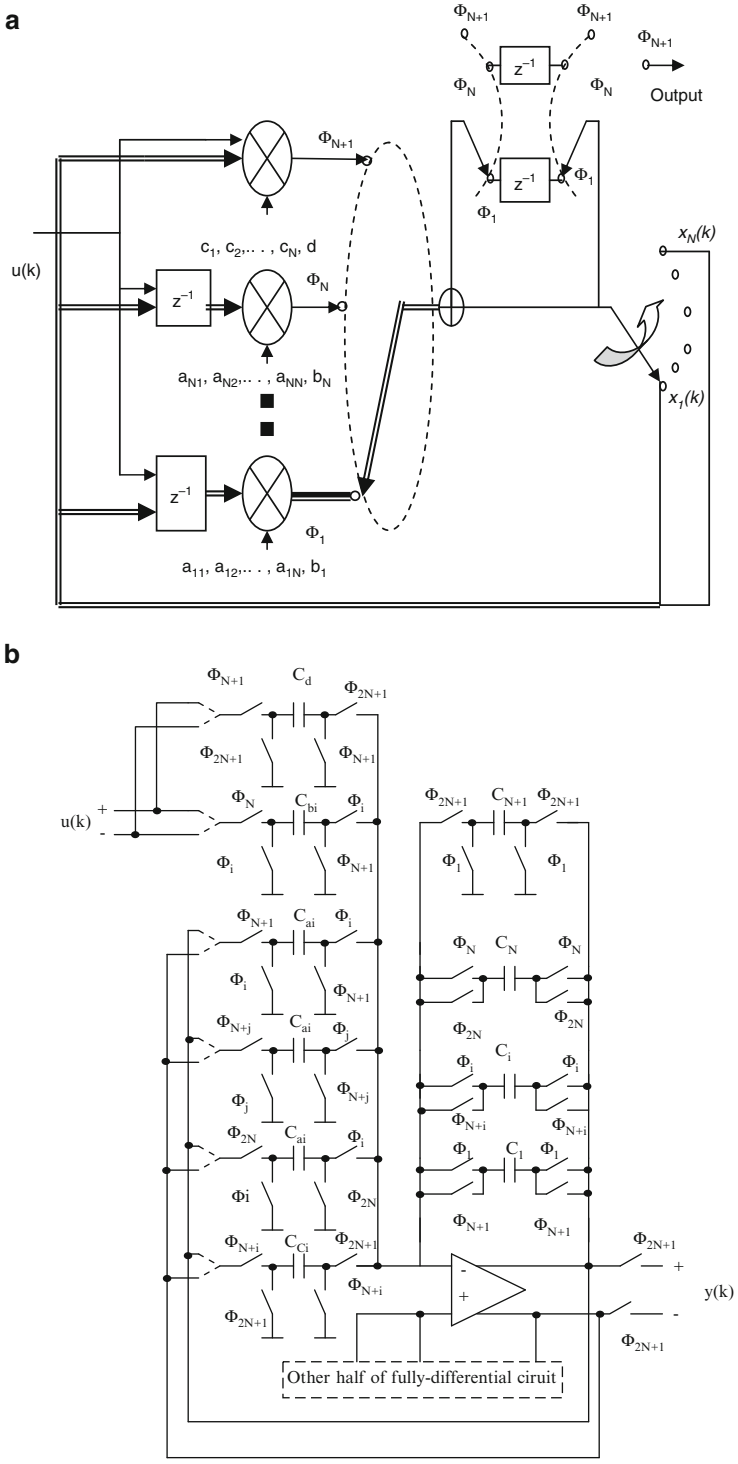


Fig. 4.10 (**a**) Functional representation of multiplexed filter, and (**b**) actual circuit of the multiplexed SC filter (Adapted from [4.21] © IEEE 1987)

computed is stored back on the feedback capacitor C_i. of the opamp. The past states are available on capacitors C_{aij} for $j = 1, \ldots, N$ and C_{bi}.

In the updating stage, the N phases φ_{N+1}, φ_{N+2}, …, φ_{2N} are used to copy the updated states on the appropriate switched-capacitors C_{ai} and C_{cj}. Note that the inputs are sampled in the $(N + 1)$th phase and stored on the capacitors C_{bi} and C_d.

In the $(2N + 1)$th phase, the output $y(k)$ is computed by summing the weighted present states and input according to (4.25b). Note that in Fig. 4.10b only one half is shown. It may be seen that the capacitor ratios in Fig. 4.10b are related to the various a, b, c, and d values in (4.25) as follows.

$$\frac{C_{a_{ij}}}{C_i} = a_{ij}, \frac{C_{b_i}}{C_i} = b_i, \frac{C_{c_i}}{C_{N+1}} = c_i, \frac{C_d}{C_{N+1}} = d \tag{4.26}$$

Note, however, that state–space filter design techniques need to be used translating the desired specifications into a realization as described by (4.25a, 4.25b).

4.6 Improved SC Biquads

4.6.1 Multiplexing of Capacitors

Several improvements have been suggested for the Fleischer–Laker biquad with a view to reducing the component spread or total area at the expense of sensitivity in some cases. Fischer and Moschytz [4.22] have suggested multiplexing the capacitor A to function as the capacitor F as well as capacitor A in the Fleischer–Laker biquad. In addition, one more inverting damping switched capacitor P is connected across the integrating capacitor B. The resulting transfer function of this circuit shown in Fig. 4.11 can be derived as

$$\frac{V_{oe}}{V_{ie}} = -\frac{AG\, z^{-1}}{D(B+A) - z^{-1}\,(2DB + PD + AD - AC) + z^{-2}\, D(B+P)} \tag{4.27}$$

It can be shown from the denominator of (4.27) and (4.19a, 4.19b) that

$$\frac{\delta}{Q_p} = \frac{D(A-P)}{AC} \tag{4.28a}$$

and

$$\frac{4\,\delta^2 - 2\frac{\delta}{Q_p} + 1}{4} = m = \frac{(B+P)D}{AC} \tag{4.28b}$$

Due to the difference term $(A - P)$ in (4.28a), the Q-sensitivity will be high. Denoting $P = kA$, and choosing $B = D = 1$, from (4.28) we obtain

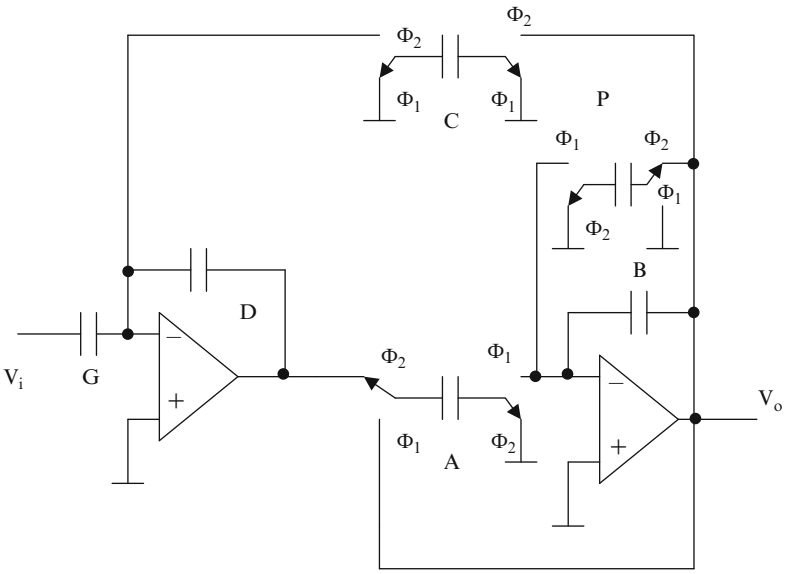


Fig. 4.11 Fischer and Moschytz SC biquad using positive feedback (Adapted from [4.22] © IEEE 1982)

$$C = \frac{Q_p\,(1-k)}{\delta} \tag{4.29a}$$

and

$$A = \frac{\delta}{m\,Q_p\,(1-k) - k\delta} \tag{4.29b}$$

As an illustration, for $\delta = 2$ and $Q_p = 10$, for $k = 0$, we have $C = 5$ and $A = 4/83$ yielding a capacitor spread of 103.75 whereas with $k = 0.5$, we have $C = 2.5$ and $A = 8/79$ yielding a capacitor spread of only 24.68. Note, however, that since the capacitor A is linked with the second integrator, scaling for optimal dynamic range cannot be done if one desires the actual output at T.

4.6.2 Split-Integrating Capacitor Technique

Huang and Sansen [4.23] have suggested techniques for reducing the capacitor spread by a *split-integrating capacitor* technique. This circuit is presented in Fig. 4.12. When $D_2 = 0$, it is same as the Fleischer–Laker biquad. However, by introducing D_2, the transfer function of the resulting SC filter can be derived as

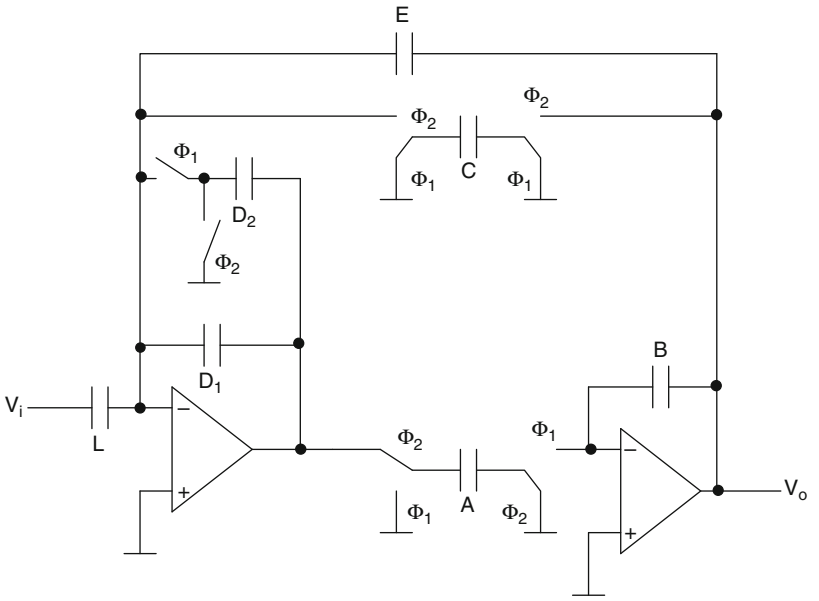


Fig. 4.12 Huang and Sansen biquad using split integrating capacitor (Adapted from [4.23] © IEEE 1987)

$$\frac{V_{oe}}{V_{ie}} = -\frac{AL}{(D_1+D_2)B}\,\frac{z^{-1}\left(1-z^{-1}\right)}{1-z^{-1}\left(2-\dfrac{AC}{D_1 B}-\dfrac{AE}{(D_1+D_2)B}\right)+z^{-2}\left(1-\dfrac{AE}{(D_1+D_2)B}\right)} \tag{4.30}$$

under the condition $V_{io} = V_{ie}z^{-1/2}$. Note that in the ϕ_1 phase (which was an idle phase), there is a charge distribution of the integrating capacitor D_1 using L and D_2. The resulting design equations are as follows.

$$\frac{\delta}{Q_p} = \frac{E\,D_1}{C(D_1+D_2)} \tag{4.31a}$$

and

$$\frac{4\,\delta^2+2\frac{\delta}{Q_p}+1}{4} = \frac{B\,D_1}{AC} \tag{4.31b}$$

For the equal time constant design, assuming $B = D_1 = 1$, we need $A = C$ yielding the following relationships.

$$A = C = \frac{2}{\sqrt{4\,\delta^2+2\frac{\delta}{Q_p}+1}} \tag{4.32a}$$

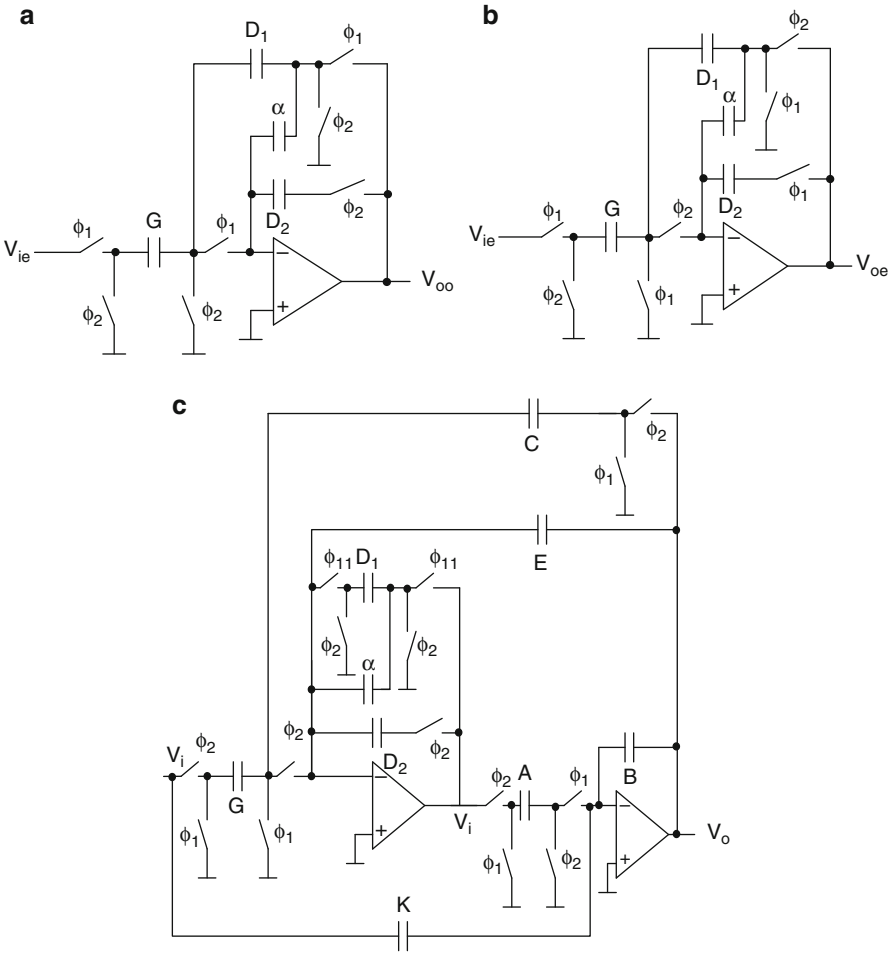


Fig. 4.13 (**a**) An inverting integrator with low capacitor spread, (**b**) noninverting integrator with low capacitance spread, and (**c**) Fleischer–Laker biquad based on (b) (Adapted from [4.24] © IEEE 1989)

$$\frac{E}{1+D_2}=\frac{2\delta/Q_p}{\sqrt{4\delta^2+2\frac{\delta}{Q_p}+1}}\approx\frac{1}{Q_p} \tag{4.32b}$$

Choosing $E = 1$, the spread of D_2 can be seen to be $Q_p - 1$. This may be compared with the E-type biquad, for which $E = 1/Q_p$. Thus instead of E being $1/Q_p$, in this case E shall be unity and D_2 shall be of the order of Q_p.

Huang [4.24] has suggested another method of reducing the capacitance spread which is useful in an F-type biquad. The inverting integrator can be realized as shown in Fig. 4.13a. Note that in the ϕ_1 phase, capacitors D_1, α, and G function

as an amplifier. During the ϕ_2 phase, only the charge contained on capacitor α is integrated on capacitor D_2. Thus, effectively, the transfer function realized is

$$\frac{V_{oo}}{V_{ie}} = -\frac{G\alpha}{(D_1+\alpha)D_2}\left(\frac{z^{-1/2}}{1-z^{-1}}\right) \tag{4.33}$$

Thus otherwise large capacitor ratio G/D is realized as the product of two capacitor ratios thus reducing the spread. It may be noted that the output of the opamp is not the same in both phases.

A noninverting integrator can be obtained by a simple modification of this circuit as shown in Fig. 4.13b.

A Fleischer–Laker E-type biquad using this technique is presented in Fig. 4.13c. The resulting transfer function can be obtained as

$$\frac{V_{oe}}{V_{ie}} = -\frac{K}{B}\frac{1-z^{-1}\left(2-\dfrac{AG}{D_2K}\right)+z^{-2}}{1-z^{-1}\left(2-\dfrac{AC}{D_2B}-\dfrac{\alpha AE}{D_1D_2B}\right)+z^{-2}\left(1-\dfrac{\alpha AE}{D_1D_2B}\right)} \tag{4.34}$$

under the condition $V_{io} = V_{ie}z^{-1/2}$. The design equations for this circuit are:

$$\frac{\delta}{Q_p} = \frac{\alpha E}{CD_1}, \quad \frac{4\delta^2+2\frac{\delta}{Q_p}+1}{4} = \frac{BD_2}{AC} \tag{4.35}$$

Note that the ratio which was originally E/C is now realized as a product of two capacitor ratios, thus effectively reducing the spread. Alternatively, it may be considered that E is replaced by $E\alpha/D_1$.

4.6.3 Nagaraj's SC Filters with Low Capacitor Spread

Much simpler circuits needing only three capacitors to realize the large spread proposed by Nagaraj [4.25] are shown in Fig. 4.14. Note that in the inverting integrator of Fig. 4.14a, in Phase 1, the capacitors C_2 and C_3 work as an attenuator of gain C_3/C_2. In the next phase, the charge is withdrawn by the capacitor C_3 and at the same time, charge redistribution takes place between C_1 and C_2. The transfer function of this circuit is given by

$$\frac{V_{oo}}{V_{ie}} = -\frac{C_1C_3}{C_2(C_1+C_2)}\frac{z^{-1/2}}{1-z^{-1}} \tag{4.36}$$

Thus, the product of two ratios now will form one ratio thus reducing the spread. Note that C_2 is typically a large capacitor and C_1 and C_3 are small. The circuit can be modified to realize a noninverting integrator as shown in Fig. 4.14b, whose transfer function is the same as (4.36) except for a sign inversion.

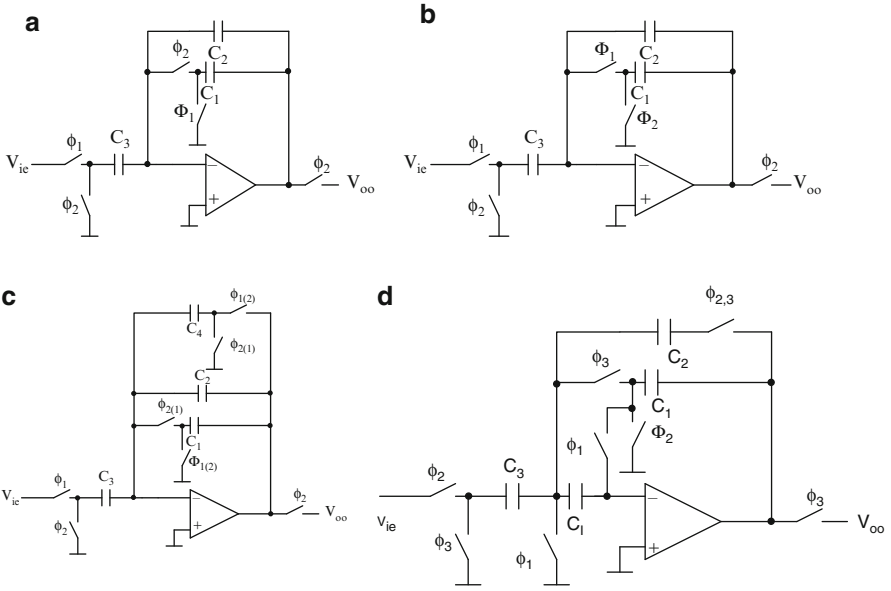


Fig. 4.14 Nagaraj's technique for capacitor spread reduction: (**a**) lossless inverting integrator, (**b**) lossless noninverting integrator, (**c**) inverting/noninverting lossy integrator, and (**d**) offset compensated version of (b) (Adapted from [4.25] © IEEE 1989)

The transfer function of the lossy inverting integrator (noninverting integrator using the switching phases shown in brackets with nonnegative sign) shown in Fig. 4.14c is given by

$$\frac{V_{oo}}{V_{ie}} = -\frac{C_1\ C_3\ z^{-1/2}}{(C_2+C_1)(C_2+C_4)-C_2\,(C_1+C_2+C_4)\,z^{-1}} \tag{4.37a}$$

The dc gain of the integrator is C_3/C_4. The realized pole-frequency is approximately

$$f_p = \frac{f_s}{2\pi}\left(\frac{C_1\ C_4}{C_1\ C_2+C_2\ C_4+C_2^2}\right) \tag{4.37b}$$

An analysis of the effect of opamp offset voltage on the circuit of Fig. 4.14a yields the transfer function as

$$V_{oe} = -V_{ie}\frac{C_1\,C_3\,z^{-1/2}}{C_2\,(C_1+C_2)(1-z^{-1})} + \frac{V_{offe}\,z^{-1/2}\,C_1\,(C_2+C_3)+V_{offo}\,(C_2\,(C_1+C_2+C_3)-z^{-1}\,(C_2+C_3)(C_1+C_2))}{C_2\,(C_1+C_2)(1-z^{-1})} \tag{4.38}$$

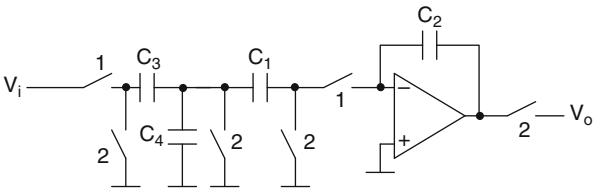


Fig. 4.15 T-cell integrator for realizing large time constants (Adapted from [4.26] © IEEE 1984)

Note that the second term in the transfer function of V_{offe} is (C_2/C_3) times the integrator transfer function. For SC integrators with large time constants, since C_3 is very small, the output offset voltage will be invariably high. Hence, offset compensation needs to be applied.

An improved integrator to meet this requirement is shown in Fig. 4.14d corresponding to an inverting/noninverting integrator. Note that this circuit needs a three-phase clock and also one extra capacitor C_I whose value is not critical. During Phase ϕ_1, the offset voltage is sampled on capacitor C_I and during the input signal integration during Phases ϕ_2 and ϕ_3, this is used to cancel the offset voltage. Note that the finite gain error as well as *1/f* noise are also cancelled. The reader is urged to confirm that the offset voltage of the opamp is not enhanced as in the previous case.

The effect of finite opamp gain on the integrator of Fig. 4.14a can be seen from the following transfer function as

$$\frac{V_{oe}}{V_{ie}} = -\frac{C_1 C_3}{\left(C_2 + \frac{(C_2+C_3)}{A}\right)} \frac{z^{-1/2}}{\left((C_1+C_2)(1-z^{-1}) + \frac{(C_1+C_2+C_3)}{A} - z^{-1}\left(\frac{C_2+C_3}{A}\right)\right)} \tag{4.39}$$

The reader may confirm that the effect of finite opamp gain is also reduced using the circuit of Fig. 4.14d.

4.6.4 T-Cell Integrator-Based Biquads

The value of the input feeding capacitor in a SC integrator becomes very small for realizing large time constants. An interesting technique suggested was to use a T of capacitors in place of the input feeding capacitor [4.26] as shown in Fig. 4.15. The transfer function of this circuit can be obtained as

$$\frac{V_{oe}}{V_{ie}} = -\frac{C_3\ C_1}{(C_3 + C_1 + C_4)\, C_2}\left(\frac{1}{1 - z^{-1}}\right) \tag{4.40}$$

It can be seen that the time constant of the integrator is now decided by the product of two ratios C_1/C_2 and $C_3/(C_1 + C_3 + C_4)$. Note that the charge

accumulated at the internal node needs to be removed by connecting the middle node to ground in every clock cycle. The disadvantage of the large time constant circuits is that the offset voltage of the opamp is amplified since the input feeding capacitance is low, as has been mentioned before. The transfer function including the offset voltage is given as

$$V_{oe} = -V_{ie}\frac{C_3\,C_1}{(C_3+C_1+C_4)\,C_2}\left(\frac{1}{1-z^{-1}}\right) + V_{offe}\frac{C_3\,C_1}{(C_3+C_1+C_4)\,C_2}\frac{1}{(1-z^{-1})}\left(\frac{C_3+C_4}{C_3}\right)+V_{offe} \tag{4.41}$$

An analysis of a simple integrator with the opamp offset denoted as V_{offe} and V_{offo} in the even and odd phases (see Fig. 4.3b) using Laker's equivalent circuit will show that the transfer function is given as

$$V_{oe} = -V_{ie}\frac{C_1}{C_2}\frac{1}{1-z^{-1}} + V_{offe}\left(1+\frac{C_1}{C_2}\frac{1}{1-z^{-1}}\right) \tag{4.42}$$

under the condition $V_{ie} = V_{io}z^{-1/2}$. Thus, the offset voltage also is integrated similarly to the input voltage and the offset voltage also appears directly at the output of the opamp. Several techniques to compensate this offset voltage have been described in the literature and are considered in detail in a later section.

4.7 Optimal Design of SC Biquads

Much work has been done on the optimum design of the SC biquads. Design procedures different from that described by Fleischer and Laker have been advanced by other authors. The problem considered is to achieve minimum total capacitance. In the realization of a second-order low-pass transfer function as in (4.43), for instance, the design requirements (also called *constraints*) are only three: pole-frequency, pole-Q, and dc gain. An additional constraint is that the maxima of both outputs of the opamps shall be equal.

$$D(z) = \frac{-z^{-1}AG}{DB + z^{-1}(AC+AE-2BD) + (BD-AE)z^{-2}} \tag{4.43}$$

A look at (4.43) shows that there are six degrees of freedom (capacitor values) whereas only four constraints are existing. Hence, the problem is to find a solution that reduces total capacitance by making effective use of the other degrees of freedom available. Ki and Temes [4.27] suggest that the fourth constraint of equal dynamic range can be approximated for high-Q designs using approximate formulae without resorting to computer simulation to find the maxima. We note from (4.43) that

$$\frac{AE}{AC} = \frac{\delta}{Q_p} \tag{4.44a}$$

$$\frac{AC}{BD} = \frac{4}{4\,\delta^2 + 2\frac{\delta}{Q_p} + 1} \cong \frac{1}{\delta^2} \tag{4.44b}$$

and the dc gain

$$M = \frac{G}{C} \tag{4.44c}$$

Note that a band-pass transfer function is realized at the T' output:

$$T' = \frac{-GB(1 - z^{-1})}{DB + z^{-1}(AC + AE - 2BD) + (BD - AE)\,z^{-2}} \tag{4.45}$$

The maximum of (4.45) can be found in terms of the capacitor ratios and equated to the maximum of (4.43) to obtain

$$\frac{GB}{AE} = M\,Q_p = Q_p\,\frac{G}{C} \quad \text{or} \quad Q_p = \frac{BC}{AE} \tag{4.46}$$

Note that $M = \frac{G}{C} = \frac{1}{Q_p}$ can be chosen to make the peak of low-pass transfer function as unity. From (4.44a) and (4.46), we have $\delta = \frac{B}{A}$. and next from (4.44b), we have $\delta = \frac{D}{C}$.

Thus we can obtain $C = Q_p G, E = \delta G, B = \delta A$, and $D = G\,\delta Q$. Next, the smallest capacitor among $C, E, D,$ and G can be seen to be G. Note also that A and B are related by δ. Thus the total capacitance considering $G = 1$ and $A = 1$ can be estimated as

$$C_T = Q_p\,(1 + \delta) + 2\delta + 2 \tag{4.47}$$

It is relevant to look again at the design procedure outlined earlier due to Fleischer and Laker in which $A = B = D = 1$ was chosen first to arrive at C and E values. Then G is identified based on the gain requirement. Next scaling will convert A and D to A/μ and D/μ. Thus the final values are $A/\mu, B = 1, D/\mu, C, E$, and G. Proceeding in the same manner as before, the capacitor values given in Table 4.1 can be obtained. Writing the denominator of the transfer function as

$$D(z) = 1 - (2 - \alpha - \beta)\,z^{-1} + (1 - \beta)\,z^{-2} \tag{4.48}$$

it may be observed that in the Flesicher–Laker design, α is realized as the single capacitor C and β is realized as the single capacitor E and scaling does not affect these values. Note also that the spread accordingly will be δ^2 or δQ_p. On the other hand, noting from (4.43) the fact that α and β are products of two capacitor ratios, they can be efficiently realized as the product of two smaller ratios. This has been pointed out by other authors as well. Note that the equal

Table 4.1 Comparison of various types of capacitance assignment

Capacitance	Fleischer–Laker	Ki–Temes	Equal time constants
C	$1/\delta^2$	Q_p	1
D	$1/\delta^2$	$Q_p\delta$	Δ
E	$1/(\delta Q_p)$	δ	δ/Q_p
G	$1/(\delta^2 Q_p)$	1	$1/Q_p$
A	$1/\delta$	1	1
B	1	δ	Δ

time constant design described earlier to evaluate the capacitor spread (see (4.20a) and (4.20b)) considers $A = C = 1$ and $B = D$. Thus directly, B $(= D)$ and E can be estimated first and then G can be evaluated to meet the dc gain requirement. This case also is presented in Table 4.1 for completeness. Note that for all designs, total capacitance can be obtained by summing all the capacitance values C, D, E, and G in one group and A and B in another group. First, these need to be scaled based on minimum capacitance in the two groups and then total capacitance can be estimated. As an illustration, for $\delta = 1$ and $Q_p = 10$, the total capacitance is $24C_u$ for all designs whereas for $\delta = 2$ and $Q_p = 10$, the total capacitance is $36C_u$. Ki and Temes [4.27] considered all generally desired digital transfer functions and listed the maxima; these can be used to optimize the capacitance assignment. Nevertheless, this approach is good for high-Q designs and low pole-Q designs still need exact computation of the maxima to facilitate scaling.

The disadvantage of the previously desired approaches is that only certain topologies such as the Fleischer–Laker biquad [4.14] or Fischer–Moschytz biquad [4.22] and the like were considered separately whereas in general many more may exist. There was no systematic exploration. Secondly, analytical approaches are manual and thus may not be efficient. The accuracy also is limited in analytical approach since low-Q_p cases cannot be considered. Furthermore, the problems of reducing the number of capacitors, sensitivity, and noise are not considered. Tang [4.28] has recently considered in a systematic manner, the capacitance assignment problem as an optimization problem using MINLP (mixed integer nonlinearly constrained programming). This method is less analytical but more numerical in nature. They also use several constraints: (a) *equality constraint* meaning matching of coefficients of the symbolic transfer function with the desired transfer function having numerical values; (b) OS (*optimum swing*) constraint (what we have called earlier realization of optimal dynamic range); (c) choice of a general versatile topology shown in Fig. 4.16 and (d) using a cost function based on pole-Q sensitivity, number of capacitors, and total capacitance. The pole-Q sensitivity due to all components is considered whereas

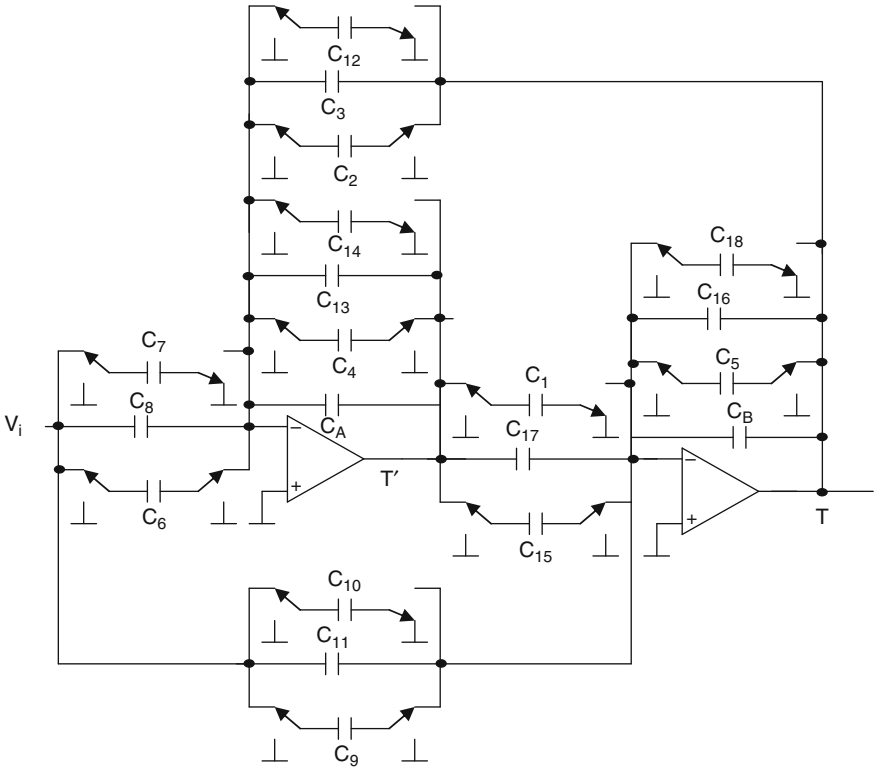


Fig. 4.16 General stray-insensitive SC biquad (Adapted from [4.28] © IEEE 2008)

pole-frequency sensitivity is not considered. The reader is referred to Tang [4.28] for more information.

Example 4.1 Using WINSPICE, perform the frequency-domain analysis of the Flesicher–Laker SC biquad using Laker's equivalent circuits. This is based on Nelin's [4.156] pioneering work. The treatment follows that of Allen and Holberg [4.155]. Laker's equivalent circuits need realization of admittances of the form $Cz^{-1/2}$. These are realized in WINSPICE using delay lines that can have a delay of $T/2$ where T is the clock period using statements such as X23PC1 2 3 23 DELAY. The subcircuit DELAY has a VCVS to produce a voltage amplified by gain 1 at terminal 3 of the voltage between input terminals 1 and 2 with a delay of $T\mu$ s. Then this voltage is converted into a floating current source between the same terminals 1 and 2 using the statement G23 2 3 23 0 2.4924694.

The capacitors and resistors are realized as capacitors and resistors.

We have considered a SC filter with all capacitors G, H, I, J, E, and F being used so that the reader can change the program accordingly. The resistor values are reciprocals of capacitor values. Note also that $1/(C + E)$ is used since in Laker's equivalent circuit the capacitor is the sum of C and E.

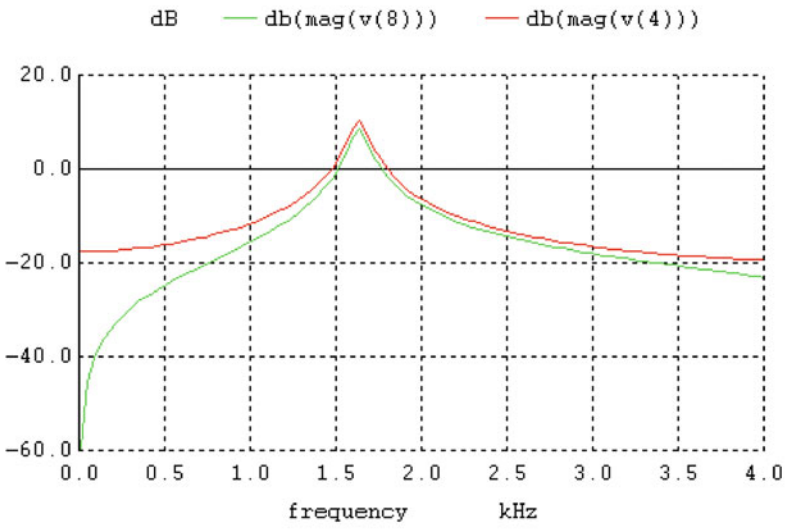
The SC filter with T output is an F-type SC bilinear bandpass filter with a center frequency of 1,633 Hz, sampling frequency 8 KHz, Q of 16, and midband gain 10 dB. The capacitor values are $E = J = 0$, $I = G = H = 0.1320836$, $F = 0.083541$, $C = 1.4924694$, $A = B = D = 1$. This example is taken from [4.14]. Evidently, $T/2 = 62.5$ μ s. Opamps of gain 100, 000 have been used. The z-domain transfer function can be obtained using standard design procedure as

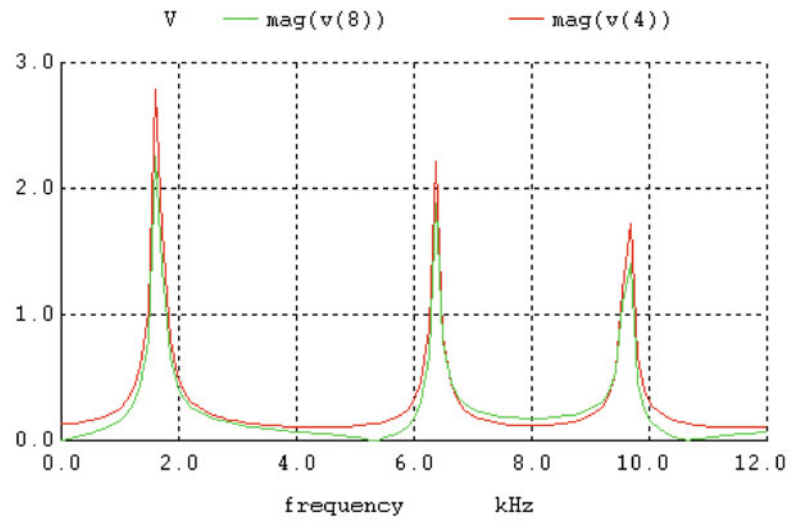
$$H(z) = \frac{0.1219(1 - z^{-2})}{1 - 0.5455\, z^{-1} + 0.9229\, z^{-2}}$$

```
* SC Biquad Fliescher Laker
Vin 1 0 ac 1
R1G 1 2 7.570962
*R1G 1 2 1/G
R2H 0 2 7.570962
*R2H 0 2 1/H
R3D 2 4 1
*R3D 2 4 1/D
R4D 3 5 1
*R4D 3 5 D
R5CE 2 8 0.67003048
*R5CE 2 8 1/(C+E)
*R6C 3 9 1/E
R7AJ 0 6 1
*R7AJ 0 6 1/(A+J)
R9BF 6 8 0.92290
*R9BF 6 8 1/(B+F)
R10B 7 9 1
*R10B 7 9 1/B
R11I 1 6 7.570962
*R11I 1 6 1/I

X23PC1 2 3 23 DELAY
*X23PC1 2 3 23 DELAY D+C
G23 2 3 23 0 2.4924694
*G23 2 3 23 0 D+C
X67PC1 6 7 67 DELAY
*X67PC1 6 7 67 DELAY B
G67 6 7 67 0 1
*G67 6 7 67 0 B
X12NC1 1 2 12 DELAY
*X12NC1 1 2 12 DELAY
G12 2 1 12 0 0.1320836
* G12 2 1 12 0 H
X20PC1 2 0 20 DELAY
*X20PC1 2 0 20 DELAY H
```

```
G20 2 0 20 0 0.1320836
*G20 2 0 20 0 H
X34NC1 3 4 34 DELAY
*X34NC1 3 4 34 DELAY
G34 4 3 34 0 1
*G34 4 3 34 0 D
X25NC1 2 5 25 DELAY
*X25NC1 2 5 25 DELAY
G25 5 2 25 0 1
*G25 5 2 25 0 D
X29NC1 2 9 29 DELAY
*X29NC1 2 9 29 DELAY
*G29 9 2 29 0 E
X38NC1 3 8 38 DELAY
*X38NC1 3 8 38 DELAY
*G38 8 3 38 0 E
X56NC1 5 6 56 DELAY
*X56NC1 5 6 56 DELAY
G56 6 5 56 0 1
*G38 8 3 38 0 E
X06PC1 6 0 60 DELAY
*X06PC1 6 0 60 DELAY
G06 6 0 60 0 1
*G06 6 0 60 0 A+J
X78NC1 7 8 78 DELAY
*X78NC1 7 8 78 DELAY B
G78 8 7 78 0 1
*G78 8 7 78 0 B
X69NC1 6 9 69 DELAY
*X69NC1 6 9 69 DELAY B
G69 9 6 69 0 1
*G69 9 6 69 0 B
X16NC1 1 6 16 DELAY
*X16NC1 1 6 16 DELAY J
*G16 6 1 16 0 J
E1ODD 0 4 2 0 1E6
E1EVEN 0 5 3 0 1E6
E2ODD 0 8 6 0 1E6
E2EVEN 0 9 7 0 1E6
*****************
.SUBCKT DELAY 1 2 3
ED 4 0 1 2 1
TD 4 0 3 0 ZO=1K TD=62.5u
RDO 3 0 1K
.ENDS DELAY
**********************
.AC LIN 99 10 4000
```





Example 4.2 In the earlier example, the input was fed directly. In practice, the input needs to be sampled and held. A circuit for this purpose adapted from [4.156] is shown in Fig. E.4.2. and the corresponding WINSPICE code is presented. The frequency response shows the $\sin(\omega T/2)/(\omega T/2)$ response of a zero-order hold. Note that a zero-order hold has a response given by $\dfrac{1-e^{-sT}}{sT}$. The full delay of 125 μs is realized as a cascade of two delay elements of 62.5 μs.

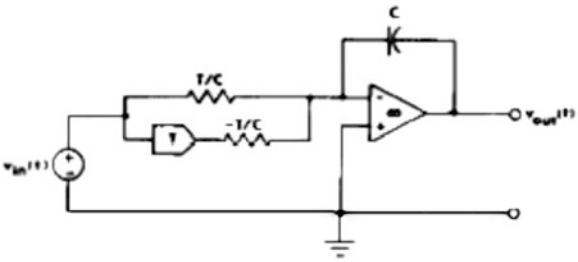
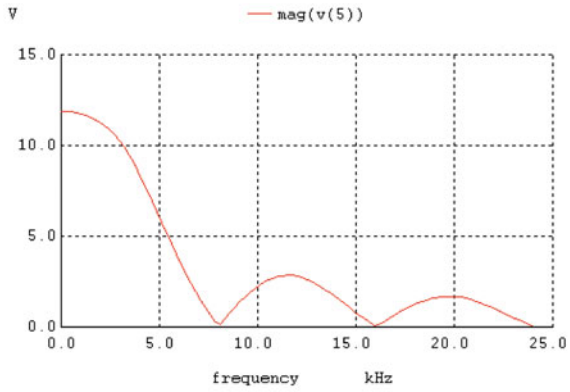


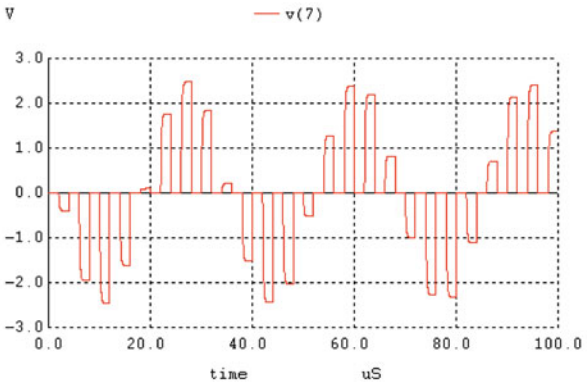
Fig. E.4.2 (Adapted from [4.156] © IEEE 1983)

```
* SC Sample and Hold
VIN 1 0 ac 1v
*VIN 1 0 sin (0 1 30000 0 0)
R1 1 4 10K
R2 3 4 -10K
X1 1 0 2 DELAY
X2 2 0 3 DELAY
E1 5 0 4 0 -100000000
C1 4 5 1N
******************
.SUBCKT DELAY 1 2 3
ED 4 0 1 2 1
TD 4 0 3 0 ZO=1K TD=62.5u
RDO 3 0 1K
.ENDS DELAY
**********************
.AC LIN 99 1 24K
```



Example 4.3 Observe the transient response of the SC amplifier using MOS transistors as switches using WINSPICE. Note that in order to discharge the feedback capacitor, a switch SMOD is used. A MOS transistor can be used but it distorts the signal unless a special design is carried out.

```
*SC amplifier transient response to sinewave input
v1 6 0 dc 2.5
VIN1 1 0 sin (0 0.25 30000 0 0)
M1 1 3 2 2 NMOS1 W = 1U L = 1U AD = 18P AS = 18P PD = 18U PS = 18U
M2 2 5 4 4 NMOS1 W = 1U L = 1U AD = 18P AS = 18P PD = 18U PS = 18U
*M5 7 3 4 4 NMOS1 W = 1U L = 1U AD = 18P AS = 18P PD = 18U PS = 18U
S1 4 7 10 0 SMOD
C1 2 0 30.0P
C2 4 7 3.0P
E1 7 0 4 0 -1000
v2 8 0 -2.5
.MODEL SMOD VSWITCH(RON=1K ROFF=10E9 VON=+2.5 VOFF=-2.5)
Vclock1 3 0 dc PULSE (-2.5 2.5 0 0 0 1u 4u)
vclock2 5 0 dc PULSE (-2.5 2.5 2u 0 0 1u 4u)
Vclock3 10 0 dc PULSE (-2.5 2.5 0 0 0 1u 4u)
.tran 10ns 100u
.MODEL NMOS1 NMOS VTO = 0.70 KP = 110U GAMMA = 0.4 LAMBDA =
0.04 PHI =0.7 MJ = 0.5 MJSW = 0.38 CGBO = 700P CGSO = 220P CGDO =
220P CJ = 770U CJSW = 380P LD = 0.016U TOX = 14N
.MODEL PMOS1 PMOS VTO = -0.70 KP = 50U GAMMA = 0.57 LAMBDA =
0.05 PHI = 0.8 MJ = 0.5 MJSW = 0.35 CGBO = 700P CGSO = 220P CGDO =
220P CJ = 560U CJSW = 350P LD = 0.014U TOX = 14N
.END
```



4.8 SC Ladder Filters Based on Component Simulation and Operational Simulation

SC ladder filters based on doubly terminated LC networks can be easily derived. As has been seen in the case of active RC and OTA-C filters, the ladder filters could be based on component simulation or operational simulation. In the component

simulation technique, floating and grounded inductances and termination resistances based on SC technique will be needed. These, however, invariably are affected by parasitic capacitances at the intermediate nodes. Hence, stray-insensitive SC filters need to be realized using operational simulation. However, interestingly, some of the concepts used in realizing operational simulation type SC filters have been adapted from the component simulation technique and in fact, have been used in the realization of OTA-C filters. Hence, we briefly consider the component simulation technique and then discuss more elaborately the operational simulation technique.

4.8.1 SC Realization of L, C, and R Elements

The components such as inductance, capacitance, and resistance are defined by the $I(s) - V(s)$ relationship in the s-domain. On the other hand, in SC networks only incremental charges flow. Hence we need to derive incremental charge-to-voltage ($\Delta Q(z) - V(z)$) relationships for the three components so that SC versions can be built [4.29, 4.30, 4.31, 4.32].

Consider an inductance L as an illustration for which we have

$$V(s) = (sL)I(s) \tag{4.49a}$$

We know that $i = \dfrac{dq}{dt}$. Thus, by taking the Laplace transform on both sides,

$$I(s) = sQ(s) \tag{4.49b}$$

From (4.49a) and (4.49b) we have

$$V(s) = (s^2 L)Q(s) \tag{4.49c}$$

It is known that there are several $s \rightarrow z$ transformations for mapping from the s-domain to the z-domain. Using the bilinear transformation (BT), we have from (4.49c)

$$V(z) = \frac{4L}{T^2}\frac{(1 - z^{-1})^2}{(1 + z^{-1})^2}Q(z) \tag{4.50}$$

Since incremental charge is related to charge using the relationship

$$\Delta Q(z) = (1 - z^{-1})Q(z) \tag{4.51}$$

for an inductor, we obtain from (4.50) and (4.51),

$$\Delta Q(z) = V(z)\frac{T^2}{4L}\frac{(1 + z^{-1})^2}{(1 - z^{-1})} \tag{4.52a}$$

On the other hand, the use of LDI transformation $s \rightarrow \dfrac{1-z^{-1}}{T\,z^{-1/2}}$ in (4.49c) yields

$$\Delta Q(z) = V(z)\frac{T^2}{L}\frac{z^{-1}}{(1-z^{-1})} \tag{4.52b}$$

It is interesting to note that (4.52a) can be rewritten as

$$\begin{aligned}\Delta Q(z) &= V(z)\frac{T^2}{4L}\frac{(1+z^{-1})^2}{(1-z^{-1})} = V(z)\frac{T^2}{4L}\frac{(1-z^{-1})^2+4\,z^{-1}}{(1-z^{-1})} \\ &= V(z)\frac{T^2\,(1-z^{-1})}{4L} + V(z)\frac{T^2\;z^{-1}}{L(1-z^{-1})}\end{aligned} \tag{4.53}$$

showing that a bilinear transformation-type inductor can be realized as a LDI type inductor (second term in (4.53)) in parallel with a capacitance of value $T^2/(4\,L)$ (the first term as shown shortly). In a similar manner, for a resistance, the corresponding incremental charge–voltage relationships corresponding to BT and LDI transformations can be derived as

$$\text{BT}: \quad \Delta Q(z) = V(z)\frac{T}{2R}(1+z^{-1}) \tag{4.54a}$$

$$\text{LDI}: \quad \Delta Q(z) = V(z)\frac{T\,z^{-1/2}}{R} \tag{4.54b}$$

Note that LDI-type resistance is not realizable due to the simple reason that charge can flow instantaneously into the circuit across the capacitor or after one full clock cycle delay. Thus, three types of $\Delta Q(z) - V(z)$ relationships can exist, given by (4.54a), and the following two given as

$$\Delta Q(z) = V(z)\frac{T\,z^{-1}}{R} \tag{4.55a}$$

$$\Delta Q(z) = V(z)\frac{T}{R} \tag{4.55b}$$

Similarly, for a capacitor C, the corresponding incremental charge–voltage relationships corresponding to BT and LDI transformations can be found interestingly to be the same:

$$\Delta Q(z) = V(z)C(1-z^{-1}) \tag{4.56}$$

It is thus clear that SC branches that can realize these $\Delta Q(z) - V(z)$ relationships are required to simulate the various components so that they can be interconnected to form the complete SC circuit. Note also that in the above discussion, charge flows only in one phase into the terminals of the device.

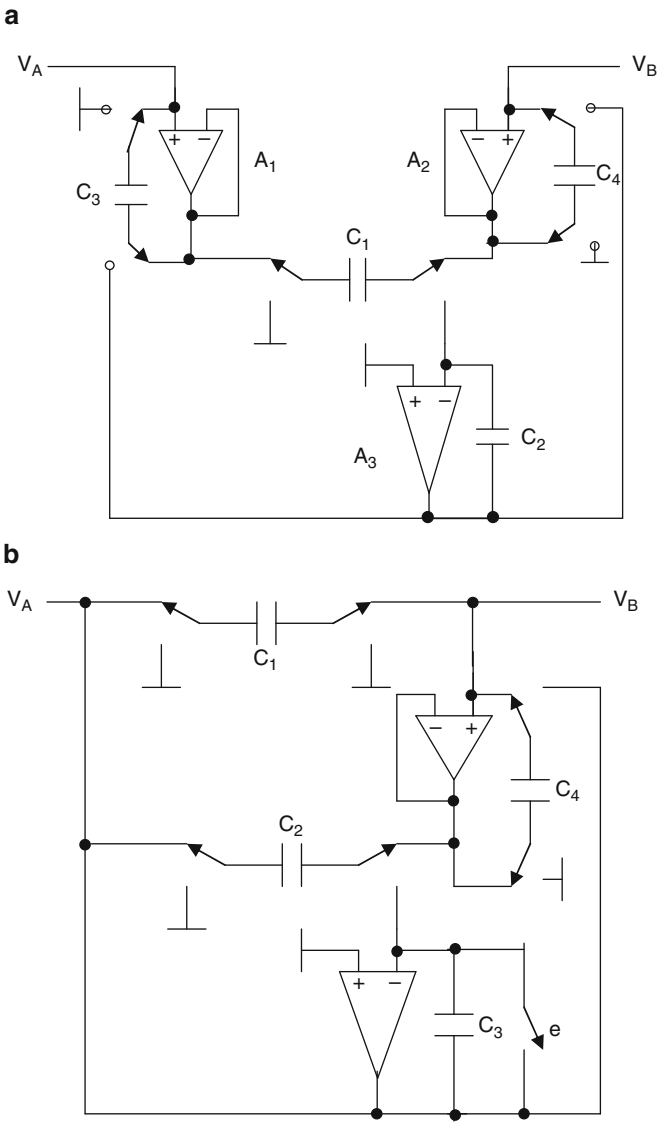


Fig. 4.17 (**a**) SC floating inductance simulation circuit, and (**b**) circuit used for realizing general termination resistance ((a) Adapted from [4.30] © IEEE 1981 (b) Adapted from [4.31] © IEE 1983)

The *SC* network of Fig. 4.17a realizes an LDI-type of inductance [4.29]. Note that the input voltage is buffered using buffer-connected opamps A_1 and A_2 and sampled by the SC C_1 in the even phase. The charge on C_1 is integrated using a differential integrator formed by OA A_3 and capacitor C_2. The output of the

integrator is $\frac{C_1}{C_2}\frac{z^{-1/2}}{(1-z^{-1})}(V_A - V_B)$. This voltage is converted into a charge using capacitors C_3 and C_4 and made to flow into the terminals A and B (i.e., by discharging the capacitors C_3 and C_4 using the buffer-connected opamps A_1 and A_2) to realize a LDI-type floating inductor (see (4.52b)). The charge flowing into the input terminal V_A can be seen to be

$$\Delta Q(z) = \frac{C_1\ C_3}{C_2}\frac{z^{-1}}{(1-z^{-1})}(V_A - V_B) \tag{4.57}$$

Shunting this floating inductor by a capacitance $T^2/(4L)$ yields a floating bilinear transformation type inductance.

For realizing ladder filters, the termination resistances need to be realized using switched-capacitors. The termination resistances have one terminal connected to source or ground and another to other components in the ladder filter. The three types of terminations that are needed can be realized using the circuit of Fig. 4.17b [4.31]. Note that this circuit is obtained from the floating inductance realization of Fig. 4.17a by first removing the buffer A_1 and associated capacitor C_3 and switches at terminal A and changing the integrator to an amplifier. The effective incremental charge flowing in the circuit of Fig. 4.17b can be written as

$$\Delta Q(z) = \left(C_1 + \frac{C_2\ C_4}{C_3}\ z^{-1}\right)(V_A - V_B) \tag{4.58}$$

Thus, by appropriate choice of capacitors (a) $C_1 = 0$, (b) $C_2 = 0$, (c) $C_2 = C_3$ and $C_4 = C_1$, the three desired types of terminations can be realized.

4.8.2 SC Low-Pass and Band-Pass Filters Derived Using Operational Simulation of LC Ladder Filters

Consider the third-order elliptic low-pass filter of Fig. 4.18a [4.33, 4.34, 4.35]. The equations describing the operation of the circuit at nodes V_1 and V_o can be first written as follows.

$$\frac{V_i - V_1}{R_s} + (V_o - V_1)\left(\frac{1}{sL_2} + sC_2\right) - V_1\, sC_1 = 0 \tag{4.59a}$$

$$(V_1 - V_o)\left(\frac{1}{sL_2} + sC_2\right) - V_o\, sC_3 - \frac{V_o}{R_L} = 0 \tag{4.59b}$$

Substituting the bilinear $s \rightarrow z$ transformation namely $s = \frac{2}{T}\left(\frac{1-z^{-1}}{1+z^{-1}}\right)$ in (4.59a, 4.59b) and multiplying throughout by $\frac{T(1+z^{-1})}{2}$, we obtain

$$\frac{(V_i - V_1)T(1+z^{-1})}{2R_s} + (V_o - V_1)\left(\frac{T^2}{4L_2}\frac{(1+z^{-1})^2}{(1-z^{-1})} + (1-z^{-1})C_2\right) - V_1(1-z^{-1})C_1 = 0 \tag{4.60a}$$

$$(V_1 - V_o)\left(\frac{T^2}{4L_2}\frac{(1+z^{-1})^2}{(1-z^{-1})} + (1-z^{-1})C_2\right) - V_o(1-z^{-1})C_3 - V_o\frac{T(1+z^{-1})}{2R_L} = 0 \tag{4.60b}$$

This equation should be rewritten such that SC blocks can realize the various terms in a stray-insensitive manner. The term $\frac{T^2}{4L_2}\frac{(1+z^{-1})^2}{(1-z^{-1})}$ can be rewritten as $\frac{T^2}{4L_2}\left((1-z^{-1}) + \frac{4z^{-1}}{(1-z^{-1})}\right)$. Similarly, the first term $\frac{(V_i - V_1)T(1+z^{-1})}{2R_s}$ can be rewritten as $(V_i - V_1)\left(\frac{T}{R_s} - \frac{T(1-z^{-1})}{2R_s}\right)$.

Thus from (4.60a, 4.60b), we have after regrouping terms connected with $-V_1$, V_o and $V_o - V_1$ and V_i as

$$V_i\left(\frac{T}{R_s} - \frac{T(1-z^{-1})}{2R_s}\right) + V_o\left(C_2 + \frac{T^2}{4L_2}\right)(1-z^{-1}) - V_1(1-z^{-1})\left(C_1 + C_2 + \frac{T^2}{4L_2} - \frac{T}{2R_s}\right) - V_1\frac{T}{R_s} + (V_o - V_1)\frac{T^2}{L_2}\frac{z^{-1}}{(1-z^{-1})} = 0 \tag{4.61a}$$

$$-V_1\left(C_2 + \frac{T^2}{4L_2}\right)(1-z^{-1}) + V_o(1-z^{-1})\left(C_3 + C_2 + \frac{T^2}{4L_2} - \frac{T}{2R_L}\right) + V_o\frac{T}{R_L} + (V_o - V_1)\frac{T^2}{L_2}\frac{z^{-1}}{(1-z^{-1})} = 0 \tag{4.61b}$$

It can be seen that the terms $\alpha(1 - z^{-1})$ correspond to an unswitched capacitor of value α and frequency-independent terms correspond to SC resistors, whereas the term $(V_o - V_1)\frac{T^2}{4L_2}\frac{z^{-1}}{(1-z^{-1})}$ can be realized using a stray-insensitive differential integrator. This term can be shared in implementing both (4.61a) and (4.61b) as well. The complete SC filter thus obtained is as shown in Fig. 4.18c. Note that the source resistance implementation needs an inverting amplifier of unity gain as shown to realize $-\frac{T(1-z^{-1})}{2R_s}$. Note also that $-V_1$ is realized at the output of an opamp as is also seen in the case of active RC filters based on operational

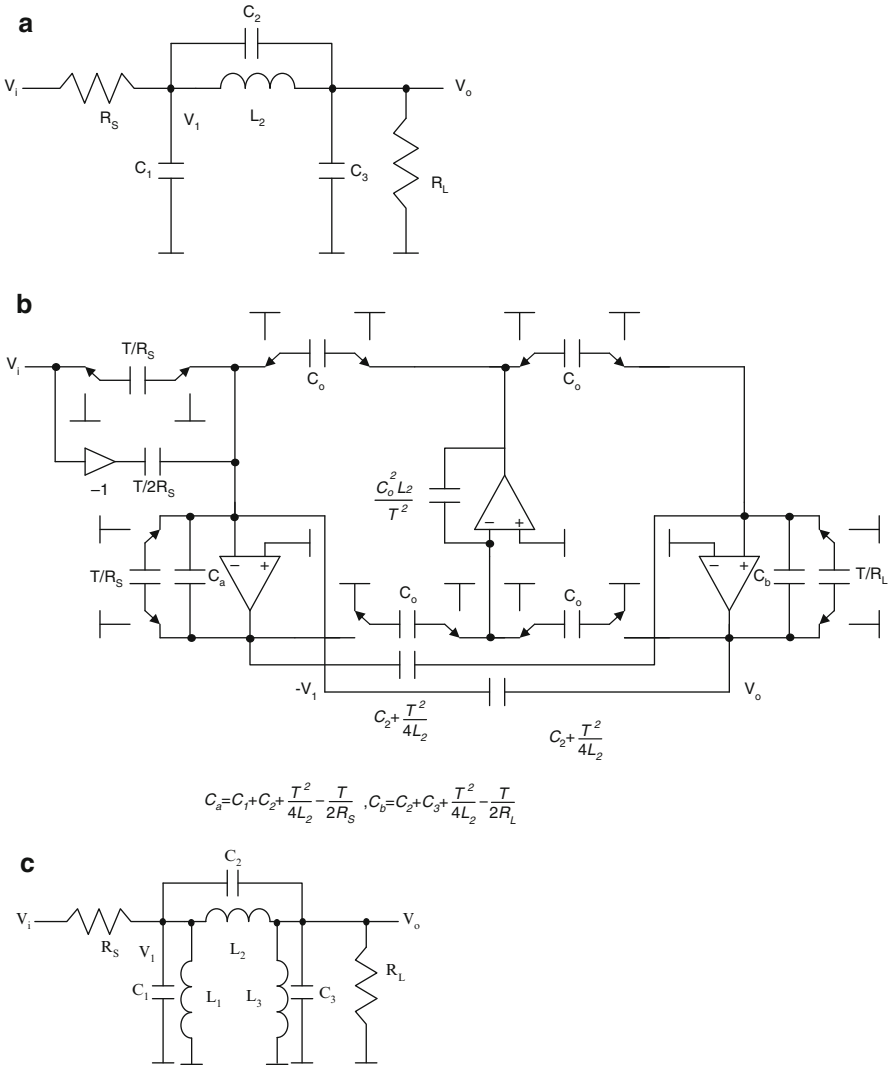


Fig. 4.18 (**a**) Prototype third-order low-pass elliptic ladder filter, (**b**) SC circuit based on (a), (**c**) prototype of bandpass filter obtained from (a) using LP to BP transformation, and (**d**) SC filter derived from (c) (b Adapted from [4.35] © IEEE 1981)

simulation. The cross-coupling capacitors will be needed for low-pass all-pole realization also (i.e., the case with $C_2 = 0$) of value $\dfrac{T^2}{4L_2}$. The same procedure can be applied to high-order filters as well. Note that C_o can be a unit capacitance.

The application to band-pass filters is straightforward. Consider the prototype of Fig. 4.18b and the SC filter of Fig. 4.18d derived therefrom. In this case since L_2 and L_3 are different, the equations to be realized are different:

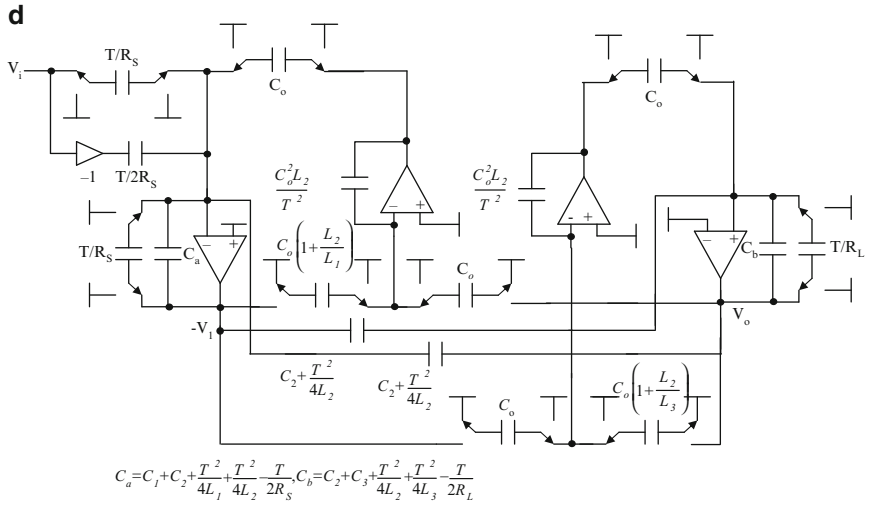


Fig. 4.18 (continued)

$$V_i\left(\frac{T}{R_s}-\frac{T(1-z^{-1})}{2R_s}\right)+V_o\left(C_2+\frac{T^2}{4L_2}\right)(1-z^{-1})-V_1(1-z^{-1})$$
$$\left(C_1+C_2+\frac{T^2}{4L_1}+\frac{T^2}{4L_2}-\frac{T}{2R_s}\right)-V_1\frac{T}{R_s}+\frac{T^2}{L_2}\frac{z^{-1}}{(1-z^{-1})}\left(V_o-V_1\left(1+\frac{L_2}{L_1}\right)\right)=0 \tag{4.62a}$$

and

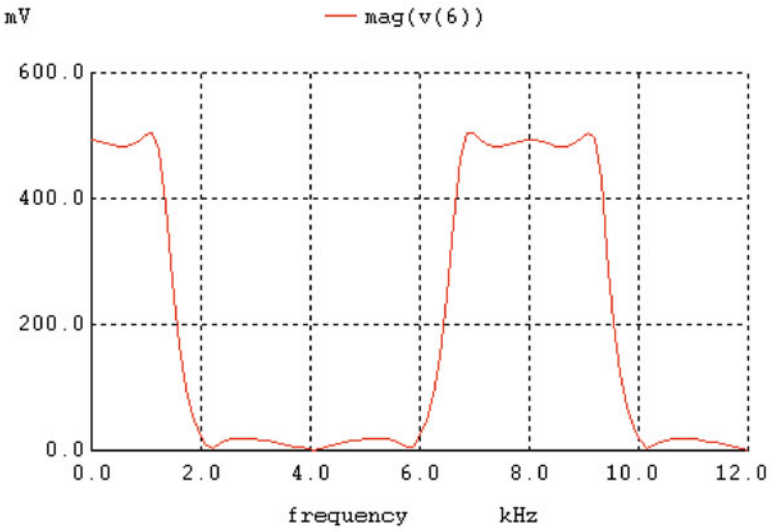
$$-V_1\left(C_2+\frac{T^2}{4L_2}\right)(1-z^{-1})+V_o(1-z^{-1})\left(C_2+C_3+\frac{T^2}{4L_2}+\frac{T^2}{4L_3}-\frac{T}{2R_L}\right)$$
$$+V_o\frac{T}{R_L}+\frac{T^2}{L_2}\frac{z^{-1}}{(1-z^{-1})}\left(V_o\left(1+\frac{L_2}{L_3}\right)-V_1\right)=0 \tag{4.62b}$$

Due to the unequal last terms in (4.62a) and (4.62b), two different opamp-based circuits will be needed to realize (4.62a) and (4.62b) as shown in the SC implementation shown in Fig. 4.18d.

Example 4.4 Plot the frequency response of the bilinear third-order elliptic low-pass SC filter of Fig. 4.18b using opamps with gain 100. Note that we have simulated here the simplified z-domain equivalent circuit considering the sampled and held input. This reduces the size of the code as the number of elements are very few in the equivalent circuit as compared to those using the complete balanced lattice

equivalent of Laker. The design specifications are clock frequency/pass-band edge ratio of 9.25, 0.28 dB ripple and a pass-band to stop-band edge ratio of 2. The values of components of Fig. 4.18a are $R_S = R_L = 1$, $C_1 = 1.20301$, $C_2 = 0.201627$, $C_3 = 1.20301$, $L_2 = 0.962438$. After prewarping using the formula $\omega_c = \frac{2}{T} \tan \frac{\omega_D T}{2}$, prewarped values considering T = 1 s are $R_S = R_L = 1$, $C_1 = 1.1564$, $C_2 = 0.193814$, $C_3 = 1.1564$, $L_2 = 0.9251446$. Using these values in (4.61), the various capacitor values can be obtained, which are used in the simulation.

```
*Third -order ellptic filter
Vin 1 0 ac 1
R12 1 2 2
R23 2 3 0.4716024
R42 2 4 1
R47 4 7 1
R67 7 6 0.4716024
R62 6 2 2.1549866
R37 3 7 2.1549866
R45 4 5 1.0809116
X12PC1 1 2 12 DELAY
G12 1 2 12 0 0.5
X32NC1 2 3 32 DELAY
G32 3 2 32 0 1.12043
X45NC1 4 5 45 DELAY
G45 5 4 45 0 0.925145
X62NC1 6 2 62 DELAY
G62 2 6 62 0 0.46404
X67NC1 6 7 67 DELAY
G67 7 6 67 0 1.12043
X37NC1 3 7 37 DELAY
G37 7 3 37 0 0.46404
X35NC1 3 5 35 DELAY
G35 5 3 35 0 1
X56NC1 5 6 56 DELAY
G56 6 5 56 0 1
E1 3 0 2 0 -1E2
E2 6 0 7 0 -1E2
E3 4 0 5 0 -1E2
*****************
.SUBCKT DELAY 1 2 3
ED 4 0 1 2 1
TD 4 0 3 0 ZO=1K TD=125u
RDO 3 0 1K
.ENDS DELAY
**********************
.AC LIN 99 10 12000
```



4.8.3 SC High-Pass Filters Derived Using Operational Simulation of LC Ladder Filters

The realization of SC high-pass filters based on the RLC prototype (see, e.g., Fig. 4.19a for a third-order filter) using the bilinear transformation technique described above is not feasible [4.35]. The reason is that the corresponding to the source resistance, the $\Delta Q(z) - V(z)$ relationship will have a term of the type $k(1 + z^{-1})$ and this creates an anomalous situation. At $f_s/2$, the input to the high-pass filter is cut off since the $(1 + z^{-1})$ term becomes zero. As such, Lee et al. [4.35] suggest the use of scaling (dividing) all the impedances in the prototype by s. After scaling, as an illustration, the s-domain nodal equation can be obtained as

$$\frac{s(V_i - V_1)}{R_s} + (V_2 - V_1)\left(\frac{1}{L_2} + s^2\, C_2\right) = \frac{V_1}{L_1} \tag{4.63a}$$

Substituting for s the bilinear $s \rightarrow z$ transformation, $s = \frac{2}{T}\left(\frac{1 - z^{-1}}{1 + z^{-1}}\right)$ and multiplying throughout by $(1 + z^{-1})$, and using the identity $\frac{(1 - z^{-1})^2}{(1 + z^{-1})} C_2 = C_2 (1 + z^{-1}) - \frac{4 z^{-1}}{(1 + z^{-1})} C_2$, we have

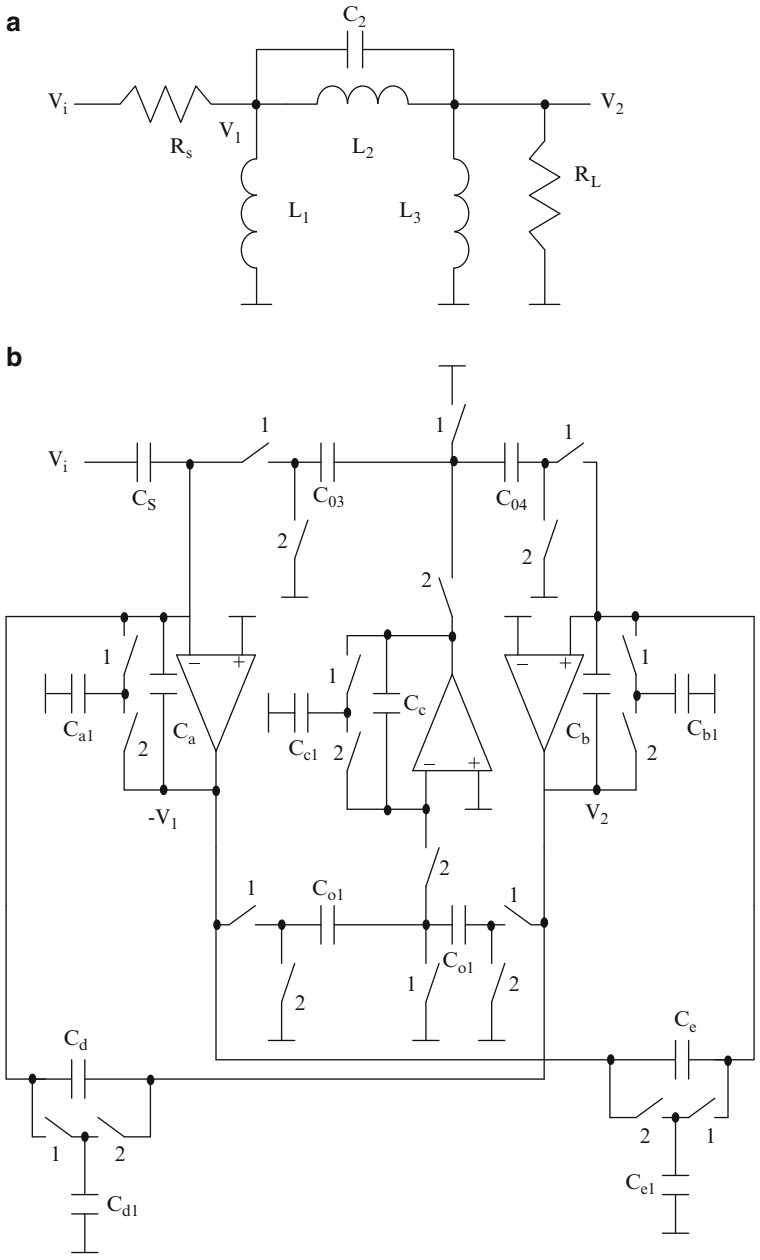


Fig. 4.19 (**a**) A prototype third-order high-pass filter, (**b**) SC implementation of (a) (Adapted from [4.35] © IEEE 1981)

$$V_i \frac{2(1-z^{-1})}{TR_s} - V_1 \left((1-z^{-1}) \left(\frac{2}{TR_s} + \frac{1}{L_1} + \frac{1}{L_2} + \frac{4C_2}{T^2} \right) + 2z^{-1} \left(\frac{1}{L_1} + \frac{1}{L_2} + \frac{4C_2}{T^2} \right) \right)$$
$$+ V_2 \left(\left(\frac{1}{L_2} + \frac{4C_2}{T^2} \right) (1-z^{-1}) + 2z^{-1} \left(\frac{1}{L_2} + \frac{4C_2}{T^2} \right) \right) - (V_2 - V_1) \frac{16 C_2 z^{-1}}{T^2 (1+z^{-1})} = 0 \tag{4.63b}$$

Note that parasitic-sensitive branches are needed for realizing the z^{-1} terms as well, since $\frac{1}{1+z^{-1}} = \frac{1}{(1-z^{-1})+2z^{-1}}$ as shown in Fig. 4.19b. The various capacitor values are as follows.

$$C_a = \frac{2}{TR_s} + \frac{1}{L_1} + \frac{1}{L_2} + \frac{4C_2}{T^2}, C_s = \frac{2}{TR_s}, C_{a1} = 2(C_a - C_S),$$
$$C_d = \frac{C_{d1}}{2} = \frac{1}{L_2} + \frac{4C_2}{T^2}, C_{c1} = 2\,C_c, \frac{C_{o1}\,C_{o3}}{C_c} = \frac{16C_2}{T^2} \tag{4.64a}$$

In a similar manner, the equation at node V_2 gives the other capacitor values as

$$C_b = \frac{1}{R_L} + \frac{1}{L_2} + \frac{1}{L_3} + C_2, C_L = \frac{1}{R_L}, C_{b1} = 2(C_b - C_L), C_e = \frac{C_{e1}}{2}$$
$$= \frac{1}{L_3} + C_2\,. \tag{4.64b}$$

4.9 High-Frequency SC Filters

High-frequency filters based on the LC technique cannot achieve the out-of-band attenuation of about −80 dB needed in certain applications. These are generally not integrable on CMOS VLSI chips and hence are used external to the chip. On the other hand, CT (continuous-time) filters realize a large corner frequency variation of ±5% to ±10% due to process variation and matching. Hence, SC filters are attractive for these high-frequency applications. Several opamp architectures are known in the literature to which the reader is referred to excellent books. However, among the various opamp topologies, five types can be distinguished: single-stage folded-cascode opamp, single-stage telescopic opamps, two-stage telescopic opamps, current mirror OTA, OTA based on complementary differential pairs, and three-path OTA as shown in Fig. 4.20(a)–(f). The reader is referred to Moon [4.36] and Adut et al. [4.157] for an exhaustive discussion on the choice of opamp topology.

The clock frequency naturally is large for high-frequency SC filters, therefore the stringent requirements on the folded cascode opamp of Fig. 4.20a arise. The bandwidth of the opamp has to be high, meaning that large G_m needs to be used thereby leading to large power dissipation. Due to the large G_m, the opamp input capacitance also tends to be large. Moreover, multiple branches of Bias current are

needed increasing the power dissipation. Due to the large input capacitance, for high-frequency filters, and due to the high f_c/f_s ratio, the feedback factor around the opamp gets reduced when small unit capacitance is used.

On the other hand, the telescopic opamp of Fig. 4.20b needs less power since of the reduced number of current branches but a large input capacitance still exists. Moreover, due to the high common-mode voltage, complementary transmission

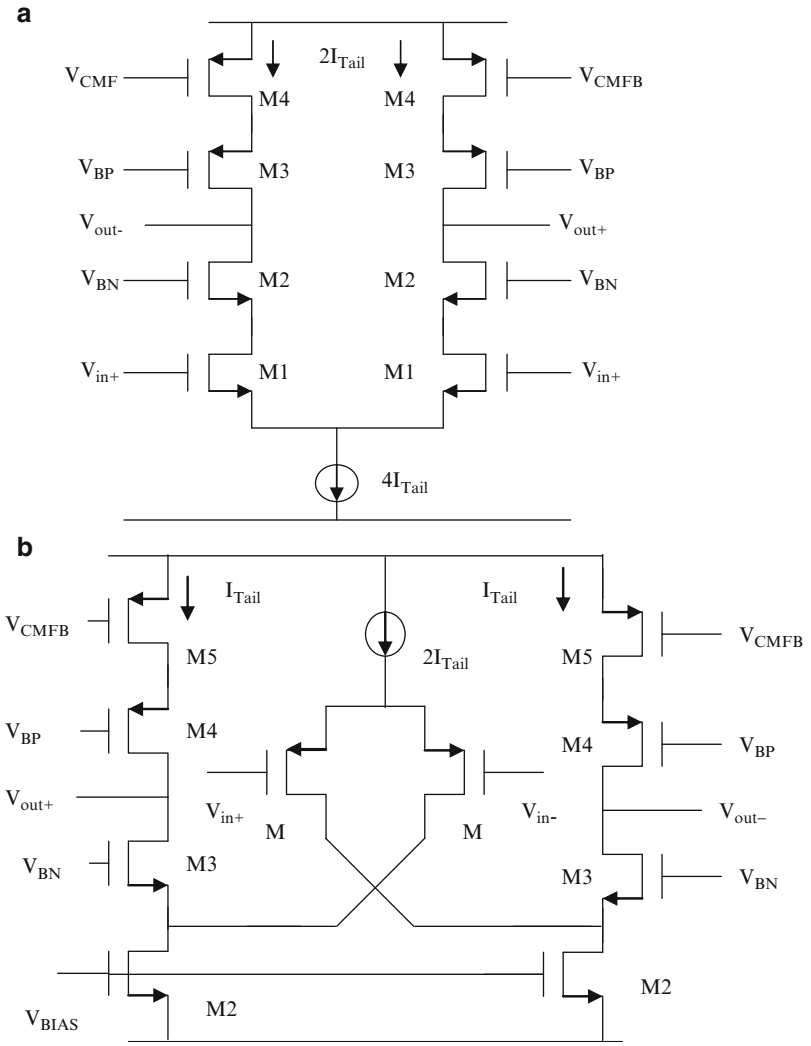


Fig. 4.20 OTA architectures for high-frequency SC filters: (**a**) telescopic architectures, (**b**) folded-cascode topology, (**c**) two-stage OTA, (**d**) current-mirror folded cascode OTA, (**e**) OTA based on complementary differential pairs, and (**f**) a three-path OTA ((c) Adapted from [4.36] © IEEE 2000, (a), (b), (d)–(f) Adapted from [4.157] © IEEE 2006)

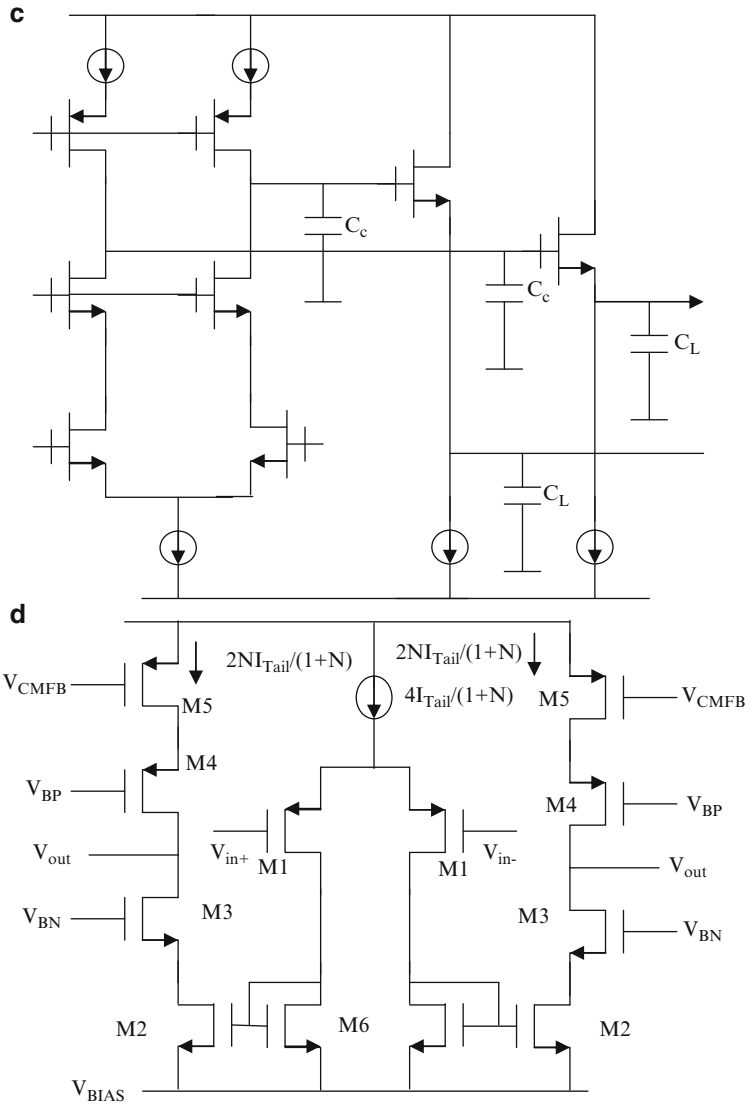


Fig. 4.20 (continued)

gate switches need to be used. Next, if the two-stage opamp of Fig. 4.20c is used, the power consumption will be of the second stage since it needs to drive the capacitor load. A very small capacitance will be needed at the output of the first stage for frequency compensation. Moon [4.36] has recommended this architecture in view of its low noise, low dissipation first stage, and good high-frequency response by dominant pole compensation.

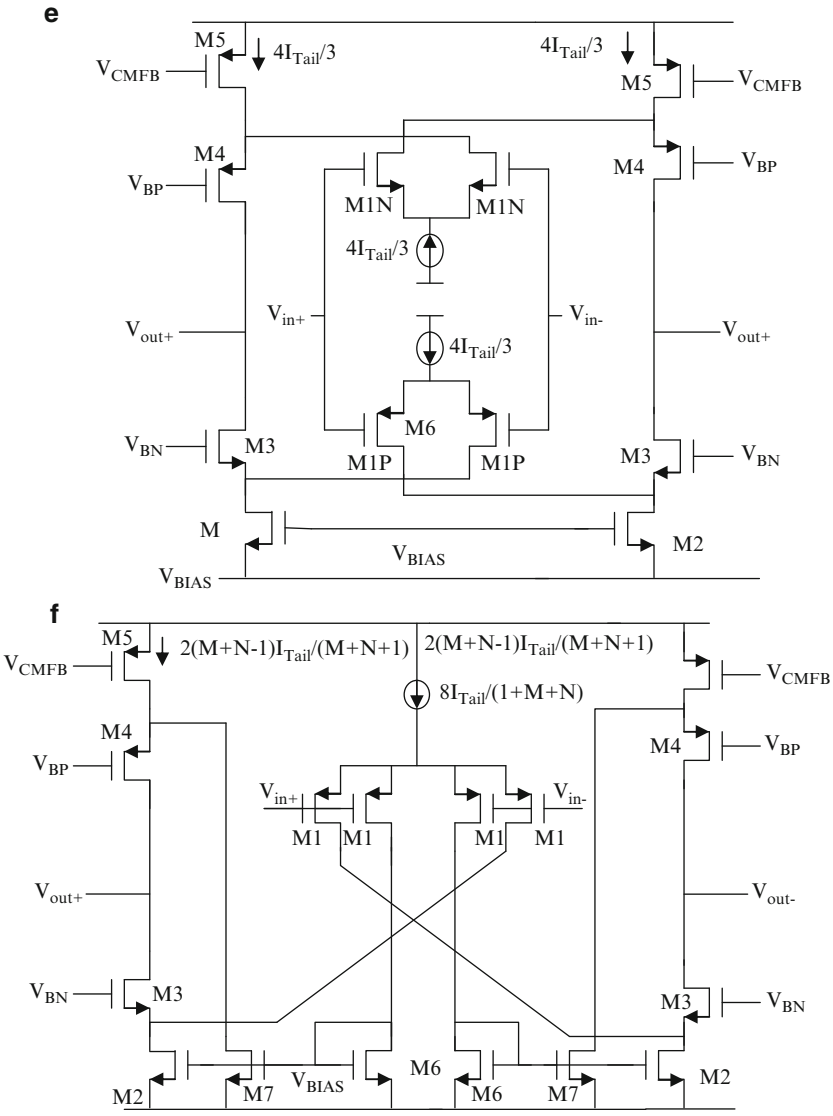


Fig. 4.20 (continued)

Next, we consider the current-mirror cascode OTA shown in Fig. 4.20d which may settle faster than the folded cascode since of its enhanced slew rate and smaller input capacitance. If $N > 1$, a large portion of the overall dc current used will be transferred to the load.

A complementary folded-cascode OTA is presented in Fig. 4.20e in which two differential pairs are used to exploit both cascode transistors. The two feedforward

signal paths create a zero which compensates for the phase degradation due to the two nondominant poles. A greater fraction of the dc current is available for the load in this topology. The noise level is slightly higher than the folded-cascode topology.

Finally, the 3-path OTA is shown in Fig. 4.20f which comprises three OTAs. A folded-cascode OTA is implemented by $M1$, $M2$, and $M3$ and a current mirror cascode is realized using $M1$, $M2$, $M3$, and $M6$. A current mirror folded-cascode OTA is realized using $M1$, $M4$, $M6$, and $M7$. A major portion of the dc current is available as the OTA output current.

4.9.1 SC Filters Using Double Sampling Scheme

High-frequency filters can use the double-sampling scheme (DSS) so that in both phases, the filtering function can be realized. This effectively means that the sampling frequency is doubled. A buffer using double sampling [4.36] is illustrated in Fig. 4.21a. Note that the input is sampled in both phases by two separate feed-in branches and delivered to the output in the other phase. Note that during the interval between the clock phases, the possibility of opamp output glitching out of range can be avoided by using a small capacitor between the output and inverting input of the opamp.

Note that the above circuit has to settle in each clock phase to give the correct output. The settling time requirements can be relaxed at the expense of additional hardware using fully duplicated hardware. An example of an integrator [4.37, 4.38] using double sampling scheme (DSS) but which has full clock cycle time to stabilize is shown in Fig. 4.21b. Moreover, finite gain compensation can be achieved due to the presence of a free clock phase. Such compensation is not possible in the circuit of Fig. 4.21a.

The capacitors C_{B1} and C_{B2} are called battery capacitors which compensate for the opamp finite gain error during integration. The capacitors C_{M1} and C_{M2} are memory capacitors on which the previous samples are stored. Note that C_I is the integrating capacitor. The top opamp operates on the input $V_i(nT)$ and produces the output $V_o(nT)$ in Phase 1. On the other hand, the bottom opamp operates on the input $V_i((n + 1)T)$ and produces the output $V_o((n + 1)T)$ in Phase 2. In Phase 2, the top opamp does the finite gain compensation using the output sample stored on C_{M1} and in Phase 1, the bottom opamp does the finite gain compensation using the output sample stored on C_{M2}.

An E-type biquad based on this concept is presented in Fig. 4.21c to realize a 10.7 MHz IF bandpass filter with a Q of 27 that could successfully work with a clock frequency of 42.8 MHz. The buffer stage is used to enable driving a large capacitive load. The capacitive load was needed to be large in order to meet the low noise requirement.

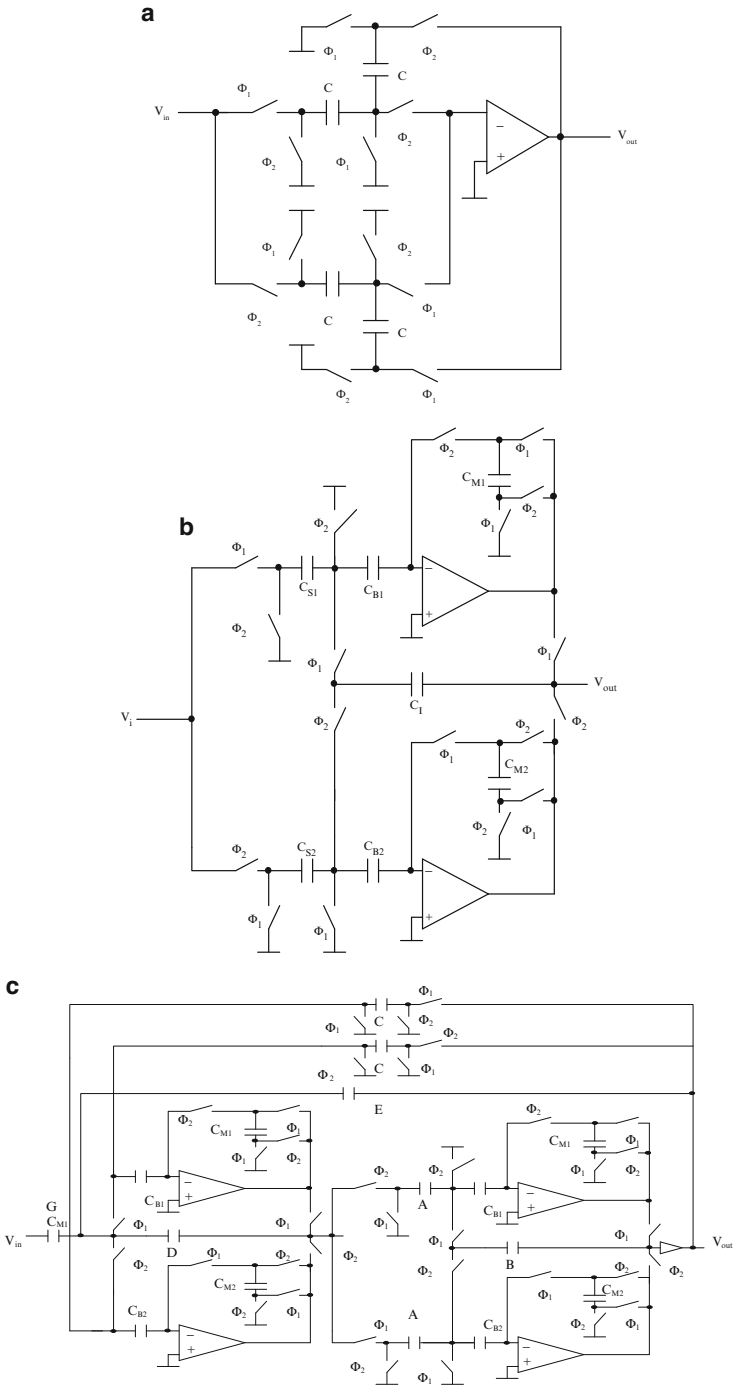


Fig. 4.21 (**a**) Double sampling scheme-based SC buffer stage, (**b**) SC integrator using DSS with compensation for opamp finite gain, and (**c**) E-type biquad using (b) ((a) Adapted from [4.36] © IEEE2000 and (b),(c) Adapted from [4.38] © 1997)

4.9.2 SC Filters Based on POG (Precise Opamp Gain)

The performance of SC filters depends on the sampling frequency and in the case of high sampling frequencies, the gain available from the OTA may not be high [4.39, 4.40, 4.41]. Hence designers have investigated the possibility of designing SC filters using opamps with precise but fixed gain. This technique is known as POG (precise opamp gain). This is briefly considered in this section.

Consider the SC lossy integrator of Fig. 4.22a using an opamp of gain A_o. The transfer function can be easily derived as

$$\frac{V_o}{V_i} = -\frac{C'_1}{\left(C'_2 + C'_3 + \frac{C'_1 + C'_2 + C'_3}{A_o}\right) - C'_2\left(1 + \frac{1}{A_o}\right) z^{-1}} \tag{4.65a}$$

Considering the ideal desired transfer function as

$$\frac{V_o}{V_i} = -\frac{C_1}{(C_2 + C_3) - C_2\, z^{-1}} \tag{4.65b}$$

from (4.65a) and (4.65b), the following relationships can be obtained.

$$C'_1 = C_1, \quad C_2 = C'_2\left(1 + \frac{1}{A_o}\right), \quad C_3 = C'_3 + \frac{C'_1 + C'_3}{A_o} \tag{4.66a}$$

or alternatively as

$$C'_1 = C_1, \quad C'_2 = \frac{C_2}{\left(1 + \frac{1}{A_o}\right)}, \quad C'_3 = \frac{C_3 - \frac{C'_1}{A_o}}{1 + \frac{1}{A_o}} \tag{4.66b}$$

This effectively amounts to predistortion. The expected value of the fixed gain A may vary slightly from to $A(1 + \varepsilon)$ where ε is the error. The resulting pole of the first-order low-pass filter due to this variation can be estimated from (4.65a) by substituting these values and approximating $\frac{1}{1+\varepsilon} = 1 - \varepsilon$ as

$$p' = \frac{C_{2p}\left(1 + \frac{1-\varepsilon}{A}\right)}{C_{2p} + C_{3p} - \frac{C_1}{A} + C_1(1-\varepsilon)\left(\frac{1}{A} + \frac{1}{A^2}\right) + \left(C_{2p} + C_{3p} - \frac{C_1}{A}\right)\left(\frac{1-\varepsilon}{A}\right)} \tag{4.67a}$$

which can be approximated as

$$p' = \left(\frac{C_{2p}}{C_{2p} + C_{3p}}\right)\left(1 + \left(\frac{\varepsilon}{1 + A}\right)\left(\frac{C_{1p}}{C_{2p} + C_{3p}}\right)\right) \tag{4.67b}$$

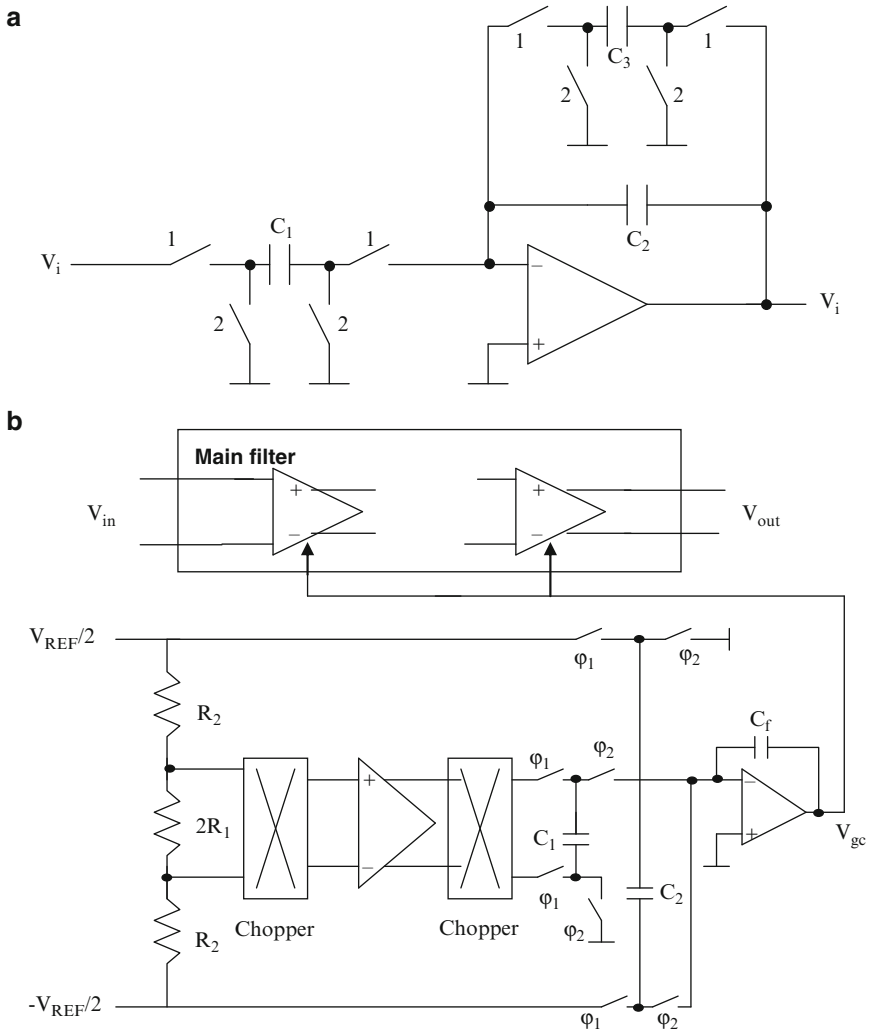


Fig. 4.22 (**a**) A lossy SC integrator using a finite gain opamp, and (**b**) gain control loop for SC filters using POG technique (Adapted from [4.41] © IEEE 2000)

Thus, the error ε can be seen to be divided by A. In other words, if we use an amplifier of gain $A = 100$ with an error ε of 1%, the error looks as though we have used an amplifier of gain 10,000.

It needs to be seen next how to realize a precise gain opamp. It is difficult to control the gain of a CMOS amplifier without a gain control loop. The schematic of such a gain control loop [4.41] is shown in Fig. 4.22b. A replica opamp exactly similar to the actual opamp used in the filter is required. A dc voltage reference $V_{Ref}R_1/(R_1 + R_2)$ is obtained using a potential divider comprising resistors $2R_1$ and two resistors

of value R_2. This voltage is applied to the open-loop opamp of desired gain A whose output voltage evidently is $AV_{Ref}R_1/(R_1 + R_2)$. The difference $\left(C_2\ V_{REF} - \frac{C_1 A V_{REF}\ R_1}{R_1 + R_2}\right)$ is estimated by a stray-insensitive SC integrator formed by capacitors C_1, C_2, and C_f to yield the control voltage V_{gc}. This control voltage varies the gain of the replica amplifier to make the difference zero thus yielding

$$A = \left(\frac{C_2}{C_1}\right)\left(\frac{R_1 + R_2}{R_1}\right) \tag{4.68}$$

The opamp shall be designed to have a high dc gain. The architecture of Fig. 4.22b uses resistive as well as capacitive dividers to reduce the spread. The SC filter uses a low-frequency clock. For example, using $C_2/C_1 = 9$ and $R_2/R_1 = 9$, a gain of 80 can be realized. The offset of the replica opamp may be avoided by using the chopper configuration as shown. The gain control loop settles in a few milliseconds with 0.1% accuracy. The typical clock frequencies for the SC filter, gain control loop, and chopper are, respectively, 100 MHz, 100 KHz, and 50 KHz.

4.9.3 SC N-Path Filters

An alternative method of designing narrow-band SC filters is based on a technique known as *N-path filtering* [4.42]. This technique is considered in detail in this section. By virtue of the sampling theorem, SC filters using a sampling frequency of f_s can process signals in the frequency range $f_s/2$ denoted as the *Nyquist Range*. Increasing the Nyquist Range effectively means that the number of samples in one sample period $1/f_s$ need to be increased. This is possible by having one filter in each path in a N-path system with each path using a sampling frequency of f_s and then combining the outputs of all these paths as shown in Fig. 4.23a for $N = 4$. Note that all the paths having identical filter responses are cyclically sampling at the same frequency f_s. The output signal is composed of N samples per period $T_c = 1/f_s$. The effective sampling frequency of an N-path filter is Nf_s and hence the Nyquist range is $Nf_s/2$. The overall frequency response of the N-path filter is the same as the frequency response of the individual path for all switch positions i. Considering the use of a low-pass filter in each path of cutoff frequency f_o, the result is that the spectrum of the base-band LPF repeats at kf_s as shown in Fig. 4.23b. Thus, effectively, a comblike band-pass response is created. The bandwidth of the band-pass response is $2f_o$ thus effectively realizing a Q for the band-pass filter of $kf_s/2f_o$. for the band-pass response centered at kf_s.

Note that any one of the band-pass responses centered around f_s, $2f_s$, $3f_s$, and so on can be selected using a postfilter (a band-pass filter centered at that frequency). The advantage gained in this approach is that due to the higher sampling frequency, the antialiasing filter will be very simple.

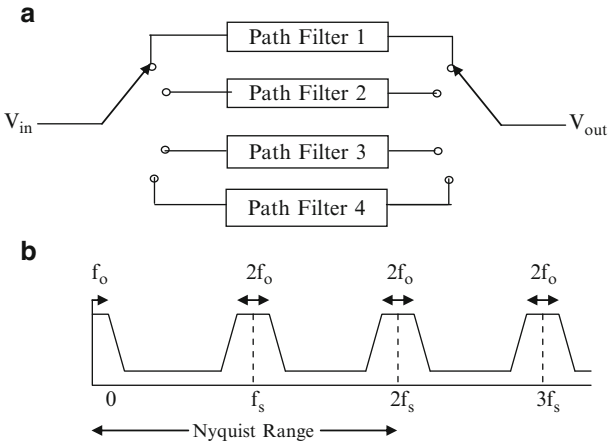


Fig. 4.23 (**a**) *N*-Path filter structure using a low-pass filter in each path, and (**b**) its frequency response

Some simple circuits will be useful [4.43] for selecting only the response centered around f_s and rejecting the response at dc and at all even multiples of f_s. One such z-domain transfer function is

$$H(z) = (1 - z^{-1/2}) \tag{4.69}$$

The SC low-pass filter response is shown in Fig. 4.24a. This transfer function (4.69) has a response as shown in Fig. 4.24b thus yielding the overall band-pass response as shown in Fig. 4.24c.

It is further important to note that the unwanted mirror frequencies appear at the output due to the path mismatch at various multiples of f_s, for example, $2f_s - f_o$, $2f_s + f_o$. These may exist in the pass-band of the filter and hence care has to be taken to match the various paths. In addition due to the parasitic drain-gate and gate-source capacitances of the switches used, there will be a clock feedthrough signal at the output that not only produces an offset voltage but also produces additional spectral components at multiples of the clock frequency. These will reduce the dynamic range of the SC filter.

If the path filter is a high-pass filter, then the spectrum will have a band-pass response at multiples of $f_s/2$. Interestingly, in this case, the clock feedthrough does not exist in the pass-band.

The significant advantage of N-path filter is that the center frequency does not depend on capacitor ratios. Moreover, high-Q band-pass filters can be realized using low-Q blocks. Thus the sensitivity to component tolerances can be controlled easily. Moreover, since the center frequency of the band-pass filter depends only on the sampling frequency or its multiple, component tolerances of the filter will not come into the picture. Only the mid-band gain and Q are dependent on the capacitor ratios.

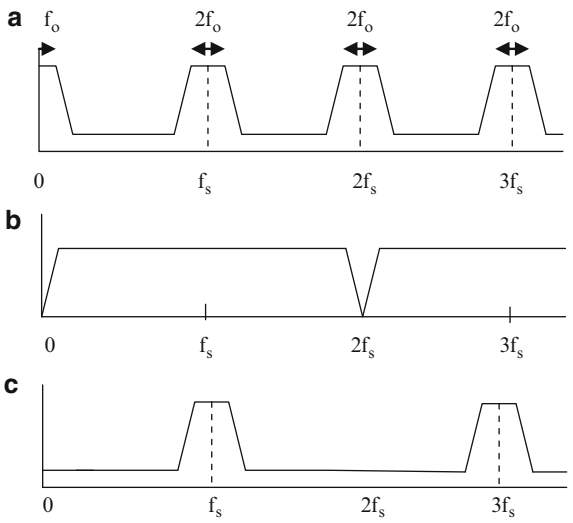


Fig. 4.24 Frequency response of (**a**) SC low-pass filter, (**b**) frequency-sampling filter, and (**c**) combined low-pass and frequency sampling filter

4.9.3.1 Single-Path Frequency Translated SC Systems

As a generalization of the *N*-path filter, Franca and Haigh have suggested the use of single-path frequency translated SC systems [4.44]. These are based on the fact that all sampled-data filters have band-pass frequency response at multiples of clock frequency and any one of the band-pass responses can be chosen by inserting an appropriate antialiasing filter (AAF) and anti-imaging filter (AIF) as shown in the architecture of Fig. 4.25a. They have suggested the use of two constants m and n defined as $m = f_s/f_o$ and n defined as the band centered at $nf_s + f_o$ or $nf_s - f_o$. Evidently, the realized Q of the band-pass filters is $Q = kQ_1$ where $k = mn \pm 1$ and $Q_1 = f_o$/Bandwidth of the SC bandpass filter. Thus there is Q enhancement. The advantage is that from a relatively low-Q prototype band-pass filter, a very high-Q band-pass filter can be obtained. This can be seen by noting that the bandwidth of the band-pass response remains the same whereas the center frequency changes depending on m and n.

Evidently, a variety of choices for m and n is possible. The choice of the upper or lower sideband ($nf_s - f_o$) or ($nf_s + f_o$) depends on the selectivity of the antialiasing filter needed. If $m > 1$, the frequency translated bands are close to odd multiples of $f_s/2$, thus needing a steeper cutoff for the AAF at the upper transition band. Similarly, if $m = 2$, the lower transition band will need higher selectivity. On the other hand, if $m = 4$, a symmetric AAF will be needed. Due to the sample and held nature of the signals at the output of the SC band-pass filter, there will be slowly decreasing gain as n increases. This needs to be corrected by the anti-imaging band-pass filter.

Often, a decimator may precede the SC filter (see Fig. 4.25b) so as to ease the prefiltering requirement of the continuous-time antialiasing filter. Decimators are

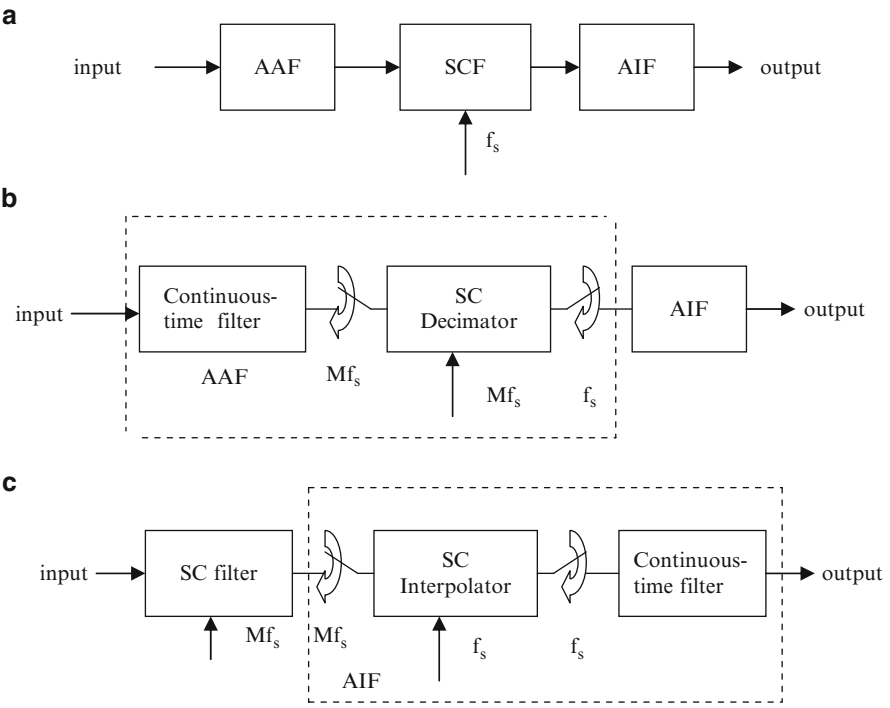


Fig. 4.25 (**a**) A SPFT SC filter system architecture, (**b**) antialiasing filter with a SC decimation filter, and (**c**) anti-imaging filter with interpolation filter (Adapted from [4.44] © IEEE 1988)

used to reduce the sampling rate. As an illustration, if a SC filter works at a sampling frequency of 100 KHz, a decimation by 10 implies that the sampling rate of the input of the decimator is 1 MHz. Thus, the antialiasing filter in this case needs to attenuate to the desired extent the aliasing frequency corresponding to the higher sampling rate. Thus, in place of complex continuous-time filters, a simple first- or second-order antialiasing filter will serve the purpose. In a similar manner, the AIF also can have a counterpart interpolation filter (see Fig. 4.25c) which increases the sampling rate at the output to 1 MHz thus enabling the use of a simple smoothing filter. The interpolation and decimation filters can be single-stage designs based on FIR filters or a combination of IIR and FIR filters. The reader is referred to [4.44] for details on possible designs.

A typical N-path filter structure using a passive path filter is shown in Fig. 4.26b based on the path filter shown in Fig. 4.26a. Note that the path transfer function is given by

$$H(z) = \frac{C_1 z^{-1}}{(C_1 + C_2) - C_2 z^{-1}} \tag{4.70a}$$

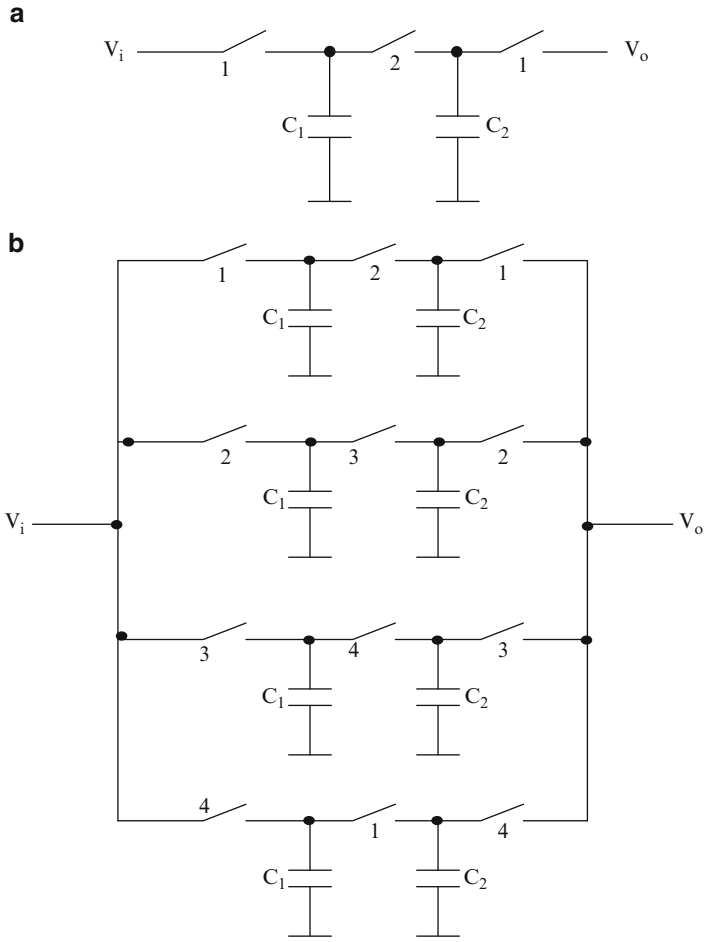


Fig. 4.26 (**a**) A low-pass path filter, (**b**) four-path filter based on (a)

The overall transfer function of the four-path filter needing a four-phase clock is given by

$$H(z) = \frac{C_1\, z^{-4}}{(C_1 + C_2) - C_2\, z^{-4}} \tag{4.70b}$$

Note that (4.70b) can be obtained by using $z \rightarrow z^N$ transformation [4.45] from (4.70a). Note that the output is available in each phase and hence is available all the time. Effectively, the sampling frequency is increased fourfold. It is important to note that there may be a mismatch between capacitor values in the various paths, which leads to generation of additional mirror frequency components in addition to the desired output signal.

4.9.3.2 Z to Z^N Transformation

It is relevant to mention that $z \rightarrow z^N$ transformation creates several pass-bands at if_s/N ($i = 0, 1, 2, \ldots, (N-1)$) where f_s is the sampling frequency. In the case of an integrator transfer function $H(z) = \frac{1}{1-z^{-1}}$, it is mapped into an Nth-order band-pass filter of transfer function $H(z) = \frac{1}{1-z^{-N}}$. This can be seen from the fact that $z^N = e^{j\omega TN} = e^{j2\pi k}$ for $f = \frac{kf_s}{N}$. Thus, the center frequency of the bandpass response is at f_s/N, $2f_s/N$, $3f_s/N$ and so on.

Similarly, using the transformation $z \rightarrow -z^N$, an integrator transfer function is mapped into an Nth-order band-pass filter [4.46]. In this case, it may be observed that

$$-z^N = -e^{j\omega NT} = e^{j(\omega NT+\pi)} = -e^{jNT\left(\omega+\frac{\pi}{NT}\right)} \tag{4.71}$$

meaning that the low-pass response is shifted by $\frac{\pi}{NT}$ along the frequency axis.

In this case, several pass-bands at $if_s/(2N)$ ($i = 1, 3, 5, \ldots$) where f_s is the sampling frequency are created. The advantage of the latter is that the passband is free from clock feedthrough noise.

For $N = 2$, an HP N-path filter is possible, whereas for $N \geq 3$ only an LP N-path filter is realizable. The reason is that for $N = 2$, in the LP case, the desired passband will be centered at $f_s/2$ and hence the signal in the upper half will alias into the lower half and vice versa.

4.9.3.3 Pseudo *N*-Path Filters

In order to avoid the mismatch related problems, an alternative solution known as the *pseudo N-path filter* has been suggested in the literature [4.47]. In this method, only one path exists but each memory processing element in the path is sequentially connected to a circulating delay line that discharges and recharges the various elements such that the overall circuit still appears to have N paths. The circuit of course becomes complicated. Two architectures based on a circulating delay line and RAM (random access memory) are described in the literature [4.48]. These are considered next.

Pseudo *N*-Path Filters Based on Circulating Delay Line

The SC N-path filter based on the single-path lossless integrator is shown in Fig. 4.27a which uses a circulating delay line. The basic N-path filter must be able to integrate the injected charge with a stored charge that held N sample periods before. The three-path filter derived from Fig. 4.27a is shown in Fig. 4.27b which needs a four-phase clock as shown in Fig. 4.27c. Note that the capacitor C is used for the integration whereas the capacitors C_1, C_2, and C_3 are used to form the delay

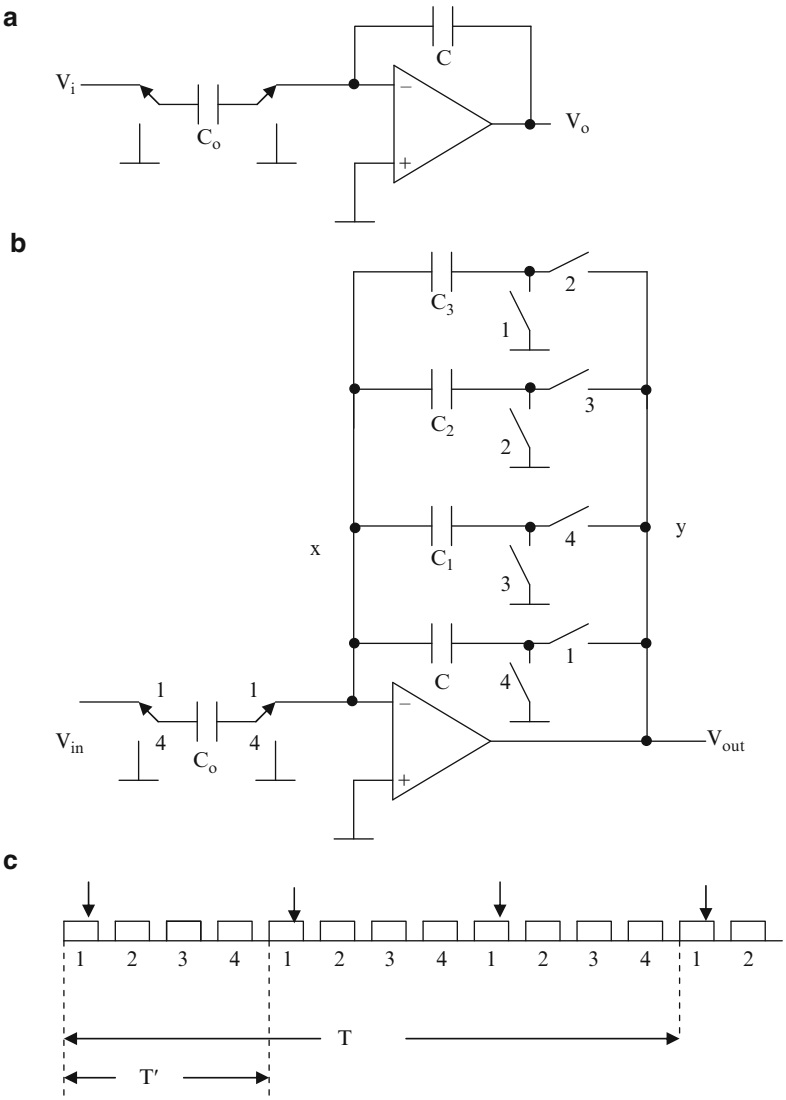


Fig. 4.27 (**a**) Stray-insensitive inverting integrator, (**b**) SC pseudo-three-path integrator based on (**a**), and (**c**) timing waveforms (b,c Adapted from [4.48] © IEEE 1982)

line. The operation of the circuit is as follows. In Phase 1, the input capacitor C_o and the memory capacitor C_3 update the charge on feedback capacitor C. In Phase 2, the charge on capacitor C_2 is shifted to C_3 using the opamp. In a similar manner in Phases 3 and 4, the charge on C_1 is successively transferred to C_2, the charge updated in Phase 1 on C is transferred to C_1, and C_o is discharged. The above cycle is repeated. In other words, in four clock cycles the charge on C is moved to C_3.

The values of C, C_1, C_2, and C_3 do not matter since all the charge available on one capacitor is transferred to the other using the opamp. The transfer function is only determined by C_o and C. In four cycles, the charge on C_1 has moved one step forward. Thus the charge on C_3 corresponds to an input fed to C_o reached after 12 cycles. Evidently, an output sample is available in $(N + 1)$ th, the clock Phase. The lowest clock feedthrough frequency (since output is taken only in phase 1) is $1/T'$ which is far away from the pass-band. (Note that the pass-band is centered round $f_o = 1/T$). Note that this type of N-Path filter has only one circulating loop and all the charge packets follow the same path in the circuit. The pass-band thus will be free from clock feedthrough noise.

The transfer function realized is

$$H(z) = -\frac{C_o/C}{1 - z^{-3}} \tag{4.72a}$$

Noninverting operation can be obtained easily by interchanging the clock phases at the right-hand side of the capacitor C_o in Fig. 4.27b. The transfer function then becomes

$$H(z) = \frac{C_o/C}{1 - z^{-3}} \tag{4.72b}$$

Pseudo N-Path Filters Based on RAM

An alternative pseudo N-path filter structure has the advantage that the number of clock steps required can be reduced to 8 instead of the 12 needed in the circulating delay line technique described earlier. This three-path integrator circuit is shown in Fig. 4.28a. The operation of the circuit is as follows. In Phase 1 (synchronous with Phase 3), the input charge fed through C_o together with the charge stored on C_1, is transferred to the capacitor C. In Phase 4 (synchronous with Phase 2), the updated charge on C is transferred back to C_1. Similarly, in the next Phase 1 (synchronous 2 with Phase 5), the charge on C_2 is integrated together with the input charge on C_o, and the resulting charge on C is transferred back to C_2 in Phase 6 (synchronous with Phase 2). In the next step the process repeats for C_3. It can be observed that each capacitor C_1, C_2, or C_3 stores charge for three intervals of T' since each is updated in Phase 1 and when Phase 3 or 5 or 7 occurs. Evidently, the RAM-based design needs eight clock signals as against four in the circulating delay line-type SC N-path filter. Evidently, an output sample is available in every second clock phase. Moreover, it is not immune to the clock feedthrough noise in the center of the passband, since charge packets belonging to different paths are stored on different capacitors. Note that N circulating loops exist in this type of N-path filter. Thus asymmetries in clock signals and switch dimensions are not automatically balanced out.

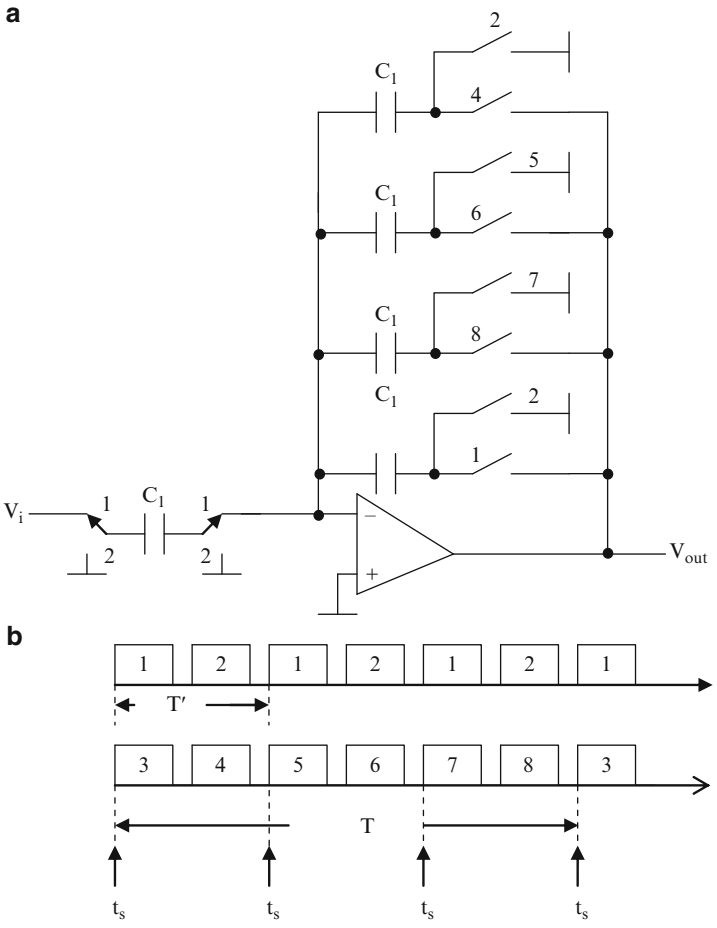


Fig. 4.28 (**a**) A RAM-type pseudo *N*-path filter, and (**b**) timing waveforms (Adapted from [4.48] © IEEE 1982)

It is possible to combine both techniques, using circulating delay line and RAM, as well to obtain *hybrid pseudo N-path filters*. These need, however, one extra opamp but use two phases only as in the case of RAM-based designs considered earlier. The operation of this circuit [4.49] shown in Fig. 4.29 is as follows. In Phase 1 (i.e., Phase 3), the charge from input on C_3 is transferred to C. Simultaneously, the charge on C_4 is transferred to C_1. In Phase 2, synchronous with Phase 4, the charge on C is transferred to C_4. Simultaneously, the charge on C_2 is transferred to C_3. During the next Phase 1 synchronous with Phase 5, in a similar manner as before, the charge on C_4 is transferred to C_2 . In Phase 2 synchronous with Phase 6, the charge on C_1 is transferred to C_3. Thus there are two charge circulations $C \rightarrow C_4 \rightarrow C_1 \rightarrow C_3 \rightarrow C$ and $C \rightarrow C_4 \rightarrow C_2 \rightarrow C_3 \rightarrow C$. There are two delay lines comprising (C_4, C_1, C_3) and (C_4, C_2, C_3). Note that their values do not affect the performance.

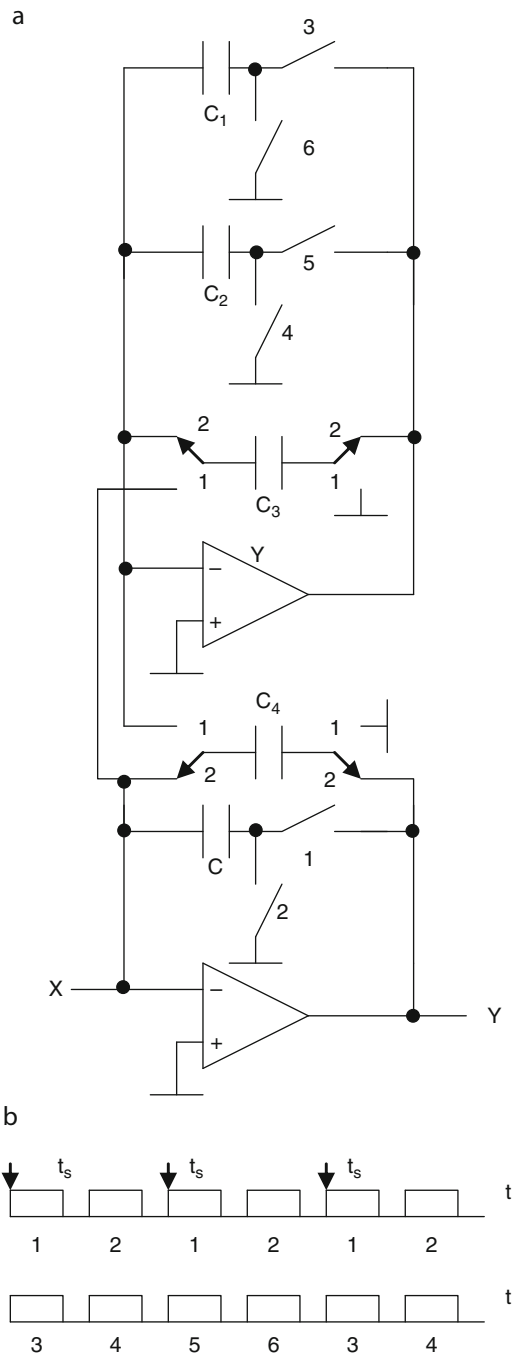


Fig. 4.29 (**a**) A hybrid pseudo *N*-path filter, and (**b**) switching waveforms (Adapted from [4.49] © IEEE 1985)

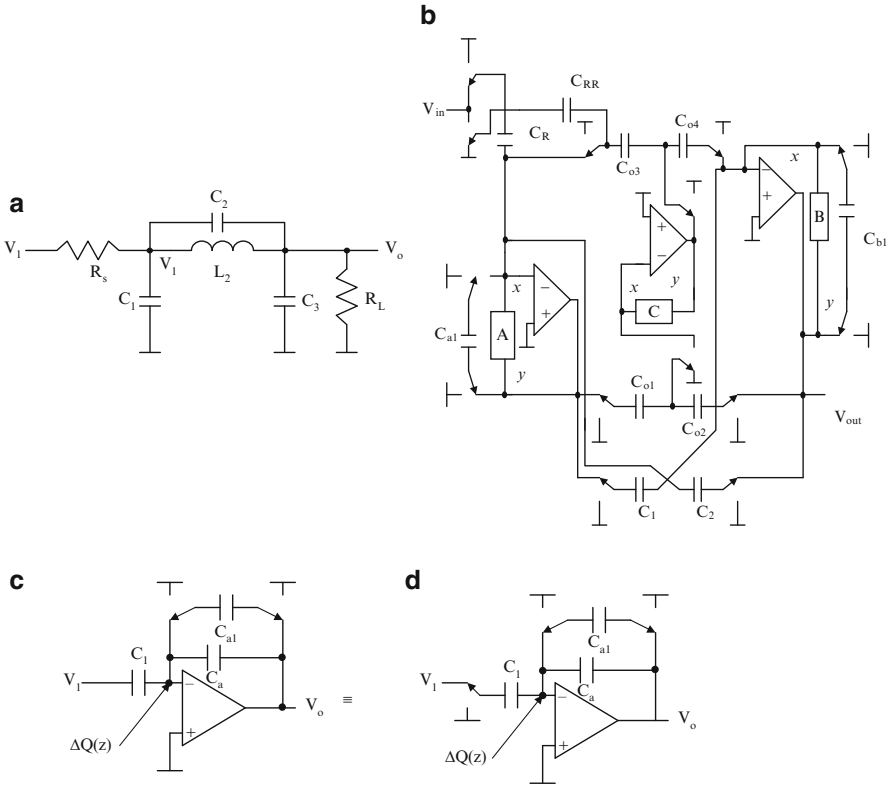


Fig. 4.30 (**a**) A third-order low-pass elliptic filter prototype, (**b**) SC bilinear *N*-path ladder filter, (**c**) capacitive coupling needed for realizing elliptic filters, and (**d**) equivalent of (c) to simplify the circuit of the *N*-path filter (Adapted from [4.48] © IEEE 1982)

It can be seen from the timing waveform that the number of clock phases is more than that of circulating delay line type pseudo *N*-path filters but the clock feedthrough now occurs at $f_c/2$ and f_c and not at the pass-band centered at $f_c/3$.

Application to Ladder Filters

The integrators in high-order SC filters derived from prototype RLC ladder filters can be substituted by the pseudo *N*-path integrators to obtain very narrow band and low-sensitivity band-pass filters. As an illustration, the technique for realizing an elliptic band-pass *N*-path filter [4.48] using a circulating delay line based on a low-pass elliptic filter of Fig. 4.30a is presented in Fig. 4.30b. Note that the resistor simulating switched capacitors remain as they are whereas the integrating capacitors are replaced by the blocks containing $N + 1$ switched capacitors as shown in Fig. 4.30b. The important point to note is that the coupling capacitors needed in the realization of elliptic filters need not be replaced by the *N*-path branches by a simple observation that the circuits of Fig. 4.30c, d are identical.

Thus a switched-capacitor can take the place of the coupling capacitor. Note that by replacing the branches A, B, and C in Fig. 4.30b with capacitors, a bilinear SC low-pass filter can be identified.

A stray-insensitive SC N-path filter can be obtained from the high-pass filter of Fig. 4.19b. This uses z to z^{-N} transformation. The inversion is realized using a fully differential topology. It may be recalled that the circuit of Fig. 4.19b is not stray-insensitive due to capacitors C_{a1}, C_{b1}, C_{c1}, C_{d1}, and C_{e1}. A stray-insensitive realization can be obtained [4.46], which is amenable for realizing a N-path filter based on RAM. This is seen by rewriting (4.63b) as

$$V_i\frac{(1-z^{-1})}{R_s}-V_1\left((1-z^{-1})\left(\frac{1}{R_s}+\frac{1}{L_1}+\frac{1}{L_2}+C_2\right)+2z^{-1}\left(\frac{1}{L_1}+\frac{1}{L_2}+C_2\right)\right)$$
$$+V_2\left(\left(\frac{1}{L_2}+C_2\right)(1-z^{-1})+2z^{-1}\left(\frac{1}{L_2}+C_2\right)\right)-(V_2-V_1)C_2\frac{4z^{-1}}{(1-z^{-1})}=0 \tag{4.73a}$$

and the equation at node V_2 can be written similarly as

$$\frac{V_i}{R_s}-V_1\left(\frac{1}{R_s}+\frac{1}{L_1}+\frac{1}{L_2}+C_2\right)+V_2\left(\frac{1}{L_2}+C_2\right)$$
$$-z^{-1}\left(-\frac{V_i}{R_s}-V_1\left(-\frac{1}{R_s}+\frac{1}{L_1}+\frac{1}{L_2}+C_2\right)+V_2\left(\frac{1}{L_2}+C_2\right)\right)$$
$$-(V_2-V_1)C_2\frac{4z^{-1}}{(1-z^{-1})}=0 \tag{4.73b}$$

Note that in Phase 1 (i.e., Phase 3), the input capacitor C_s, the damping capacitor C_{AA}, capacitor C_x, and the memory capacitor C charge the lower capacitor C_x. This charge upon inversion together with the input is used in Phase 2 (i.e., Phase 4) to update the charge on memory capacitor C. The circuit can be obtained by pooling all z^{-1} terms and all non $-z^{-1}$ terms and realizing them using common capacitors/switched-capacitors as shown. In the next Phases 1 and 2 (and Phases 5 and 6), the memory capacitor of the other path comes into picture. Note that the SC branches A' and C' have capacitors C_{AA} whereas the branch B′ does not have C_{AA}. The various capacitor values are as follows.

$$C_a=\frac{1}{L_1}+\frac{1}{L_2}+C_2-\frac{1}{R_s},C_s=\frac{1}{R_s},C_{aa}=\frac{1}{R_s},C_{bb}=\frac{1}{R_L},C_d=C_e=\frac{1}{L_2}+C_2,$$
$$C_{o1}=C_{o2},C_{o3}=C_{o4},C_b=\frac{1}{L_2}+\frac{1}{L_3}+C_2-\frac{1}{R_L},C_c=\frac{C_{o1}\,C_{o3}}{4\,C_2} \tag{4.74}$$

The reader may note the difference in the capacitor values. The RAM-type branch is shown in Fig. 4.31a and the complete SC HP2-path filter is shown in Fig. 4.31b.

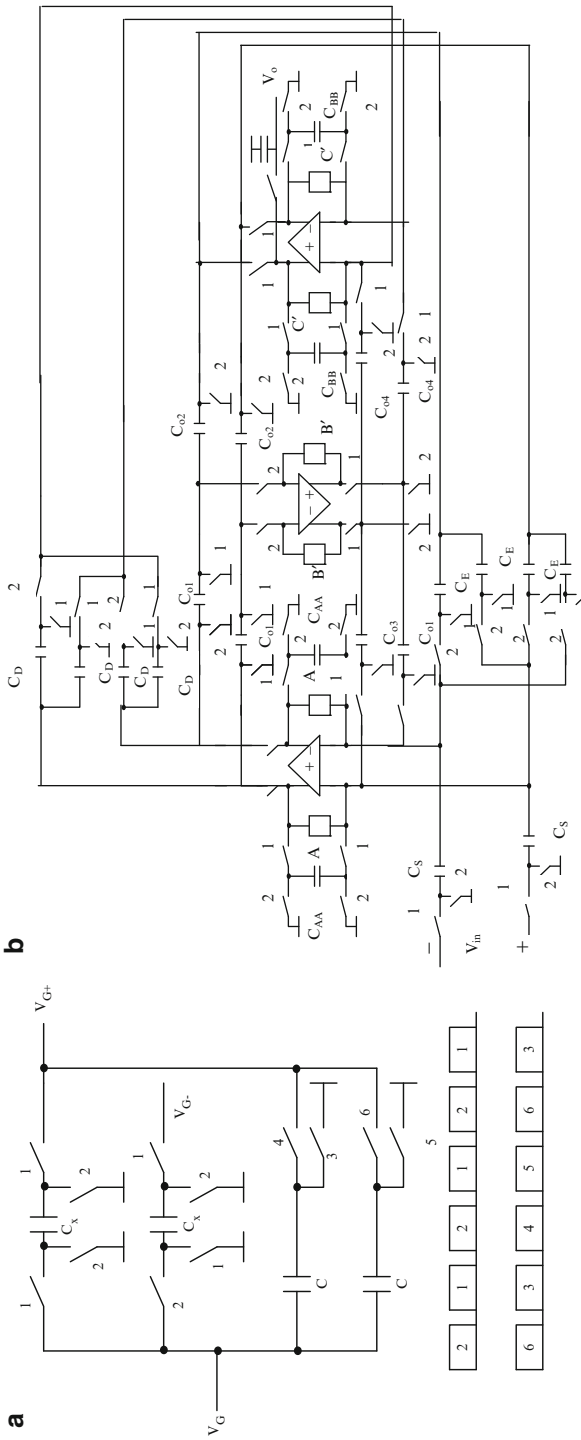


Fig. 4.31 (**a**) A RAM-type feedback branch, and (**b**) stray-insensitive differential HP two-path SC filter (Adapted from Lin and Nevin [4.46] © IEEE 1988)

Palmisano and Montecchi [4.50] have suggested a technique for realizing $z \rightarrow -z^{-N}$ transformed SC filters. This method also uses differential-output differential-input opamps. The basic RAM-type pseudo N-path cell is shown in Fig. 4.32a together with the relevant timing waveforms. A differential 2-path SC lossless integrator based on Fig. 4.32a is shown in Fig. 4.32b. In this circuit, C_F is the integrating capacitor and the capacitors C_1 and C_2 form the storage array of capacitors. The circuit is made stray-insensitive due to the availability of differential outputs and differential inputs. When phases A and 1 are ON, capacitor C'_F receives charge from the input capacitor C'_1 and from the storage capacitor C''_1 which belongs to the opposite path. This operation provides the needed sign inversion required by the transformation. During Phase 2, the updated charge in C'_F is transferred back to C'_1 in the storage array. This charge is held on C'_1 for two sampling periods. The same operation is repeated during phase B with the charge stored on C''_2. The resulting transfer function is thus

$$H(z) = \frac{V_{out2} - V_{out1}}{V_{in2} - V_{in1}} = \frac{C_1}{C_F}\left(\frac{1}{1 + z^{-2}}\right) \tag{4.75a}$$

The application of this cell to realize sixth-order band-pass ladder filters is shown in Fig. 4.32c. Note that the low-pass SC filter needs unswitched coupling capacitors between outputs of certain opamps and inverting the input of certain opamps which need to be replaced by switched capacitors so that the memory function of the capacitors is realized by the RAM cells. The reader is urged to verify the correctness of this approach.

Several N-path filter structures and variants have been suggested in the literature with an aim to increase the frequency of operation for applications in video filters and band-pass sigma-delta modulators. These are considered briefly in this section.

Quinn [4.51] and Quinn et al. [4.52] have suggested a technique known as "charge redistribution" shown in Fig. 4.33a. Note that this three-path fully differential filter realizes a transfer function given by

$$H(z) = \frac{1 - \beta^3}{1 + \beta^3\ z^{-3}} \tag{4.75b}$$

where $\beta = e^{\frac{-\pi f_o}{Qf_s}}$ is chosen to realize the desired pole-Q and the center frequency is $f_s/6$. (Note that only the single-ended version is shown). The Q realized can be shown to be $\frac{\pi}{6\ln(\beta)}$. The reader is urged to prove this. Thus Q realized is a function of the ratio of capacitors. The circuit, however, uses four-paths to realize a delay of three clock periods. A simplified single-ended version of this 4-phase circuit is shown in Fig. 4.33b, which shows two antiphase filter paths. Initially, C_a samples V_{in} and C_b samples V_{out}. After three clock periods, C_a and C_b are connected in parallel to redistribute their charge realizing the transfer function for the path as

$$\frac{V_{out}}{V_{in}} = \frac{C_a\ z^{-3}}{(C_a + C_b) + C_b\ z^{-3}} \tag{4.75c}$$

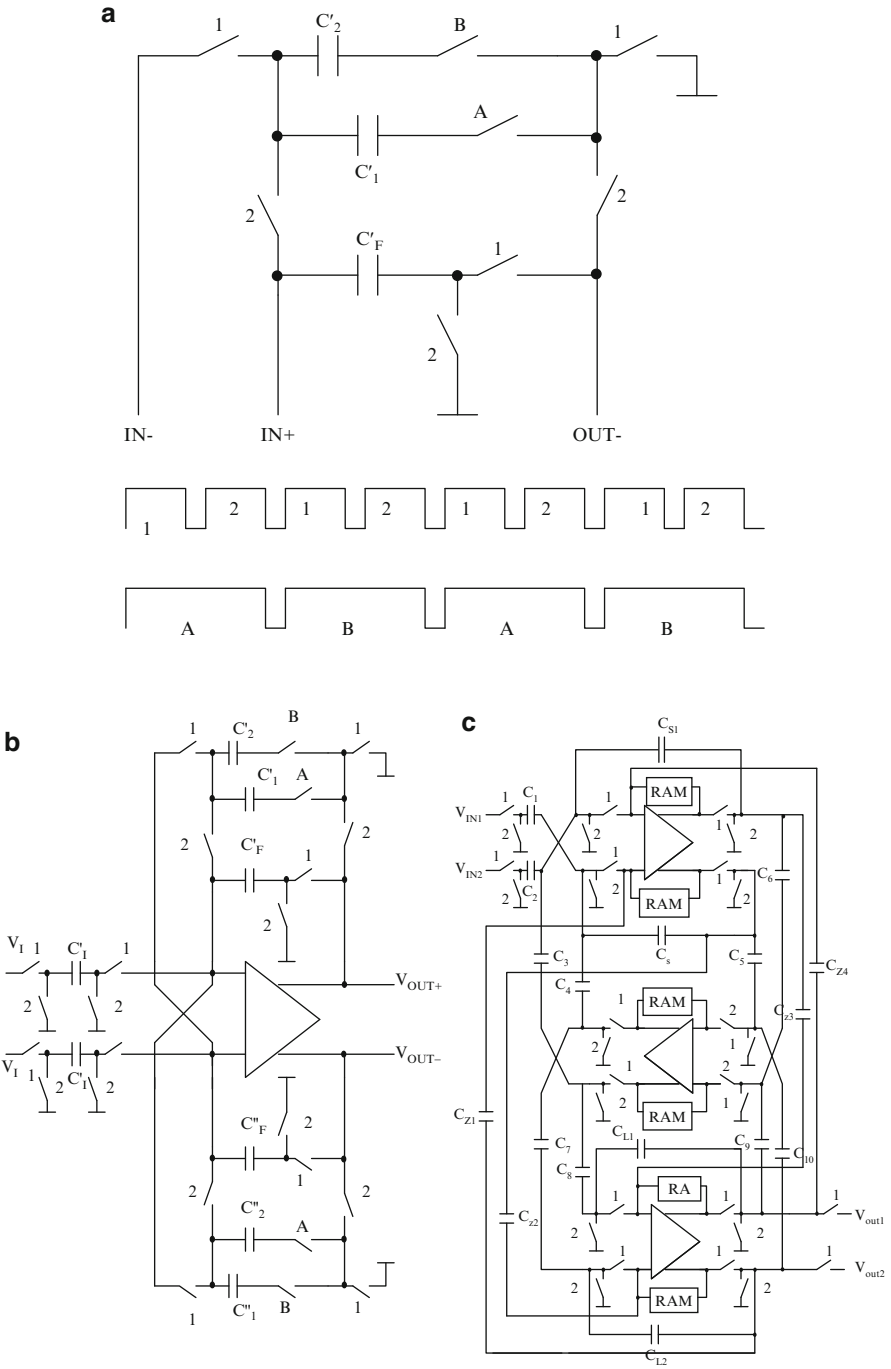


Fig. 4.32 (**a**) RAM-type pseudo N-path cell for realizing $z-z^{-N}$ transformation for $N = 2$ with timing waveforms, (**b**) differential SC two-path lossless integrator based on (a), and (**c**) sixth-order band-pass SC filter derived from third-order low-pass prototype (Adapted from [4.50] © IEEE 1989)

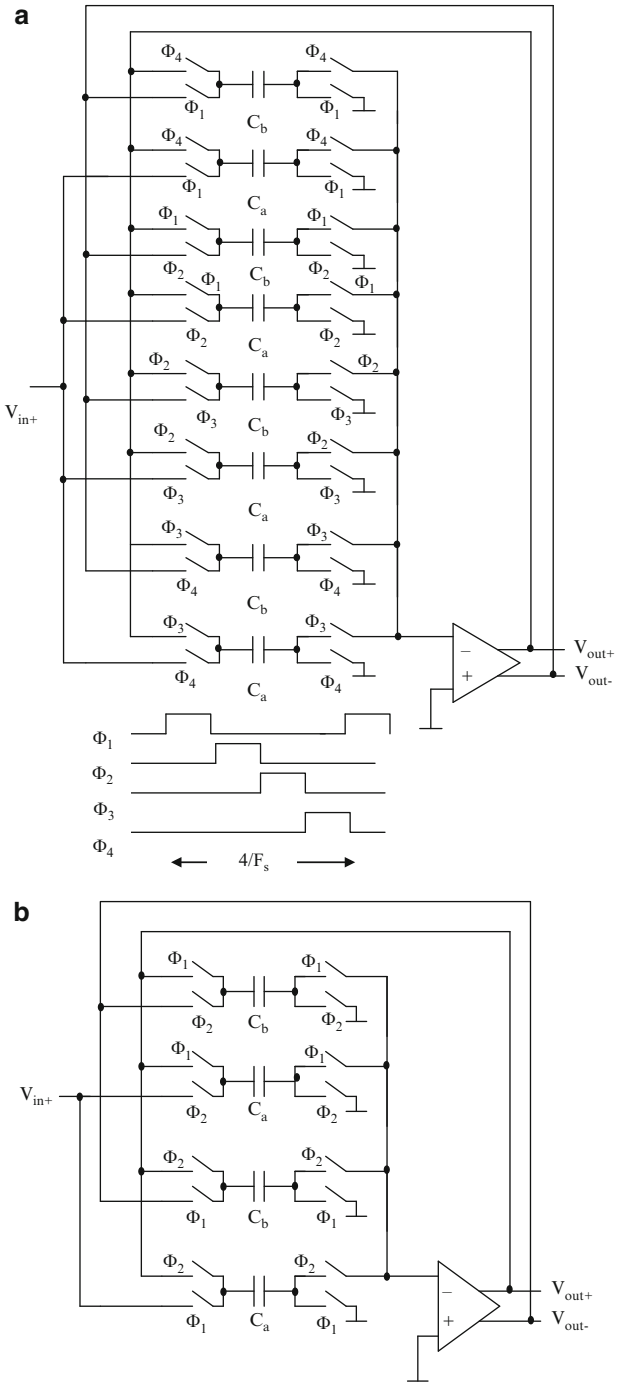


Fig. 4.33 (**a**) SC recursive charge-distribution bandpass filter having three paths, (**b**) simplified version of (a) for two paths (Adapted from [4.51] © IEEE 1998)

Evidently, $\beta = \left(\frac{C_b}{C_a + C_b}\right)^{1/3}$. A Q of 16 at a center frequency of 4.286 MHz has been shown to be realizable with $\beta = 0.9678$. Quinn et al. [4.52] have extended the work for realizing a 10.7-MHz radio IF filter for details of which the reader is referred to their work.

4.9.3.4 SC *N*-Path Filters Using Double-Sampling

The double-sampling principle has been applied to N-path filters in order to increase the over-sampling rate in sigma-delta converters. Liu et al. [4.53] have proposed a pseudo 2-path band-pass filter shown in Fig. 4.34a which uses only one opamp per stage. This circuit needs five clock waveforms (see Fig. 4.34b). The operation of the circuit is as follows. In the circuit of Fig. 4.34a, the capacitors (C_1,C_2) and (C_3,C_4) are sampling capacitors and (C_{a1},C_{a2}), (C_{b1},C_{b2}), and (C_{c1},C_{c2}) are storage capacitors. All the capacitor values can be the same. For this circuit, at time n, Clk1 is high, Clk2 is low, and ClkC1 is high. The input voltage is sampled on capacitors C_1 and C_2. The output voltage appearing at the capacitor pair C_{C1}, C_{C2} is given as

$$V_{out}(n) = V_{in}(n-1) - V_{out}(n-2) \tag{4.76a}$$

where $V_{in}(n-1)$ was sampled to C_3 and C_4 at time $(n-1)$ and $V_{out}(n-2)$ is the voltage on C_{b1},C_{b2} at time $(n-2)$. Note that C_3 and C_{b2} transfer charge to C_{C1} and C_4 and C_{b1} transfer to C_{c2}. In this process, evidently, the charges on C_{b1} and C_{b2} have become zero. At time $n+1$, the same operation continues and clock signal ClkB1 is high. In this step, the input voltage is sampled on capacitors C_3 and C_4. The output voltage appears at the capacitor pair C_{b1}, C_{b2}. The charges on C_{a1} and C_{a2} also are transferred in this step to C_{b1} and C_{b2}. It is evident that now C_{a1},C_{a2} are free. The charge transfer is described as

$$V_{out}(n+1) = V_{in}(n) - V_{out}(n-1) \tag{4.76b}$$

In the next step, a similar operation takes place but with input stored on C_1 and C_2 and storage carried out on C_{a1}, C_{a2} and capacitors with the old charge being C_{c1} and C_{c2}. This cycle repeats. The charge transfer is described as

$$V_{out}(n+2) = V_{in}(n+1) - V_{out}(n) \tag{4.76c}$$

Thus the transfer function realized is $z^{-1}/(1+z^{-2})$. The circuit thus has performed the double-sampling function. The frequency of clocks ClkA1, ClkB1, and ClkC1 is two-thirds of the frequency of Clk1 and Clk2, therefore the clock feedthrough occurs at $f_s/3$, $2f_s/3$, and f_s which are outside the pass-band.

The DSP2P (double-sampling pseudo two-path filter) described in Fig. 4.34a cannot realize variable bandwidth since the application was for realizing a

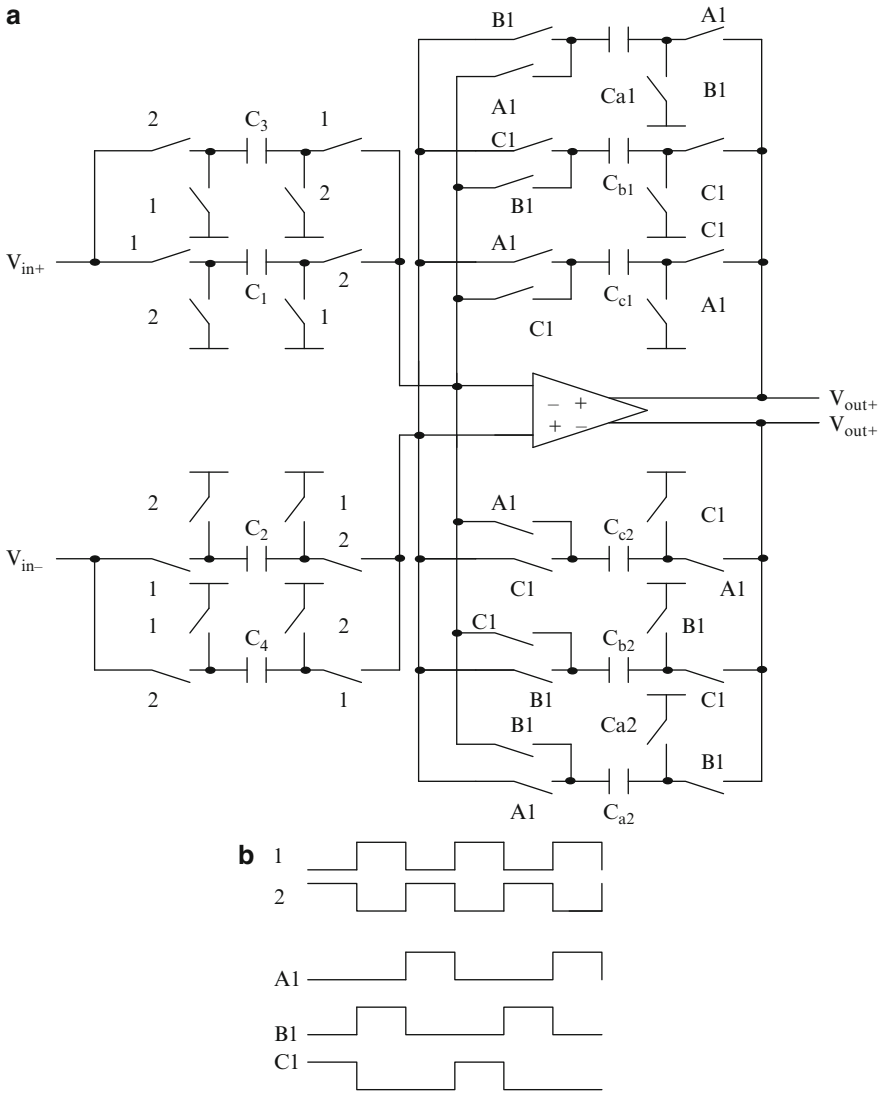


Fig. 4.34 (**a**) Double sampled pseudo two-path filter for realizing $z^{-1}/(1 + z^{-2})$, (**b**) switching waveforms (Adapted from [4.53] © IEEE 2000)

sigma-delta modulator. However, a variable bandwidth band-pass filter can be realized using an alternative circuit due to Ng et al. [4.54] wherein they introduce an additional degree of freedom. The operation of this circuit shown in Fig. 4.35a is as follows. In this circuit using a three-phase clock and fully differential topology, the integrating capacitor is made up of two parts: capacitors C_{FA} and C_{DA}. During Phase C, the input is sampled on the capacitor C_{SA}. In Phase A, the charge on C_{SA}

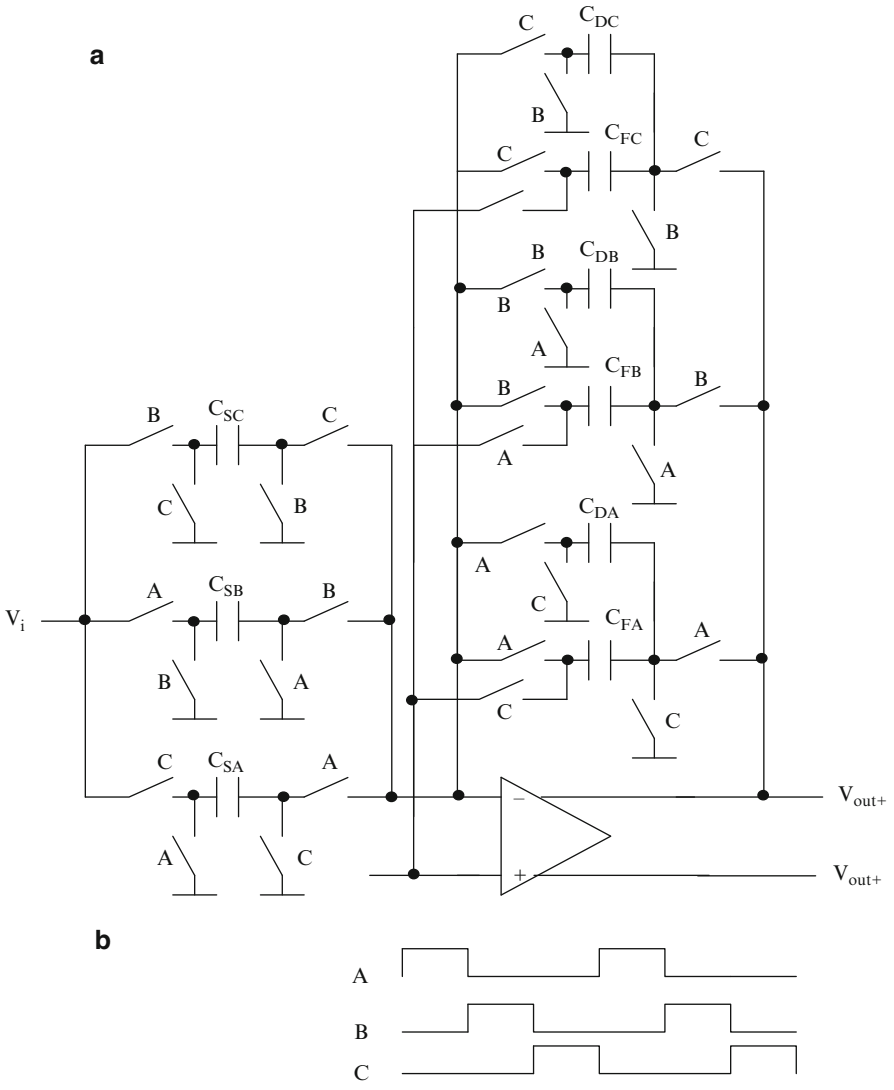


Fig. 4.35 (**a**) DSP2P band-pass filter architecture with variable bandwidth, (**b**) clocking waveforms (Adapted from [4.54] © IEEE 2005)

is updated on the capacitors C_{FA}, C_{DA}. The signal is held for one clock period. Later, in Phase C, only the charge in the feedback capacitor C_{FA} is transferred to the integrating capacitor in the other path (in order to realize the inversion needed), that is, C_{FA} in parallel with C_{DA}. As such, the circuit implements a first-order high-pass filter. The transfer function realized is given as

$$H(z) = \frac{\dfrac{C_s}{C_F + C_D}\, z^{-1}}{1 + \dfrac{C_F}{C_F + C_D}\, z^{-2}} \tag{4.77}$$

Note that double-sampling here is achieved using only three phases of the clock. The center frequency is $f_s/4$ and is decided by the sampling frequency. The mid-band gain is unity. The authors have demonstrated that a 44 MHz center frequency band-pass filter with a bandwidth of 6.28 MHz using a clock frequency of 176 MHz could be realized with very low power consumption since only one opamp is used.

4.10 High-Frequency SC Ladder Filters

High-frequency SC filters were first realized by using the double-sampling principle by Choi and Brodersen [4.55]. Their proposed SC integrator is shown in Fig. 4.36a. This is achieved by putting two sampling capacitors C_1 with opposite clock phases in parallel as shown. The transfer function of this integrator is given by

$$V_o = \frac{C_1}{C_2}\left(\frac{1}{1 - z^{-1}}\right)\left(V_1\, z^{-1} - V_2\right) \tag{4.78a}$$

Note that the delay for the inverting and noninverting inputs is different.

The double-sampling integrator of Fig. 4.36a can be used to realize a biquad based on the doubly-terminated second-order low-pass ladder filter of Fig. 4.36b which works effectively at twice the sampling frequency as shown in Fig. 4.36c. Note that the left integrator realizes a transfer function given by

$$\frac{V_o}{V_i} = \frac{C_1\, z^{-1/2}}{C_1 + C_2\,(1 - z^{-1/2})} \tag{4.78b}$$

clearly showing that the sampling frequency is doubled. The same is true for the right integrator.

The design of high-frequency SC filters [4.56] involves lot of problems due to high clock rates and resulting stringent requirements on settling time of opamps. Most high-frequency applications also require large Qs (narrow bandwidths) leading to high sensitivity-to-capacitor ratios. Moreover, high-Q filters also need large capacitor ratios. N-path filters discussed in the previous section have the advantage that the center frequency is dependent only on the clock frequency. However, they suffer from clock feedthrough due to mismatch of the various paths which will degrade the dynamic range. Hence, there are some moderate Q applications, where conventional techniques will be useful.

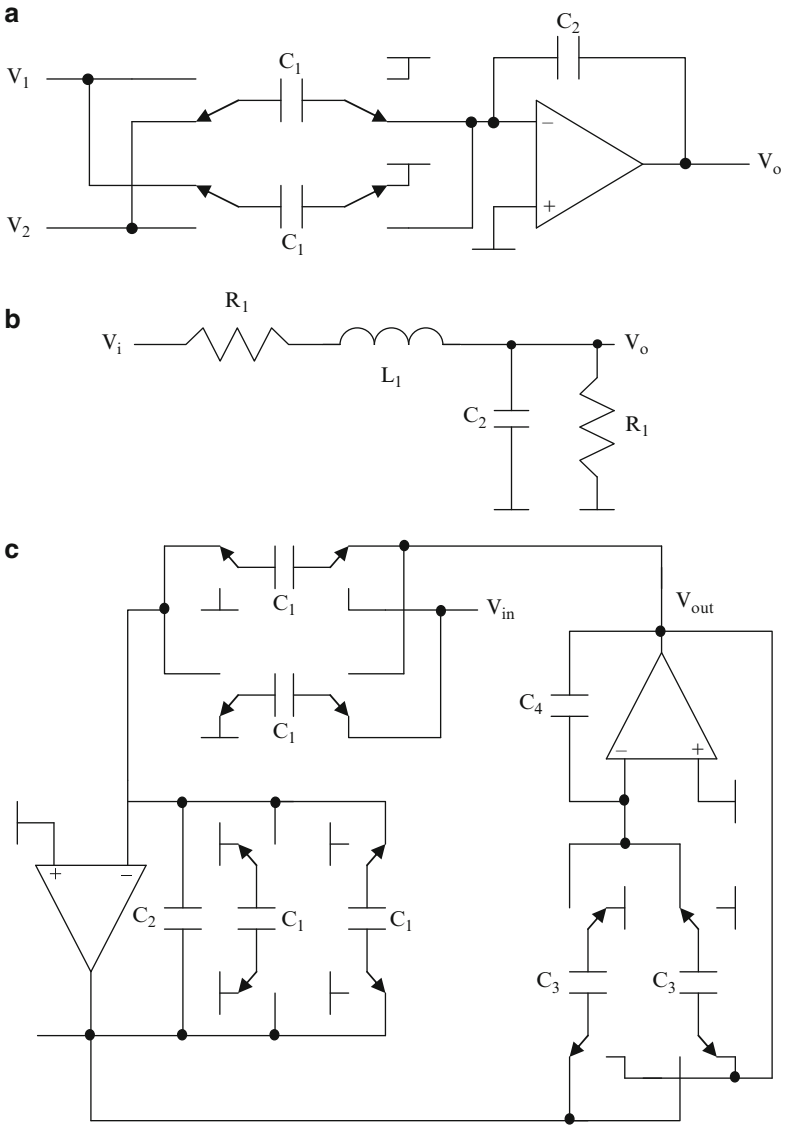


Fig. 4.36 (**a**) Double-sampled LDI type integrator, (**b**) doubly terminated RLC prototype second-order filter, and (**c**) a SC filter derived from (a) working in both phases ((a) and (c) Adapted from [4.55] © IEEE 1980)

The operating frequency of the SC filter is mainly limited by the settling time of the amplifier. However, the opamp gain still has to be large. At high clock frequencies, the capacitor charging time should be small, implying the use of large switches which in turn leads to high charge injection. The large feedthrough may degrade the

effective settling time. Fully differential circuits are recommended so that the power supply noise, which is a common mode signal, gets cancelled.

The sensitivity in high-Q band-pass filters has been analyzed in detail by Choi et al. [4.56]. They have suggested the use of coupled identical resonators for realizing narrow-band high-frequency filters. They have observed that at the pass-band edges, the sensitivity of the magnitude of the frequency response to integrating capacitors is Q times more than that to the coupling capacitors. Hence they have recommended the use of identical integrating capacitors so that good matching can be achieved. Thus, the center frequencies of individual resonators can be matched well. The time constants of the integrators can thus track together. Moreover, this can simplify the layout of the complete SC filter.

A sixth-order band-pass filter using identical resonators obtained from a third-order low-pass prototype of Fig. 4.37a by using LP to BP transformation is presented in Fig. 4.37b [4.57, 4.58]. Note that all the resonators have the same pole frequency ω_o. Note that the coupling branches are inversely proportional to Q. The resonators use two integrators in a negative feedback loop. All integrators have the same time constants. The dotted lines show the additional coupling paths needed in the case of elliptic low-pass filters of Fig. 4.37d derived from the prototype of Fig. 4.37c. Some of these paths feed into the integrator outputs using feedforward capacitors whereas those feeding into the inputs of the integrators are sampling capacitors.

In high-Q, high-frequency filters, the coupling between resonators can need large capacitor ratios. The coupling capacitors in such cases can be implemented using a T-network scheme [4.56]. As an illustration, the original integrator and integrator needing less capacitor ratio are presented in Fig. 4.38a, b. Thus, instead of a ratio of 100, a ratio of 10 will be sufficient. The gains of the amplifiers of Fig. 4.38a, b are, respectively, as follows:

$$\frac{V_o}{V_i} = -\frac{C_1}{C_2} \quad \text{and} \quad \frac{V_o}{V_i} = -\left(\frac{C_1}{C_2 + C_3 + C_4}\right)\left(\frac{C_4}{C_2}\right) \tag{4.79}$$

Typically, C_2:C_3:C_1:C_4 = 10:8:1:1 for realizing a gain of 0.01. Thus the maximum capacitor ratio is 10 instead of 100. The sensitivity to parasitics at the intermediate node can be reduced by proper layout. The T-network scheme, however, cannot be employed for the sampling capacitors and hence, alternative techniques that convert the paths using sampling capacitors to paths using feedforward capacitors have been suggested. These involve additional hardware by rerouting the signal paths as shown in Fig. 4.37b.

The high-Q filters tend to have a low dynamic range since the noise gets amplified by Q times in the resonators. As an illustration, the noise of the two-integrator-based resonator in a high-order ladder filter can be modeled through the use of two input-referred noise sources at the inputs of the integrators as shown in Fig. 4.39. A simple analysis shows that

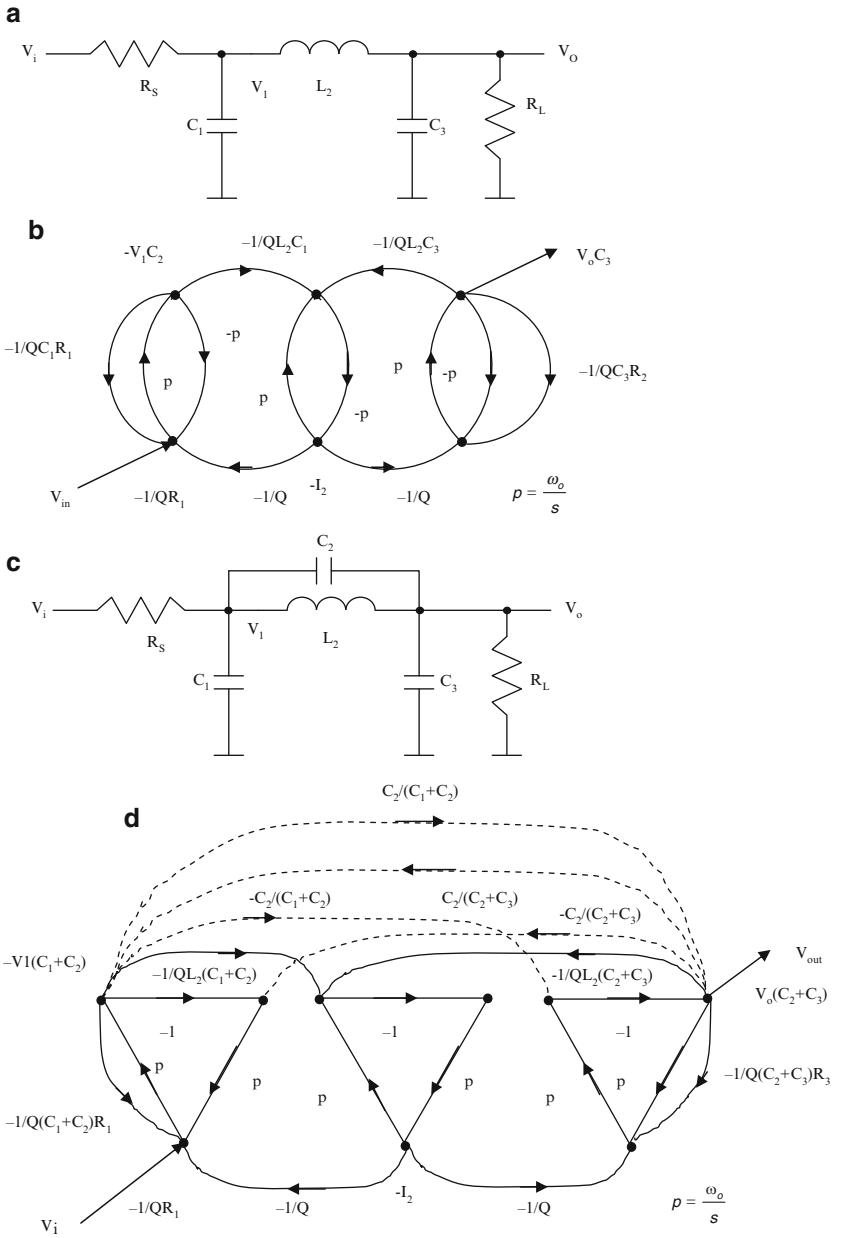


Fig. 4.37 (**a**), (**c**) Prototype all-pole and elliptic low-pass filters (**b**) and (**d**) operational simulation-based SFGs derived from (**a**) and (**c**) using LP to BP transformation (a,c Adapted from [4.56] © IEEE 1983)

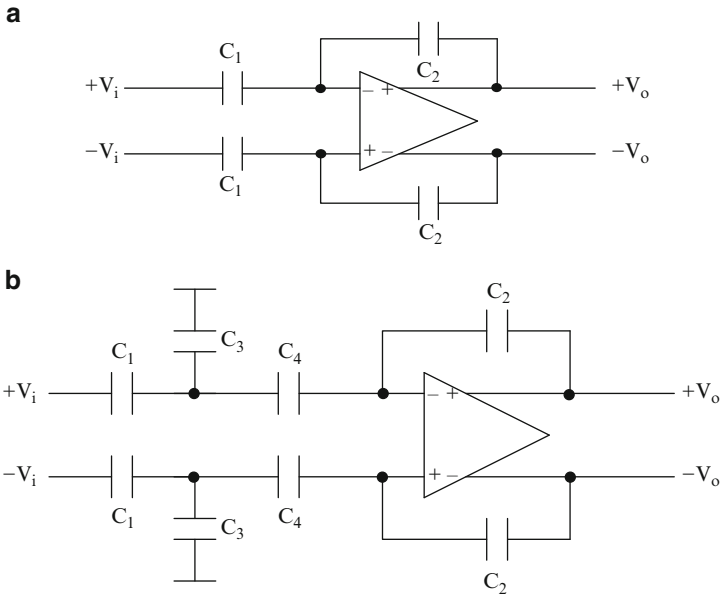


Fig. 4.38 (**a**) Direct realization of coupling gain of 0.01, (**b**) realization using a T-network with reduced capacitor spread (Adapted from [4.56] © IEEE 1983)

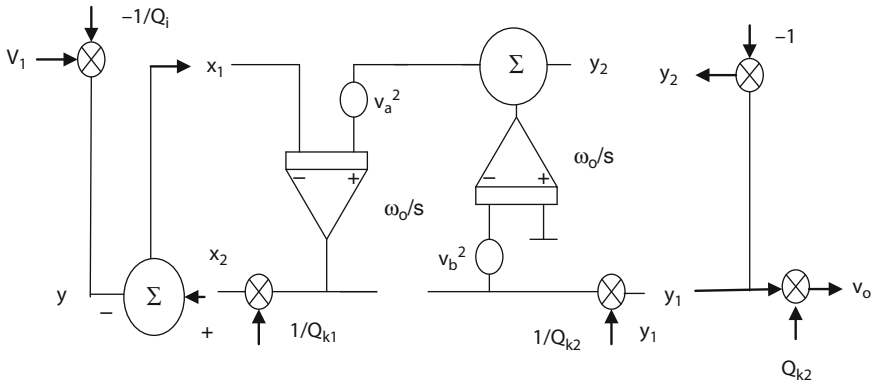


Fig. 4.39 Schematic of the two-integrator loop including noise sources and source and load termination realization (Adapted from [4.57] © IEEE 1986)

$$x_1 = y_2 + v_{ak} + \left(\frac{\omega_k}{j\omega}\right) v_{bk} - \frac{j\omega\, Q_{k2}}{\omega_k}\left(1 - \frac{\omega_k^2}{\omega^2}\right) y_1 \tag{4.80a}$$

At frequencies near resonance (i.e., ω_k), the v_{bk} and v_{ak} terms will be equal in (4.82a) and thus both can be combined as a single source v_{nj} with an amplitude

$\sqrt{2}\,v_{aj}$ or $\sqrt{2}\,v_{bj}$. For a singly terminated filter (i.e., a resonator cascaded by a load resistance), the output can be derived as

$$v_o = \frac{v_i - Q\,v_{n1}}{1 + \dfrac{j\omega Q}{\omega_o}\left(1 - \dfrac{\omega_o^2}{\omega^2}\right)} = v_i - Q\,v_{n1} \quad \text{at} \quad \omega = \omega_o \tag{4.80b}$$

Thus, the combined noise source is amplified by Q.

Song and Gray [4.57] present an interesting discussion on the effect of LP-to-BP transformation. Note that while using LP to band-pass transformation, the unity gain frequency ω_{co} of the integrators in low-pass filters is transformed to ω_o which is defined as $Q = \omega_o/2\omega_{co}$ and thus ω_o is Q times higher than of the integrators in the low-pass filter. Hence if the same size integrating capacitors are used in the desired band-pass filters, the integrator resistor needs to be Q times smaller. The advantage is that the noise power density is reduced Q times. The noise is amplified by the two-integrator loop by Q^2 as shown earlier, the overall noise will be $Q^2/Q = Q$ and the dynamic range of the band-pass filter reduced by $\sqrt{Q}$. The effect of LP band-pass transformation is summarized in Table. 4.1.

We next present some general observations on the design of high-frequency SC filters. The pole-frequency of a SC integrator is given by

$$f_o = \frac{1}{2\pi R_{equ}\,C_I} = \frac{f_c\,C_s}{2\pi\,C_I} \tag{4.81a}$$

where C_s is the switched capacitor that realizes an equivalent resistance R_{equ} and f_c is the sampling frequency. As the frequency of operation of SC filters increases, C_s shall be small for fast charging. Hence, C_I must be small. Small values of C_I lead to higher noise as can be seen from the following expression;

$$v_{noise} = \sqrt{\frac{4kT\left(2 + L_2^2\,C_1^2\right)}{2\pi}}\sqrt{\frac{Q}{C_I}} \tag{4.81b}$$

thereby decreasing the dynamic range. Hence the integrating capacitor must be large to decrease the noise level of the filter. The settling time constant of the two-integrator loop can be derived as

$$\tau = \frac{(C_I + C_s)}{C_I}\,\frac{\gamma C_L}{g_m} \tag{4.82a}$$

where g_m is the transconductance of the opamp differential pair and C_L is the load capacitance. Typically γ is between 2 and 4 for CMOS opamps. The wide bandwidth for the opamps used in the SC filter needs smaller capacitances which lead to large noise. The switches are large devices to reduce their on resistance but the feedthrough effect will be more.

The settling time of a SC integrator is typically given as

$$\tau_{\text{settle}} < \frac{\delta}{f_c} \tag{4.82b}$$

where δ is less than 1 but close to 1. The settling time of the opamp should be 10 times the settling time of the integrator as a rule of thumb, which means from (4.82a, 4.82b) that

$$g_m > \frac{10(C_I + C_s)}{C_I} \frac{\gamma f_c C_L}{\delta} \tag{4.83a}$$

Assuming that the clock frequency f_c is four times higher than f_o, the bias current can be estimated from (4.83a) as

$$I > \frac{800\,(C_I + C_s)^2}{C_I^2} \frac{\gamma^2 f_o^2 C_L^2}{\delta^2 \mu C_{ox} (W/L)} \tag{4.83b}$$

It can be noted from (4.83b) that the power consumption is quadrupled as the center frequency is doubled. Only a small C_L will reduce power consumption. The increase of W/L will not help much since large devices add their own parasitic capacitance to C_L.

4.11 SC FIR Filters

Several architectures have been described in the literature for realizing FIR filters [4.59, 4.60, 4.61, 4.62, 4.63, 4.64, 4.65, 4.66, 4.67, 4.68, 4.69, 4.70]. Reddy and Swamy [4.59] described the use of a SC FIR filter (see Fig. 4.40) for which the input samples b_i were output bits of a delta modulator. Hence, these bits, stored in an analog shift register (SR), effectively form a delay line. The SC network weighs these bits based on the tap weights realized using the capacitors C_0, C_1, and so on, and sums them in real-time using the opamp and feedback capacitor C_f. The capacitor C_d together with C_f realizes a lossy SC integrator so that a low-pass filtering function is also carried out. The lossy integrator is offset-compensated using the additional switches and capacitor C_{o2}, by storing the offset in the even phase and employing it in the odd phase as explained later.

Reddy and Swamy [4.60] have also described the application of the real-time summation capability of SC networks to realize a discrete Fourier transformer. This follows the straightforward approach for the realization of FIR filters by having a tapped delay line and weighing the taps by the desired coefficients and summing the weighted samples. Each of the DFT points of a sequence $x_o, x_1, x_2, x_3, \ldots, x_{n-1}$ may be expressed as the outputs of band-pass filters with a FIR transfer function given by

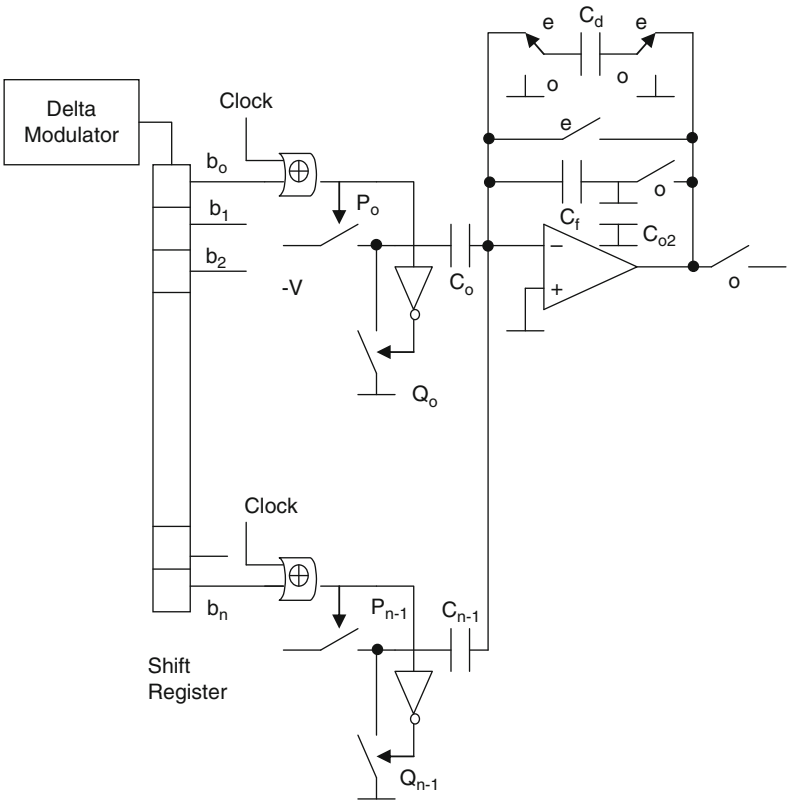


Fig. 4.40 SC FIR filter realization to work on the output of Delta modulator (Adapted from [4.59] © IEEE 1983)

$$H_k(z) = \sum_{n=0}^{N-1} \exp\left(-j\frac{2\pi}{N}nk\right) z^{-n} = \frac{1 - z^{-N}}{1 - z^{-1}\exp\left(-j\frac{2\pi}{N}nk\right)} \tag{4.84}$$

Each $H_k(z)$ can be expressed as transversal filter realization and the coefficients of the transversal filters can be made real by combining (taking sum or difference) of $H_k(z)$ and $H_{n-k}(z)$. An example four-point DFT implementation is shown in Fig. 4.41a and its SC implementation is presented in Fig. 4.41b.

Interestingly, in SC filters, once a delay line is available, the weighting and summation can be performed in one clock cycle using a switched-capacitor-based summer needing just one opamp as has been seen in the case of Fig. 4.40b. The stray-insensitive delay of Enomoto et al. [4.61] using a three-phase clock can be used to realize the complete FIR filter. The tapped outputs of the delay line are simultaneously converted into charges by different feedforward SC branches and summed using separate opamps to obtain the various DFT outputs.

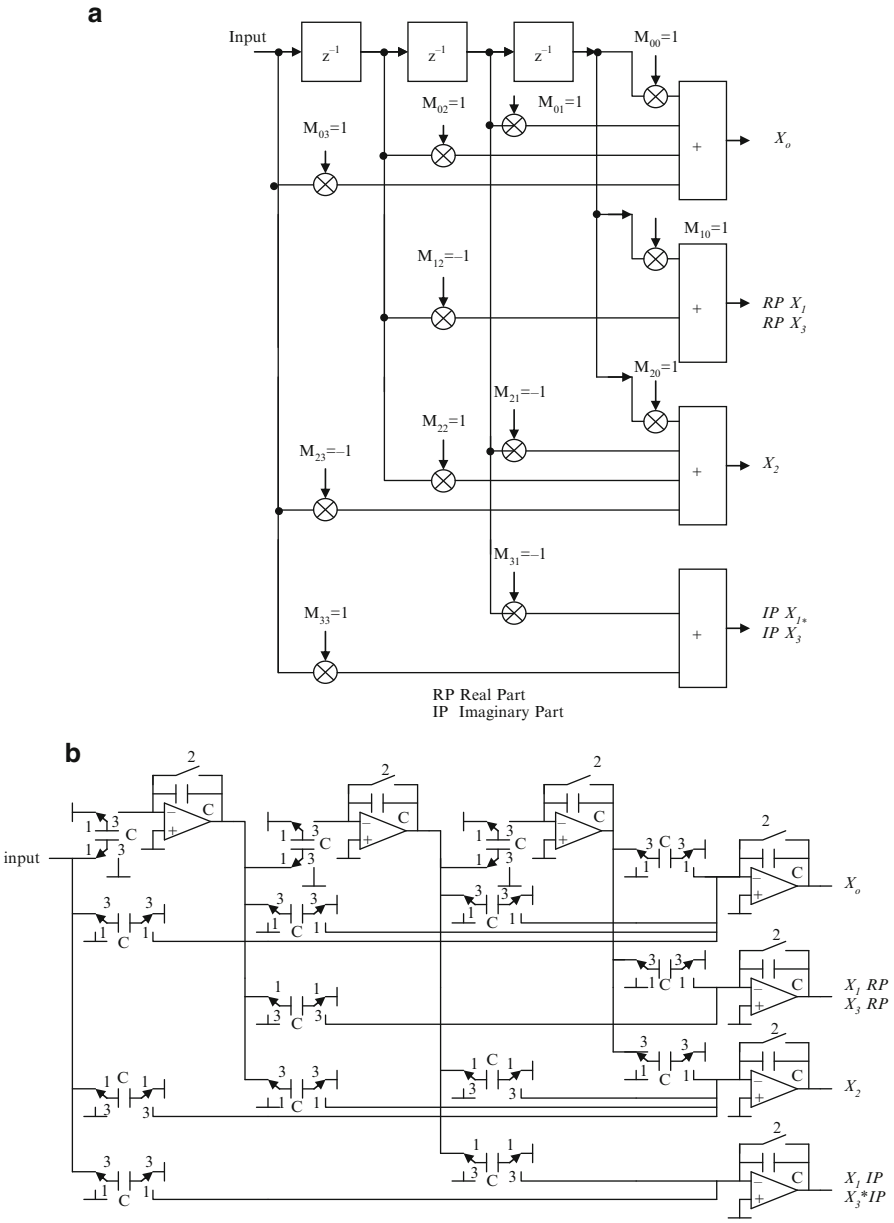


Fig. 4.41 (**a**) Architecture of four-point DFT computation using frequency sampling approach, and (**b**) SC implementation of (a) (Adapted from [4.60] © IEEE 1983)

One of the disadvantages of the above technique of using a tapped delay line comprising several unit delay stages is that the errors in delay stages due to the offsets of opamps will add up due to the transfer through the analog delay line. On the other

hand, if a parallel approach is taken, these cumulative errors can be avoided. Lee and Martin suggested such an approach to realize multiple FIR filters on a single chip [4.63].

Fischer [4.64] has suggested, the use of N-path filter architectures using circulating delay-type shift register described earlier in Sect. 4.9.3.3 in connection with N-path filters, for realizing FIR filters using one opamp. A three-stage stray-insensitive delay line is presented in Fig. 4.42a which needs a four-phase clock as shown in Fig. 4.42b. In Phase 1, the input is acquired on capacitor C_o and in Phase 4, the acquired charge is transferred to capacitor C_4. In phase 4, the capacitor C_1 is discharged, since it contains old sample which will no longer be needed.

Next in the following Phase 1, the charge on capacitor C_2 is transferred to C_1 (implying that C_2 is discharged). Next, in Phase 2, the charge on capacitor C_3 is transferred to C_2 (implying that C_3 is discharged). Finally, in Phase 3, the charge on capacitor C_4 is transferred to C_3 (implying that C_4 is discharged). The opamp facilitates the charger transfer during these phases. The output voltages in various phases taking into account the finite opamp gain can be derived as

$$V_{o4} = z^{-3/4}\, V_{in1}\, \frac{C_0}{C_4}\left(1 - \frac{1}{A_o}\left(1 + \frac{C_0}{C_4} - z^{-1}\,\frac{C_4}{C_3}\right)\right) \tag{4.85a}$$

$$V_{o3} = z^{-6/4}\, V_{in1}\, \frac{C_0}{C_3}\left(1 - \frac{1}{A_o}\left(1 + \frac{C_0}{C_4} + \frac{C_4}{C_3} - z^{-1}\left(\frac{C_4}{C_3} + \frac{C_3}{C_2}\right)\right)\right) \tag{4.85b}$$

$$V_{o2} = z^{-9/4}\, V_{in1}\, \frac{C_0}{C_2} \times \left(1 - \frac{1}{A_o}\left(1 + \frac{C_0}{C_4} + \frac{C_4}{C_3} + \frac{C_3}{C_2} - z^{-1}\left(\frac{C_4}{C_3} + \frac{C_3}{C_2} + \frac{C_2}{C_1}\right)\right)\right) \tag{4.85c}$$

$$V_{o1} = z^{-12/4}\, V_{in1}\, \frac{C_0}{C_1} \times \left(1 - \frac{1}{A_o}\left(1 + \frac{C_0}{C_4} + \frac{C_4}{C_3} + \frac{C_3}{C_2} + \frac{C_2}{C_1} - z^{-1}\left(\frac{C_4}{C_3} + \frac{C_3}{C_2} + \frac{C_2}{C_1}\right)\right)\right) \tag{4.85d}$$

Note that the delays are fractional delays of a clock cycle which can be made integers by appropriate delay in the summing amplifier realizing the FIR filtering operation. Note that the circuit of Fig. 4.44a can be offset-compensated using the arrangement of Fig. 4.42c. The reader is urged to verify this. Evidently, the opamp is connected as a buffer in Phase 1 in order to sample the offset voltage of the opamp. For this reason, there is a reduction in the number of active phases of the clock unlike in the circuit of Fig. 4.42a where V_{out1} is also available.

A FIR filter can be realized as shown in Fig. 4.42d by tapping the outputs in various phases and charging capacitors C_{2i} with these outputs. Then, all these capacitors are discharged during Phase 1 to capacitor C_{26}. The ideal z-domain transfer function can be obtained as

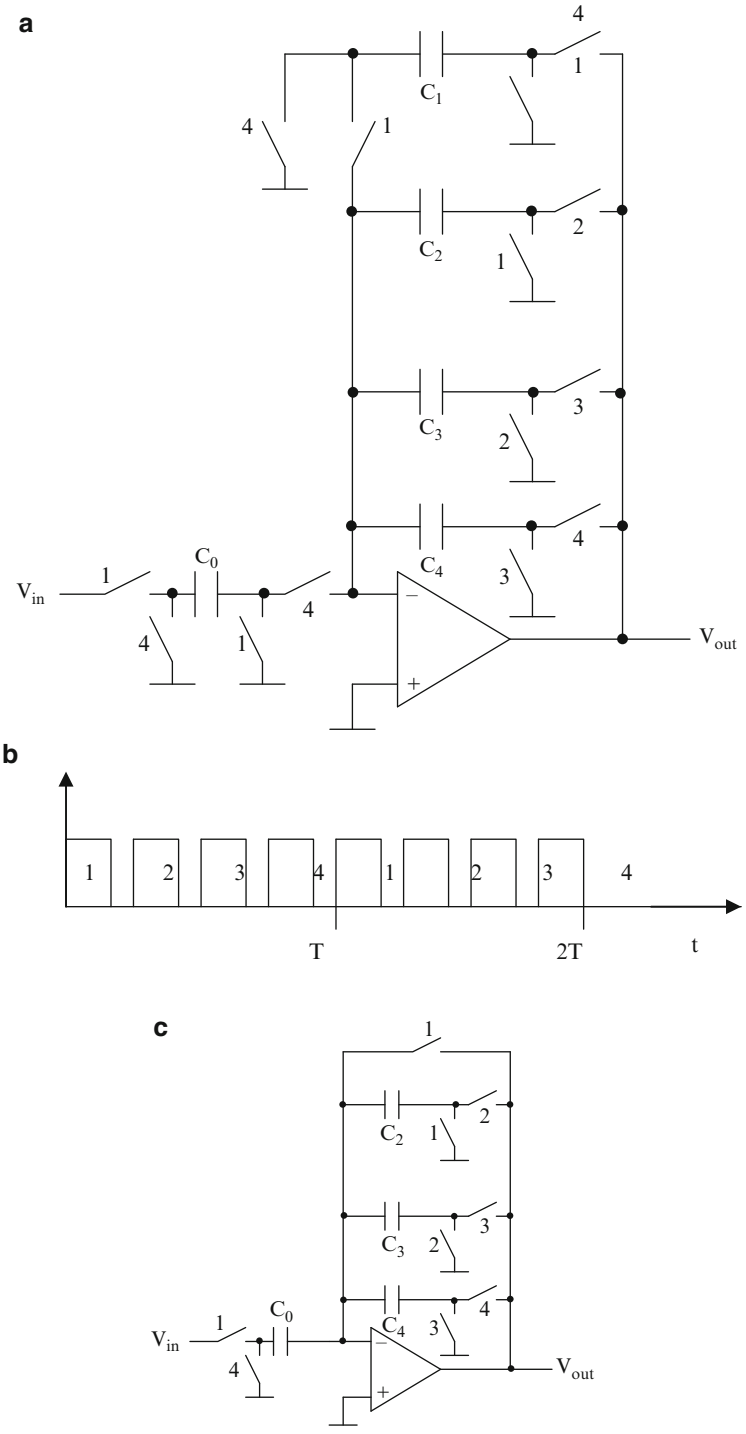


Fig. 4.42 (**a**) Stray-insensitive SC delay line using single opamp, (**b**) timing waveforms, (**c**) offset-compensated three-stage delay line, (**d**) complete sixth-order SC filter based on (a), and (**e**) alternative cascade realization of sixth-order FIR filter (Adapted from [4.64] © IEEE 1990)

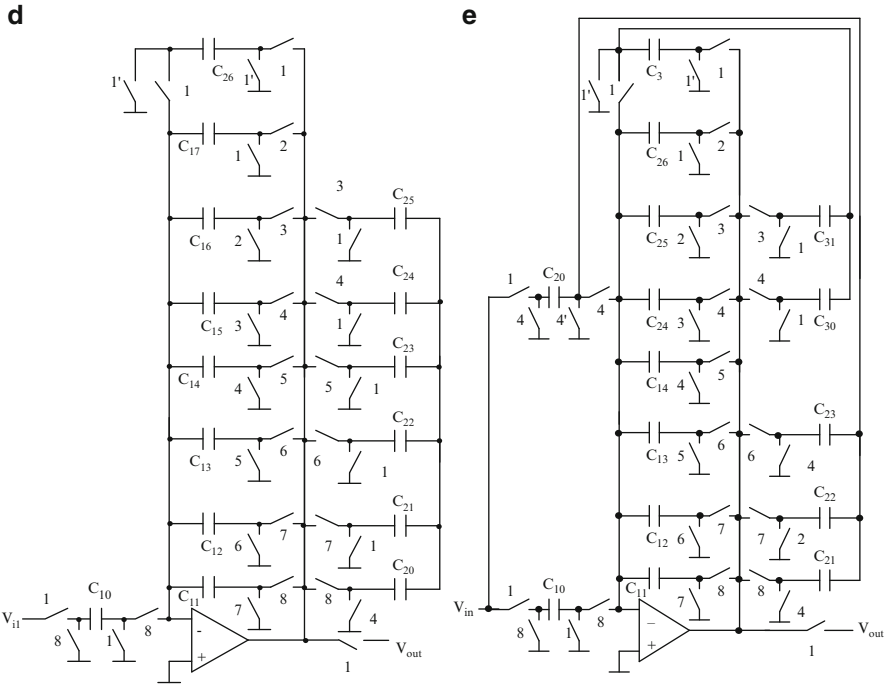


Fig. 4.42 (continued)

$$H_o(z) = z^1\ V_{in1}\ \frac{C_{10}}{C_{26}}\left(\frac{C_{20}}{C_{11}} + \frac{C_{21}}{C_{12}}\,z^{-1} + \frac{C_{22}}{C_{13}}\,z^{-2} + \frac{C_{23}}{C_{14}}\,z^{-3} + \frac{C_{24}}{C_{15}}\,z^{-4} + \frac{C_{25}}{C_{16}}\,z^{-5} + z^{-6}\right) \tag{4.86}$$

Thus the seven coefficients of the FIR filter are determined by $C_{26}, C_{25}, \ldots, C_{20}$ and the remaining capacitors are for scaling purposes only. However, they need to be equal for maximum signal swing.

Fischer [4.64] has also pointed out that cascading two stages also is feasible using a single opamp. This has the advantage that the resulting cascade of two FIR filters may have low sensitivity to coefficient errors. A sixth-order filter realization using a cascade of fourth- and second-order FIR filters is presented in Fig. 4.42e for completeness. Note that the two capacitors C_{14} and C_{26} can have arbitrary values. The two transfer functions realized are, respectively,

$$H_1(z) = z^{-3/8}\ \frac{C_{10}}{C_{24}}\left(\frac{C_{20}}{C_{10}} + \frac{C_{21}}{C_{11}}\,z^{-1} + \frac{C_{22}}{C_{12}}\,z^{-2} + \frac{C_{23}}{C_{13}}\,z^{-3} + z^{-4}\right) \tag{4.87a}$$

$$H_o(z) = z^{-5/8}\ \frac{C_{24}}{C_{32}}\left(\frac{C_{30}}{C_{24}} + \frac{C_{31}}{C_{25}}\,z^{-1} + z^{-2}\right) \tag{4.87b}$$

Thus, the coefficients of the first fourth-order FIR filter are determined by C_{24}, C_{23}, ...,C_{20} only and the remaining capacitors are for scaling purposes only. Similarly, by choosing $C_{24} = C_{25}$, the coefficients of the second-order FIR filter are determined by C_{32}, C_{31}, and C_{30} only and the remaining capacitors are for scaling purposes only. However, for maximum signal swing, $C_{14} = C_{10}$ and $C_{26} = C_{24}$ are recommended.

A half-delay circuit can be implemented [4.69] using the circuit of Fig. 4.43a. Note that the capacitor C_1 is charged by the input voltage in Phase 1 and this capacitor is connected across the feedback path of the opamp in the Phase 2. During Phase 2, another capacitor C_2 is charged with the input voltage and this capacitor is put across the feedback path of the opamp in Phase 1. Thus, effectively a half clock cycle delay is realized. Note, however, that during the interval between Phases 1 and 2, the opamp feedback loop is open. Note also that there is no need for any matching of capacitors.

A stray-insensitive delay has been described by Enomoto et al. [4.61] which uses a three-phase clock. In this circuit, shown in Fig. 4.43b, the capacitor C_1 is charged to the input voltage in Phase 1. Its charge is transferred to the feedback capacitor in Phase 3. In Phase 2, the memory of the capacitor is destroyed by discharging the feedback capacitor. In Phase 1, the output is sampled by the next stage thus effectively realizing a delay.

Another stray-insensitive delay using a two-phase clock [4.70] is presented in Fig. 4.43c. In this circuit, in Phase 1, the capacitor C_{1i} is charged to the input voltage and the charge acquired is transferred to capacitor C_{1a} in Phase 2. In the next Phase 1, the charge on capacitor C_{1a} is transfered to the input capacitor C_{2i} of the next stage. Note that XY feedback needs to be used to stabilize the circuit during the interval between Phases 1 and 2.

4.12 Compensation of Finite Gain and Offset Voltage of SC Integrators and Amplifiers

4.12.1 Offset and Finite Gain Compensation in Integrators

At the outset, it may be noted that the effect of opamp input-referred offset voltage as well input-referred noise can be analyzed in one step since both of these have the same transfer functions to the output of the circuit. On the other hand, the finite gain of the opamp can be modeled by an input voltage of $-V_{oe}/A$ and $-V_{oo}/A$ at the inverting input terminal of the opamp. Thus, by considering effective input voltage at the opamp input as $V_{offe} + V_{ne} - \frac{V_{oe}}{A}$ in the even phase and similarly $V_{offo} + V_{no} - \frac{V_{oo}}{A}$ in the odd phase, the transfer function can be derived easily. The basic principle of reduction of the effects of opamp offset voltage or noise or finite gain is to sample these during the actual operation of the circuit in one phase and subtract them from the ones occurring in the other phase. It is expected that the noise, offset voltage, and finite gain error are correlated during the sampling and subtraction phases.

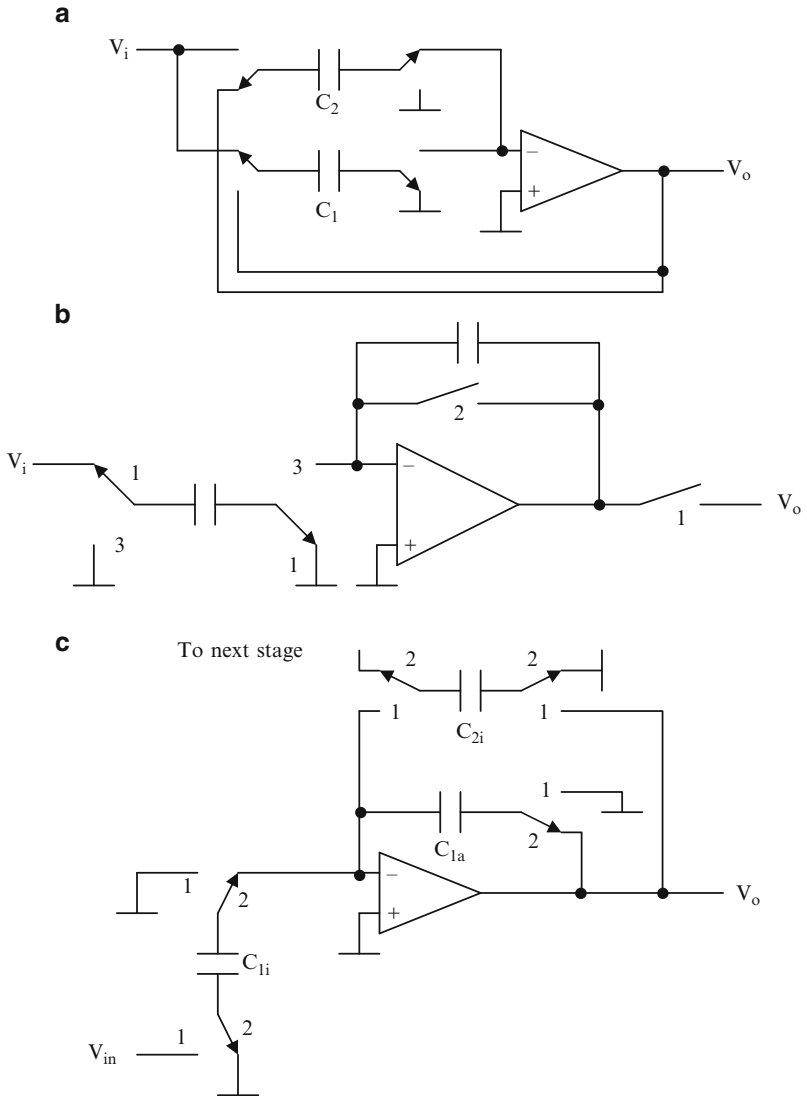


Fig. 4.43 (**a**) Stray-insensitive SC half-delay circuit due to Nagaraj, (**b**) SC delay circuit using three-phase clock due to Enomoto, Ishihara, and Yasumoto, and (**c**) SC delay circuit using two-phase clock due to Gillingham ((a) Adapted from [4.69] © IEE 1984, (b) Adapted from [4.61] © IEE 1982, (c) Adapted from [4.70] © IEE 1982)

The first offset compensation scheme for a lossy integrator was suggested by Fan and Gregorian [4.71, 4.72]. This circuit is presented in Fig. 4.44a. The transfer function of this circuit in the φ_2 phase is given as

$$V_{oo} = \frac{V_{ie}\,\alpha_3\,z^{-1/2} + \left(V_{offo} - V_{offe}\,z^{-1/2}\right)\left(\alpha_3 + \alpha_1 + 1\right) + \frac{C\,z^{-1/2}}{C+C_o}\left(V_{offe} - V_{offo}\,z^{-1/2}\right)}{\left(\alpha_1 + (1 - z^{-1}) + \frac{\alpha_3 + \alpha_1 + 1 - \frac{C z^{-1}}{C+C_o}}{A}\right)} \tag{4.88}$$

In the even phase, the output of the amp is equal to the offset voltage since the opamp is connected as a buffer. The integrator function is achieved by storing the output on capacitor C_o which acts as a memory. The loss is realized by discharging the capacitor $\alpha_1 C$ in the even phase. Considering that the offset voltages in the even and odd phases V_{offe} and V_{offo} are correlated, the effect of the offset voltage of the opamp is eliminated in the output V_{oo}. On the other hand, the finite gain effect is still present as seen from the term in the denominator. The dc gain can be seen from (4.88) to be $\dfrac{\alpha_3}{\alpha_1 + \frac{\alpha_3 + \alpha_1 + 1 - \frac{C}{C+C_o}}{A}}$.

In the case of a lossless integrator (i.e., $\alpha_1 = 0$), the dc gain is $\dfrac{A}{\alpha_3 + \alpha_1 + \frac{C_o}{C+C_o}}$.

The circuit has the disadvantage that the transitions at the output of the opamp from signal level to ground restrict the speed of operation of the circuit.

Another offset compensation scheme for an integrator due to Haug et al. [4.73] is shown in Fig. 4.44b. Note that in φ_2, the capacitors C_1 and C_2 act as an integrator realizing the transfer function

$$V_{oo} = \frac{-V_{io}\,C_1 + V_{offo}\,(C_2 + C_1\,(1 - z^{-1})) - V_{offe}\,C_1\,z^{-1/2}}{C_2\,(1 - z^{-1})} \tag{4.89a}$$

under the condition $C_3 = C_1$. It may be noted that the output in the even phase is close to the output in the odd phase. Thus, the opamp need not slew to ground voltage and quickly adapts to the output signal. The dc gain of the integrator due to the finite opamp gain A can be derived as $(A^2 + 2A)$ which evidently is larger than that for the circuit of Fig. 4.44a. The output in Phase 1 is

$$V_{oo} = \frac{-V_{io}\,z^{-1/2}\,C_1}{C_2\,(1 - z^{-1})} - 2\,V_{offo} \tag{4.89b}$$

Another circuit for compensating the offset of the opamp [4.74] is shown in Fig. 4.44c. In this circuit, the input is fed forward using capacitors C_3 and associated switches. Note that the condition $C_1 = C_3$ and $C_2 = C_4$ will be required. The input needs to be held over a clock period such that $V_{ie} = V_{io}z^{-1/2}$. The output in the even phase is close to the output in the odd phase. The dc gain of this compensated integrator is given by $\frac{A^2\,C_2}{C_1 + C_2} + \frac{A(2C_1 + C_2)}{C_1 + C_2}$ which is less than that of the circuit of Fig. 4.44b. The output in Phase 1 is

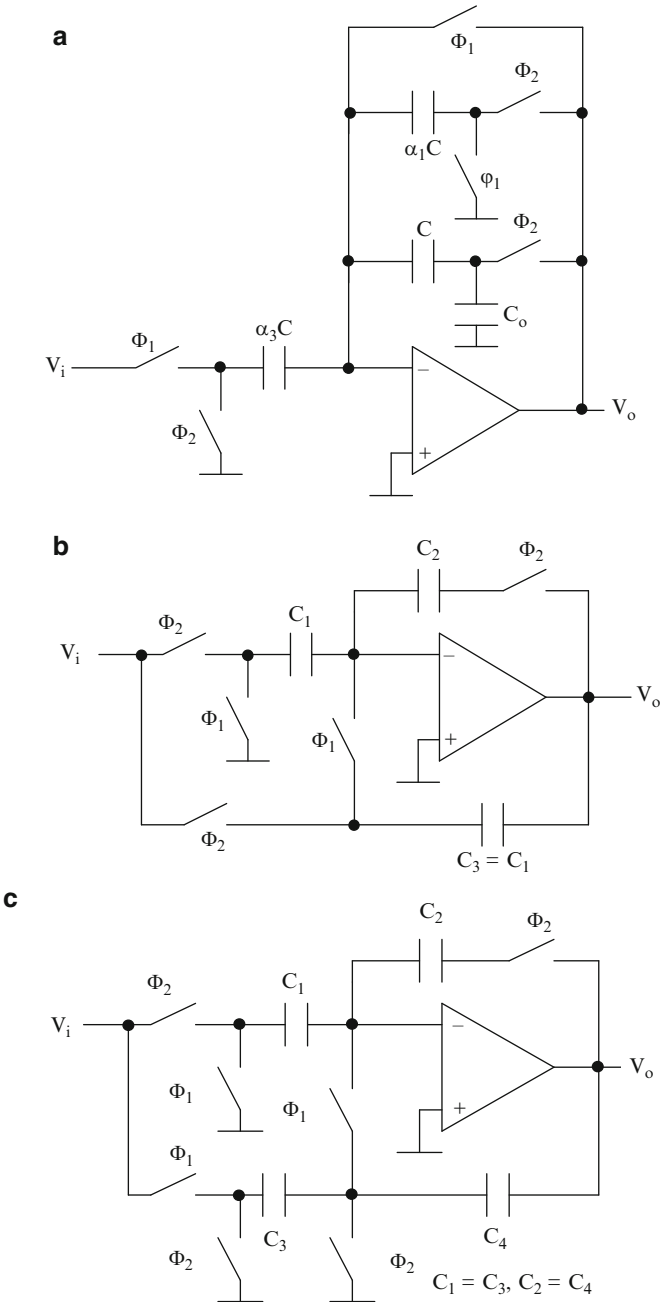


Fig. 4.44 SC integrators with offset and gain compensation due to (**a**) Gregorian, (**b**) Haug, Temes, and Martin, (**c**) Enz and Temes, (**d**) Lam and Copeland, and (**e**) Nagaraj ((a) Adapted from [4.72] © Elsevier1980, (c) Adapted from [4.74] © IEEE 1996, (d) Adapted from [4.75] © IEE 1983 and (e) Adapted from [4.76] © IEEE 1987)

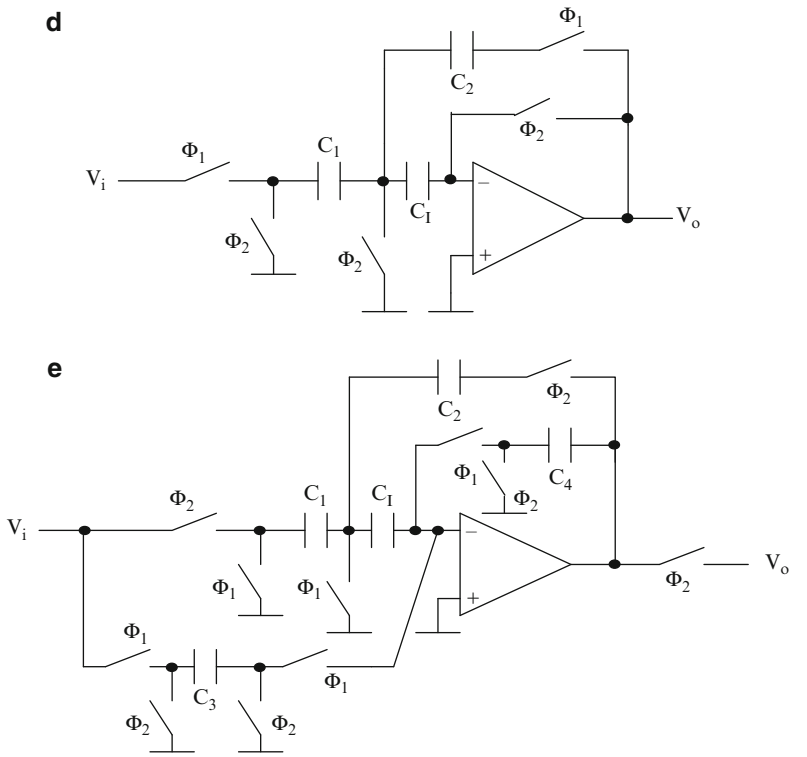


Fig. 4.44 (continued)

$$V_{oo} = \frac{-V_{io}\, z^{-1/2}\, C_1}{C_2\,(1 - z^{-1})} - V_{off}\left(\frac{C_1 + 2C_2}{C_2}\right) \tag{4.89c}$$

An interesting technique has been suggested by Lam and Copeland [4.75] which is presented in Fig. 4.44d. This uses an auxiliary memory capacitor C_I. In Phase 1, the output can be shown to be given by

$$V_{ie}\, C_1 + V_{oe}\, C_2\,(1 - z^{-1}) = \left(V_{offe} - V_{offo}\, z^{-1/2} - \frac{V_{oe}}{A}\right) \times \left(C_1 + C_2\,(1 - z^{-1})\right) \tag{4.90}$$

Note that the offset compensation is achieved whereas finite gain is not compensated. The dc gain of the integrator is A. On the other hand, in the φ_2 phase, the output slews to V_{off}. This circuit, however, has led to numerous other circuits for finite gain and offset compensation using the concept of having a memory capacitor.

Nagaraj [4.76] has suggested the circuit shown in Fig. 4.44e for opamp finite gain compensation. In this circuit, in Phase 1, the capacitors C_3, C_4 form an integrator. The error due to the finite gain of the opamp is stored on C_I. In Phase 2, the capacitors C_1 and C_2 function as an integrator and the stored error on C_I is used to cancel the error that would otherwise have occurred. The output in Phase 2 is given as

$$V_{oo} = \frac{\left(V_{offo} - V_{offe}\ z^{-1/2}\right)\left(C_1 + C_2\left(1 - z^{-1}\right)\right) - V_{io}\ C_1}{C_2\left(1 - z^{-1}\right)} \tag{4.91a}$$

under the condition $C_3 = C_1$ and $C_4 = C_2$ and the condition $V_{ie} = V_{io}z^{-1/2}$. The output in Phase 2 is offset-free. The dc gain can be shown to be the same as that of Fig. 4.44c. The output in phase 1 in the ideal case $A = \infty$ is

$$V_{oe} = \frac{-V_{io}\ z^{-1/2}\ C_1}{C_2\left(1 - z^{-1}\right)} - \frac{V_{ie}\ C_1}{C_2} + \frac{V_{offe}\left(C_1 + C_2 + C_I\left(1 - z^{-1}\right)\right)}{C_2} \tag{4.91b}$$

4.12.2 Compensation of Opamp Offset and Finite Gain in SC Amplifiers

Gregorian [4.71] has described a technique for compensation of the offset voltage of the opamp in SC amplifiers as shown in Fig. 4.45a. In Phase 1 (even phase), the opamp is connected as a buffer thus making the offset voltage of the opamp appear at its output terminals and charging the capacitors C_2 and C_1 to the offset voltage. At the same time, the input voltage is sampled. In Phase 2, the capacitors C_1 and C_2 perform the amplification operation. However, the already sampled offset voltage in Phase 1 will effectively be subtracted from the offset voltage of the opamp in Phase 2 (odd phase). Note that the offset voltages in both Phases 1 and 2 are correlated and hence are likely to be almost the same. This operation is known as "correlated double sampling" (CDS). The transfer function of the amplifier can be derived as

$$V_{oo} = \frac{C_1\ z^{-1/2}\ V_{ie} + (C_1 + C_2)(V_{offo} - V_{offe}\ z^{-1/2})}{C_2 + \frac{C_1 + C_2}{A}} \tag{4.92}$$

It is thus seen that the finite gain of the opamp still is not compensated but the offset is totally eliminated since V_{offe} and V_{offo} will not change during adjacent clock periods. The disadvantage of the circuit is that in one phase of the clock the opamp output needs to return to ground thus limiting the speed of operation. The opamp shall have a high slew rate and fast settling time.

Haug et al. [4.74] have suggested another offset compensation circuit that also compensates gain. This circuit, shown in Fig. 4.45b, has the same subcircuit comprising C_1 and C_2 and associated switches as in Fig. 4.45a whereas the rest of the circuit is different. The advantage is that the opamp output voltage will be approximately the same in both phases.

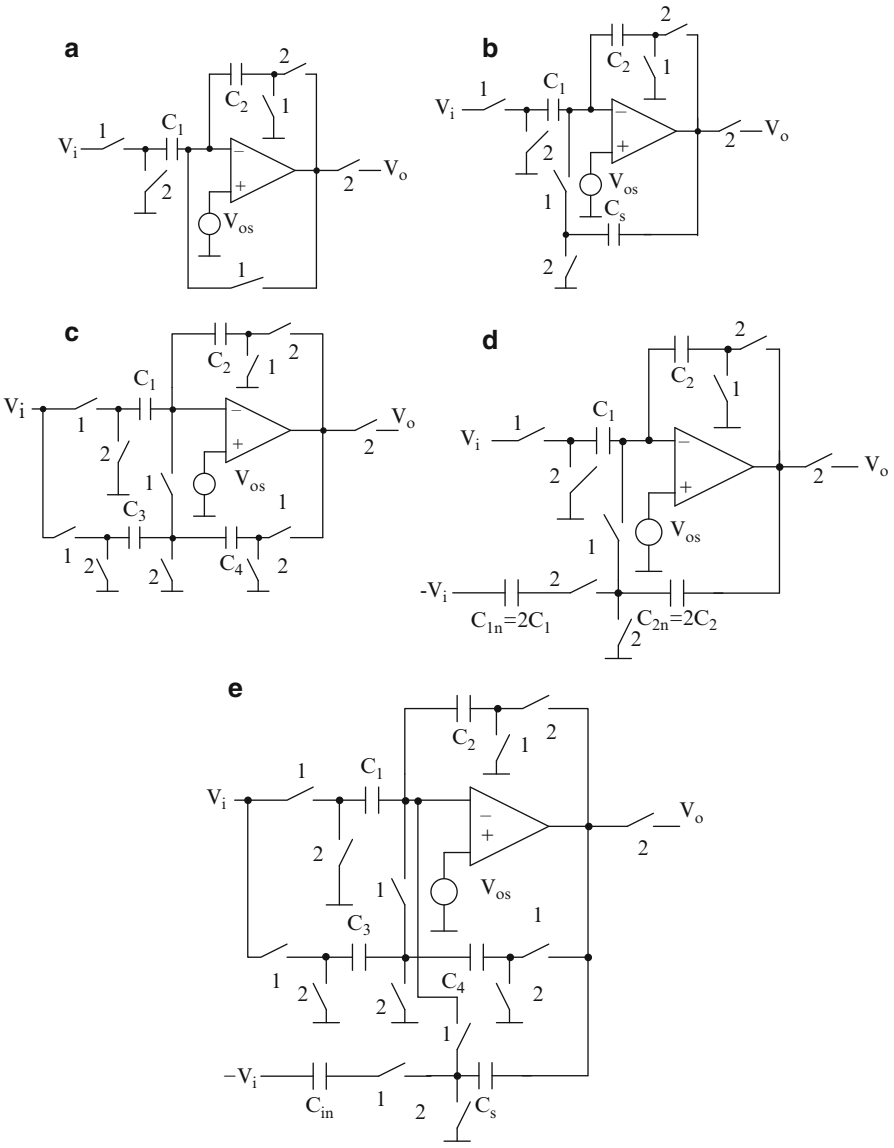


Fig. 4.45 SC amplifiers with offset and gain compensation due to (**a**) Gregorian, (**b**) Haug, Temes, and Martin, (**c**) Larson, Martin, and Temes, (**d**) Yoshizawa and Temes, and (**e**) generalized circuit obtained from (b) to (d) ((a)-(d) Adapted from [4.72] © Elsevier 1980, Adapted from [4.73] © IEEE 1984, Adapted from [4.79] © IEEE 1987, Adapted from [4.80] © IEEE 2007)

Larson et al. [4.79] have described a wideband gain and offset compensated SC amplifier architecture shown in Fig. 4.45c. Although the subcircuit comprising C_1 and C_2 and associated switches is the same in this case as in Fig. 4.45a, the rest of

the circuit is different. In this case, the input is also fed forward using capacitor C_3 and feedback exists through C_4.

Yoshizawa and Temes [4.80] have recently described another wide-band gain compensated amplifier presented in Fig. 4.45d which is an extension of Fig. 4.49b. In this case, the input is also fed forward using capacitor C_{1n} and this circuit needs a negative input voltage $-V_{in}$ which may be available in differential-mode circuits.

The circuits of Fig. 4.45b–d can be unified into one circuit for the purposes of analysis as shown in Fig. 4.45e. Note that in all the cases

$$V_{oo}\ C_2 - V_{ie}\ C_1\ z^{-1/2} + (C_1 + C_2)(V_{offe}\ z^{-1/2} - V_{offo}) = 0$$

holds and thus the offset voltage is compensated. The transfer function of the circuit of Fig. 4.45e can be obtained as

$$V_{oo} = \frac{V_{ie}\ z^{-1/2}\,\alpha - V_{offe}\,\beta}{D} \tag{4.93a}$$

where

$$\alpha = \left(\begin{array}{l} \left(\dfrac{C_1 + C_2}{A}\right)\left(C_1 + C_3 - C_{in}\left(1 - z^{-1}\right)\right) - C_1\left(C_4 + C_s\right) \\ -\dfrac{C_1\left(C_1 + C_2 + C_3 + C_4 + C_s + C_{in}\left(1 - z^{-1}\right)\right.}{A} \end{array} \right) \tag{4.93b}$$

$$\beta = \left(\frac{C_1 + C_2}{A}\right) z^{-1/2}\left(C_3 + C_4 + C_s + C_{in}\left(1 - z^{-1}\right)\right) \tag{4.93c}$$

and

$$\begin{aligned} D = &- C_2\left(C_4 + C_s\right) \\ &- \frac{(C_1 + C_2)(C_4 + C_s) + C_2\left(C_1 + C_2 + C_3 + C_4 + C_s + C_{in}\left(1 - z^{-1}\right)\right)}{A} \\ &+ \frac{(C_1 + C_2)^2\ z^{-1} - (C_1 + C_2)(C_1 + C_2 + C_3 + C_4 + C_s + C_{in}\left(1 - z^{-1}\right))}{A^2} \\ &+ \frac{(C_s + C_2)(C_1 + C_2)\, z^{-1}}{A} \end{aligned} \tag{4.93d}$$

It can be easily verified that using an infinite gain opamp (i.e., with $A = \infty$), the gain of the amplifiers of Fig. 4.45b–e is C_1/C_2. Note from (4.93) that the output V_{oo} has a filtered V_{offe}/A component which is much less due to the factor $1/A$. For the

circuits of Fig. 4.45b, d, the dc gain is the same since C_{in} does not come into the picture for dc gain evaluation. The dc gain is independent of A to a first-order:

$$A_{dc} = \frac{\frac{C_1}{C_2}\left(1+\frac{1}{A}\right)}{1+\frac{1}{A}+\frac{(C_1+C_2)}{C_2\,A^2}} \tag{4.94a}$$

Evidently, the dc gain is compensated and the offset voltage is attenuated. In the case of the Larson et al. [4.79] circuit of Fig. 4.45c (under the condition $C_s = C_{in} = 0$, $C_3 = C_1$ and $C_4 = C_2$), the dc gain can be seen to be

$$A_{dc} = \frac{\frac{C_1}{C_2}}{1+\frac{1}{A}\left(2+\frac{2C_1}{C_2}\right)+\frac{1}{A^2}\left(\frac{C_1+C_2}{C_2}\right)^2} \tag{4.94b}$$

In this case also, the gain is not compensated whereas the offset is attenuated by A.

Nagaraj et al. [4.76] described another wide-band finite gain compensation scheme as shown in Fig. 4.46a. Note that as before in the case of SC integrators of Fig. 4.45d, e, a memory capacitor C_H is added to store the offset voltage in one phase and use it in another phase for offset compensation. This circuit needs a sampled and held input. The symmetry of the upper and lower SC circuits excluding C_H and the switch S_A can be noted. A modification of the circuit due to Yoshizawa and Temes [4.80] which uses a different compensation circuit in the lower branches is shown in Fig. 4.46b. The transfer function of both these circuits can be obtained in a unified way as

$$V_{oo} = \frac{N}{D} \tag{4.95a}$$

where

$$\begin{aligned} N = &\left(-V_{io}\,C_1+\left(V_{offo}-V_{offe}\,z^{-1/2}\right)(C_1+C_2)\right)\left(C_4+C_s+\frac{m}{A}\right) \\ &+z^{-1/2}\left(\frac{C_1+C_2}{A}\right)\left(V_{offe}\,m-V_{ie}\,(C_3-C_{in}\,(1-z^{-1}))\right) \end{aligned} \tag{4.95b}$$

and

$$D = \left(C_4+C_s+\frac{m}{A}\right)\left(C_2+\frac{C_1+C_2}{A}\right)-\frac{C_s\,(C_1+C_2)\,z^{-1}}{A} \tag{4.95c}$$

$$m = (C_H+C_{in})(1-z^{-1})+C_3+C_4+C_s \tag{4.95d}$$

Both circuits of Fig. 4.46a, b are not affected by the offset of the opamp. The dc gain of V_{oo}/V_{io} under the condition $A = \infty$, can be seen to be $-C_1/C_2$. On the other hand, the dc gains of both circuits are, respectively, as follows.

$$V_{oo} = \frac{-V_{io}\,\frac{C_1}{C_2}\left(1+\frac{2(C_1+C_2)}{C_2\,A}\right)}{1+\frac{2(C_1+C_2)}{C_2\,A}+\frac{(C_1+C_2)^2}{C_2^2\,A^2}} \tag{4.96a}$$

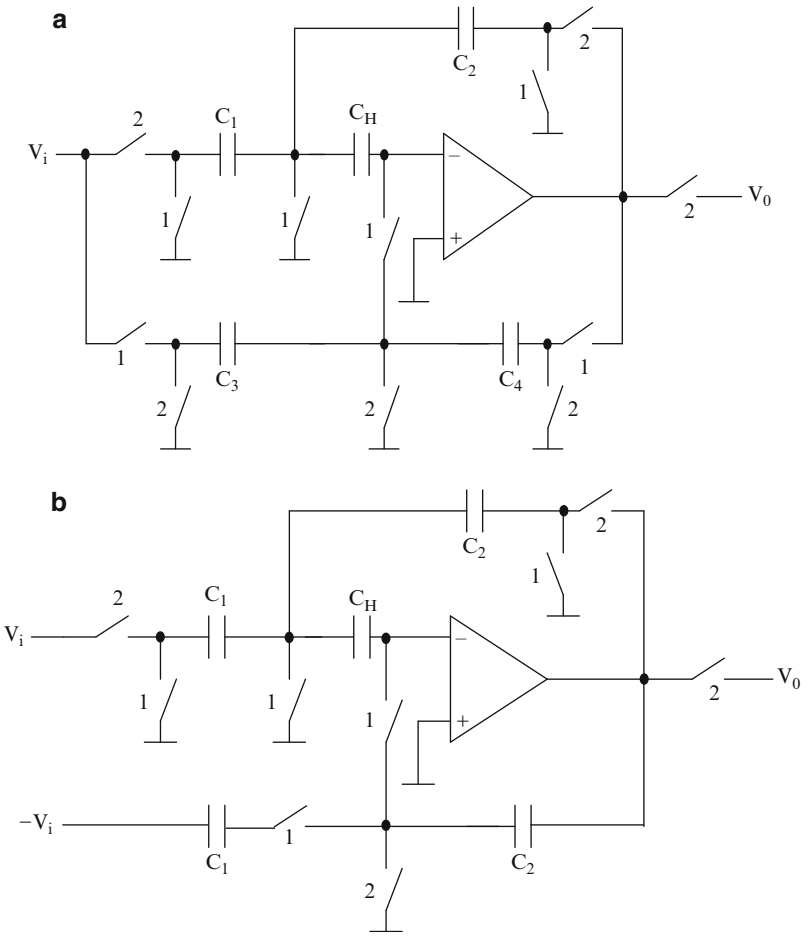


Fig. 4.46 SC amplifiers with offset and gain compensation due to (**a**) Nagaraj et al. [4.76] and (**b**) Yoshizawa and Temes [4.80] ((a) Adapted from [4.76] © IEEE 1987 and (b) Adapted from [4.80] © IEEE 2007)

$$V_{oo} = \frac{-V_{ie}\,\frac{C_1}{C_2}\left(1+\frac{1}{A}\right)}{1+\frac{1}{A}+\frac{(C_1+C_2)}{C_2 A^2}} \tag{4.96b}$$

4.13 Distortion in SC Filters

SC filters have several nonidealities associated with switches, capacitors, and opamps [4.81, 4.82, 4.83].

The capacitors used in SC filters have nonlinear voltage dependence which can be described as

$$C(V_c) = C_o\,(1 + a_1\,V_c + a_2\,V_c^2 + ...) \tag{4.97}$$

where V_c is the voltage across the capacitor, C_o is the nominal value of the capacitance at the quiescent voltage, and a_1 and a_2 are the linear and quadratic coefficients, respectively. The second and third harmonic distortions arising since of this nonlinearity can be expressed in terms of the input peak voltage V_{ip} and output voltage V_{op} as

$$HD_2 = \frac{a_1}{2}\sqrt{V_o^2 + \left(\frac{V_i}{2}\right)^2}, \quad \omega_o T_c \ll 1 \tag{4.98a}$$

$$HD_3 = \frac{a_2}{4}\left(V_o^2 + \frac{V_i^2}{3}\right), \quad \omega_o T_c \ll 1 \tag{4.98b}$$

where V_i, ω_o are the amplitude and radian frequency of the input signal and T_c is the period of the sampling clock.

The second-order distortion is proportional to the output voltage whereas the third-order distortion is proportional to the square of the output voltage. Note that by using fully differential structures, it is possible to cancel to the second harmonic distortion. The following discussion assumes the use of fully differential amplifiers.

The other nonlinearity is since of the amplifier open-loop gain nonlinearity. The nonlinearity of the amplifier open-loop gain can be expressed as

$$V_o = a_1 V_1 + a_2 V_1^2 + a_3 V_1^3 + ...) \tag{4.99a}$$

where V_1 and V_o are the amplitudes of the input and output voltages of the opamp, and a_1 and a_2 are the linear and quadratic coefficients. The resulting second-order and third-order harmonic distortion are:

$$HD_2 = \frac{a_2}{2\,a_1^3\,\beta}\,V_o\sqrt{1 + \left(\frac{V_o}{2\,V_t}\right)^2}, \ \omega_o T_c \ll 1 \tag{4.99b}$$

$$HD_3 = \frac{a_3}{4\,a_1^4\,\beta}\,V_o^2\left(1 + \frac{V_o}{3\,V_1}\right), \ \omega_o T_c \ll 1 \tag{4.99c}$$

where $\beta = \frac{C_2}{C_1 + C_2}$ is the feedback factor of the integrator.

Distortion also can be caused by the slew rate of the amplifiers. This is illustrated in Fig. 4.47. The ideal staircase type of waveform in the output stage, waveform with exponential rise, and slew-limited waveforms are shown in Fig. 4.47a–c, respectively. The errors between (b) and (a) and (c) and (a) are shown in Fig. 4.47d, e, respectively. When a capacitor with an initial voltage larger than $\sqrt{2}$ $(V_{GS} - V_{TH})$ where $(V_{GS} - V_{TH})$ is the bias voltage of the input transistors is suddenly switched across the amplifier input, the amplifier output is slew-rate limited; that is, the output is no longer proportional to the input. Thus, the output

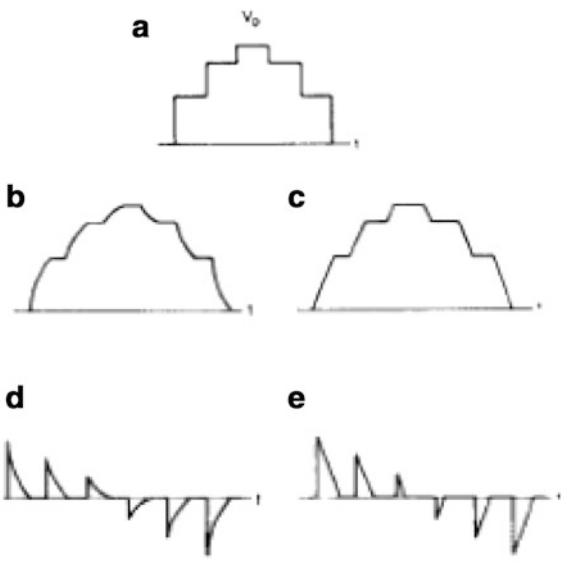


Fig. 4.47 (**a**) Ideal waveform with zero rise time, (**b**) waveform with exponential rise time, (**c**) slew-limited waveform, (**d**) linear error, (**e**) slew-limited error (Adapted from [4.81] © IEEE 1985)

of the amplifier after the end of linear settling time following a slewing time has some "memory" of slewing itself. This causes nonlinearity on the envelope of the signal. The resulting kth harmonic distortion is given by

$$HD_k = \frac{8\left(\sin\left(\frac{\omega_o T_c}{2}\right)\right)^2}{\pi k(k^2-4)}\left(\frac{V_o}{S_r\ T_c}\right)\quad k = 1,3,5,7,\ldots \tag{4.100}$$

where S_r is the slew rate of the opamp. This distortion is caused only by the last opamp unlike those discussed earlier. It can be reduced by increasing the ratio between input signal overdrive and the peak of the sine wave signal since slewing time is shorter. Furthermore, having a large bandwidth for the opamp helps since the opamp can settle quickly and has less memory of slewing.

The ON-resistance of the switches also introduces nonlinearity. This leads to incomplete charging of the switched-capacitors. The ON-resistance can be represented as

$$\mathrm{R_{ON}}(V_r) = \mathrm{R_{ONo}}\left(1 + \ \rho_1 V_r + \ \rho_2 V_r^2 + \ldots\right) \tag{4.101}$$

where R_{ONo} is the nominal value of the switch resistance at the quiescent voltage, V_r is the common source-drain voltage of the switch, and ρ_1 and ρ_2 are the linear and quadratic coefficients, respectively.

We next consider the signal-dependent charge injection of the switches. Using the optimum four-phase clock, this can be reduced. Typical two-phase and four-phase clocking waveforms used in a SC circuit of Fig. 4.48a are shown in Fig. 4.48b. These waveforms can be considered to have five distinct time slots as

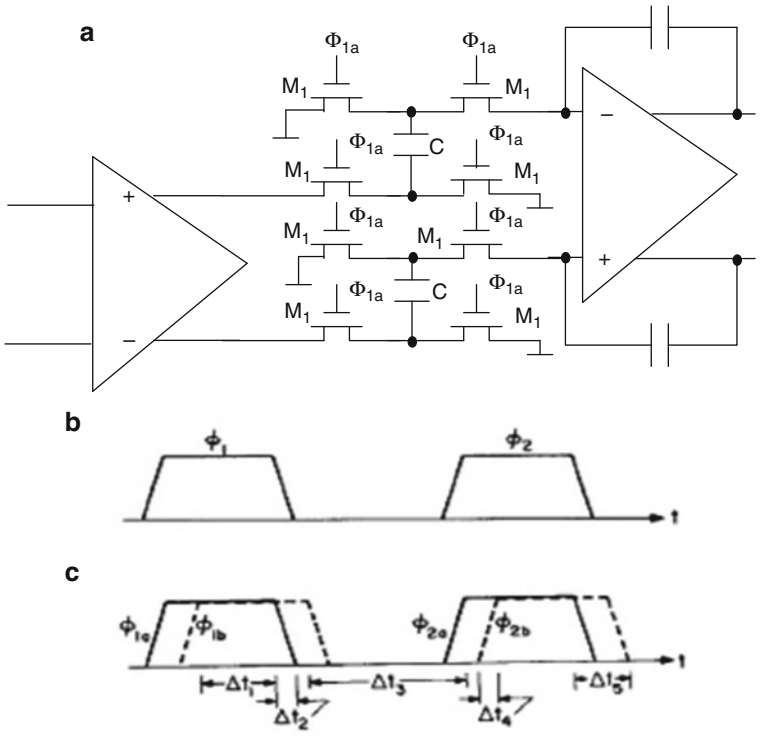


Fig. 4.48 (**a**) A fully differential SC integrator, (**b**) conventional two-phase clock, and (**c**) a four-phase clock to reduce charge injection (Adapted from [4.81] © IEEE 1985)

shown. In time slot Δ_{t2}, differential error is introduced when the ON resistances of M_2 and M_2' are not equal. This error can be minimized by using complementary switches so that the resistance variation with drain-source voltage is small.

4.14 Low-Voltage SC Filter Design Techniques

Low-voltage circuits may have reliability problems [4.84]. The CMOS circuit failure is due to device breakdown which could be for the following reasons: (a) oxide breakdown, (b) gate-induced drain leakage, (c) hot-electron effects, and (d) punch-through. CMOS technology is designed in such a way that all the degradations occur at the same stress level.

Instantaneous and time-dependent gate-oxide breakdowns limit the maximum gate-source and gate-drain potential differences that can be applied to a transistor. Similarly, gate-induced drain leakage (GIDL) tunneling current limits the voltage across the oxide. Furthermore, when the device is on, hot-electron effects can damage the device and degrade the performance over time, limiting the V_{gs} and V_{ds}

that can be applied. Finally, punch-through limits the magnitude of V_{ds} when the device is off. If these critical terminal voltages V_{ds}, V_{gs}, and V_{gd} are kept within the rated operating voltage V_{dd} of the technology, the device reliability can be assured. It may be noted that the above voltages are relative to each other and not to ground. Thus, absolute V_g referenced to ground may exceed the rated V_{dd} if $V_{gs} < V_{dd}$ is maintained. Care must be taken to see that the source to substrate and drain to substrate junctions do not exceed reverse breakdown voltages. These breakdown voltages are typically larger than the supply voltage since the substrate is doped much less than source and drain diffusions.

A critical problem in designing low-voltage SC circuits is the difficulty of implementing switches. As a result, at low power supply voltages, the power dissipation in fact increases. This can be seen from the following analysis [4.84]. The power dissipation of a SC circuit can be written as

$$P \propto IV_{dd} \tag{4.102a}$$

Next, the bias current of the OTA is given as

$$I \propto g_m\left(V_{gs} - V_T\right) \tag{4.102b}$$

The bandwidth of the OTA evidently is given as

$$\frac{g_m}{C} \propto f_s \tag{4.102c}$$

where C is the load capacitance and f_s is the sampling frequency. Noting that the dynamic range is the ratio of the signal swing (a fraction of $V_{dd} = \alpha V_{dd}$) squared over the sampled thermal noise as

$$DR \propto \frac{(\alpha V_{dd})^2}{(kT/C)} \tag{4.102d}$$

combining the above relationships we have

$$P \propto kTDRf_s\left(\frac{V_{gs} - V_t}{\alpha^2\ V_{dd}}\right) \tag{4.102e}$$

Evidently, as V_{dd} decreases, power dissipation increases. It is thus important to use circuits that maximize the available signal swing α.

Several approaches have been suggested for the design of low-voltage SC filters. These are (a) the use of low threshold voltage devices, (b) *switched-opamp* technique, (c) use of on-chip clock multipliers, (d) use of local switch bootstrapping, and (e) using unity gain reset opamps. The use of low threshold devices [4.85] is a high-cost technology. Moreover, the leakage current increases and causes charge loss thereby leading to harmonic distortion [4.86]. We consider hence the other techniques next.

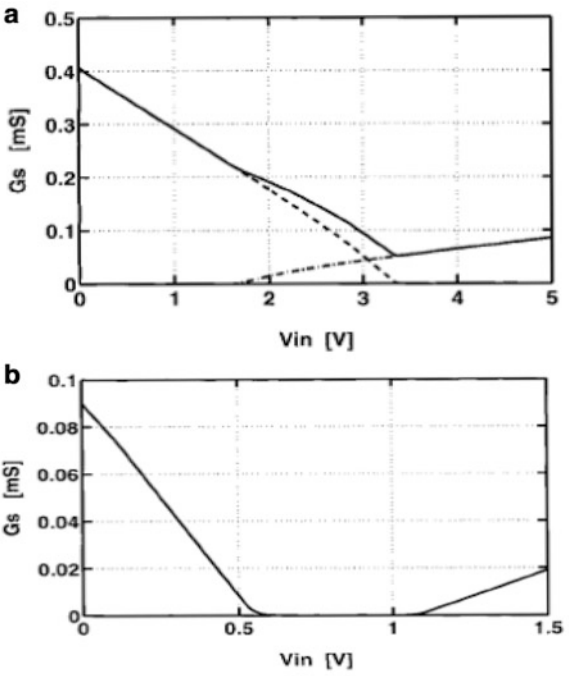


Fig. 4.49 Conductance of minimal size complementary switch (**a**) for $V_{DD} = 5$ V, and (**b**) for $V_{DD} = 1.5$ V (Adapted from [4.88] © IEEE 1997)

4.14.1 Switched-Opamp Technique-Based SC Filters

A technique that has received considerable attention for designing low-voltage SC filters is the switched-opamp technique [4.87, 4.88]. At low voltages, the telescopic cascode type of opamp may not be attractive due to the low swing that is available. Hence two-stage Miller-compensated opamps will be the best solution. As supply voltage decreases, the overdrive voltage of the CMOS switches will decrease and hence the switches will turn off. This is illustrated in Fig. 4.49a, b for a supply voltage of 5 V and for a supply voltage of 1 V. For a supply voltage of 5 V, the switch will have a minimum resistance of g_{dsmin}. On the other hand, for a supply voltage of 1 V, a critical region around $V_{DD}/2$ exists when both transistors are OFF. Hence any switch connected to the output of the opamp does not operate properly. A possible way to ensure that switch S_1 operates properly is to bias the opamp output close to ground or close to the positive supply but the swing will be less (see Fig. 4.49b).

In the switched-opamp technique, the switch following the opamp in conventional SC integrators (see Fig. 4.50a) is eliminated by having an opamp that can be switched ON or OFF. In the conventional inverting integrator of Fig. 4.50a, switches S_2, S_3, and S_4 have their source nodes always connected to reference voltage V_{REF} or virtual ground. The virtual ground also is kept on V_{REF} by the feedback system. Hence the maximum V_{DD} needed is $V_{DSsat} + V_{Tn} + V_{REF}$ where $V_{REF} = V_{DSsat,n} + (V_{swing}/2)$. On the other hand, the switch S_1 needs to handle an input signal coming

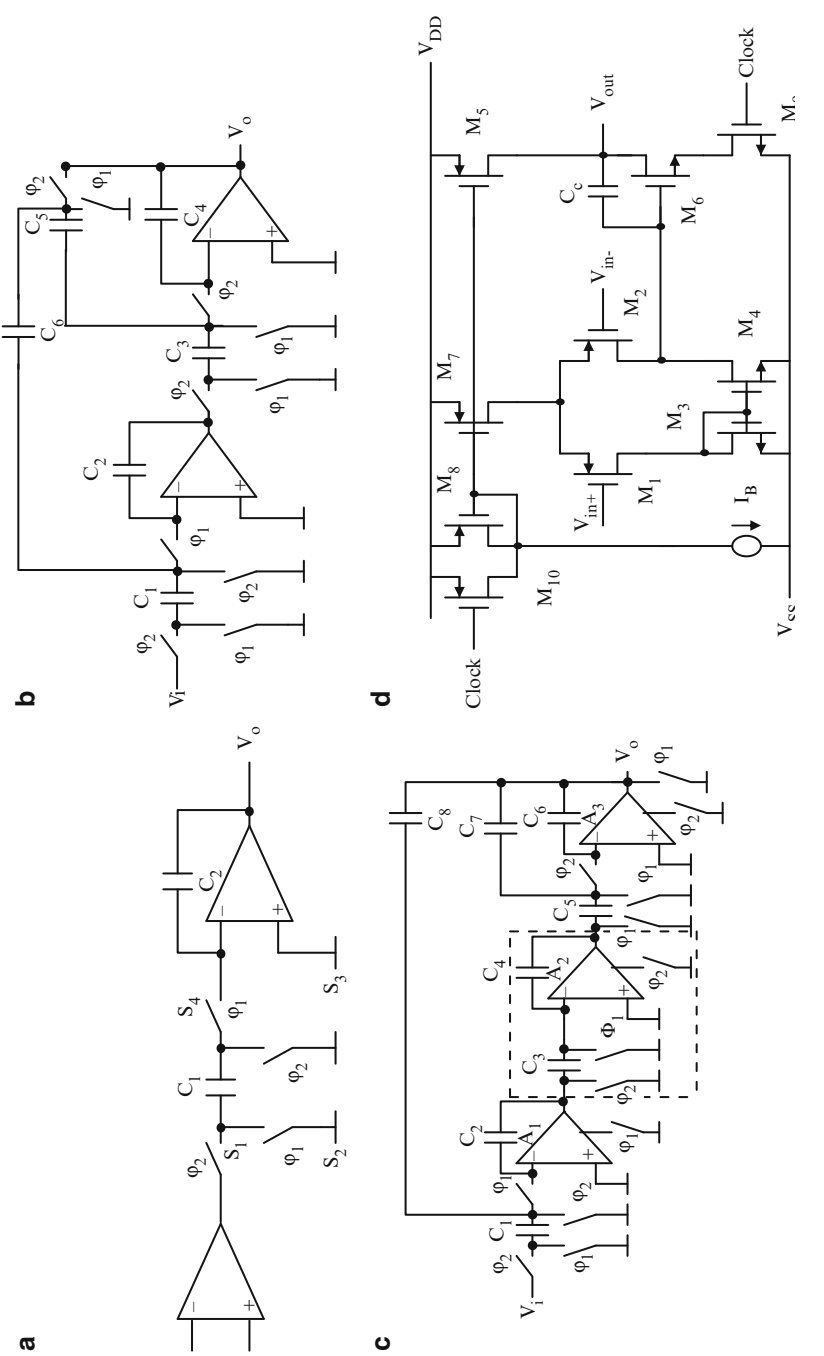


Fig. 4.50 (**a**) Conventional SC integrator in a SC biquad, (**b**) SC biquad, (**c**) modified switched opamp-based SC biquad, and (**d**) a CMOS switched opamp realization (Adapted from [4.87] © IEEE 1994)

from the output of a preceding opamp. Hence the minimum power supply needed is $V_{DSsat} + V_{Tn} + V_{DSsat,n} + V_{swing}$. Note that eliminating this switch is not possible since otherwise the transistor S_3 short-circuits the output of the opamp to ground. However, it is possible to switch OFF or switch ON the output stage of the opamp. This stipulates a restriction that the opamp has to drive and integrate in the same phase (when it is ON). Thus, modification of the basic SC circuits of Fig. 4.50b will be needed. The resulting circuit is shown in Fig. 4.50c which needs three opamps. An extra noninverting half delay is realized using opamp A_2. The switched opamp-based integrator is shown in dotted lines in Fig. 4.50c.

A typical switched opamp is shown in Fig. 4.50d which is the conventional two-stage CMOS opamp with frequency compensation. The additional transistors M_{10} and M_9 realize the switched opamp function by switching off the current mirror function realized by transistors M_5–M_7 as well as the transistor M_6. The PMOS switch M_{10} operates with any input voltage larger than $V_{Tp} + V_{DSsat}$ since its source is connected to the power supply. A clock "high" state causes M_{10} to be OFF and the current mirror will act in the normal manner. A "low" clock state turns M_{10} ON and disables the current source transistors. The opamp is switched OFF. For fast switching ON, the transistor M_8 needs to be large and has a width equaling the sum of the widths of all the devices it drives. The additional transistor M_9 is required to interrupt the current path through M_6 so that the capacitor C_c is not discharged. The size of M_9 is such that the voltage across it during the ON state of the opamp is quite low. Furthermore, its presence should not degenerate the gain of the opamp. Note also that the clocks used to control M_9 and M_{10} should be synchronized.

The switched opamp technique introduces extra active elements (one per integrator, except at the input), thus increasing the chip area. The power consumption is not, however, affected since the opamps are turned ON only in one half of the clock period.

Baschirotto and Castello [4.89] have suggested some improvements for the switched opamp technique that are described next. In the steady state, in the switched opamp-based integrator redrawn in Fig. 4.51a, the condition $V_{out,dc} - V_{3} = V_2 - V_4$ will hold. Under this condition, no charge injection into the virtual ground node occurs. In this circuit, considering the threshold voltage $V_T = 0.9$ V, $V_{DD} = 1.5$ V, $V_2 = V_3 = V_4 = V_{in,dc} = V_{out,dc} = V_{REF} = 425$ mV, the output swing is 550 mV. It can be seen thus that the dynamic range of the scheme of Fig. 4.51a is much less than the power supply voltage. Another limitation of the above circuit is that the opamp is switched OFF completely during one phase. This will cause a long turn-on time thereby decreasing the frequency of operation.

Baschirotto and Castello [4.89] observe that the power supply voltage can be reduced to $V_{TH} + 2V_{ov}$ and rail-to-rail operation is possible with suitable modifications. They suggest that only the second stage of the opamp needs to be shut off and the charge stored on the compensating capacitor is maintained during the OFF phase of the opamp. Thus high frequency of operation can be feasible. In addition, a fully differential topology also is recommended. In their circuit, whose

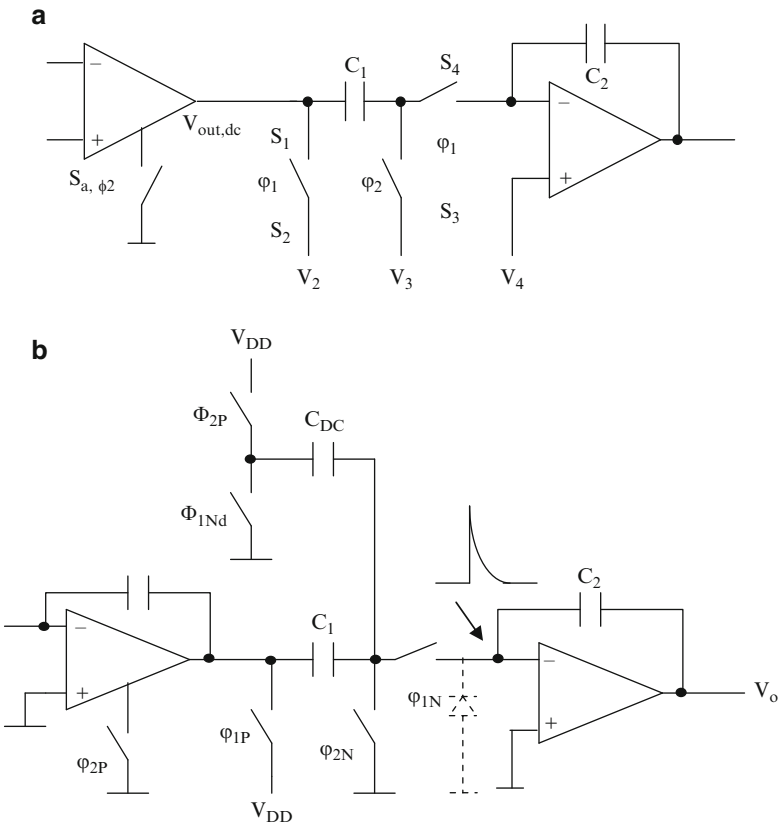


Fig. 4.51 (**a**) A switched opamp-based SC integrator, and (**b**) modification to achieve independent setting of common mode input voltage and quiescent output voltage (Adapted from [4.89] © IEEE 1997)

single-ended version is shown in Fig. 4.51b, a switched capacitor C_{DC} is used to pump a fixed amount of charge into the virtual ground to define the opamp input common mode voltage. Thus, the common mode voltage is decoupled from the opamp output dc voltage. In the steady-state condition, $C_{DC}V_{DD} + C_{IN}V_{OUT,dc} = C_{IN}V_{DD}$. Choosing $C_{DC} = C_{IN}/2$, we have $V_{OUT,dc} = V_{DD}/2$. Thus, simultaneous optimization of the switch operation and signal swing is achieved. Thus, a $V_{in,dc}$ of ground can be achieved. During the turn-on transients of the switch, due to charge injection, negative spikes result at the inverting input of the opamp which may forward bias the bulk diode (shown in dotted lines) at the input terminal of the opamp. This transient can be reduced by the charge injected by C_{DC} simultaneously. All the switches (realized using NMOS) are connected either to ground or connected to V_{DD} (realized using PMOS). Thus, the minimum supply voltage required is $V_{TH} + V_{ov}$ where V_{ov} is the overdrive voltage.

4.14.2 Clock Boosting Technique

Giustolisi et al. [4.90], and Aloisi et al. [4.91] have described a clock boosting technique that is considered next. In this circuit, shown in Fig. 4.52a, transistors M_{B1} and M_{B2} form an inverter. When V_{CLK} is high, the capacitor C_{B1} is precharged to V_{DD} through transistor M_{B3}. During this phase, the load capacitor C_{BL} is discharged through M_{B5} which is ON. Transistor M_{B4} is open during this phase. In the next phase when V_{CLK} is low, M_{B3} is OFF, M_{B4} closes, and M_{B5} is OFF. Thus, the supply voltage V_{DD} gets added to the precharged voltage available on C_{B1} to supply $2V_{DD}$ to the load through M_{B4}. The output voltage tries to reach $2V_{DD}$ but during the last part of the transient, the bulk junction of M_{B3} clamps the output to V_{DD} + 0.6.

Another well-known multiplier circuit [4.82, 4.92] is shown in Fig. 4.52b. It consists of four transistors M_1–M_4 driven by a two-phase clock. It needs two capacitors C_A and C_B. During φ_1, C_A is charged by the battery voltage V_{batt} and C_B supplies current to the load. During φ_2, C_A is connected between the battery and C_B and supplies current to the load and C_B itself. Hence, the top plate of C_B rises to almost twice the battery voltage V_{batt} after many clock periods. However, the V_{cc} value is not predictable depending on the load and on temperature and process spreads via resistances of M_1–M_4. Moreover, it also depends on the state of the battery itself.

An improved regulated power supply can be built using the circuit of Fig. 4.52c. Note that a feedback path is included to control the ON-resistance of M_2 during φ_1. This feedback applies a proportional as well as an integral transfer function to V_1–V_2 that are scaled down with respect to V_{CC} and to a precise internal reference V_{CM} thus forcing V_1 to be equal to V_2:

$$V_{CC} = V_{CM}\left(\frac{R_3}{R_3 + R_4}\right)\left(1 + \frac{R_2}{R_1}\right) \tag{4.103}$$

It may be noted that a ripple is superimposed on V_{CC} at the multiplier clock frequency but this only leads to very small offset and clock feedthrough at the SC filter output.

4.14.3 Local Switch Bootstrapping

The concept here is to maintain fixed voltage across the gate and source which is signal-independent. One such circuit [4.84] is shown in Fig. 4.53. In this circuit, the actual switch is M_{11}. The clock φ turns this switch ON and OFF. During the OFF phase, φ is low. Devices M_7 and M_{10} thus conduct grounding the gate of M_{11}. At the same time, V_{DD} is applied across capacitor C_3 through M_3 and M_{12} and devices M_8 and M_9 are OFF. Thus, C_3 is isolated while it is charging. When φ is high, M_{10} is OFF, M_5 pulls down the gate of M_8 thus first connecting gate G of M_{11} to the battery capacitor C_3. Thus both M_9 and M_{11} will turn ON thereby applying V_{DD} across gate and source terminals of the switch which is kept constant independent of the input signal at the source. Since the body of M_8 is tied to its source, latch-up is

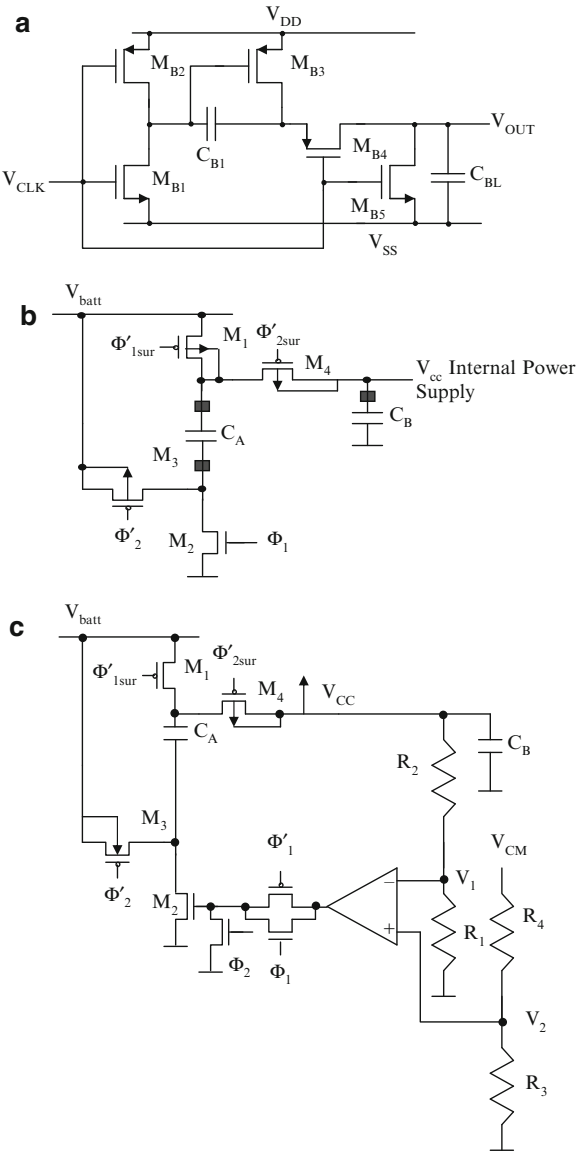


Fig. 4.52 (**a**) Clock booster schematic, (**b**) classical voltage multiplier, and (**c**) regulated voltage multiplier ((a) Adapted from [4.90] © IEEE 2000, (b) and (c) Adapted from [4.82] © IEEE 1996)

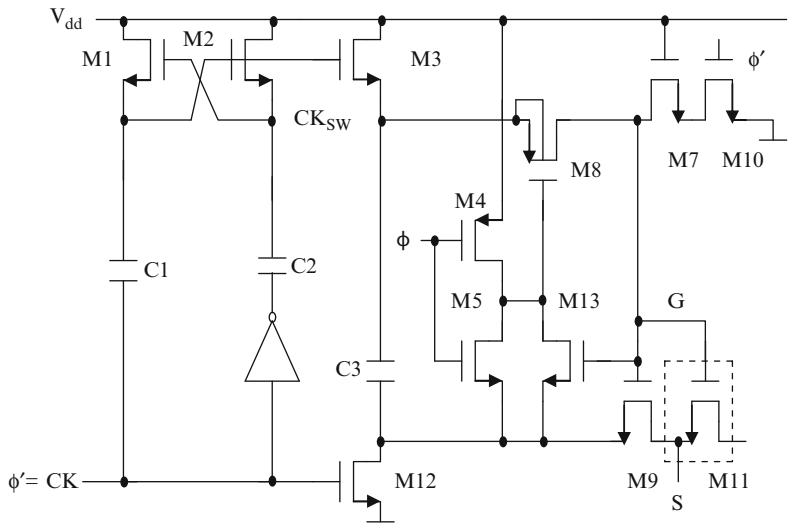


Fig. 4.53 Switch bootstrap circuit due to Abo and Gray (Adapted from [4.84] © IEEE 1999)

suppressed. Device M_7 reduces the V_{ds} and V_{gd} experienced by M_{10} when $\varphi = 0$. C_3 must be sufficiently large to supply charge to the gate of the switch in addition to parasitic capacitances C_p in the charging path, where C_p is the parasitic of the top plate of C_3. In the design of [4.84], C_3 is typically 0.5–1.8 pF which is six times C_p. The gate voltage is given by

$$V_G = V_S + V_{DD}\left(\frac{C_3}{C_3 + C_p}\right) \tag{4.104}$$

The transistors M_1, M_2 and capacitors C_1 and C_2 perform as a clock multiplier [4.93, 4.94] that enables M_3 to unidirectionally charge C_3 during the OFF phase. The operation of the clock multiplier is as follows. The capacitors C_1 and C_2 are charged to V_{DD} via cross-coupled NMOS transistors $M_1$and M_2. When the input clock CK goes high, the output clock CK_{SW} approaches a value slightly less than $2V_{DD}$ due to charge sharing with parasitic capacitances. The capacitor C_1 can be small whereas C_2 has to be large. The feedback technique employed can eliminate a voltage loss due to threshold voltage V_t of MOSFETs.

We next consider alternative bootstrapping techniques [4.95]. A basic bootstrapped switch circuit is shown in Fig. 4.54a. In this circuit, in Phase 2, the capacitor C_{offset} is charged to the supply voltage $V_{DD} - V_{SS}$ and the gate of the switch is grounded thus making MNSW OFF. In Phase 1, the capacitor C_{offset} is connected across the gate and source terminals of the switch MNSW so that the V_{gs} is kept constant independent of the input signal level. Thus, rail-to-rail signal switching is feasible. Note that all switches in a SC circuit need not be bootstrapped. As an illustration, a SC low-pass filter is presented in Fig. 4.54b. Note that only the switches S_1 and S_6 need to handle large signal levels whereas the switches S_4 and S_3 handle only ground or virtual ground. It may be observed that two reference voltages are used: $V_{DD}/2$ and V_{SS}. At

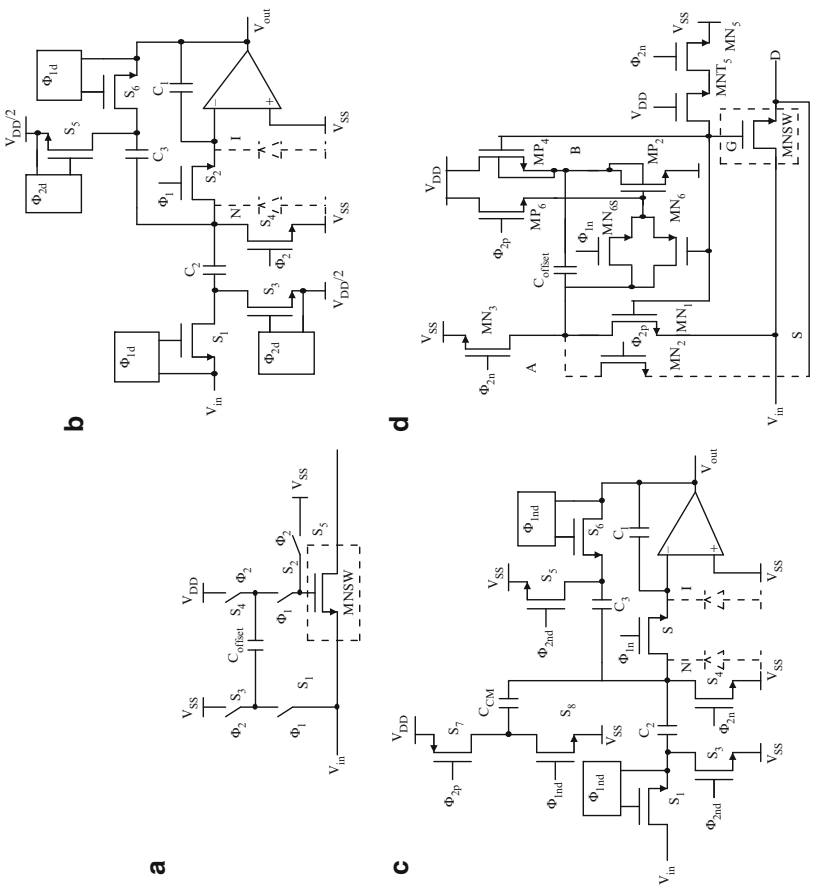


Fig. 4.54 (**a**) Basic switch bootstrapping circuit, (**b**) low-voltage SC first-order low-pass filter based on switches of (a), (**c**) low-voltage SC first-order low-pass filter using charge cancellation and single reference, and (**d**) complete transistor-level implementation of (a) (Adapted from Dessouky and Kaiser [4.95] © IEEE 2001)

the opamp input, for the switch S_4, V_{ss} can be used since it is switching ground or virtual ground and this switch can be a normal switch. The $V_{DD}/2$ reference voltage is used for the switches S_3 and S_5 since they need to handle large signals and these use bootstrapped switches. Using V_{ss} at the opamp input eases the biasing of the input transistors of the opamp. However, it may cause charge leakage due to negative transient spikes. The reverse-biased diodes due to the drain-source-bulk junctions of switches S_4 and S_2 (shown in dotted lines) conduct due to these negative spikes thereby discharging the integrating capacitor. Nodes N and I are subject to these spikes. Note also that the switched capacitors C_2 and C_3 are not reset to zero but to $V_{DD}/2$ thus reducing the voltage step to $V_{DD}/2$. Furthermore, due to opamp finite bandwidth, the spike amplitude will be much lower than 0.5 V when a supply voltage of 1 V is used.

The number of bootstrapped switches can be reduced using a single analog reference voltage V_{ss}. However, the signal still varies around $V_{DD}/2$ at the input as well as the output of the opamp. The difference between the two reference voltages can be compensated by injecting a fixed charge into the node N using additional switched capacitor C_{CM} as shown in Fig. 4.54c. The extra capacitor, however, increases the switching noise.

The transistor-level implementation of the bootstrapped switch is shown in Fig. 4.54d wherein some additional devices have been employed to make it symmetrical. The transistors *MN*1, *MP*2, *MN*3, *MP*4, and *MN*5 correspond to the five ideal switches S_1–S_5, respectively. Additional switches are introduced to facilitate rail-to-rail operation and they also help to limit all gate-source voltages to V_{DD}. Gate connection of *MP*4 and *MP*2 prevent their overstress when the voltage at node *B* rises to V_{DD}. Transistor *MN*6*S* triggers *MP*2 ON at the beginning of φ_1 and transistor *MN*6 keeps it on as the voltage on node A rises to the input voltage V_{in}. Gate connections of switches *MN*1 and *MN*6 allow them to turn on like MNSW. In addition, the transistor *MNT*5 has been added to prevent the gate drain voltage of *MN*5 exceeding V_{DD} during φ_1 while it is OFF. During φ_1 when *MNT*5 is off, its drain–bulk diode junction voltage reaches $2V_{DD}$. This must be compatible with the technology limits. Finally, note that the bulk of transistors *MP*2 and *MP*4 must be tied to the highest potential: that is, node *B* and not to V_{DD}. The voltage at the drain side of the main switch MNSW must be greater than that at the source side at the switching moment so as to prevent the drain source voltage to exceed V_{DD} during the turn on transient. In order to overcome the limitation, anther transistor *MN*2 has been added to the drain side as shown in dashed lines to make the switch symmetrical. The gate voltage is thus clamped at a voltage V_{DD} higher than the terminal of the lowest terminal voltage.

4.14.4 Reset-Opamp Technique

Another technique for designing low-voltage switched-capacitor circuits is based on reset-opamp low-voltage SC integrators which is described next. The reader may recall that in the switched opamp technique, the integration is performed in one

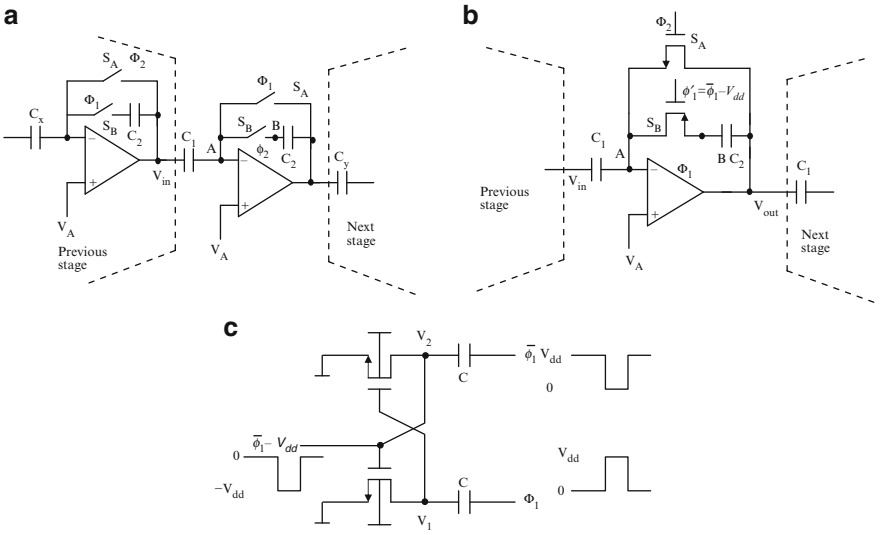


Fig. 4.55 (**a**) Reset-opamp SC integrator, (**b**) low-voltage SC integrator with MOS switches, and (**c**) level-shifted clock generator (Adapted from Keskin et al. [4.86] © IEEE 2002)

phase and in the other phase the opamp is switched off. This reduces the operating speed of the resulting SC filter due to the transients introduced by the required power up/down of the opamp. In the technique, we consider next, the opamp is not switched off and is always in linear operation. This is called the *reset-opamp* technique [4.86] since the opamp output is reset during one clock phase.

The reset-opamp technique is based on the offset compensation scheme presented earlier due to Gregorian (see Fig. 4.45a). Consider the cascaded SC integrators shown in Fig. 4.55a. In Phase ϕ_1, the feedback loop of the opamp is closed using the switch S_A (i.e., opamp output voltage is reset to ground) and the switch S_B opened so as to preserve the charge on the integrating capacitor. The capacitor C_1 acquires the charge $C_1(V_{in} - V_A)$. In the phase ϕ_2, the output of the previous stage is reset to V_A thereby discharging C_1 into the virtual ground of the opamp at the second stage. Also, since the integrating capacitor C_2 is reconnected back into the feedback branch, it absorbs the charge of C_1. The resulting V_{out} is sampled by the input capacitor of the next stage. Thus a noninverting integrator of a half-cycle delay is realized.

The circuit, in practice, has some problems when the feedback switch is closed. Usually NMOS devices are used for S_A and S_B, since they can be turned on easily. Assuming that at the end of $\phi_2 = 1$, the output voltage is V_{DD}, at the beginning of phase ϕ_1, the closure of S_A will pull V_{out} to ground thereby pulling the floating node B to $-V_{dd}$ by C_2. As a result, the source–substrate junction will be forward-biased with conduction leading to a loss of charge from C_2 to the substrate. One method of overcoming this problem is to use a PMOS switch in place of NMOS switch so that the source substrate junction will be reverse-biased thus not causing the loss of charge as shown in Fig. 4.55b. A new situation arises since the PMOS switch needs a

negative clock voltage for conduction. This can be solved by using a level-shifted clock generator as shown in Fig. 4.55c based on the Nakagome et al. clock booster stage [4.93] (which was considered earlier in Fig. 4.53).

4.14.5 BIOC (Biased Inverting Opamp Configuration) Based SC Filters

Low voltage analog circuit design based on biased inverting opamp configuration (BIOC) has been suggested by Karthikeyan et al.[4.149]. This technique is superior to switched opamp technique since no critical switches for processing analog signals are needed. Furthermore, the need for high common mode input range opamp is avoided.

The basic concept is illustrated in Fig. 4.56a using a current source and (b) using a resistor. Simple circuit analysis shows that

$$V_o = V_x\left(1+\frac{R_f}{R_{eq}}\right) - R_f\left(\frac{1}{R}V_1+\frac{1}{R}V_2+\frac{1}{R}V_3+....+\frac{1}{R}V_n\right) \tag{4.105}$$

where $R_{eq} = R_1 /\!/ R_2 /\!/ \ldots /\!/ R_n$. For maximum output swing, input/output quiescent voltage is set at $V_{DD}/2$ and as such v_x is required to be set to $V_{DD}/2$. Considering a PMOS differential amplifier for the opamp, due to the limited common mode input range, supply voltage is required to be greater than $2(V_{Dssat}+|V_{tp}|)$. As such, the circuit cannot operate at 1-V supply voltage, if $|V_{tp}|>0.4V$.To reduce the supply voltage, the opamp input common mode voltage V_x has to be biased a voltage close to ground independent of input and output quiescent voltage. This can be achieved by choosing I_B such that

$$I_B = \left(\frac{V_{DD}}{2}-V_x\right)\left(\frac{1}{R_f}+\frac{1}{R_{eq}}\right) \tag{4.106}$$

The current source I_B can be realized by a NMOS transistor. Hence V_x must be greater than V_{DSsat} and hence the minimum supply voltage for the new circuit is $V_{DSsat} + 2V_{SDsat} + |V_{tp}|$. Note that in the case of the NMOS input differential amplifier, a PMOS current source is connected between the virtual ground and positive supply voltage. In place of the current source, a resistor can be used as well and realized using a MOSFET operating in the triode region with a value given by

$$R_B = \left(\frac{v_x}{\frac{V_{DD}}{2}-v_x}\right)(R_f /\!/ R_{eq})$$

The performance of both circuits at high frequencies is different since of the finite resistance of the current source. A circuit for generating I_B is shown in Fig. 4.56c

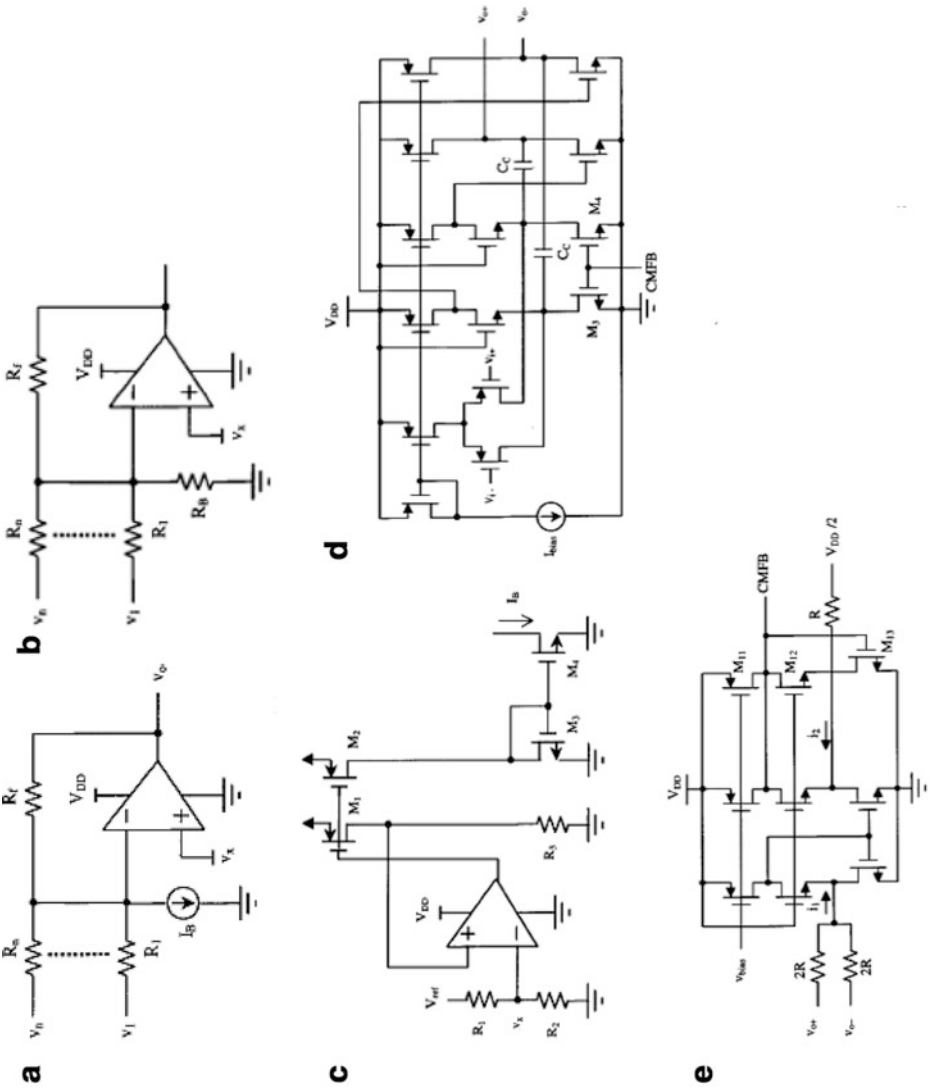


Fig. 4.56 (**a**) Biasing scheme using a current source, (**b**) biasing scheme using a resistor, (**c**) biasing circuit for generating I_B, (**d**) 1 V fully differential opamp, and (**e**) continuous CMFB circuit (Adapted from [4.149] © IEEE 2000)

which can track with variations in resistor values. The feedback loop around the opamp ensures that drain current of M_1 is V_x/R_3. Assuming all matched transistors,

$$I_B = \frac{V_{ref}\ R_2}{(R_1 + R_2)\, R_3} \tag{4.107}$$

For fully differential amplifiers, the input common mode voltage can be sensed by using resistors R and compared with V_x using a single-ended differential amplifier. Due to the feedback loop, opamp input common mode voltage is set at V_x and the biasing current set according to R_1, R_f, and the input and output common mode voltages. The fully differential opamp and the CMFB circuit are presented in Fig. 4.56d, e. The opamp is a two-stage design with a folded cascade input stage, a common source output stage, and a continuous time CMFB. Two resistors of value $2R$ sense the common mode voltage and produce a current i_1 which is compared with a reference current i_2. Note that i_2 is set by $V_{DD}/2$ and resistor R. The difference between these currents is converted into a voltage CMFB by transistors M_{11}, M_{12}, and M_{13}. The control voltage is then used to adjust the V_{GS} of M_3 and M_4 such that the output common mode voltage is set to $V_{DD}/2$.

Huang and Lee [4.150] have described a continuous time filter with automatic tuning based on this technique. The Akerberg–Mossberg biquad using the BIOC technique is presented in Fig. 4.57a which is a modified version of the original AM biquad of Fig. 2.19. Note that C_B is omitted and a resistor is added in parallel with C_A of the first integrator to vary the Q factor. The Q can be tuned by adjusting the value of C_B only for a given value of C_A. Note, however, that Q and ω_o cannot be tuned independently. The switches used in the PCA for implementing C_A and C_B need to handle low voltages only. The parasitic resistance of the switches together with the feedback capacitor introduces parasitic zeroes which need to be placed at a higher frequency than ω_o by properly choosing transistor widths. Large transistor widths lead to large parasitic capacitances at the opamp inputs.

The authors have proposed a tuning system (shown in Fig. 4.57b) for frequency tuning and Q tuning. It consists of an oscillator, a reference filter, two binary counters (m-counter and f-counter) and two analog comparators. The oscillator is similar to the AM biquad of Fig. 4.57a with C_B omitted. By tuning the frequency of the oscillator ω_o, the filter pole frequency can be tuned. f_{osc} is measured by the m-counter which is controlled by the reference clock signal f_{clk}. The value of f_m-counter is latched at the end of each clock period of T_{clk} and compared with the digital word using a digital comparator. When the value of the m-counter is less (greater) than B_f, evidently f_{osc} is lower (greater) than the desired value. Accordingly, the f-counter decrements (increments) all the PCA control words. When the value of the m-counter equals B_f, there will be no change of an f-counter. It can be seen that $\omega_o = 2\pi B_f f_{clk}$. The clock signal should have a relatively long period together with a long m-counter to minimize the errors.

The frequency tuning accuracy depends on a good match between f_{osc} and the center frequency of the filter ω_o. Simulations show that f_{osc} is always smaller than f_o

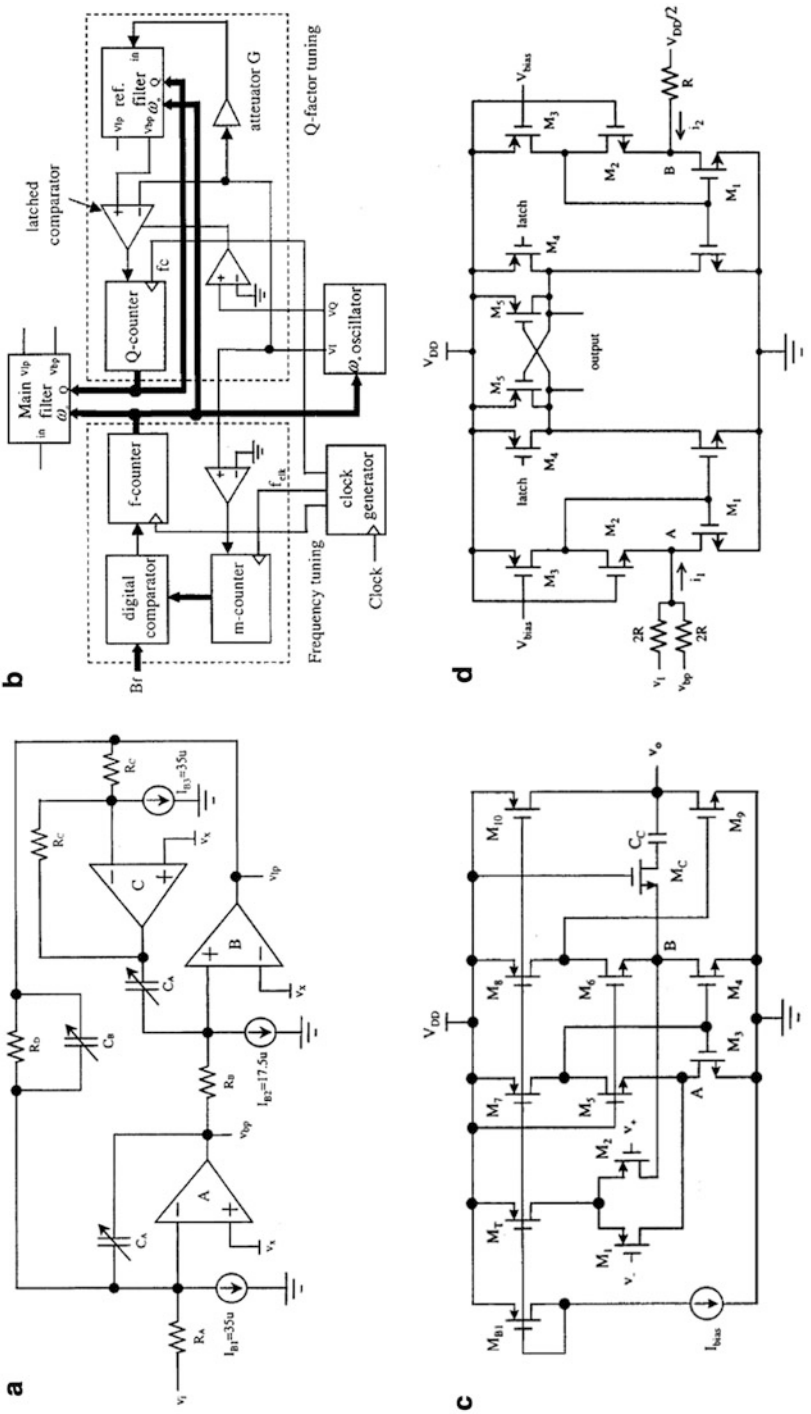


Fig. 4.57 (**a**) Low voltage modified Akerberg–Mossberg biquad, (**b**) automatic tuning circuit for (a), and (**c**) a 1-V opamp design (**d**) 1V current mode latched comparator (Adapted from [4.150] © IEEE 2001)

by an error of 2–5% due to different loading effects of opamps in the filter and oscillator.

The Q-tuning is carried out after frequency tuning. The oscillator output is attenuated by G $(=1/Q)$ and fed to the reference filter. The magnitude of the BP output of the reference filter is compared with the magnitude of the input and then adjusts C_B until the magnitudes are equal. The authors do not use peak detectors but instead use latched comparators. The quadrature phase signal is used as the latch signal for the latched comparator. The output of the latched comparator is fed to the Q counter which is incremented or decremented by 1 if V_{bp} is higher than V_{I}. The updating rate of the Q counter is determined by the external clock signal f_c. The tuning range of the Q factor depends on C_B and ω_o since $Q = \frac{1}{\omega_o C R_B}$.

The 1-V opamp is presented in Fig. 4.57c based on a two-stage architecture. The low voltage current mirror formed by M_3, M_4, M_5, M_6 is used together with a PMOS differential pair to form the first stage. The second stage is a NMOS common source amplifier.

The latched comparator shown in Fig. 4.57d works in current mode. The wide input signal swing is achieved by connecting inputs to resistors that convert voltage into current to flow into the low impedance node A.

This is compared with the reference current i_2. Note that i_1 and i_2 will be equal if V_i and V_{bp} have the same amplitude. Otherwise, i_1 and will be different and a logic signal is produced at the output after the latch signal goes high.

4.15 Noise in SC Filters

SC filters use switches and opamps that contribute to the noise. It is necessary to evaluate the contribution of these various noise sources to the output of the SC filters so that the dynamic range can be estimated [4.97].

A switch in a SC filter using a MOS transistor operating in the triode region can be modeled as shown in Fig. 4.58a by a noiseless resistance R_{on} together with a Johnson noise source in series with the resistance whose power spectral density (PSD) is given by

$$S_{vt}(f) = 4kT R_{on} \left(V^2/Hz\right) \tag{4.108}$$

where $k = 1.38 \times 10^{-23}$ J/K is Boltzmann's constant and T is the absolute temperature of the device in degrees Kelvin. The mean value of the thermal noise is zero. The PSD is considered to be a one-sided distribution.

For a MOS transistor operating in strong inversion and in the active region, the thermal noise can be modeled by a current source in parallel with the channel. The PSD is approximately given by

$$S_{it}(f) = \frac{8}{3} kT g_m \left(A^2/Hz\right) \tag{4.109}$$

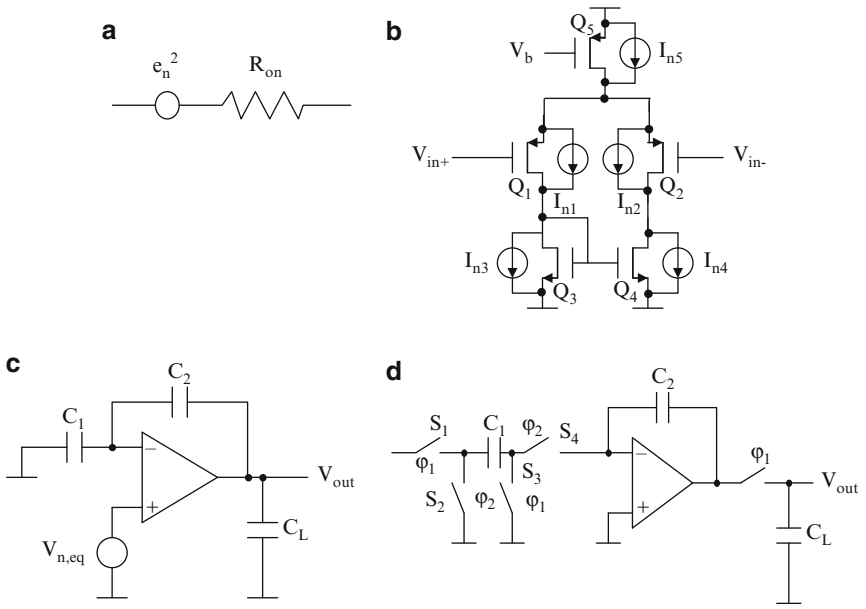


Fig. 4.58 (**a**) Noise model of a switch, (**b**) single-stage CMOS opamp showing various noise sources, (**c**) typical opamp circuit with capacitive feedback and load capacitance, and (**d**) SC integrator followed by a switched-capacitor (Adapted from [4.97] © IEEE 2005)

where g_m is the transconductance of the device. On the other hand, another source of noise known as flicker noise or $1/f$ noise exists which is modeled by a series voltage source connected to the gate of the MOS transistor whose PSD can be written as

$$S_{vf}(f) = \frac{K}{WLf}(V^2/Hz) \tag{4.110}$$

where W and L are the channel width and channel length, respectively; f is frequency; and K is a process-dependent parameter. Note that this noise is dominant at low frequencies and hence not white. The $1/f$ noise can be reduced by using large input devices or by using PMOS transistors in place of NMOS transistors as input devices. Other techniques such as correlated double-sampling can be used to reduce this noise.

We next consider a simple single-stage opamp shown in Fig. 4.58b in which the noise current of transistor Q_5 does not contribute to the input referred noise since it is a common mode signal. On the other hand, the noise current of Q_1 and Q_2 is described by (4.109) and can be converted into an input referred noise voltage source with PSD of $\frac{8kT}{3g_m}$. Similarly, the noise current of the diode-connected load transistor Q_3 can be referred to the input as a voltage source of $\frac{8kT}{3}\frac{g_{m3}}{g_{m1}^2}$. The noise current of Q_4 can be referred to the other input of the differential amplifier. Thus the total noise PSD of the differential amplifier can be written as

$$S_{vt}(f) = \frac{16kT}{3\,g_{m1}}\left(1 + \frac{g_{m3}}{g_{m1}}\right) \tag{4.111}$$

Evidently, for low noise $g_{m3} \ll g_{m1}$.

We next consider an opamp with capacitive feedback and capacitive loading. Assuming a single-pole response for the opamp, the noise transfer function of the circuit in Fig. 4.58c can be written as

$$\frac{V_o}{V_n} = \frac{G_o}{1 + s\tau} \tag{4.112}$$

where $\tau = \frac{C_3\,C_1 + C_1\,C_2 + C_2\,C_3}{C_2\,G_{m1}} = \frac{C_o}{\beta G_{m1}}$, $\frac{1}{G_o} = \beta = \frac{C_2}{C_1 + C_2}$, $C_o = C_3 + \frac{C_1\,C_2}{C_1 + C_2}$.

The white noise given by (4.111) gets shaped from the frequency response given in (4.112). Thus, the mean square value of the output noise can be computed as

$$\bar{v}_{out}^2 = \int_0^\infty S_{vt}(f)\,|H(j2\pi f)|^2\,df = \frac{16kT}{3\,g_{m1}}\,\frac{G_0^2}{4\tau} \tag{4.113a}$$

From (4.112) and (4.113a), we have

$$\bar{v}_{out}^2 = \frac{4kT}{3}\,\frac{1 + \frac{C_1}{C_2}}{C_o} = \frac{4kT}{3\beta\,C_o} \tag{4.113b}$$

It is thus evident that in the expression for the output noise, the effect of g_m gets cancelled.

Schreier et al. [4.97] derive an interesting result for the case of a SC following an opamp-based continuous-time circuit as shown in Fig. 4.58d. The capacitor now has to charge to the full value of the input signal during the sampling period when the switch is ON. The charging process is exponential and typically is of the form $e^{-t/\tau}$. For achieving a settling error of less than ½ of a bit to realize N-bit performance, the condition to be satisfied is

$$e^{-\frac{1}{2f_s\,\tau}} < 2^{-(N+1)} \tag{4.114a}$$

Thus we have

$$\frac{f_{3dB}}{f_s} > \frac{(N+1)ln2}{\pi} \text{ or } \frac{f_{3dB}}{f_s} > 2.43 \text{ for N} = 10 \tag{4.114b}$$

This is an impossible case. This can be explained by the reasoning that the noise is white and extends up to frequencies much higher than the sampling frequency and hence, the sampling process aliases this wide-band noise into pass-band and the resulting noise is white. This is known as *foldover noise*. It is uniformly distributed in the frequency band 0 to $f_s/2$, thus the PSD becomes

$$S_{nos}(f) = \frac{\bar{v}_{no}^2}{f_s/2} = \frac{G_o^2 S_v}{2\tau f_s} \tag{4.115}$$

Thus, the noise is increased by the factor $1/(2\tau f_s)$ which is larger than the limit given (4.114b). Thus for $N = 10$, the noise PSD is enhanced by 7.6 or 8.8 dB. Therefore sampled data circuits have inherently more noise than their continuous-time counterparts.

Fischer [4.98] has presented an expression for evaluating the foldover noise. The white noise of the switches is wide-band in nature and due to the sampling process, the frequency-shifted side-bands are uncorrelated with each other. As such, they can be added to compute the total output noise density. Thus, for $-f_s < f < f_s$, we have

$$\eta_T = \eta_n + \left(\left(\frac{2BW_n}{f_s}\right) - 1\right)\eta_{sb} \tag{4.116a}$$

where BW_n is the bandwidth of the white noise and η_n is the spectral density of the noise source spread uniformly over BW_n. Evidently $\left(\left(\frac{2BW_n}{f_s}\right) - 1\right)$ is the number of side-bands falling in the frequency range $dc < f < f_s$. Recalling that $\eta_{sb} = \eta_n$, (4.116a) can be simplified as

$$\eta_T \leq 2\,\eta_n \left(\frac{BW_n}{f_s}\right) V^2/Hz \tag{4.116b}$$

Using the above models, we can derive the noise of SC filters. We consider the SC integrator of Fig. 4.58d. In phase φ_1, the equivalent circuit is as shown in Fig. 4.59a which can be simplified as Fig. 4.59b wherein the ON resistances of both the switches S_1 and S_3 have been represented as $2R_{ON}$. The PSD of the noise voltage v_{c1} across C_1 can be found to be

$$S_{c1}(f) = \frac{2\,S_{vt}(f)}{1 + (2\pi f\,\tau_o)^2} = \frac{8kT\,R_{ON}}{1 + (2\pi f\,\tau_o)^2} \tag{4.117a}$$

where $\tau_o = 2R_{ON}C_1$. The total power (mean-squared value) of $v_{c1}(t)$ can be found by integrating $S_{c1(f)}$ for frequencies from dc to infinity yielding once again the important relationship

$$\bar{v}_{c1}^2 = \frac{kT}{C_1} \tag{4.117b}$$

Thus, the noise of a switched capacitor is not dependent on the resistance of the switches and is only dependent on the value of the capacitance. In Phase 2, the equivalent circuit is as shown in Fig. 4.59c taking into account the opamp noise as well. We once again find v_{c1} approximately as

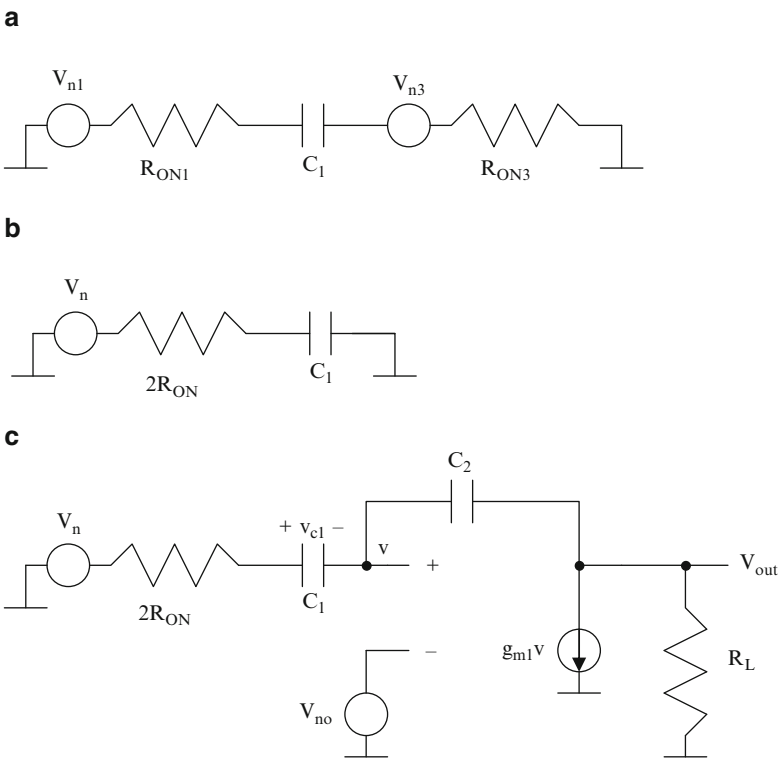


Fig. 4.59 (**a**) Noise equivalent circuit in Phase 1, (**b**) simplification of (a), and (**c**) noise equivalent circuit in Phase 2 using opamp model (Adapted from [4.97] © IEEE 2005)

$$V_{c1}(s) = \frac{V_n(s) - V_{no}(s)}{1 + s\tau} \tag{4.118a}$$

where

$$\tau = C_1\left(2R_{ON} + \frac{1}{g_{m1}}\right) \tag{4.118b}$$

Following in a similar manner as before, the mean-square value of the noise voltage on C_1 can be estimated from (4.118) as

$$\bar{v}^2_{c1,sw} = \frac{S_n(0)}{4\tau} = \frac{8kT\,R_{ON}}{4\left(2R_{ON} + \dfrac{1}{g_{m1}}\right)C_1} = \frac{kT}{C_1}\left(\frac{1}{1+\frac{1}{x}}\right) \tag{4.119a}$$

where $x = 2R_{ON}g_{m1}$. In a similar manner, the noise voltage on C_1 due to opamp noise can be found as

$$\bar{v}_{c1,op}^2 = \frac{S_{no}}{4\tau} = \frac{(16/3)(kT/g_{m1})}{4\left(2R_{ON} + \dfrac{1}{g_{m1}}\right)C_1} = \left(\frac{4}{3}\right)\frac{kT}{C_1}\left(\frac{1}{1+x}\right) \tag{4.119b}$$

The total noise acquired by the capacitor C_1 is thus the difference between that accumulated in φ_1 given by (4.117b) and the sum of the switch and opamp noise contributions in Phase 2 given in (4.119a) and (4.119b). Since these are statistically independent, the total noise is the sum of these quantities:

$$\bar{v}_{c1}^2 = \frac{kT}{C_1}\left(\frac{\frac{7}{3}+2x}{1+x}\right) \tag{4.120}$$

The ratio of switch noise power to the opamp noise power generated during ϕ_2 is $3x/4$. Thus for $x \ll 1$ (i.e., $g_{m1} \ll 1/R_{ON}$), the opamp noise dominates whereas for $x \gg 1$, the switch noise dominates.

For a given capacitor size, the g_{m1} needed for the opamp, to achieve minimum noise can be estimated as

$$g_{m1} = \frac{kT\left(\frac{7}{3}+2x\right)}{\tau\,\bar{v}_{c1}^2} \tag{4.121}$$

which is minimized for $x = 0$. The total noise in this case is $\frac{2.33kT}{C_1}$. This may be seen to be 17% larger tan for the case $x \gg 1$ (i.e., $2kT/C_1$). The noise stored on C_1 is transferred to C_2 and thus the noise voltage on C_2 is given as

$$\bar{\Delta}\,\bar{v}_{c2}{}^2 = \frac{kT\,C_1}{C_2^2}\left(\frac{\frac{7}{3}+2x}{1+x}\right) \tag{4.122}$$

The noise analysis of biquads is also of interest. Walscharts et al. [4.99] have suggested a simple noise optimization procedure for the Fleischer–Laker SC biquad. These biquads can be coupled or uncoupled, therefore the coupled biquads are preferred since the noise optimization can be carried out efficiently since few capacitors can be unswitched and hence noiseless. It is assumed that the noise is the same in both phases of the clock. This assumption may lead to overestimation of noise by 1–2 dB as pointed out by Walscharts et al. [4.99]. However, this assumption simplifies matters considerably. In the method being considered, we associate a noise source with each of the switched capacitors G, H, I, J, A, C, and F since other unswitched capacitors do not contribute to the noise. The noise spectral density of these noise sources is given by kT/C_i where C_i refers to each of these capacitors. The aggregated noise of capacitors connecting to each inverting input of the opamp is filtered by the biquad. Thus, noise transfer functions need to be derived for the two aggregated sources. The total noise can be found as

$$v_n^2 = \frac{4kT.2A^2\,(C+G+H)}{f_s}\int_{f_L}^{f_H}\left.\frac{1}{D(z)D(z^{-1})}\right|_{z=e^{j2\pi f/f_s}}.df$$
$$+\frac{4kT.2D^2\,(A+F+I+J)}{f_s}\int_{f_L}^{f_H}\left.\frac{(1-z)(1-z^{-1})}{D(z)D(z^{-1})}\right|_{z=e^{j2\pi f/f_s}}.df \qquad (4.123a)$$

where

$$D(z) = D(B+F) + (AC + AE - DF - 2BD)\,z^{-1} + (BD - AE)\,z^{-2} \qquad (4.123b)$$

Note that the squared magnitudes of the noise transfer functions are used in (4.123a).

The transformations suggested by Fleischer and Laker for combining switched capacitors into unswitched capacitors such as when $G = H$ as a single unswitched capacitor L will reduce noise associated with switches. Tradeoff is possible between area and noise. This can be appreciated by noting that the area and noise of an arbitrary SC filter having n integrators can be expressed as follows.

$$\text{Area} = k_1\,C_1 + k_2\,C_2 + k_3\,C_3 \ldots + k_n\,C_n \qquad (4.124a)$$

$$\text{Noise} = \frac{l_1}{C_1} + \frac{l_2}{C_2} + \frac{l_3}{C_3} \ldots\ldots + \frac{l_n}{C_n} \qquad (4.124b)$$

where k_1,k_2, …, k_n and l_1,l_2, …, l_n are constants. The optimum distribution of chip area for achieving low noise can be achieved by choosing

$$\frac{k_1\,C_1^2}{l_1} = \frac{k_2\,C_2^2}{l_2} = \frac{k_3\,C_3^2}{l_3} = \ldots = \frac{k_n\,C_n^2}{l_n} \qquad (4.124c)$$

Fischer [4.98] has suggested an approximate approach to obtain noise using SPICE. In this method illustrated for the SC biquad of Fig. 4.60b, the noise equivalent can be derived as shown in Fig. 4.60c. Note that switched capacitors C_i are replaced by resistors of value T/C_i. The foldover noise of the opamp is represented by an additional output denoted as switched output S_o whereas the continuous output C_o is connected to the paths that are not switched (see Fig. 4.60a). Both the un-sampled *1/f* noise and white noise are treated as separate sources using the voltages $v_{1/f}$ and v_{n1}. The switched output is connected to all the switched capacitors connected to outputs of the opamps. To model the noninverting integrator, a VCVS of gain -1 can be used. The $1/f$ noise source is simulated using a MOSFET noise. The reader is referred to [4.98] for a complete SPICE model for noise estimation. The foldover noise is described by the switched output where $k = \sqrt{\frac{BW_n}{f_s} - 1}$ where BW_n is the noise bandwidth of the opamp.

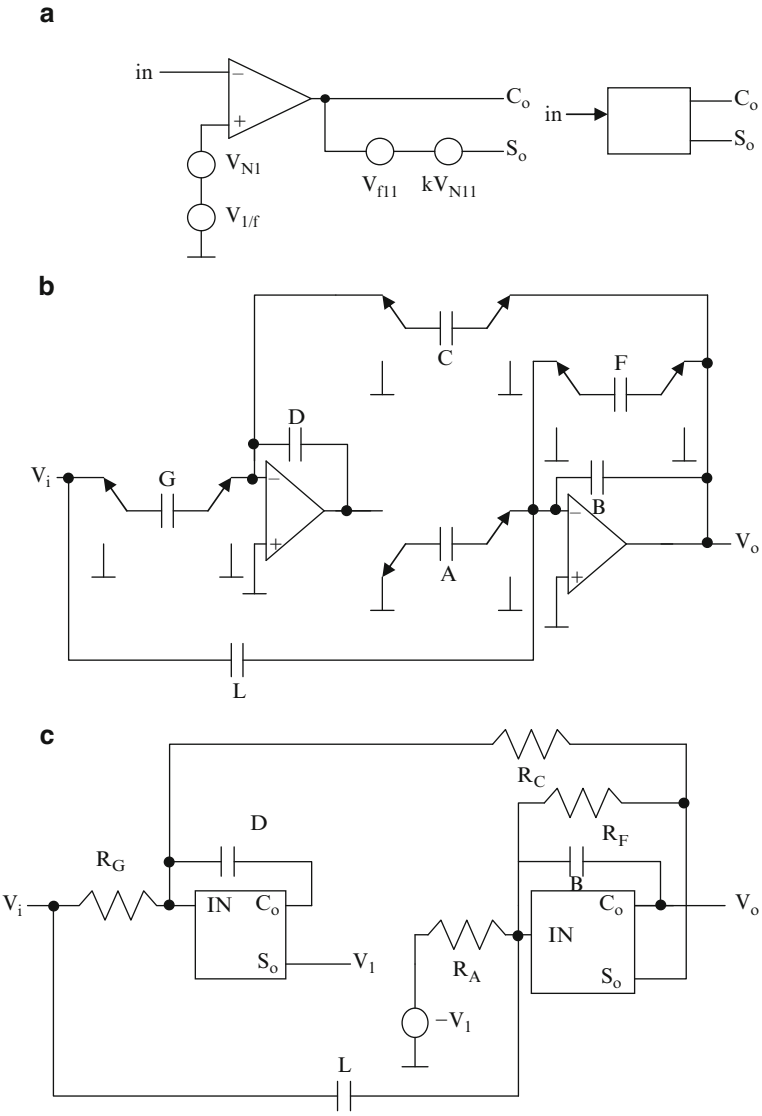


Fig. 4.60 (**a**) Frequency domain noise simulation model of opamp, (**b**) SC biquad, and (**c**) noise equivalent circuit for use in SPICE (Adapted from [4.98] © IEEE 1982)

Example 4.5 We analyze the noise of the SC high-pass notch filter of Fig. 4.60b. The zero frequency is at 1 KHz and sampling frequency is 8 KHz. The pole frequency is 2 KHz and pole-Q is 3. First, the analog transfer function can be written easily as

$$H(s) = \frac{s^2 + (2\pi \times 1,000)^2}{s^2 + +s(2\pi x2,000/3) + (2\pi \times 2,000)^2}$$

Bilinear transformation is used, thus the prewarping needs to be carried out using the mapping rule $\Omega = \frac{2}{T}\tan\left(\frac{\omega T}{2}\right) = 6630.38 rads/\text{s}$.

Thus, substituting for s, $\frac{s}{\Omega}$ we obtain the prewarped analog transfer function as

$$H(s) = \frac{s^2 + (6630.38)^2}{s^2 + +s(4190.47) + 158040816.32}$$

Substituting the bilinear s $\rightarrow$ z transformation $s = \frac{2}{T}\left(\frac{1-z^{-1}}{1+z^{-1}}\right)$ and simplifying, we obtain the z-domain transfer function

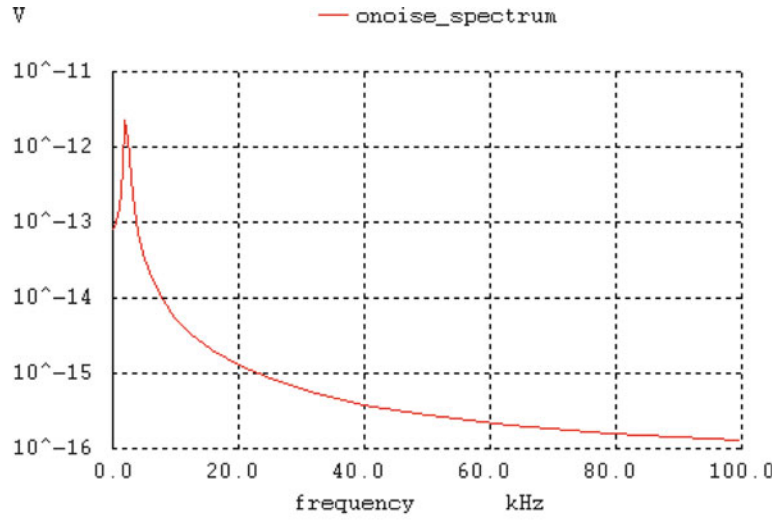
$$H(z) = \frac{0.86446 - z^{-1}\,(1.222146) + 0.86446\,z^{-2}}{1.386448 + z^{-1}\,(0.564617) + z^{-2}}$$

Identifying with the Fleisher–Laker biquad T-type transfer function in (4.15a), we obtain the various capacitor values as $I = J = 0.86446$, $H = 0$, $E = 0$, $A = B = D = 1$, $G = 0.506774$, $F = 0.386448$, and $C = 2.951065$. Since $I = J$, a single unswitched-capacitor is used. Next considering the SPICE equivalent, the resistances corresponding to capacitance C_i can be obtained as $\frac{T}{C_i}$ where T =1/8,000. Thus, resistances corresponding to A, C, G, F can be obtained. The capacitor values I, B, D are the same as above. Considering the opamp bandwidth for instance as 2 MHz, the factor k can be seen to be 22.3. The input current noise is ignored. The WINSPICE code is as follows.

```
* SC High-pass Notch filter noise analysis
R1 1 2 24665.8K
R3 2 7 4235.7K
C1 2 3 10pf
C2 6 7 10pf
R2 5 6 12500K
R4 6 7 32345.8K
C3 1 6 8.6446pf
E1 0 5 3 0 1
Xblk1 2 3 4 noisyopamp2out
xblk2 6 7 8 noisyopamp2out
.subckt noisyopamp2out ninp cont switched
V1 58 0 dc 0.1
V2 60 0 dc 0.1
D1 58 59 DIODE
R30 59 0 726.4
D2 60 61 DIODE
```

```
R31 61 0 726.4
E2 9 0 59 61 1
E3 cont 0 9 ninp 100000
V17 62 0 0
R32 62 0 73.6
E4 cont switched 62 0 22.3
.ends noisyopamp2out
vin 1 0 ac 0
.noise v(7) vin dec 10 0.5 100000 1
.MODEL DIODE D(AF=1.0,IS=0.001F, KF=1.667E-9)
```

The noise spectrum and total integrated noise output results are as follows.



sqrt(onoise_total) = 4.809854e-05

4.16 Effect of Finite Bandwidth of Opamp on the Performance of SC Filters

The effect of finite bandwidth of the opamp on the performance of SC filters is considered next. The analysis can be done for two cases: (a) using opamps with low output impedance, and (b) using OTAs. The results are slightly different for both these cases [4.100, 4.101, 4.102].

4.16.1 *Effect of Opamp Bandwidth on SC Filters Using Opamps*

Consider the SC integrator of Fig. 4.63a [4.101]. In Phase 2, since the opamp takes a certain amount of time to respond to the changes in the circuit topology, the various capacitors exchange charges instantaneously. The voltages at the input and output of the opamp, assuming that the input is held constant during clock phase 2, are

$$v_o(t) - v_o\left(n-\frac{1}{2}\right) = \left(\frac{C_1+C_2}{C_1}\right)\left(V_1(t) - V_1\left(t-\frac{1}{2}\right)^+\right) \tag{4.125}$$

Thus, the output voltage is not continuous but jumps to the opposite direction with respect to its final increment. Thereafter the opamp settles slowly and the output reaches the final value as explained next. The equations describing the behavior are:

$$C_1\frac{dV_1(t)}{dt} = C_2\frac{d}{dt}(V_o(t) - V_1(t)) \tag{4.126a}$$

or alternatively

$$\left(\frac{C_1+C_2}{C_1}\right)\frac{dV_1(t)}{dt} = \frac{dV_o(t)}{dt} \tag{4.126b}$$

We also note that the single-pole model of the opamp

$$\frac{V_o}{V_1} = -\frac{B}{s} \tag{4.127a}$$

yields the relationship

$$\frac{dV_o}{dt} = -BV_1(t) \tag{4.127b}$$

From (4.126b) and (4.127b), we have the solution

$$v_1(n) = v_1\left(n-\frac{1}{2}\right)^+ e^{-k_1} \tag{4.128a}$$

where

$$k_1 = \left(\frac{BC_1}{C_1+C_2}\right)\frac{T}{2} \tag{4.128b}$$

Substituting for $v_1(n)$ from (4.128a) in (4.125), we have

$$v_o(t) = v_o\left(n-\frac{1}{2}\right) - \left(\frac{C_1+C_2}{C_1}\right)(1-e^{-k_1})\, v_1\left(n-\frac{1}{2}\right)^{+} \tag{4.129}$$

In a similar manner, during phase φ_1, we have

$$v_1\left(n-\frac{1}{2}\right)^{-} = e^{-k_2}\, v_1(n-1) \tag{4.130a}$$

where

$$k_2 = \frac{BT}{2} \tag{4.130b}$$

Also, we can obtain that

$$v_o\left(n-\frac{1}{2}\right) = v_o(n-1) - (1-e^{-k_2})\, v_1(n-1) \tag{4.131}$$

At time $t = (n - 1/2)T$, the capacitor C_1 is connected to the inverting input of the opamp. The charge on C_1 is instantaneously distributed between C_1 and C_2 according to

$$v_1\left(n-\frac{1}{2}\right)^{+} = \left(\frac{C_2}{C_1+C_2}\right) v_1\left(n-\frac{1}{2}\right)^{-} + \left(\frac{C_1}{C_1+C_2}\right) v_{in}\left(n-\frac{1}{2}\right) \tag{4.132}$$

Using (4.130a), (4.131), and (4.132) in (4.129), we get

$$v_o(n) = v_o(n-1) - \left(\frac{C_1}{C_2}\right)(1-e^{-k_1})\, v_{in}\left(n-\frac{1}{2}\right) - (1-e^{-(k_1+k_2)}) \times v_1(n-1) \tag{4.133a}$$

Furthermore, using (4.130a) and (4.132) in (4.128a), we have

$$v_1(n) = \left(\frac{C_2}{C_1+C_2}\right) e^{-(k_1+k_2)})\, v_1(n-1) + \left(\frac{C_1}{C_1+C_2}\right) e^{-k_1}\, v_{in} \times \left(n-\frac{1}{2}\right) \tag{4.133b}$$

Assuming that the input is held constant during φ_2, we can substitute $v_{in}(n - 1/2) = v_{in}(n)$. Next, taking the z-transform of (4.133a) and (4.133b) and solving, we obtain the transfer function of the integrator as

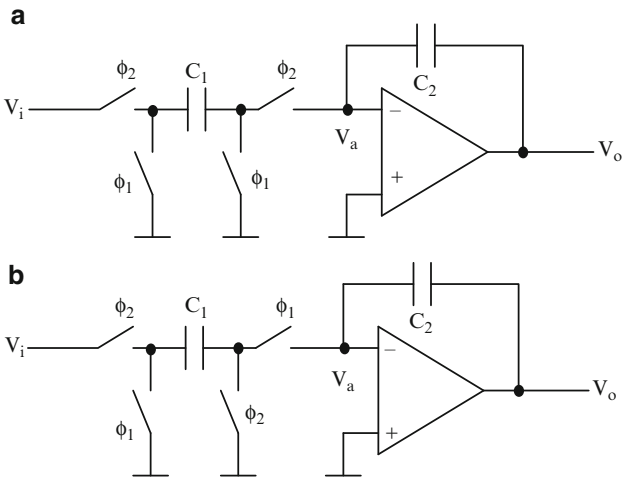


Fig. 4.61 Stray-insensitive SC integrators: (**a**) inverting, and (**b**) noninverting (Adapted from [4.102] © IEEE 1985)

$$\frac{V_o(z)}{V_i(z)} = \frac{-C_1}{C_2(1-z^{-1})} \times \left(1 - e^{-k_1} + e^{-k_1}\left(\frac{C_2}{C_1+C_2}\right) z^{-1}\left(\frac{1-e^{-(k_1+k_2)}}{1-z^{-1}\left(\frac{C_2}{C_1+C_2}\right)e^{-(k_1+k_2)}}\right)\right) \tag{4.134a}$$

Noting that $e^{-(k_1+k_2)} \ll 1$, (4.134a) can be simplified as

$$\frac{V_o(z)}{V_i(z)} = \frac{-C_1}{C_2(1-z^{-1})}\left(1 - e^{-k_1} + e^{-k_1}\left(\frac{C_2}{C_1+C_2}\right) z^{-1}\right) \tag{4.134b}$$

Similarly, the transfer function for a noninverting integrator of Fig. 4.61b can also be derived. Note, however that, in this case, the voltage across C_1 is applied to the opamp inverting input during φ_1. Thus, the discontinuity in $v_I(t)$ will occur at $t = (n-1)T$. The resulting transfer function at the end of Phase φ_2 can be derived as

$$\frac{V_o(z)}{V_i(z)} = \frac{C_1\, z^{-1}}{C_2(1-z^{-1})}\left(1 - e^{-k_1}\left(\frac{C_1}{C_1+C_2}\right) - \left(\frac{C_2}{C_1+C_2}\right)e^{-(k_1+k_2)}\right). \left(1 + \frac{C_2}{C_1+C_2}\left(\frac{e^{-(k_1+k_2)}\, z^{-1}}{1-z^{-1}\left(\frac{C_2}{C_1+C_2}\right)e^{-(k_1+k_2)}}\right)\right) \tag{4.135a}$$

which can be approximated as

$$\frac{V_o(z)}{V_i(z)} = \frac{C_1\, z^{-1}}{C_2\,(1-z^{-1})}\left(1 - e^{-k_1}\left(\frac{C_1}{C_1+C_2}\right)\right) \tag{4.135b}$$

The errors in the integrator transfer function can be approximated as

$$H_{actual} = \frac{H_{ideal}}{1 - m_i(\omega) - j\,\theta_i(\omega)} \tag{4.136}$$

where i stands for ith integrator. It can be easily shown that a two-integrator loop consisting of one lossless and one lossy integrator exhibits a variation in pole-frequency and pole-Q given by

$$\frac{\Delta\omega_o}{\omega_0} \cong \frac{1}{2}\left(m_1(\omega_o) + m_2(\omega_o)\right) \tag{4.137a}$$

and

$$Q_a = \frac{Q}{1 + Q(\theta_1(\omega_o) + \theta_2(\omega_o))} \tag{4.137b}$$

4.16.2 *Effect of Opamp Bandwidth on SC Filters Using OTAs*

The difference between the previous case of using opamps and present case of using OTAs [4.102] is that there is a feedforward path through the integrating capacitor to the output of the OTA due to the high output impedance of the OTA. Furthermore, the capacitive load connected to the output terminal of the OTA also affects the transient response. Eqs. 4.133a and 4.133b get modified as

$$v_o(n) = v_o(n-1) - \left(\frac{C_1}{C_2}\right)\left(1 - \left(\frac{C_1+C_2}{C_1}\right)e^{-k_3}\right) v_{in}\left(n-\frac{1}{2}\right) - v_1(n-1) \tag{4.138a}$$

and

$$v_1(n) = e^{-k_3}\, v_1(n-1) \tag{4.138b}$$

where

$k_3 = \left(\frac{G_m C}{C_{L2}(C_{in}+C)}\right)\frac{T}{2}$ and $C_{L2} = \frac{C_1 C_2}{C_1+C_2}$.

Note that in the case of a fixed capacitor C_4 being connected to the output of the OTA, (4.138a) becomes

$$v_o(n) = v_o(n-1) - \left(\frac{C_1}{C_2}\right)\left(1 - \left(1 + \left(\frac{C_2}{C_{L2}}\right)\left(\frac{C_1 + C_2}{C_1}\right)\right) e^{-k_3}\right) \times v_{in}\left(n - \frac{1}{2}\right) - v_1(n-1)\left(1 - \frac{C_4}{C_{L2}}\, e^{-k_3}\right) \tag{4.138c}$$

The transfer function in the case of inverting and noninverting integrators can be shown to be, respectively,

$$\frac{V_o(z)}{V_i(z)} = \frac{-C_1}{C_2(1 - z^{-1})}\left(1 - \left(\frac{C_1 + C_2}{C_1}\right) e^{-k_3} + e^{-k_3}\left(\frac{C_2}{C_1}\right) z^{-1}\right) \tag{4.139a}$$

and

$$\frac{V_o(z)}{V_i(z)} = \frac{C_1\, z^{-1}}{C_2(1 - z^{-1})}\left(1 - e^{-k_3}\right) \tag{4.139b}$$

Interestingly, the phase error in the noninverting case can be seen from (4.139b) to be zero.

Martin and Sedra [4.101] have estimated the pole-frequency deviation and deviation in the transfer function due to finite bandwidth of the opamp for various clock frequency to pole-frequency ratios. Their conclusion is that for a given resonant frequency, use of as low a clock frequency as possible decreases the errors due to the finite bandwidth of the opamps. They have also observed that the errors in SC filters are far fewer than those in active RC filters.

We next consider design considerations for realizing SC filters that are not sensitive to finite bandwidth of the opamps. SC biquads can be realized using differential-output differential-input opamps. Several distinct variations are possible for the realization of biquads. There are four types of two-integrator loops possible: (a) using one inverting integrator and one noninverting integrator, (b) using two inverting integrators, (c) using two noninverting integrators, and (d) using two differencing-input integrators. The negative feedback needed in the two-integrator loop is realized in cases (b) and (c) by connecting the appropriate output of the opamp since both normal and inverted outputs are available.

The arrangement of (d) uses SC integrators as shown in Fig. 4.62a in which input-differencing is employed for realizing the integrator. A complete biquad using this technique is shown in Fig. 4.62b. In the circuit of Fig. 4.62a, in both phases, the input and delayed input are integrated thus reducing the input capacitance to $C_1/2$ in place of C_1. Thus, the total capacitance is reduced thereby reducing the loading on the previous input stage. The charging time of the input capacitor is also reduced. Moreover, the error due to the finite gain of the opamp is also reduced. The capacitor spread, on the other hand, increases. The errors of this integrator have been shown to be as the average of the amplitude and phase errors of the inverting and noninverting integrators.

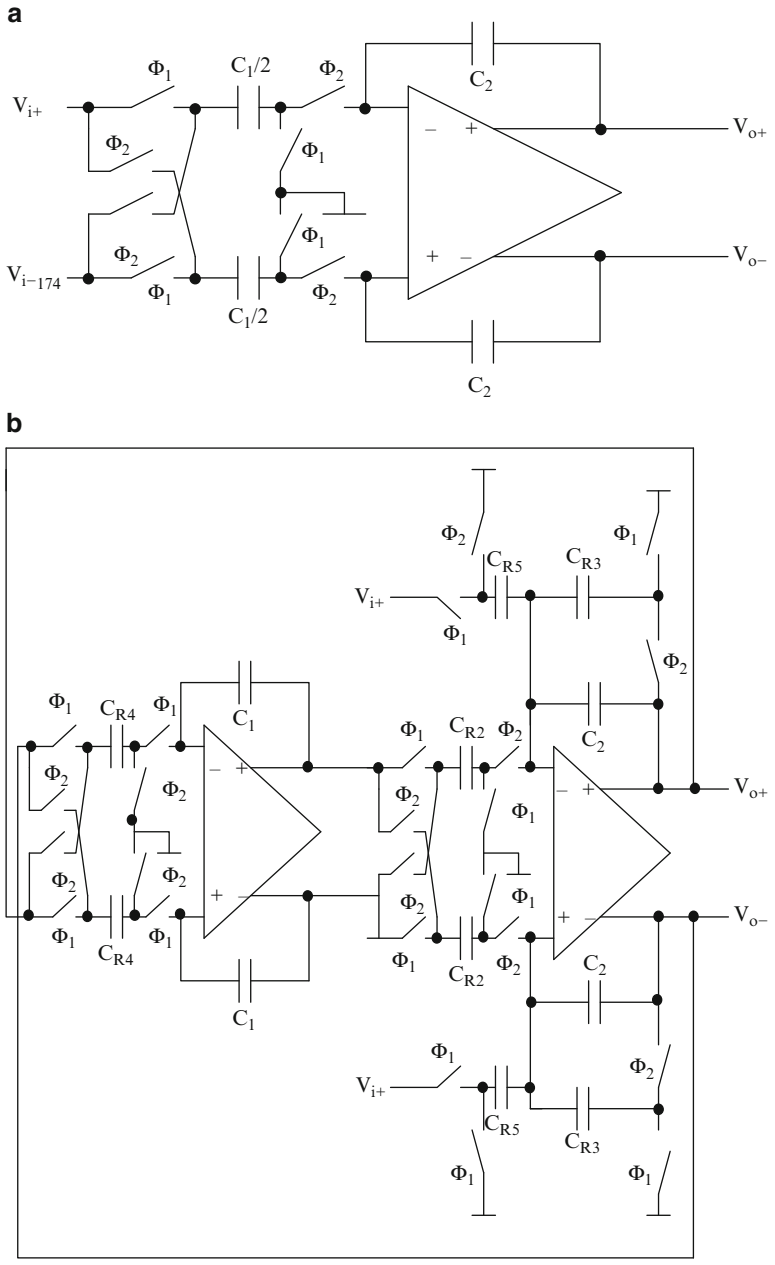


Fig. 4.62 (**a**) Differencing-input integrator, and (**b**) biquad based on the integrator of (a) (Adapted from [4.102] © IEEE 1985)

Interestingly however, the effect of the finite bandwidth of the opamp is different for these circuits. As has been shown earlier, the inverting integrator has amplitude and phase errors whereas the noninverting integrator has only amplitude error. An analysis of the pole-frequency and pole-Q errors for the various circuits by Ribner and Copeland [4.102] shows that the differencing-input filter has the lowest pole-frequency error and the second lowest gain error whereas the filter based on inverting integrators has the opposite performance. The biquads using noninverting integrators has the worst performance followed by the slightly better inverting/noninverting biquad.

4.17 Charge Injection in MOS Switches

One of the fundamental factors that limits the accuracy of the SC circuits is the charge injection occurring when the MOS FET turns off [4.103, 4.104, 4.105, 4.106, 4.107, 4.108, 4.109, 4.110, 4.111, 4.112]. A finite amount of mobile carriers are stored in the channel when the MOS transistor conducts. When the MOS transistor is turned off, this channel charge exits either through the source/drain or the substrate electrodes. The charge transferred to the data node during the switch turning-off period superimposes an error component on the signal voltage. In addition to the channel charge, the charge associated with the feedthrough effect of the gate-to-diffusion overlap capacitance also increases the error voltage after the switch turns off. The error voltage could be in the range of a few millivolts. As an illustration for a typical capacitor of size 8×8 μm and a sampling capacitor of 5 pF, a gate overdrive of 5 V introduces an error on the order of 20 mV.

A simple approach to reduce the effect of charge injection is to use large external sampling capacitors. This, however, leads to large circuit complexity and reduces the speed of operation of the SC filters. First-order cancellation of the switch charge injection is possible using dummy switch-based compensation technique [4.103, 4.104, 4.105]. This is shown in Fig. 4.63a. The charge cancelling device is a dummy device with its source shorted to drain to prevent dc current flow and with one half the channel area of the actual switch. The voltage applied to the gate of the dummy transistor is the complement of the voltage applied to the actual switch.

Note, however, that complete compensation is not possible since the complete charge of Q_2 flows through the sampling capacitor C, whereas a portion of the charge of Q_1 only flows through C. This fraction is dependent on gate voltage waveform as well as source resistance. Improved techniques use another dummy capacitor as shown in Fig. 4.63b so that there is symmetry in the circuit. This modification also may not be adequate unless the source impedance, clock frequency, and fall time are well controlled. An attractive solution could be the use of a fully differential configuration that needs matching capacitors as shown in Fig. 4.63c and its improved version shown in Fig. 4.63d which reduces the effect of source impedances as well. Alternative techniques of mitigating charge injection have been considered before that use delayed clocks appropriately (see Fig. 4.48c).

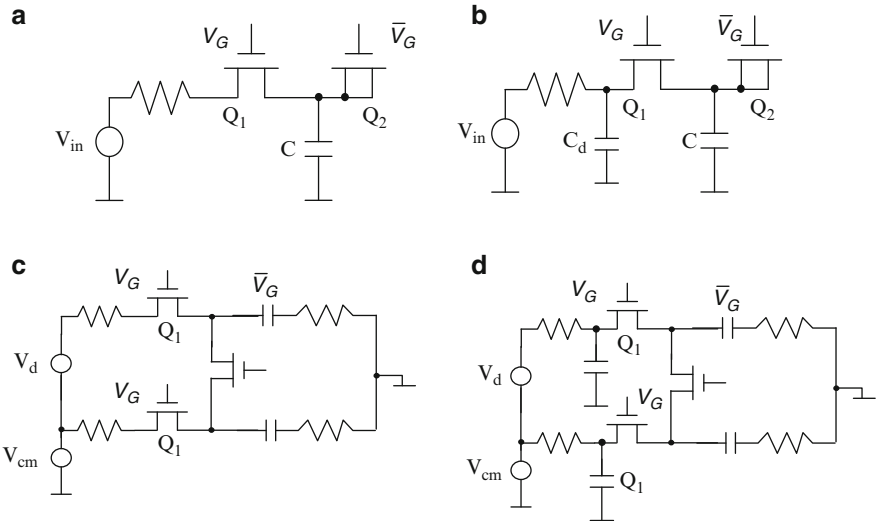


Fig. 4.63 Switch channel charge cancellation techniques: (**a**) using dummy switch, (**b**) using dummy switch and dummy capacitor, (**c**) using differential scheme, and (**d**) using dummy capacitors (Adapted from [4.103] © IEEE 1982)

There are three types of charge injection (a) due to the channel charges in strong inversion, (b) due to channel charges in weak inversion, and (c) the channel charges due to gate-to-diffusion overlap capacitance. These are considered next for a switch and a capacitor in Fig. 4.64a. In Fig. 4.64b–d we also present the waveforms at the gate, at the drain, and the current i_d through the holding capacitor C_H. The error voltage ΔV_{out} is caused by the three components and shown as Q_a, Q_b, and Q_c. The waveform has three phases; from t_1 to t_2 (the gate voltage is larger than the threshold voltage (strong inversion)), from t_2 to t_3 (the gate voltage is lower than the threshold voltage (weak inversion)). During the latter period, the conducting channel does not exist. During this period, the overlap capacitance also comes into the picture. At t_1, the transistor begins to turn off. The reader is referred to [4.109] for a detailed description of a quantitative model explaining charge injection.

4.18 SC Sigma-Delta Modulators

4.18.1 First-Order and Second-Order Modulators

The block diagram of a single-loop sigma-delta modulator (also known as oversampled A/D converter) [4.113, 4.114] is shown in Fig. 4.65a which uses a differential integrator, a comparator, a latch, and a 1-bit D/A converter in a negative feedback loop. The output stream of the latch $v_o(n)$ contains information about the

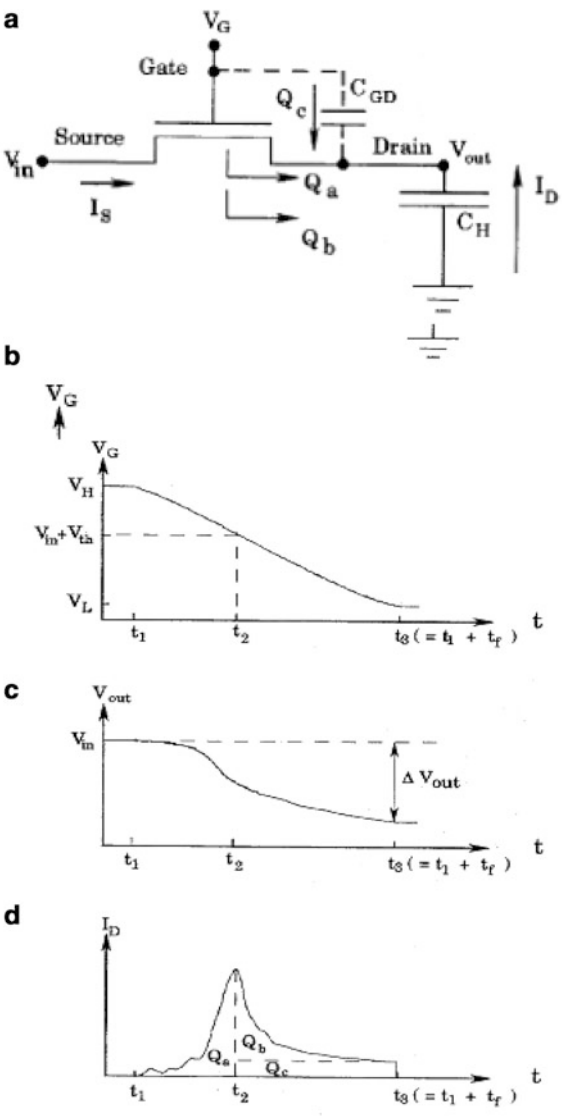


Fig. 4.64 (**a**) MOS switch and waveforms of (**b**) gate voltage, (**c**) output voltage, and (**d**) drain current (Adapted from [4.109] © IEEE 1996)

input signal. A model of Fig. 4.65a is presented in Fig. 4.65b, by representing the quantization noise as an additive white-noise source.

Sigma-delta modulators can be implemented in two ways: (a) continuous-time (CT) and (b) discrete-time (DT). The filters in the modulator will be realized in CT sigma-delta modulators using OTA-C filters or active RC filters whereas in DT sigma-delta modulators, the filters are realized using the SC technique. CT sigma-delta modulators are sometimes preferred over discrete-time sigma-delta

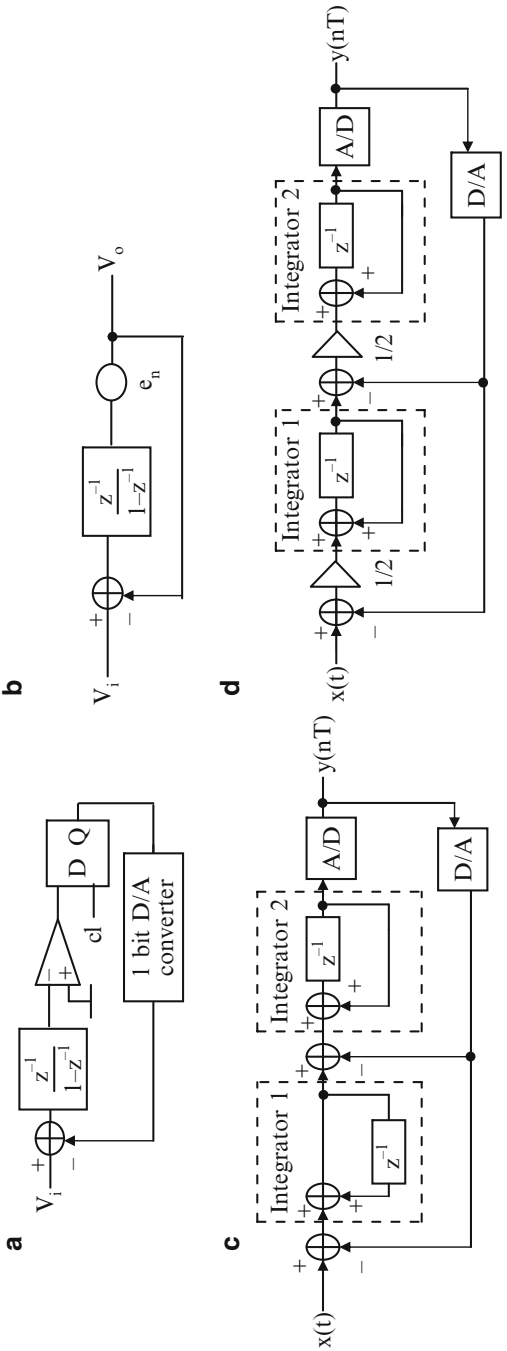


Fig. 4.65 (**a**) First-order sigma-delta modulator, (**b**) model of (a) showing quantization noise, (**c**) model of a second-order modulator, and (**d**) improved version of (c) (c and d Adapted from [4.118] © IEEE 1988)

modulators due to their lower power consumption and wide bandwidth performance in the case where high resolution is required. However, DT sigma-delta modulators are preferred for their easy implementation. Higher resolution can be obtained by increasing the order of noise shaping. The matching required in DT sigma-delta modulators is much less than that in CT modulators. Moreover, CT modulators are sensitive to jitter and process variations. On the other hand, DT sigma-delta modulators are preferred due to their robustness as the performance depends only on dependence on capacitor ratios. Moreover, they can be reconfigurable by changing the sampling frequency. In this section, we consider discrete-time sigma-delta modulators only.

Expressing the quantization noise arising out of representing the analog input signal to the comparator as a 1-bit digital output + V_{REF} or $-V_{REF}$, as e_n, the output of the sigma-delta modulator can be written as

$$V_o(z) = z^{-1}\, V_i(z) + (1 - z^{-1})\, E_n(z) \tag{4.140}$$

Evidently, the output comprises the delayed input signal together with the first-order high-pass filtered quantization noise of the 1-bit A/D converter. Thus, by low-pass filtering the output stream $v_o(n)$ of the sigma-delta modulator, the quantization noise at high frequencies can be filtered (noise spectrum can be shaped) thus retaining only the base-band input signal. The quantization noise can be reduced by using a very high sampling clock.

The main advantage of the first-order sigma-delta modulator is the non-existence of linearity errors due to the use of a single-bit quantizer. However, there can be gain and offset related errors. Note that there no need for a precision sample and hold circuit at the input. Sometimes, the first-order sigma-delta modulator can be unstable, making it lock into a mode that repeats a pattern in the output bit stream. Consequently, the spectrum of the output bit stream contains *tones*. These *tones* or *spurs* can be prevented by adding *dither* with the analog input so as to randomize the input. However, this requires another signal source to generate the dither and, moreover, the input dynamic range is lowered [4.115].

In view of the limitations of the first-order sigma-delta modulator, second-order sigma-delta modulators are attractive. A second-order sigma-delta modulator shown in Fig. 4.65c comprises two integrators in a negative feedback loop followed by a comparator (which can be seen to be an extension of the first-order sigma-delta modulator by adding an additional loop). The signal and noise transfer functions of the sigma-delta modulator of Fig. 4.65c can be derived as

$$V_o(z) = z^{-1}\, V_i(z) + (1 - z^{-1})^2\, E_n(z) \tag{4.141}$$

thus showing that a second-order high-pass transfer function for noise shaping is realized. The quantization noise in a second-order sigma-delta modulator is less correlated with the input than in a first-order sigma-delta modulator [4.115].

Several alternative architectures are proposed for realizing higher resolution than possible with second-order sigma-delta modulators. These are considered next.

Based on simulations [4.118], it has been pointed out for the second-order sigma-delta modulator of Fig. 4.65c, that the integrator output can exceed the analog input range $\Delta/2$ several times, where the two levels of the quantizer are considered as $\pm\ \Delta/2$. Hence, a modified structure shown in Fig. 4.65d is suggested. Note that each integrator is preceded by an attenuation of ½ and furthermore, the location of the delay block in each integrator is also changed. The transfer function of this sigma-delta modulator is same as that given in (4.137). It has been observed by simulation that the integrator output signal range is slightly larger than the full-scale input range. Note that in Fig. 4.65d, the multiplier ½ preceding the second integrator has no real value since the comparator is only interested in the sign of the signal.

It is possible to extend the second-order sigma-delta modulator to higher order by adding more feedback loops but it has been found that these systems are prone to instability [4.116]. Hence, alternative structures are explored which are described later.

The spectrum of the quantization noise of an Lth-order sigma-delta modulator having a noise transfer function of the type $(1 - z^{-1})^L$ can be obtained [4.117] by substituting $z = e^{j\omega T}$ as

$$S_n(\omega T) = \delta\left(2\sin\left(\frac{\omega T}{2}\right)\right)^{2L} \tag{4.142a}$$

where δ is a variable related to component mismatch or finite amplifier gain, and so on. The resolution of the converter can be estimated by first integrating the noise PSD given in (4.142a) from $\pi/(RT)$ to 0 to yield

$$\sigma_\delta^2 \frac{T}{\pi}\int_0^{\pi/(RT)}\left(2\sin\left(\frac{\omega T}{2}\right)\right)^{2L} d\omega = \frac{\pi^{2L}}{2L+1}\left(\frac{1}{R}\right)^{2L+1}\sigma_\delta^2 \tag{4.142b}$$

where R is the oversampling ratio and σ_δ is the standard deviation of δ. The resolution in bits can be written from (4.142b) in general, using a Q-bit quantizer in place of a 1-bit quantizer, as

$$bits = \left(L + \frac{1}{2}\right)\log_2 R - \log_2\left(\frac{\pi^L}{\sqrt{2L+1}}\right) + Q - 1 \tag{4.143a}$$

where Q is the number of quantizer bits. Thus every doubling of sampling frequency increases the resolution by 15 dB for a second-order sigma-delta modulator (see (4.142b)). Note also that higher resolution can be obtained for a given oversampling ratio by using high-order sigma-delta modulator (large L) or using a multibit quantizer (large Q).

The dynamic range of the sigma-delta modulator can be written from (4.142b) as

$$DR = \frac{3}{2}\frac{2L+1}{\pi^{2L}}M^{2L+1}\left(2^B - 1\right)^2 \tag{4.143b}$$

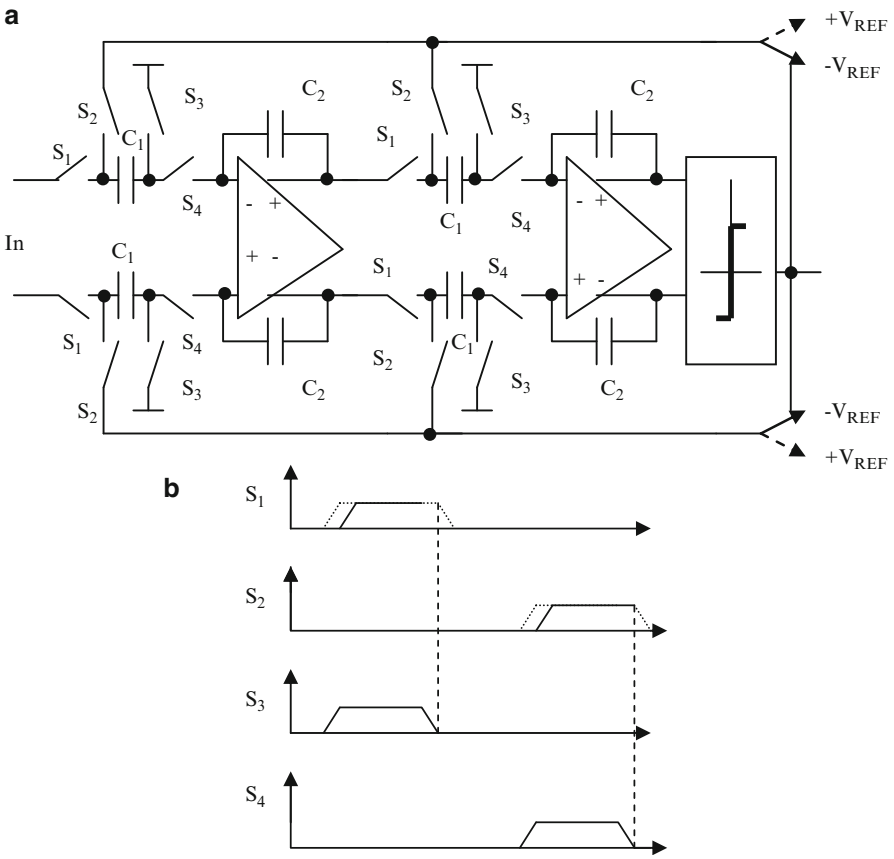


Fig. 4.66 (**a**) SC implementation of a second-order sigma-delta modulator, and (**b**) clocking waveforms (Adapted from [4.118] © IEEE 1988)

A SC implementation of the sigma-delta modulator [4.118] is shown in Fig. 4.66a. Note that this uses fully differential implementation in view of its advantages: high power supply rejection, reduced clock feedthrough, and switch charge injection errors, improved linearity, and increased dynamic range. The clocking waveforms are as shown in Fig. 4.66b. During Phase 1, switches S_1 and S_3 are closed and switches S_2 and S_4 are open. Thus, the input is sampled on capacitors C_1. In Phase 2, switches S_2 and S_4 are closed and switches S_1 and S_3 are open. Thus the output signal is subtracted from the input available on capacitors C_1 and integration is performed. Thus a half-cycle is available for the purpose of finding difference and integration.

Note that the signal-dependent charge injection is suppressed [4.118] by using the clocking arrangement of Fig. 4.66b in which the switches S_3 and S_4 are opened slightly before S_1 and S_2, respectively. Once S_3 or S_4 is opened, C_1 is floating and hence opening S_1 or S_3 during the interval when both S_3 and S_4 are open will not to a

first-order inject any charge into C_1. The switches S_3 and S_4 do not have charge injection since they are switched between ground and virtual ground. The clocks S_1 and S_3 are generated by delaying the clocks S_2 and S_4.

4.18.2 High-Order Sigma-Delta Modulators

Next we consider architectures of high-order sigma-delta modulators. A structure known as MASH (*multistage noise shaping*) [4.119] (also known as triple first-order cascade TFOC1) is presented in Fig. 4.67a which consists of three first-order sigma-delta modulators in cascade. In this structure, the quantization noise of the first first-order sigma-delta modulator is extracted by taking the difference between the input and output of the comparator. This extracted quantization noise is fed to the second first-order sigma-delta modulator and similarly, the extracted quantization noise of the second first-order sigma-delta modulator is fed to the third first-order sigma-delta modulator. The digital 1-bit output C_2 of the second first-order sigma-delta modulator is differentiated once and that of the third first-order second-order C_3 sigma-delta modulator is differentiated twice and both of these are summed with the output of the first sigma-delta modulator C_1 to obtain the desired third-order noise shaping. Note that in Fig. 4.67a, we have

$$C_1 = X z^{-1} + \left(1 - z^{-1}\right) Q_1 \tag{4.144a}$$

$$C_2 = -Q_1\, z^{-1} + \left(1 - z^{-1}\right) Q_2 \tag{4.144b}$$

$$C_3 = -Q_2\, z^{-1} + \left(1 - z^{-1}\right) Q_3 \tag{4.144c}$$

and

$$\begin{aligned} Y = {} & C_1 z^{-2} + z^{-1}\left(1 - z^{-1}\right) C_2 + \left(1 - z^{-1}\right)^2 C_3 = X z^{-3} + z^{-2}\left(1 - z^{-1}\right) \\ & Q_1 - z^{-2}\left(1 - z^{-1}\right) Q_1 + z^{-1}\left(1 - z^{-1}\right)^2 Q_2 - z^{-1}\left(1 - z^{-1}\right)^2 Q_2 + \left(1 - z^{-1}\right)^3 \\ & Q_3 = X z^{-3} + \left(1 - z^{-1}\right)^3 Q_3 \end{aligned} \tag{4.144d}$$

The computation of Y can be done digitally. Component matching as well as finite opamp gain errors, however, degrade the cancellation, leaking the quantization noise of the first and second stages to the output thus degrading the output SNR as shown later.

In another structure known as the triple first-order cascade (TFOC2) (4.69) [4.120], shown in Fig. 4.67b, the input to the quantizer of the first first-order Σ-Δ modulator is fed to the second stage and so on. Another structure known as SOFOC1 (second-order first-order cascade), in which the quantization noise of a second-order Σ-Δ modulator is fed to a first-order Σ-Δ modulator is shown in

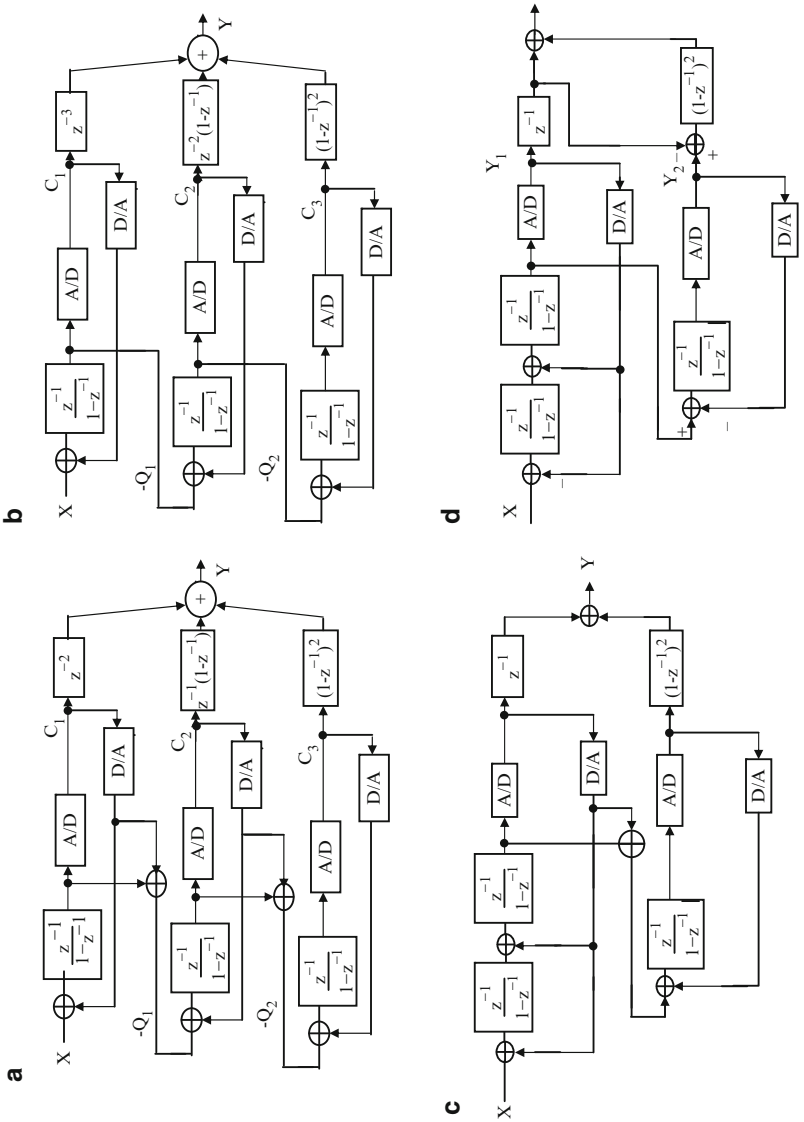


Fig. 4.67 Third-order sigma-delta modulators: (**a**) MASH (multistage noise shaping) type, (**b**) triple first-order cascade (TFOC2), (**c**) second-order first-order cascade (SOFOC1), and (**d**) SOFOC2 (Adapted from [4.117] © IEEE 1991)

Fig. 4.67c [4.121]. The second-stage output is differentiated twice so that it develops a cancellation signal component comparable to the noise of the first stage and combined to form a third-order noise shaping. Note that the leakage now is of second-order which is an improvement over the previous case where leakage of both first-order and second-order exists. The disadvantage, however, is that it overloads prematurely. Ribner [4.117] has proposed an alternative structure shown in Fig. 4.67d in which the input to the quantizer of the second-order sigma-delta modulator is fed as input to a first-order sigma-delta modulator. This circuit is tolerant to capacitor mismatch errors. It may be noted that the structures of Fig. 4.6b–d realize the same transfer function as in (4.144d).

The advantage of 2–1 architecture is that the quantization noise tones of the first stage are largely suppressed by the second stage and the remaining quantization noise is nearly white. It is also less sensitive to component mismatch than cascade third-order modulators [4.122].

Brandt and Wooley [4.123] have used a 2–1 topology shown in Fig. 4.68a for realizing a third-order sigma-delta modulator but using a multibit quantizer in the first-order sigma-delta modulator. The advantage is that the first-stage second-order noise is cancelled and the quantization noise of the second stage is attenuated by third-order noise shaping. The quantization error of the second stage comes from a multibit quantizer, thus the modulator dynamic range is improved by 20 log $(2^N - 1)$ dB where N is the resolution of the multibit quantizer. The DAC nonlinearity undergoes a second-order noise shaping. Note that $E_1(z)$ and $E_2(z)$ are the quantization errors whereas $E_D(z)$ models the errors resulting from the nonlinearity of the multibit D/A converter. The following equations describe the structure.

$$Y_1(z) = z^{-1} X(z) + (1 - z^{-1})^2 E_1(z) \tag{4.145a}$$

$$Y_2(z) = z^{-1} (E_1(z) - E_D(z)) + (1 - z^{-1}) E_2(z) \tag{4.145b}$$

$$Y(z) = z^{-1} Y_1(z) - (1 - z^{-1})^2 Y_2(z) \tag{4.145c}$$

or

$$Y(z) = z^{-2} X(z) + z^{-1} (1 - z^{-1})^2 E_D(z) - (1 - z^{-1})^3 E_2(z) \tag{4.145d}$$

The large quantization noise of the second-order first stage will overload the second stage. Hence the attenuation using α and β will be needed as shown in Fig. 4.68a. Note that α and β can be equal. Thus, the output $Y_2(z)$ needs to be scaled digitally by α^{-1} before the error cancellation logic. The complete SC structure is shown in Fig. 4.68b. Note that in this structure, both integrators have delays in the forward path as well as gain factors ½ yielding a transfer function $\frac{1}{2}\left(\frac{z^{-1}}{1-z^{-1}}\right)$. The input to the second stage is the differential output of the second-stage opamp effectively implementing $\alpha = 0.25$ and $\beta = 0$.

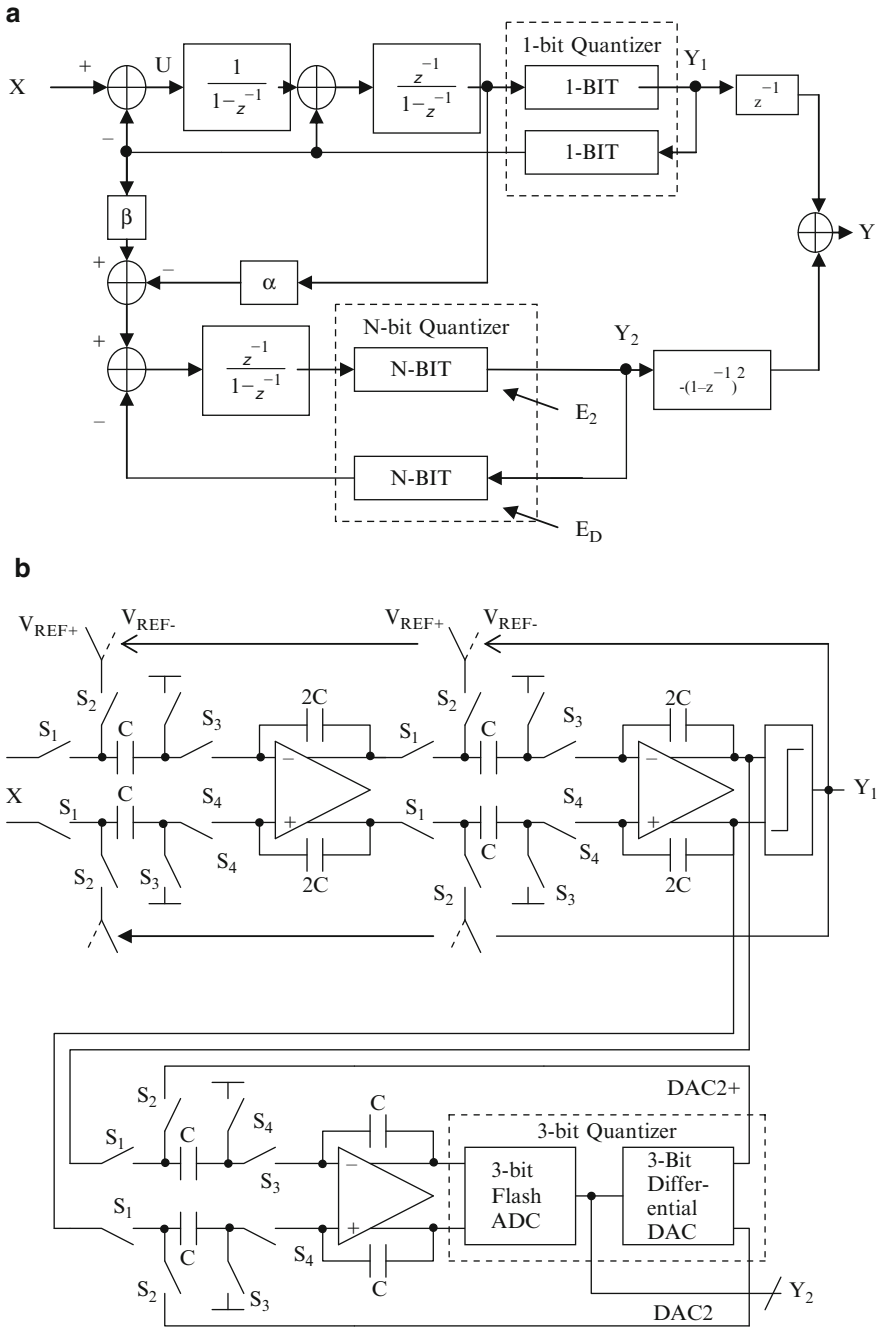


Fig. 4.68 (**a**) Cascaded multibit sigma-delta modulator, and (**b**) SC implementation (Adapted from [4.123] © IEEE 1991)

Nam et al. [4.124] have suggested a sigma-delta modulator topology denoted as *reduced integrator swing range* (RISR) topology. In this topology (shown in Fig. 4.69a) note that U_1 and V_1 no longer depend on the input voltage:

$$Y = X + (1 - z^{-1})\, E_N \tag{4.146a}$$

$$U_1 = -(1 - z^{-1})\, E_N \tag{4.146b}$$

$$V_1 = -z^{-1}\, E_N \tag{4.146c}$$

$$W_1 = X - z^{-1}\, E_N \tag{4.146d}$$

By using multibit quantization, signal ranges of U_1 and V_1 can be reduced. Smaller U_1 avoids opamp slewing and savings in power enabling the use of a single-stage opamp. Large full-scale input range can be used allowing an increase in the circuit noise floor. Note that W_1 can still be large, but since it precedes the quantizer, it is not problematic. A second-order sigma-delta modulator using this approach is presented in Fig. 4.69b.

The equations describing its behavior are as follows.

$$Y = X + (1 - z^{-1})^2\, E_N \tag{4.147a}$$

$$U_1 = -(1 - z^{-1})^2\, E_N \tag{4.147b}$$

$$V_1 = -z^{-1}\,(1 - z^{-1})\, E_N \tag{4.147c}$$

$$V_2 = -z^{-2}\, E_N \tag{4.147d}$$

$$W_1 = X + z^{-1}\,(z^{-1} - 2)\, E_N \tag{4.147e}$$

Note that the output Y is composed of nondelayed X and the second-order difference of the quantization error E_N. The integrator inputs and outputs U_1,V_1, and V_2 are independent of the modulator input X thereby preserving the advantage cited for the first-order modulator.

The RISR sigma-delta modulator maintains a very small integrator input and output signals across the full modulator input range whereas other topologies show a significant increase in the integrator signals at large input levels. Furthermore, also as a function of the oversampling ratio, the same results hold good. A fourth-order sigma-delta modulator based on RISR is presented in Fig. 4.69c. A SC implementation of the first stage is as shown in Fig. 4.69d together with the switch timing waveforms. Note that in order to improve the linearity of the D/A converter, rotational data-weighted-averaging (DWA) technique is used. The 5-bit output of the A/D converter is converted into analog using the capacitors C_{s1j}. The pulses driving S_{4Pj} and S_{4Nj} are generated by gating the ϕ_2 phase clock with the control signals generated by the DWA logic.

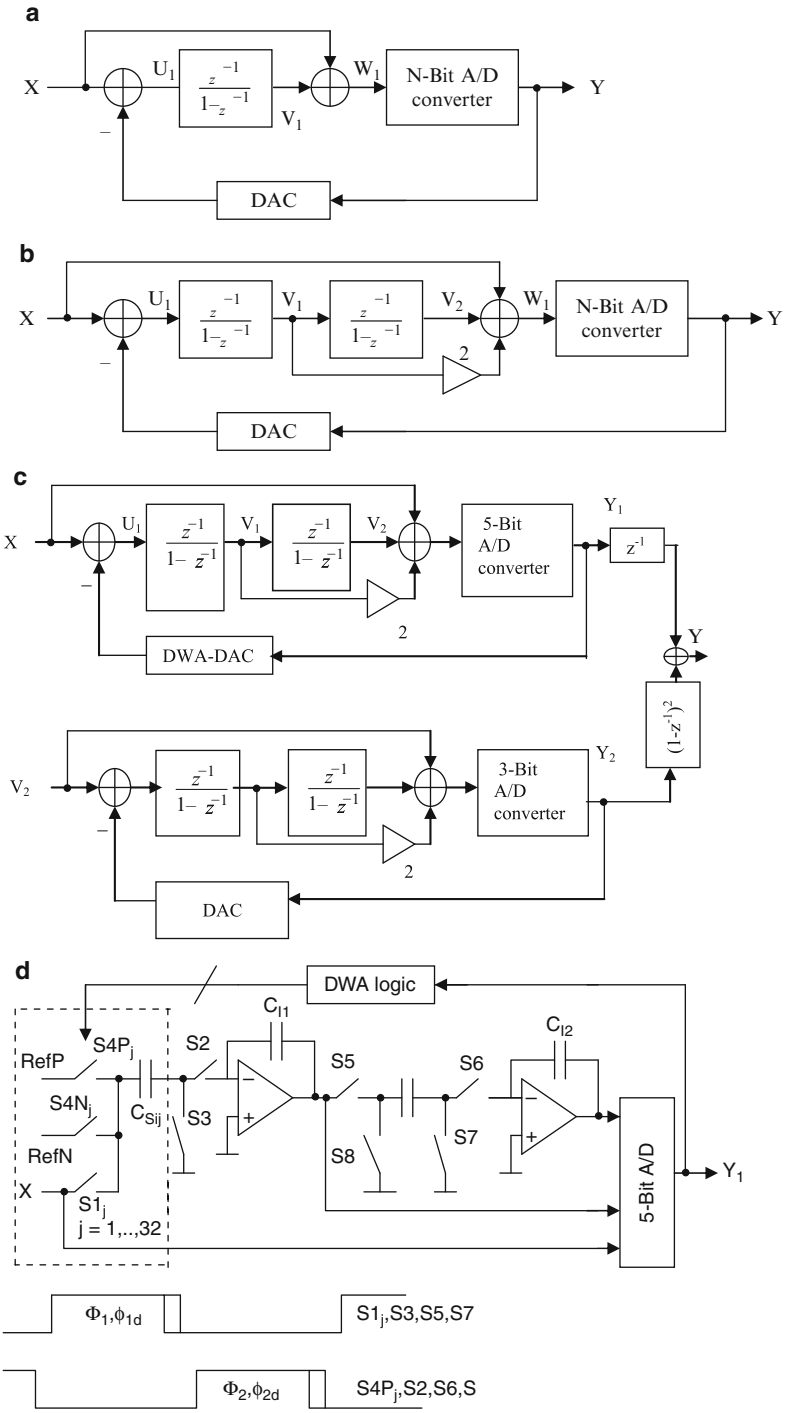


Fig. 4.69 (**a**) First-order RISR modulator, (**b**) second-order RISR modulator, (**c**) fourth-order sigma-delta modulator based on (b), and (**d**) SC implementation of the first stage (Adapted from [4.124] © IEEE 2005)

The first integrator in a sigma-delta modulator usually is the largest contributor in the overall power consumption. Errors in the first stage are not filtered by the loop. Hence the first integrator must be designed to meet the overall dynamic range requirements. By reducing the sampling rate in the first stage, power consumption can be decreased and the resulting loss in resolution can be recovered by increasing the sampling rate in the succeeding stages. Hence multirate processing has been suggested [4.125]. However, this needs additional hardware in the feedback path to perform decimation. A block diagram of a multirate architecture is presented in Fig. 4.70a which is a 2–1 cascade with the first stage operating at a lower sampling rate than the second stage. In this architecture, the first stage operates at a sampling frequency F_{s1} and the second at the sampling rate $F_{s2} = NF_{s1}$. An up-sampler is introduced in the second stage to increase the sampling rate to NF_{s1}. The output streams of both stages are digitally combined and can either use decimation for the second stream or interpolation for the first stream. The first option is presented in Fig. 4.70a. The authors used a RISR topology and use 1.5-bit quantizers (three-level DAC) to reduce the output swing of the first integrator. The complete implementation is as shown in Fig. 4.70b. The outputs Y_1 and Y_2 can be derived as

$$Y_1(z) = \frac{b_1}{a_1} z^{-2} X_1(z) + m_2 z^{-1}(1 - z^{-1}) X_1(z) + (1 - z^{-1})^2 E_1(z) \quad (4.148a)$$

$$Y_2(z) = \frac{b_3}{a_3} z^{-1} H_{Ups} X_2(z^N) + (1 - z^{-1}) E_2(z) \quad (4.148b)$$

with

$$\begin{aligned} X_2(z) &= \frac{Y_1(z) - E_1(z)}{k_{q1}} - \frac{c_3}{b_3} Y_1(z) \\ &= b_2 a_1 (Y_1(z) - E_1(z)) - \frac{c_3}{b_3} Y_1(z) \end{aligned} \quad (4.148c)$$

Note that the up-sampling filter is described by the digital transfer function

$$H_{Ups}(z) = 1 + \ldots + z^{-N+1} \quad (4.149)$$

and k_{q1}, k_{q2} are the gains of the quantizers, $E_1(z), E_2(z)$ are the quantization noises of the first and second stages, and $X_1(z)$ and $X_2(z)$ are the input signals of the first and second stages, respectively. For achieving second-order noise shaping in the first stage and first-order noise shaping in the second stage, the following relationships need to be met.

$$b_2 a_1 k_{q1} = 1, \; a_2 = 2 b_1 b_2 \text{ and } a_3 k_{q2} = 1 \quad (4.150)$$

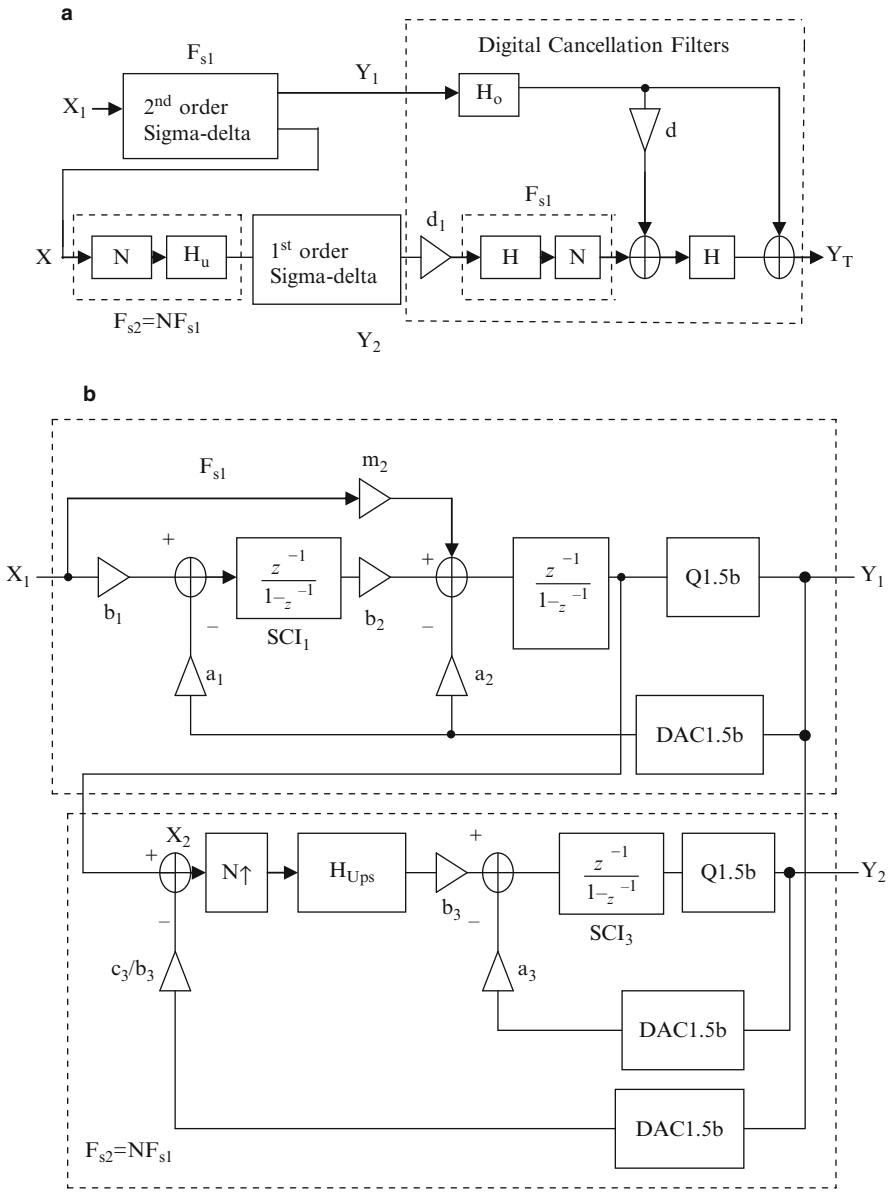


Fig. 4.70 (**a**) Architecture of a multirate 2–1 cascade sigma-delta modulator with digital cancellation filters, and (**b**) circuit implementation of (a) (Adapted from [4.125] © IEEE 2010)

After up-sampling the digital output of the first stage and processing both streams in the cancellation filter, the output obtained is given as

$$Y_{out}(z) = H_{d1}(z)(1 + ... + z^{-N+1})\, Y_1(z^N) + H_{d2}(z)\, Y_2(z) \tag{4.151}$$

By choosing

$$H_{d1}(z) = z^{-1}\left(d_0\ (1 - z^N)^2 + 1\right) \tag{4.152a}$$

$$H_{d2}(z) = d_1\ (1 - z^N)^2 \tag{4.152b}$$

with

$$d_o = \frac{c_3}{b_3\ b_2\ a_1} - 1 \text{ and } d_1 = \frac{a_3}{b_3\ b_2\ a_1} \tag{4.152c}$$

the final output of the cascade can be written as

$$\begin{aligned} Y_{tot}(z) = {} & H_{Ups}(z)\, z^{-(N+1)} \left(\frac{b_1}{a_1}\, z^{-N} + m_2\ (1 - z^{-1})^N\right) X_1(z) \\ & + d_1\ (1 - z^{-N})^2 \left(1 - z^{-1}\right) E_2(z) \end{aligned} \tag{4.153}$$

Evidently, perfect cancellation of $E_1(z)$ is realized.

In multibit sigma-delta modulators, the input to the integrator is small and hence the linear settling of the opamp is dominant. The limitation of multibit modulators is the increase in sampling delay in the outer feedback path.

Fourth-order cascade SC sigma-delta modulators can be derived based on a 2–2 architecture or 2-1-1 architecture [4.126], and are presented in Fig. 4.71a, b.

The outputs of both these modulators can be expressed as

$$Y_{2-2}(z) = X(z)\, z^{-4} + d_1^2\ (1 - z^{-1})^4\ E_2(z) \tag{4.154a}$$

and

$$Y_{2-1-1}(z) = X(z)\, z^{-4} + d_3^2\ (1 - z^{-1})^4\ E_3(z) \tag{4.154b}$$

under the conditions

$H_1(z) = z^{-2}, H_2(z) = (1 - z^{-1})^2$ for the architecture of Fig. 4.71a and $H_1(z) = z^{-1}, H_2(z) = (1 - z^{-1})^2, H_3(z) = z^{-1}, H_4(z) = (1 - z^{-1})^3$ in the case of the architecture of Fig. 4.71b. In addition, the following conditions need to be satisfied for the analog and digital coefficients.

2–2 Modulator:

$$\begin{aligned} & g'_1 = g_1, g'_2 = 2\, g_2\ g'_1, g'_4 = 2\, g_4\ g'_3, \\ & d_0 = 1 - \frac{g'_3}{g_1\ g_2\ g_3}, d_1 = \frac{g''_3}{g_1\ g_2\ g_3} \end{aligned} \tag{4.155a}$$

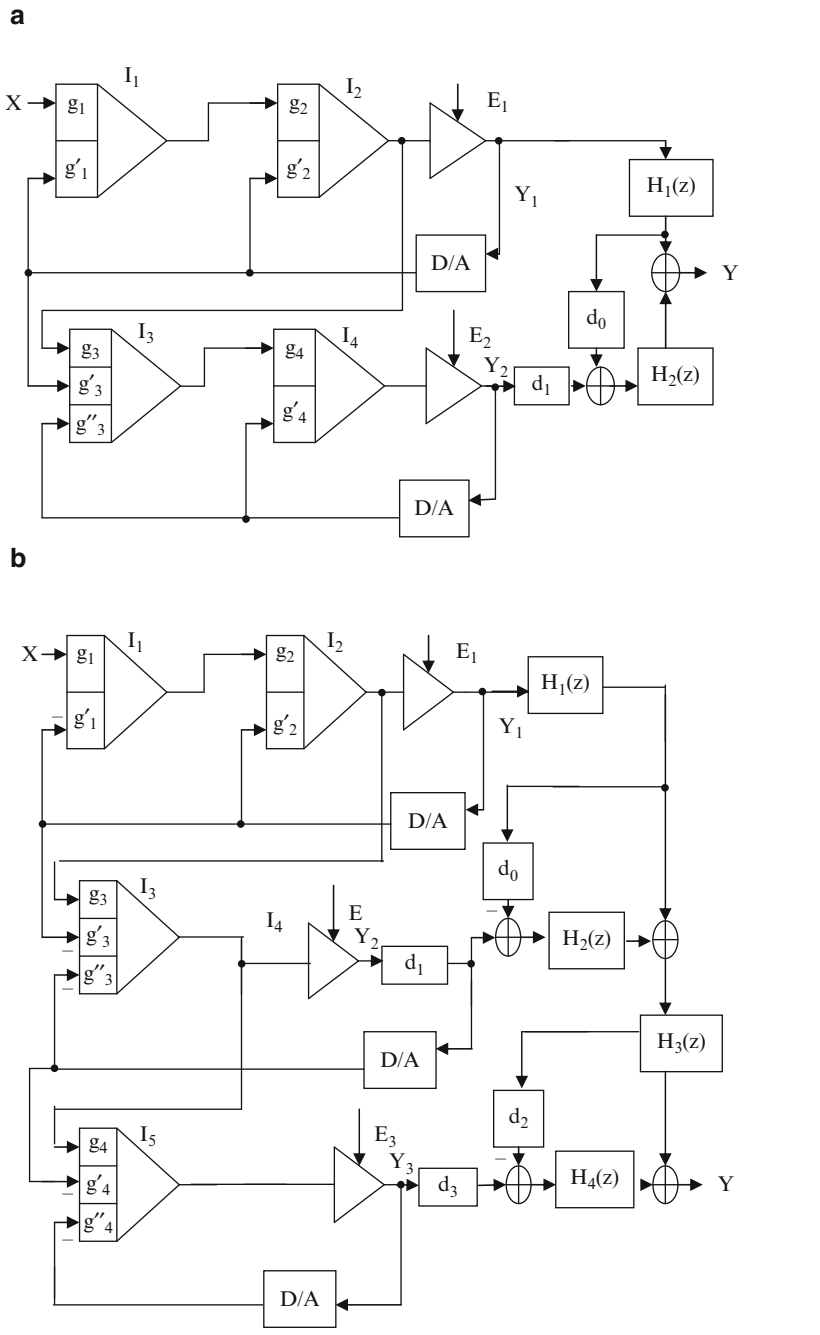


Fig. 4.71 (**a**) Two-stage fourth-order cascade sigma-delta modulator (2–2), and (**b**) three-stage fourth-order cascade sigma-delta modulator (Adapted from [4.126] © IEEE 1998)

For 2-1-1 modulator:

$$g'_1 = g_1, g'_2 = 2\,g_2\;g'_1, g'_4 = g_4\;g''_3, d_0 = 1 - \frac{g'_3}{g_1\;g_2\;g_3}, d_1 = \frac{g''_3}{g_1\;g_2\;g_3},$$
$$d_2 = \left(1 - \frac{g'_3}{g_1\;g_2\;g_3}\right)\left(1 - \frac{g'_4}{g''_3\,g_4}\right), d_4 = \frac{g''_4}{g_1\;g_2\;g_3\;g_4} \tag{4.155b}$$

The authors have shown that the optimization of coefficients is possible for realizing minimum quantization noise and to ensure that intermediate signal levels do not overload the next modulator. Medeiro et al. [4.126] have also observed that the 2–2 modulator is less sensitive to mismatches than the 2-1-1 modulator. They have also extended the structures of Fig. 4.71 using multibit quantizers in place of single-bit quantizers.

A second-order sigma-delta modulator using a resonator is presented in Fig. 4.72a [4.127]. The resonator realizes in-band zeroes so that the quantization noise can be suppressed and SNR can be improved. The authors also used tri-level quantization which avoids the use of DWA. In addition, the RISR concept is used to reduce the signal swing and suppress distortion caused by integrator nonlinearities.

The signal and noise transfer functions of this second-order sigma-delta modulator of Fig. 4.72a can be derived as

$$NTF = \frac{1 - 2\,z^{-1} + (1 + r)\,z^{-2}}{1 - (2 - k_q\,c)\,z^{-1} + (1 + r + k_q\,(d - c))\,z^{-2}} \tag{4.156a}$$

and

$$STF = \frac{k_q\,(1 - (2 - d)\,z^{-1} + (1 + r + c - d)\,z^{-2})}{1 - (2 - k_q\,c)\,z^{-1} + (1 + r + k_q\,(d - c))\,z^{-2}} \tag{4.156b}$$

where $c = g_1\;a_1, d = g_1\;g_2\;a_2, r = g_1\;g_2\;b_1$. Note that r is the loop gain of the resonator and k_q is the gain of the quantizer.

Fourth-order sigma-delta modulators can be derived based on 2–2 (RMASH2-2) and 2-1-1 (RMASH 2-1-1) architecture as shown in Fig. 4.72b, c. The digital transfer functions needed in the case of 2-1-1 architecture are as follows.

$$H_1(z) = 1 - 2z^{-1} + (1 + r)\,z^{-2},$$
$$H_2(z) = (1 - z^{-1})(1 - 2\,z^{-1} + (1 + r)\,z^{-2}) \tag{4.157}$$

The noise transfer function $Y(z)/Q_3(z)$ can be derived as

$$\frac{Y(z)}{Q_3(z)} = d_2\,(1 - 2\,z^{-1} + (1 + r)\,z^{-2})\,(1 - z^{-1})^2 \tag{4.158}$$

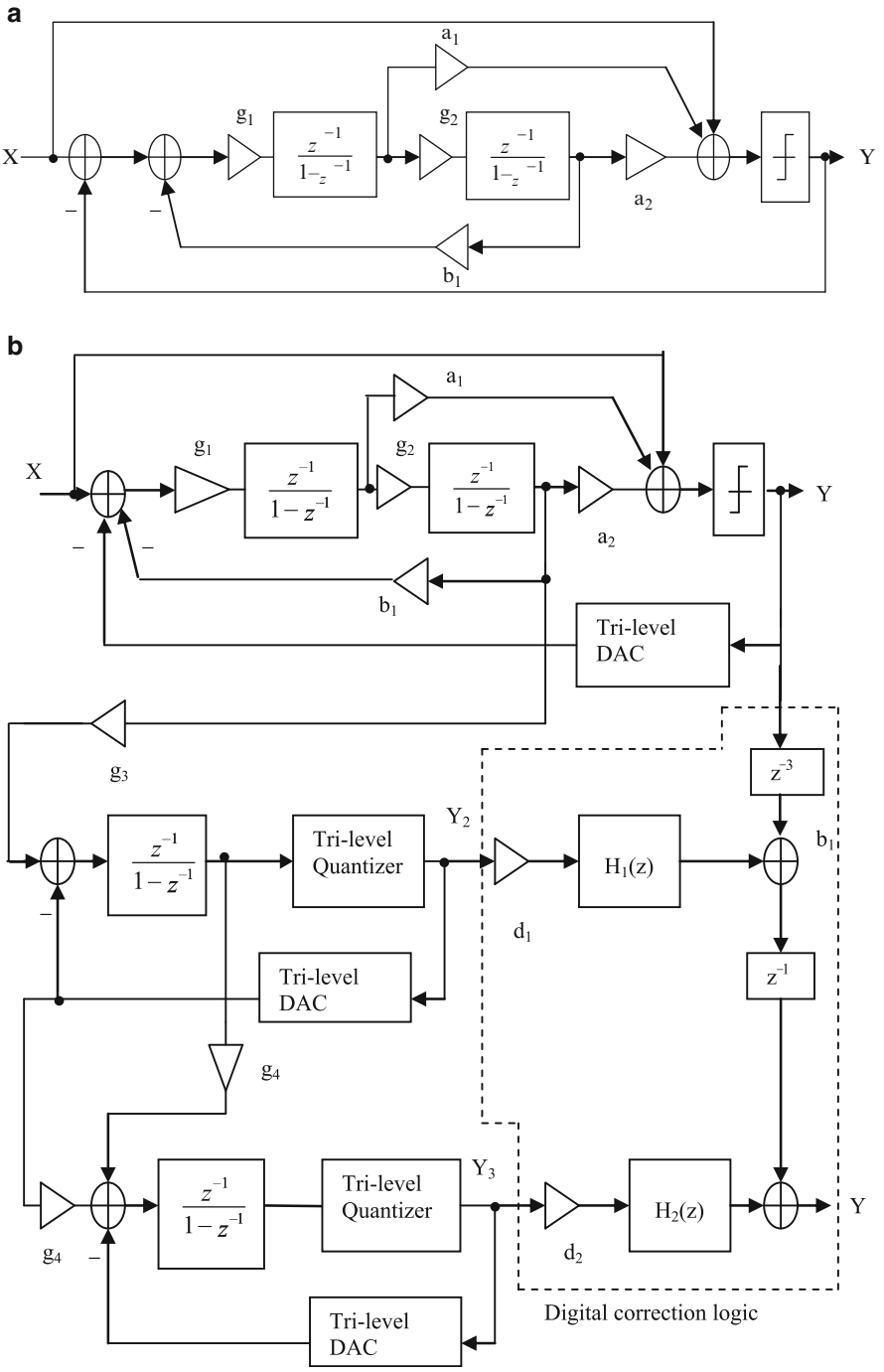


Fig. 4.72 (**a**) Resonator-based second-order 1.5b ΣΔ modulator, (**b**) fourth-order RMASH architecture based on a 2-1-1 configuration, and (**c**) based on 2–2 configuration (Adapted from [4.127] © IEEE 2008)

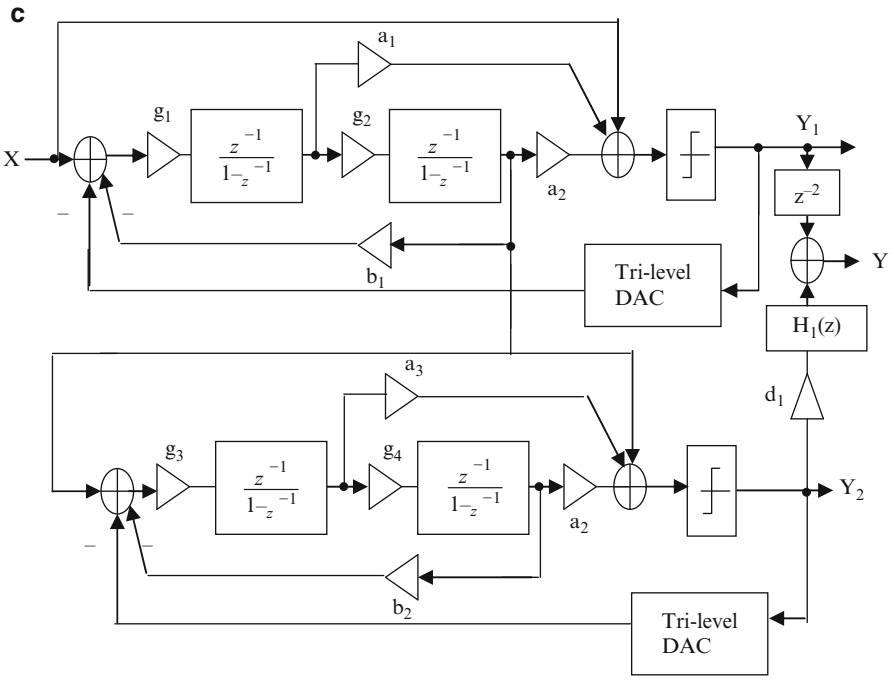


Fig. 4.72 (continued)

where $d_2 = 1/(g_1g_2g_3g_4)$. Note that SNR can be improved by tuning the parameters d_2, r, and $Q_3(z)$. With careful selection of the resonator loop gain r, the zeroes can be placed near the edge of the signal band to suppress the quantization noise over the desired signal band.

A high-order topology using a single quantizer has been proposed by Chao et al. [4.128]. In this structure (shown in Fig. 4.73), the signal and noise transfer functions can be realized independently. The feedforward coefficients $A_0, A_1, \ldots, A_N$ and feedback coefficients $B_0, B_1, \ldots, B_N$ need to be appropriately chosen. The realized signal and noise transfer functions are, respectively, as follows.

$$H_x(z) = \frac{\sum_{i=0}^{N} A_i\,(z-1)^{N-i}}{z\left[(z-1)^N - \sum_{i=1}^{N} B_i\,(z-1)^{N-i}\right] + \sum_{i=0}^{N} A_i\,(z-1)^{N-i}} \tag{4.159a}$$

and

$$H_E(z) = \frac{(z-1)^N - \sum_{i=1}^{N} B_i\,(z-1)^{N-i}}{z\left[(z-1)^N - \sum_{i=1}^{N} B_i\,(z-1)^{N-i}\right] + \sum_{i=0}^{N} A_i\,(z-1)^{N-i}} \tag{4.159b}$$

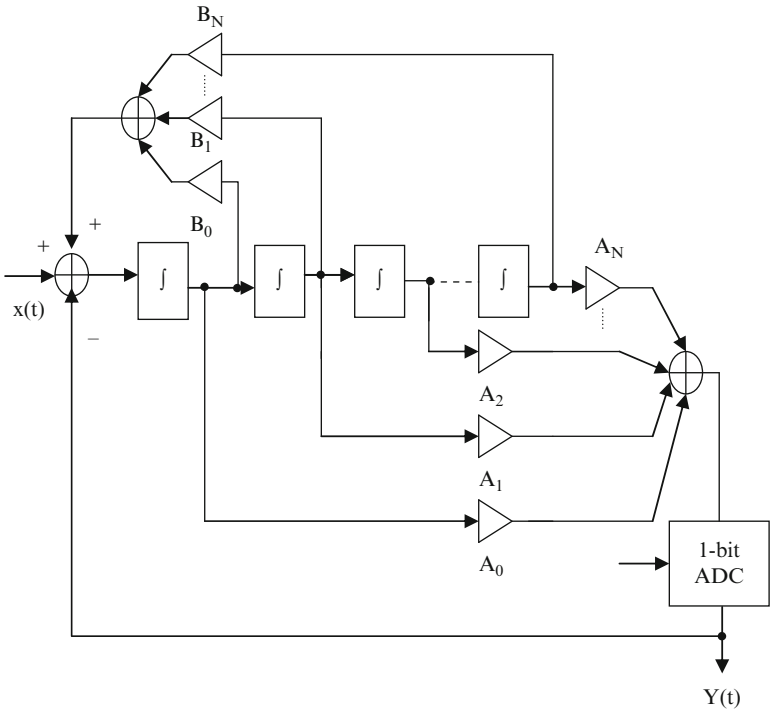


Fig. 4.73 *N*th order ΣΔ modulator topology with feedforward and feedback coefficients (Adapted from [4.128] © IEEE 1990)

Stability requirements dictate that the realized poles are within the unit circle. Absolute control over location of poles will allow optimization of the loop response for maximum effective resolution. The limited input range of the quantizer places further restriction on the design of the loop filter. A signal at the input of the quantizer that exceeds the quantizer limits leads to an increase in quantization noise $|E(z)|$. The excess noise is circulated through the loop and causes an even larger signal to appear at the quantizer input, eventually causing instability. For a fourth-order loop, through simulations Chao et al. [4.128] have observed that $|H_E(z)| < 2$ for $|z| = 1$ at high frequencies is a necessary condition for stable operation with zero input. This condition is known as *Lee's rule*.

The poles can be first computed in the *s*-domain, say for a Butterworth-type of response and using bilinear transformation mapped to the *z*-domain so that the A_is can be determined by setting all B_is to zero. The B_i coefficients can next be determined to move the zeroes from $z = 1$ away. The reader is referred to Chao et al. [4.128] for more information.

Hamoui and Martin [4.129] have proposed a sigma-delta modulator architecture presented in Fig. 4.74a. The realized noise transfer function will be of the form

$$NTF = (1 - z^{-1})^{L-2}(1 - \delta z^{-1} + z^{-2}) \tag{4.160}$$

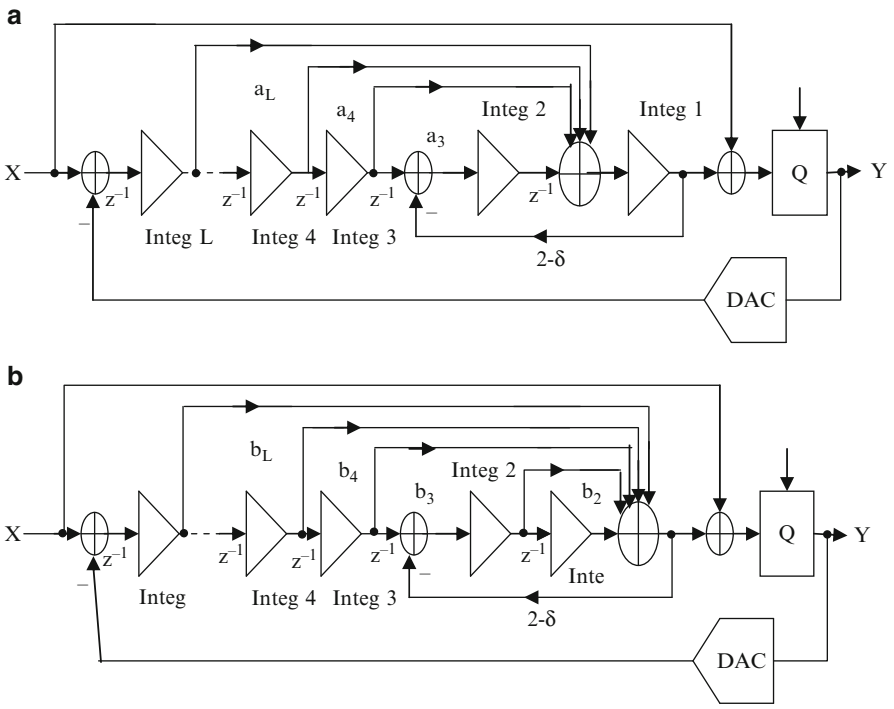


Fig. 4.74 (**a**) Hamoui and Martin sigma-delta modulator architecture, and (**b**) conventional high-order sigma-delta modulator architecture (Adapted from [4.129] © IEEE 2004)

The result is a high-pass notch characteristic having a notch frequency f_o given by

$$\delta = 2\cos(2\pi f_o / f_s) \tag{4.161}$$

Note that the signal transfer function (STF) realized is one. This configuration is feasible for order of the modulator greater than three. The complex conjugate transmission zeroes are realized by the last two-integrator loop. The a_3, a_4, and a_5 values for orders $L = 3$, 4, and 5 are, respectively, as follows.

$$L = 3 : a_3 = \delta + 1$$

$$L = 4 : a_3 = 2 \text{ and } 2z^{-1},\ a_4 = \delta + 2$$

$$L = 5 : a_3 = 5,\ a_4 = 5 \text{ and } a_5 = \delta + 3$$

It has been observed by Hamoui and Martin [4.129] that the capacitor spread required is low for this architecture. Furthermore, the circuit enjoys low sensitivity to modulator coefficients. The use of summer before the last integrator overcomes the need for summer before the quantizer in other architectures, for example, as shown in Fig. 4.74b. This architecture can realize modulators for $L \geq 2$ and needs the following coefficient values.

$$L = 2 : b_1 = \delta - 1,\ b_2 = \delta$$

$$L = 3 : b_1 = \delta^2 - \delta - 1,\ b_2 = \delta^2 - 1,\ b_3 = \delta + 1$$

$$L = 4 : b_1 = \delta^3 - \delta^2 - 2\delta - 1,\ b_2 = \delta^3 - 2,\ b_3 = \delta^2 + \delta,\ b_4 = \delta + 2$$

$$L = 5 : b_1 = \delta^4 - \delta^3 - 3\delta^2 + 2\delta + 1,\ b_2 = \delta^4 - 3\delta^2 + 1,\ b_3 = \delta^3 + \delta^2 - \delta,$$
$$b_4 = \delta^2 + 2\delta + 2,\ b_5 = \delta + 3$$

4.18.3 Practical Considerations in the Design of Sigma-Delta Modulators

There can be several nonidealities in the actual SC implementation of the sigma-delta modulator. These are briefly considered next.

4.18.3.1 Jitter in the Sampling Clock

There can be jitter in the sampling clock used in the sigma-delta modulator. Sampling clock jitter causes nonuniform sampling and increases the total error power in the quantizer output. The effect of this jitter can be estimated as follows [4.118, 4.130, 4.131]. Considering a sine wave of amplitude A and frequency f_s, the error since of sampling of a signal $x(t)$ at $(t + \delta)$ instead of (t) is

$$x(t + \delta) - x(t) = 2\pi f_s A\delta \cos(2\pi f_s t) = \delta \frac{d}{dx} x(t) \tag{4.162}$$

The sampling uncertainty δ in the clock edge can be considered as a random process with standard deviation Δt yielding from (4.162) the power of this error signal due to jitter as

$$S_\delta = \frac{A^2}{2} (2\pi f_x \Delta t)^2 \tag{4.163a}$$

The in-band error power can be estimated by noting that the decimation filter following the sigma-delta modulator limits the noise at frequencies above this band. Noting that the maximum A can be $\Delta/2$ and denoting f_x as B the bandwidth of the signal, the in-band error power can be found as

$$S_{\Delta t} \leq \frac{\Delta^2}{8} \frac{(2\pi B \Delta t)^2}{M} \tag{4.163b}$$

Since the clock jitter is assumed to be white, the total power of the error in the decimation process is reduced by M, the oversampling ratio. Evidently, the noise

power due to jitter is inversely proportional to the oversampling ratio and adds to the quantization noise power. It is independent of the architecture of the sigma-delta modulator [4.131].

The static nonidealities that need to be considered are the finite opamp gain and capacitor matching.

4.18.3.2 Power Dissipation

The first integrator dominates the power dissipation since it is limited by the *kT/C* noise and must settle to the accuracy of the overall modulator independent of the oversampling ratio used [4.94].

The noise power within the base-band introduced by the first integrator is given by

$$S_{kT/c} = \frac{4kT}{M\,C_s} \tag{4.164a}$$

where C_s is the sampling capacitance. The factor 4 arises considering a fully differential circuit and two paths through which noise is sampled in ϕ_1 and ϕ_2.

The dynamic range DR is expressed as

$$DR = \frac{S_s}{S_{kT/c}} = \frac{V_{sw}^2\,M\,C_s}{8kT} \tag{4.164b}$$

The power dissipation of the SC integrator is

$$P = I_{amp}\ V_{DD} \tag{4.165a}$$

where I_{amp} is the average amplifier current. The quiescent current of the opamp must be sufficient so that the load capacitor can be charged to the worst case output voltage within the integration period (half a clock period T_s). Thus, we have

$$I_{amp} = \frac{C_I\ \Delta V_{out}}{\frac{T_s}{2}} \tag{4.165b}$$

where ΔV_{out} is the worst-case differential step change in the output voltage. Next, we note that

$$\Delta V_{out} = (V_{sw} + V_{ref})\frac{C_S}{C_I} \tag{4.165c}$$

where V_{sw} is the input voltage. Using (4.165b) and (4.165c), and noting that $T_s = \frac{1}{f_s}$ $= \frac{1}{Mf_N}$ with f_s as the sampling frequency, M is the oversampling ratio and f_N is the Nyquist sampling rate, we obtain

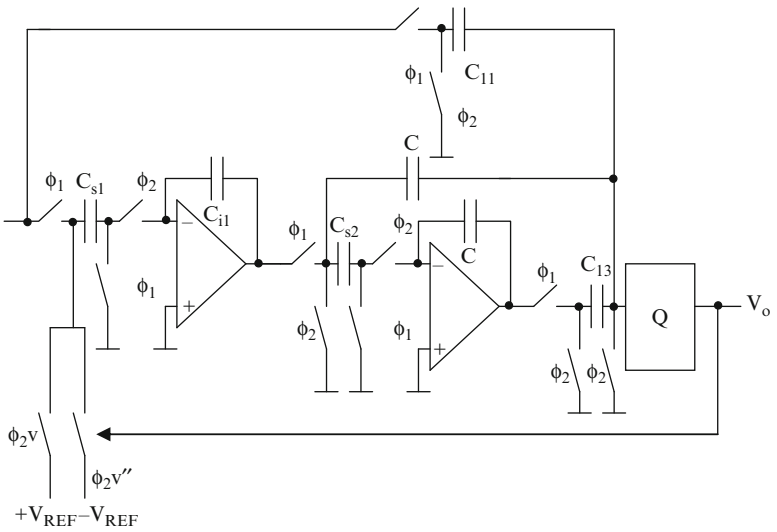


Fig. 4.75 Schematic of SC sigma-delta modulator using feedforward (Adapted from [4.97] © IEEE 2005)

$$I_{amp} = 2\,C_S\,M f_N\,(V_{sw} + V_{ref}) \tag{4.165d}$$

Thus, the power dissipation can be written as

$$P = 16kT(DR) f_N\,\frac{V_{DD}\,(V_{sw} + V_{ref})}{V_{sw}^2} \tag{4.166a}$$

Assuming that V_{sw} and V_{ref} are full rail signals, (4.166a) reduces to

$$P = 32kT(DR) f_N \tag{4.166b}$$

It is important to note that the power dissipation is proportional to the dynamic range and Nyquist sampling rate (i.e., bandwidth of the signal) and is independent of the oversampling ratio.

4.18.3.3 Noise

SC sigma-delta modulators are affected by the thermal noise arising from the finite switch on-resistance and thermal and 1/*f* noise of the OTA used to realize the SC integrator during the sampling and integration phases.

Schreier et al. [4.97] have presented a procedure for noise estimation of sigma-delta modulators. Consider the second-order SC sigma-delta modulator shown in Fig. 4.75. There are five thermal noise sources due to the five SC branches. There

are two opamps. The mean square value of the input referred noise of the first integrator has already been derived in (4.120) and is reproduced for convenience:

$$\overline{v_{n1}^2} = \left(\frac{kT}{C_{s1}}\right)\frac{7/3 + 2x}{1 + x} \tag{4.167a}$$

The noise at the output of the first integrator can be obtained from (4.113b) taking into account the total capacitive load C_{o1} as

$$\overline{v_{no1}^2} = \frac{4}{3}\frac{kT}{C_{o1}} \tag{4.167b}$$

where $C_{o1} = C_{s2} + \frac{C_{f2}(C_{f1}+C_{f3})}{C_{f1}+C_{f2}+C_{f3}}$. The noise voltages at the input and output of the second integrator can be obtained in a similar manner. The noise contribution of three SC branches at the input of the quantizer can be combined to yield the noise power as

$$\overline{v_{n3}^2} = \frac{2kT}{C_{f1}}\left(1 + \frac{C_{f2}}{C_{f1}} + \frac{C_{f3}}{C_{f1}}\right) = \frac{2kT}{C_{f1}}(1 + 2 + 1) = \frac{8kT}{C_{f1}} \tag{4.167c}$$

Next the noise transfer functions of these five noise sources to the output of the modulator need to be estimated. These are, respectively, as follows.

$$\begin{aligned} &NTF_{i1}(z) = 2z^{-1} + z^{-2}, NTF_{o1}(z) = (1 - z^{-1})(2 - z^{-2}), \\ &NTF_{i2}(z) = z^{-1}(1 - z^{-1}), NTF_3(z) = NTF_{o2}(z) = 2(1 - z^{-1})^2 \end{aligned} \tag{4.168}$$

The noise PSDs need to be multiplied by the respective squared magnitudes of the noise transfer functions and integrated over the base-band to obtain the following results.

$$\overline{N_{i1}^2} = \overline{v_{ni1}^2}\left(\frac{5}{M} - \frac{4}{\pi}\sin\left(\frac{\pi}{M}\right)\right) \tag{4.169a}$$

$$\overline{N_{o1}^2} = \overline{v_{no1}^2}\left(\frac{14}{M} + \frac{4}{\pi}\sin\left(\frac{\pi}{M}\right)\cos\left(\frac{\pi}{M}\right) - \frac{18}{\pi}\sin\left(\frac{\pi}{M}\right)\right) \tag{4.169b}$$

$$\overline{N_{i2}^2} = \overline{v_{ni2}^2}\left(\frac{2}{M} - \frac{2}{\pi}\sin\left(\frac{\pi}{M}\right)\right) \tag{4.169c}$$

$$\overline{N_3^2} = (\overline{v_{no2}^2} + \overline{v_{n3}^2})\left(\frac{6}{M} - \frac{8}{\pi}\sin\left(\frac{\pi}{M}\right) + \frac{2}{\pi}\sin\left(\frac{\pi}{M}\right)\cos\left(\frac{\pi}{M}\right)\right) \tag{4.169d}$$

For large M, the above equations can be simplified as

$$\overline{N_{i1}^2} = \frac{\overline{v_{ni1}^2}}{M},\ \overline{N_{o1}^2} = \overline{v_{no1}^2}\frac{\pi^2}{3M^3},\ \overline{N_{i2}^2} = \overline{v_{ni2}^2}\frac{\pi^2}{3M^3},\ \overline{N_3^2} = (\overline{v_{no2}^2} + \overline{v_{n3}^2})\frac{\pi^4}{5M^5} \quad (4.170)$$

It is important to reduce the noise of the first stage (kT/C noise) in a sigma-delta modulator which may necessitate the use of large capacitances. The use of the large oversampling ratio M also reduces the thermal noise. The SNR of the sigma-delta modulator can be expressed as

$$SNR = \frac{S}{N_C + N_Q} \quad (4.171)$$

where N_C is the circuit noise and N_Q is the quantization noise.

4.18.3.4 Bandwidth and Slew Rate of Opamp/OTA

The effects of finite bandwidth and slew rate are related to each other and may be interpreted as nonlinear gain [4.130]. These lead to incomplete charge transfer. During the integration period, the behavior of the integrator can be seen from the equation:

$$v_o(t) = v_o(nT_s - T_s) + \alpha V_s(1 - e^{-t/\tau}),\ 0 < t < \frac{T_s}{2} \quad (4.172a)$$

where $V_s = V_{in}(nT_s - T_s/2)$, α is the integrator leakage (which accounts for opamp finite gain), and $\tau = 1/(2\pi B)$ is the time constant of the integrator and B is the bandwidth of the opamp. The slope of this curve reaches its maximum value when $t = 0$ and is

$$\frac{d}{dt} v_o(t)|_{\max} = \alpha\frac{V_s}{\tau} \quad (4.172b)$$

If the slew rate SR of the opamp is greater than the slope given in (4.172b), no SR limitation appears. On the other hand, if the SR of the opamp is less than the slope given by (4.172b), the opamp is slewing and hence, the first part of the transient $v_o(t < t_o)$ is linear with slope SR. The following equations apply.

$$t \le t_o, v_o(t) = v_o(nT_s - t_s) + SRt \quad (4.173a)$$

$$t > t_o, v_o(t) = v_o(t_o) + (\alpha V_s - SR\, t_o)(1 - e^{-(t-t_o)/\tau}) \quad (4.173b)$$

The slew rate and bandwidth limitations produce harmonic distortion reducing the total SDNR (signal-to-distortion noise ratio) of the sigma-delta modulator.

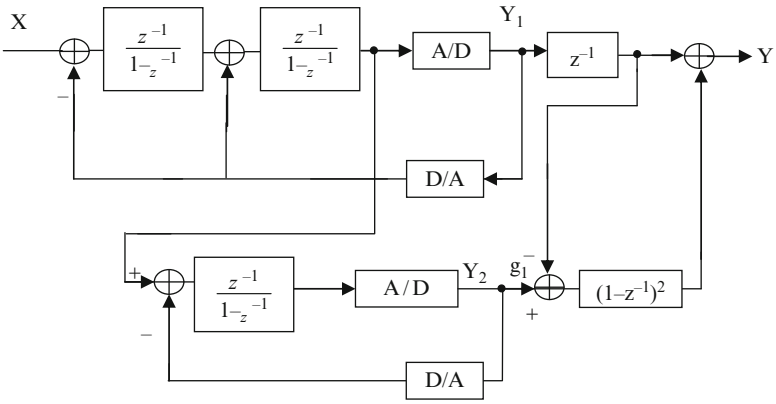


Fig. 4.76 SOFOC2 architecture used for analysis of the effect of opamp finite gain and capacitor mismatch

4.18.3.5 Finite Gain of the Amplifier

Taking into account the amplifier finite gain A of the opamp in a SC integrator, the transfer function can be written as

$$H_I(z) = \frac{V_o(z)}{V_i(z)} = \frac{-\alpha_{1a}}{(1-z^{-1})(1+\mu)+\alpha_{1a}\mu} \tag{4.174}$$

where $\mu = 1/A$ and $\alpha_{1a} = C_{ia}/C_2$ and C_{ia} is the total input capacitance of all the feed-in branches. Taking this model into account, the transfer function of the complete sigma-delta modulator can be derived [4.117]. We consider the SOFOC2 architecture shown in Fig. 4.76. for illustrating the procedure. For the purpose of this analysis, we consider the second integrator to be ideal having a transfer function $\frac{z^{-1}}{1-z^{-1}}$ since its nonidealities will be suppressed by the feedback loop. The first integrator will have nonideal response $H_I(z)$ given by (4.174). By routine analysis, we can obtain $Y_1(z)$ as

$$Y_1(z) = (X(z)H_I(z) + Y_1(z)(H_I(z)+2)\left(\frac{z^{-1}}{1-z^{-1}}\right) + E_{n1}(z) \tag{4.175a}$$

Substituting for $H_I(z)$ from (4.174), we have

$$\begin{aligned} Y_1(z) =& X(z)\frac{z^{-2}}{1+\mu(1+\alpha+\alpha z^{-1}-z^{-2})} \\ &+ E_{n1}(z)\frac{(1+\mu)(1-z^{-1})^2 + \alpha\mu(1-z^{-1})}{1+\mu(1+\alpha+\alpha z^{-1}-z^{-2})} \end{aligned} \tag{4.175b}$$

The output of the integrator preceding the quantizer in the first stage is given by

$$I_2(z) = Y_1(z) - E_{n1}(z) \tag{4.176a}$$

The output of the second stage with $I_2(z)$ as the input is

$$Y_2(z) = z^{-1}\left(Y_1(z) - E_{n1}(z)\right) + \left(1 - z^{-1}\right)E_{n2}(z) \tag{4.176b}$$

After digital scaling and subtraction, we obtain

$$V_3(z) = -E_{n1}(z)\,z^{-1} + \left(1 - z^{-1}\right)E_{n2}(z) \tag{4.176c}$$

Next, after double differentiation and subtraction, we obtain $Y(z)$ as

$$\begin{aligned} Y(z) = X(z)&\frac{z^{-3}}{1+\mu(1+\alpha+\alpha z^{-1}-z^{-2})} \\ &+ E_{n1}(z)\frac{\mu z^{-3}\left(\left(1-z^{-1}\right)^2+\alpha(1-z^{-1})\right)}{1+\mu(1+\alpha+\alpha z^{-1}-z^{-2})} + \left(1-z^{-1}\right)^3 E_2(z) \end{aligned} \tag{4.177a}$$

Note that (4.177a) can be simplified by ignoring the $(1 - z^{-1})^2$ terms and ignoring the gain and frequency-dependent term in $X(z)$ yielding finally

$$Y(z) = X(z) + E_{n1}(z)\alpha\mu\, z^{-3}\left(1 - z^{-1}\right) + \left(1 - z^{-1}\right)^3 E_{n2}(z) \tag{4.177b}$$

It is evident that first-order quantization noise is leaked into the final output as a result of finite opamp gain. Assuming the noise variances of the noise sources as σ^2_{Q1} and σ^2_{Q2}, the mean square noise at the output of the sigma-delta modulator can be written from (4.177b) as

$$\sigma_N^2 = \frac{(\alpha\mu\pi)^2}{3R^3}\sigma_{Q1}^2 + \frac{\pi^6}{7R^7}\sigma_{Q2}^2 \tag{4.178a}$$

Alternatively, the increase in mean square noise in dB can be found with respect to the value with $\mu = 0$ as

$$\Delta MSE(dB) = 10\log_{10}\left(1 + \frac{7}{3}\left(\frac{\alpha\mu}{g_2}\right)^2\left(\frac{R}{\pi}\right)^4\left(\frac{\sigma_{Q1}}{\sigma_{Q2}}\right)^2\right) \tag{4.178b}$$

In a similar manner, the effect of finite gain of the opamp can be analyzed for all sigma-delta modulator architectures.

4.18.3.6 Effect of Capacitor Mismatch

Carrying out the analysis as before, considering ideal opamps, the final output of the SOFOC2 modulator of Fig. 4.76 can be obtained as

$$\begin{aligned} Y(z) = X(z)\,z^{-3}\,(1-(1-g_1\,j_1)\,(1-z^{-1})^2 \\ + E_{n1}\,(z)(1-g_1\,j_1)\,z^{-1}\,(1-z^{-1})^2\,(1-(1-z^{-1})^2) \\ + g_1\,(1-z^{-1})^3\,E_{n2}\,(z) \end{aligned} \tag{4.179a}$$

Ignoring the gain and frequency-dependent terms in $X(z)$ and dropping the fourth-degree terms, we have

$$\begin{aligned} Y(z) = X(z)\,z^{-3} + E_{n1}\,(z)(1-g_1\,j_1)\,z^{-1}\,(1-z^{-1})^2 \\ + g_1\,(1-z^{-1})^3\,E_{n2}\,(z) \end{aligned} \tag{4.179b}$$

This shows that the effect of mismatch is to leak second-order-shaped quantization noise. Assuming the noise variances of the noise sources as ${\sigma^2}_{Q1}$ and ${\sigma_{Q2}}^2$, the mean square noise at the output of the sigma-delta modulator can be written from (4.179b) (denoting $(1 - g_1 j_1) = \delta$) as

$$\sigma_N^2 = \sigma_\delta^2\,\frac{\pi^4}{5R^5}\,\sigma_{Q1}^2 + g_1^2\,\frac{\pi^6}{7R^7}\,\sigma_{Q2}^2 \tag{4.180a}$$

where ${\sigma^2}_\delta$ is the standard deviation of δ. Alternatively, the increase in mean square noise in dB can be found with respect to the case with no mismatch ($\sigma_\delta = 0$) as

$$\Delta MSE(dB) = 10\log_{10}\left(1+\frac{7}{5}\left(\frac{\sigma_\delta}{g_1}\right)^2\left(\frac{R}{\pi}\right)^4\left(\frac{\sigma_{Q1}}{\sigma_{Q2}}\right)^2\right) \tag{4.180b}$$

Note that the parameter σ_δ can be determined from the relation $\delta = (1 - g_1 j_1 k_{1a} k_{1b})$ (taking into account the scaling by $k_{1a}k_{1b}$ which affects the path from input I_2 to output V_2) as

$$\begin{aligned} \sigma_\delta^2 &= \left(\frac{\sigma_{j_1}}{j_1}\right)^2 + \left(\frac{\sigma_{k_{1a}}}{k_{1a}}\right)^2 + \left(\frac{\sigma_{k_{1b}}}{k_{1b}}\right)^2 \\ &= \left(\frac{\sigma_{V_{REF1}}}{V_{REF1}}\right)^2 + \left(\frac{\sigma_{V_{REF2}}}{V_{REF2}}\right)^2 + \left(\frac{\sigma_{k_{1a}}}{k_{1a}}\right)^2 + \left(\frac{\sigma_{k_{1b}}}{k_{1b}}\right)^2 \end{aligned} \tag{4.181}$$

In a similar manner, the effect of finite gain of the opamp can be analyzed for other sigma-delta modulator architectures.

4.18.3.7 Effect of Comparator Hysteresis

The comparators used in sigma-delta modulators can have hysteresis which is defined as the minimum overdrive required to change the output. Defining h as the magnitude of hysteresis relative to the step-size Δ, its effect can be evaluated similar to noise at the comparator input [4.118]. The sum of the quantization noise and comparator hysteresis for a second-order sigma-delta modulator of Fig. 4.65d can be written as

$$S_N = \frac{\pi^{2L}}{2L+1}\frac{\Delta^2}{M^{2L+1}}\left[\frac{1}{12} + 4\,h^2\right],\ \mathrm{M} \gg 1 \tag{4.182}$$

Note also that the factor 4 arises since of the gain of the second integrator 0.5.

4.18.4 Band-Pass Sigma-Delta Modulators

So far, we have considered sigma-delta modulators that can code base-band signals. On the other hand, it is also of great interest to be able to code band-pass signals directly without translating the band-pass signal to the base-band. As an illustration, A/D conversion at the I/F radio stage can follow one of the architectures shown in Fig. 4.77a, b [4.133]. In the architecture of Fig. 4.77a, the conversion into the digital domain is after the signal has been separated into I and Q components. On the other hand, in the architecture of Fig. 4.77b, the band-pass signal is converted into the digital domain at the IF location. The conversion to the digital domain at IF has several advantages. The mismatch in I and Q paths that may exist in the architecture of Fig. 4.77a will not exist in Fig. 4.77b. The effect of offset voltages of opamps in the path hardware and effect of $1/f$ noise of opamps in the two paths can be avoided. The need to implement precise mixers will not affect the quality of the direct conversion. However, the sigma-delta converter needs to work at a very high sampling frequency and the signal that needs to be digitized has a very high dynamic range. The I and Q demodulators can be simpler if the sampling frequency is four times the pass-band center frequency.

Several interesting architectures have been suggested to realize band-pass sigma-delta modulators at very high frequencies which are considered in some detail next.

The architecture of a band-pass sigma-delta modulator will be the same as that of a first-order low-pass sigma-delta modulator except for replacing the loop filter (realized using an integrator) by another block [4.134]. It may be noted that using a loop filter with the z-domain transfer function $\left(\frac{-z^{-2}}{1+z^{-2}}\right)$ yields the output of the band-pass sigma-delta modulator of Fig. 4.78a as

$$V_o(z) = -z^{-2}\,V_i(z) + \left(1+z^{-2}\right)E_n(z) \tag{4.183}$$

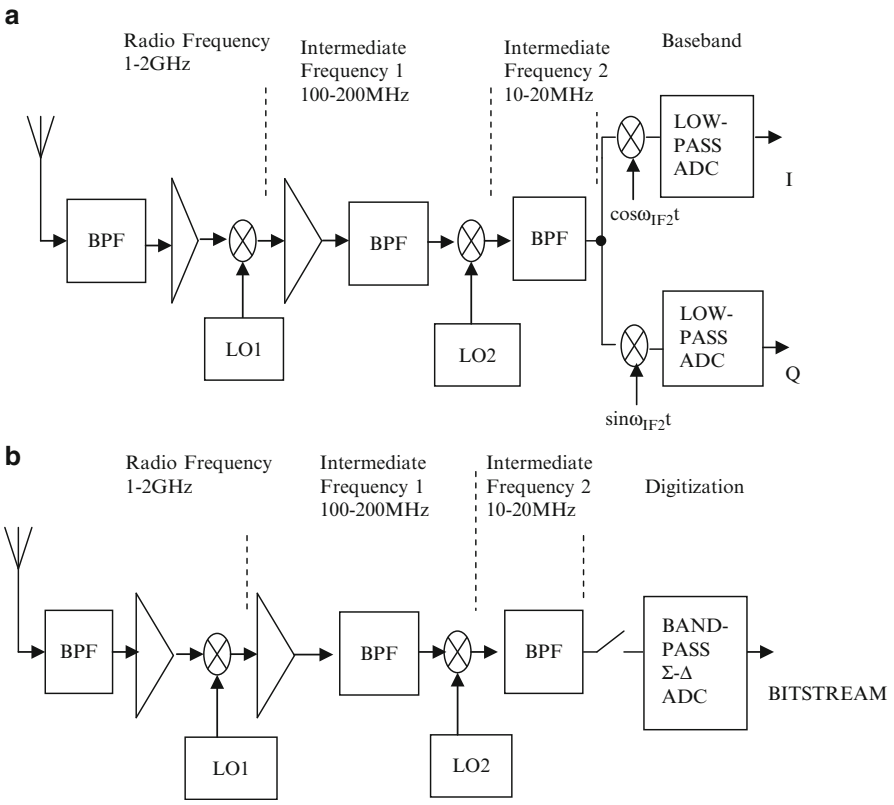


Fig. 4.77 (**a**) Low-pass A/D conversion and (**b**) band-pass A/D conversion (Adapted from [4.133] © IEEE 1997)

It can be seen that the input signal is delayed whereas the quantization noise has a transmission zero at frequency $f_s/4$ (since $\cos\theta = 0$ or $\theta = \omega T = \pi/2$). Evidently, by choosing the sampling frequency to be four times the center frequency, the quantization noise at the center frequency of the band-pass response can be attenuated. It is clear that the band-pass sigma-delta modulator can be obtained by the substitution $z^{-1} \rightarrow -z^{-2}$ in the transfer function of the integrator block.

Several techniques have been suggested [4.134, 4.135] for the SC implementation of the pole-forming loop in the band-pass sigma-delta modulator, that is, realizing the denominator $(1 + z^{-2})$ needed in the transfer function $\left(\frac{-z^{-2}}{1+z^{-2}}\right)$ which is considered next. These are shown in Fig. 4.78b–d.

It is important to note that realized poles are exactly on the unit circle so that the noise is cancelled satisfactorily. Equal coefficients for the constant and z^{-2} terms will realize exact center frequency at $f_s/4$ thus making the notch depth only dependent on R in the case of Fig. 4.78b and the realized transfer function is $1 - (2 + R)z^{-1} + z^{-2}$. This is called the LDI loop. On the other hand, in the case

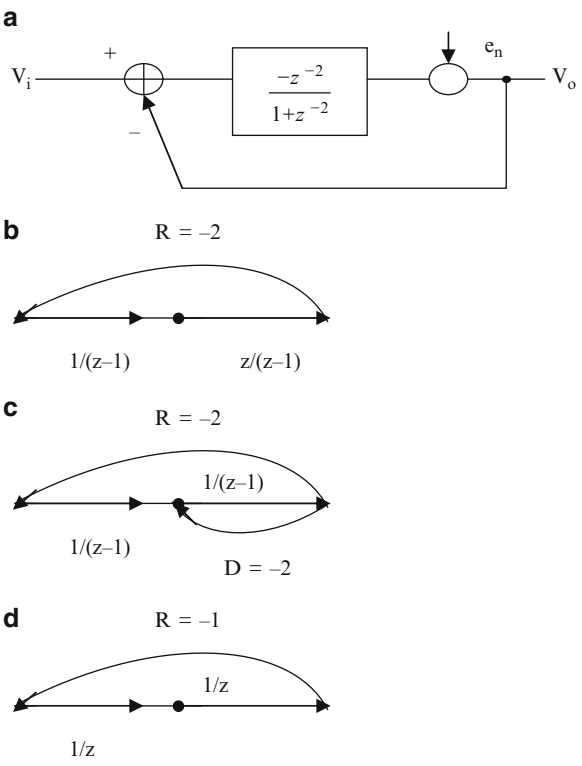


Fig. 4.78 (**a**) Schematic of a band-pass sigma-delta modulator, (**b**) LDI-based loop, (**c**) FEI-based loop, and (**d**) loop using two delays (Adapted from [4.134] © IEEE 1995)

of Fig. 4.78c, a forward-Euler loop is employed with $R = D = -2$. In this case, the poles can be away from the unit circle due to tolerances in R and D. The realized denominator of the transfer function is $1 - (2 + D)z^{-1} + (1 - R + D)z^{-2}$. Note that the errors in R and D can move the poles inside or outside the unit circle. However, the gain errors in the first integrator and errors in R do not affect the notch frequency to first-order. Note also that one of the opamps used to realize the loop can settle quickly. In the third design option, denoted as a *two-delay loop* and shown in Fig. 4.78d [4.136], two delays have been used to realize a denominator of transfer function $1 - \alpha z^{-2}$. This case is opposite to that of Fig. 4.78a in the sense that here the pole-frequency is fixed but the notch depth is sensitive to gain. This case is useful only for band-pass modulators centered at $f_s/4$.

A SC implementation of LDI- and FE-type feedback loops is presented in Fig. 4.79. Singer and Snelgrove [4.134] have analyzed the effect of opamp finite bandwidth and slew rate on the three configurations of Fig. 4.78b–d. It is known that the LDI loop can be connected with two opamps together during settling or so that they are decoupled. They point out that forward-Euler switch phasing gives a significant advantage over LDI and its higher sensitivity to capacitor ratios does not appear to seriously degrade the performance.

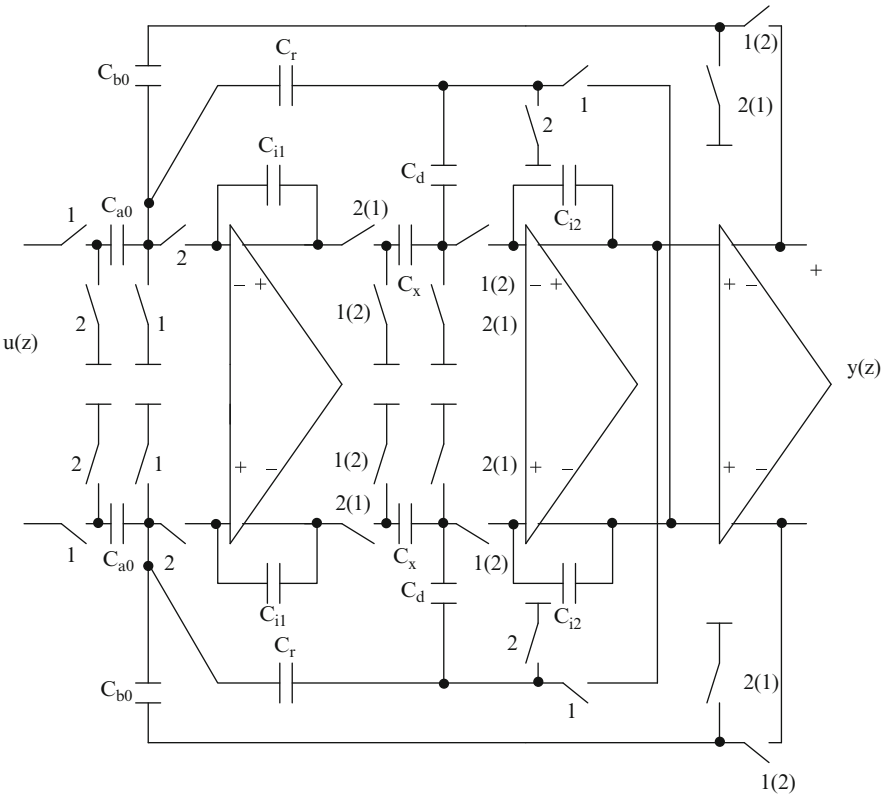


Fig. 4.79 SC second-order FEI- (clock phasing in brackets) and LDI-based band-pass sigma-delta modulator (Adapted from [4.134] © IEEE 1995)

Jantzi et al. [4.137] have implemented fourth-order band-pass sigma-delta modulators using the two architectures of Fig. 4.80a, b. The architecture of Fig. 4.80a uses an integrator-based companion form whereas that of Fig. 4.80b uses cascaded resonators. Considering component sensitivity, the architecture of Fig. 4.80b has been found to be better.

The noise-shaping frequency response can be derived for a $2M$th-order band-pass sigma-delta modulator as [4.135]

$$H(e^{j\omega T}) = g\,(2\cos(\omega T))^M \tag{4.184}$$

Hence, the resolution can be found following a similar approach to that in the case of a low-pass sigma-delta modulator as

$$Bits = \left(M + \frac{1}{2}\right)\log_2 R - \log_2\left[\frac{g\,\pi^M}{\sqrt{2M+1}}\right] + \log_2\left(2^Q - 1\right) \tag{4.185}$$

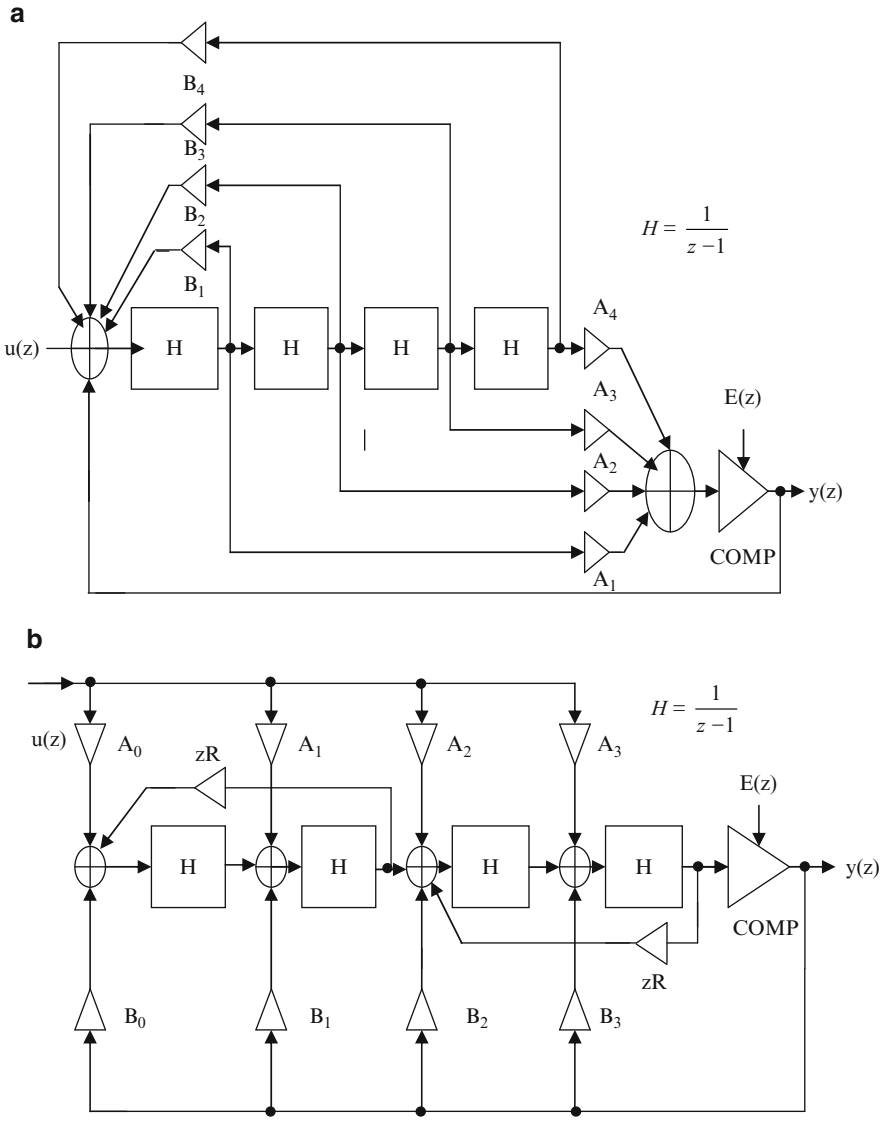


Fig. 4.80 (**a**) Cascade of integrator-based companion form structure, and (**b**) cascade of resonators structure (Adapted from [4.137] © IEEE 1993)

Note that the same expression applies to a low-pass modulator of half the order of a band-pass modulator (see (4.143a)).

Ribner [4.135] has suggested the implementation based on MASH-type low-pass sigma-delta modulators using LP–BP transformation. The reasons are (a) the low sensitivity-to-capacitor ratios, (b) possibility of using multibit quantizers without

increasing the sampling frequency, and (c) guaranteed stability as has been seen in the case of low-pass sigma-delta modulators. Two such structures are presented in Fig. 4.81a, b. Note that the structure of Fig. 4.81a uses several second-order modulators in cascade whereas the structure of Fig. 4.81b is based on a cascade of a fourth-order modulator and a second-order modulator. It is possible to have multiple fourth-order cascades also. Note that in the circuits of Fig. 4.81a, b, the weighting coefficients are different from those in the LP modulators.

A SC delay circuit is immune to capacitor nonlinearity and can operate at a higher speed. Bazarjani and Snelgrove [4.138] have suggested the use of a double-sampled SC delay circuit as shown in Fig. 4.82a using a fully differential amplifier. During ϕ_1, the input is stored on the sampling capacitor C_s and during ϕ_2, the capacitor C_s is switched to the output and plays the role of a holding capacitor. In this circuit, the input is sampled every half clock cycle and it appears at the output after a half clock cycle delay. The realized transfer function taking into account the finite gain of the opamp is given by

$$H(z) = \frac{1}{1 + \frac{1}{A}\left(\frac{C_s + C_{in}}{C_s}\right)} z^{-1/2} \tag{4.186}$$

where C_{in} is the opamp input capacitance.

A double-sampled resonator can be obtained by using two such delay blocks as shown in Fig. 4.82b. It can be shown that the location of resonator pole is not affected by the capacitor mismatch δ between C_I and C_{s1}:

$$H(z) = (1 + \delta)\frac{C_I}{C_{s1}}\left(\frac{z^{-2}}{1 + z^{-2}}\right) \tag{4.187}$$

A fourth-order sigma-delta modulator can be easily derived using two such resonators and a comparator with appropriate SC branches to feed input and the switched reference voltages.

The mismatch in the two paths of the double-sampled circuit (see Fig. 4.83) causes an in-band image of the signal. The effect is equivalent to feeding an input and an attenuated version of the input to the circuit. Assuming a mismatch of delta, the output can be written as

$$H(z) = (V_{ie}(z) + \delta V_{io}(z))H(z) \tag{4.188}$$

Nonuniform sampling due to uneven phases (i.e., of unequal duration) also causes images to appear in-band. Note, however, that the mismatch in the second stage is second-order noise-shaped and will not cause an appreciable image.

Several band-pass sigma-delta modulator architectures have been described in the literature with subtle differences. The basic band-pass sigma-delta modulator obtained by z^{-1} to $-z^{-2}$ transformation from a low-pass sigma-delta modulator is shown in Fig. 4.84a. Note that by simulation, the gains of the integrators have been

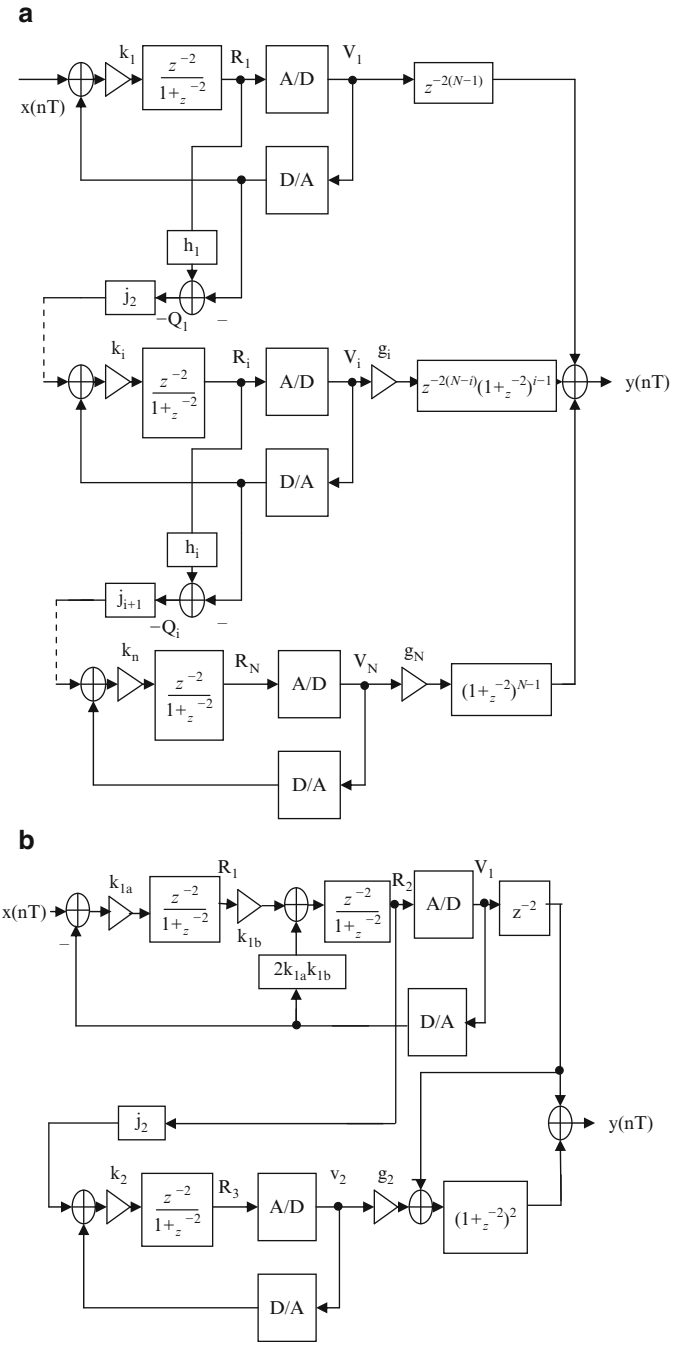


Fig. 4.81 (**a**) Multiple second-order resonator cascade band-pass sigma-delta modulator, and (**b**) fourth-order second-order resonator cascade (Adapted from [4.135] © IEEE 1994)

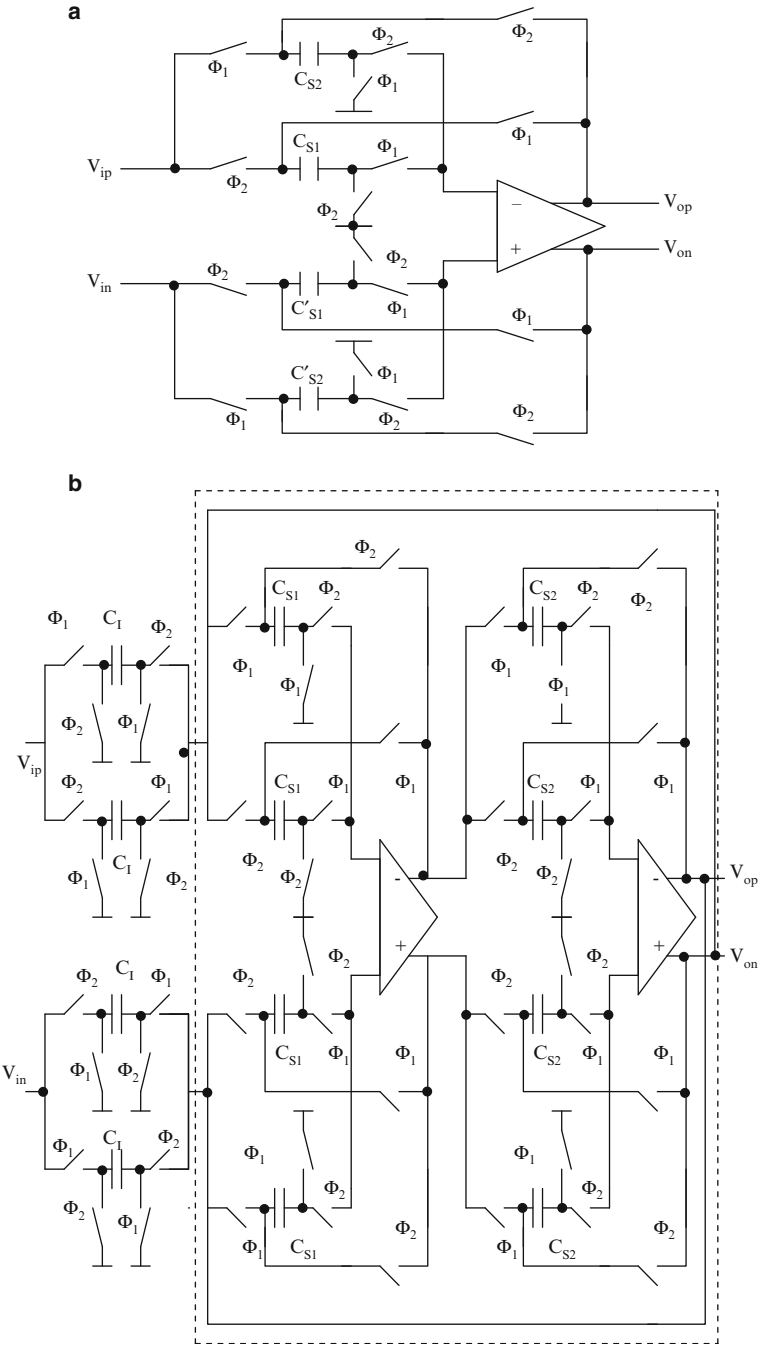


Fig. 4.82 (**a**) Double-sampled SC delay cell, and (**b**) resonator using two delay blocks of (a) (Adapted from [4.138] © IEEE 1998)

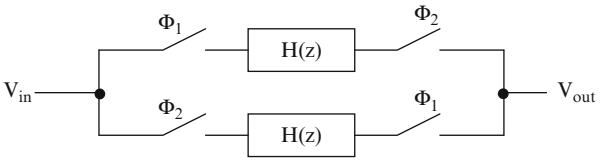


Fig. 4.83 Two-path SC filter

suggested by Ong and Wooley [4.133] as shown. A two-path version of this sigma-delta modulator for operation at double the speed can be derived as shown in Fig. 4.84b.

The circuit can be partitioned into two independent high-pass paths as shown in Fig. 4.84c. It is important to note that the quantization noise is not doubled due to the two separate quantizers in the two paths, since the two paths are interleaved and not summed. This architecture makes the modulator lead to a simple layout. The SC circuit realizing the transfer function $z^{-2}/(1 + z^{-2})$ is presented in Fig. 4.84d. The transfer function of this fully differential circuit is given by

$$V_{out} = \frac{C_{1A}}{C_{3A}} \left(\frac{z_p^{-1}}{1 + \left(\frac{C_{2B}}{C_{3A}} - 1 \right) z_p^{-1}} \right) \left(V_{in}(z_p) + V_{REF}(z_p) \right) \tag{4.189a}$$

where z_p^{-1} corresponds to a delay in a path. In the case where C_{2B}/C_{3A} is greater than two due to component tolerances, the circuit can be unstable. It has been found by simulation [4.133] that if the matching is 1%, the internal states in the circuit will be bounded. The effect of amplifier gain can be seen to alter the transfer function as

$$V_{out} = \frac{C_{1A}}{C_{3A}} (1 - \delta) \left(\frac{z_p^{-1}}{1 + (1 - \gamma) \left(\frac{C_{2B}}{C_{3A}} - 1 \right) z_p^{-1}} \right) \left(V_{in}(z_p) + V_{REF}(z_p) \right) \tag{4.189b}$$

An amplifier gain of 1,500 has been found to be sufficient to reduce the image component to −40 dB arising due to finite amplifier gain. The effect of amplifier settling time is to result in a transfer function

$$V_{out} = \frac{C_{1A}}{C_{3A}} (1 - \varepsilon) \left(\frac{z_p^{-1}}{1 + \left(\frac{C_{2B}}{C_{3A}} - 1 \right) z_p^{-1}} \right) \left(V_{in}(z_p) + V_{REF}(z_p) \right) \tag{4.189c}$$

where $\varepsilon = e^{-T/\tau}$ and T is the time for settling. If the two paths settle with different time constants, the mirror signal is incompletely suppressed. Thus, the amplifiers in the first stage must be designed to settle to the full precision of the modulator. The slew-rate of the opamp will further affect the settling behavior.

Song [4.139] has suggested some modifications of the sigma-delta modulator architectures shown in Fig. 4.85a. Note that the signs of the inputs of the summers in an alternative architecture of Fig. 4.85b are different from those shown in Fig. 4.85a. This architecture can enable economical realization of the resonators using fewer

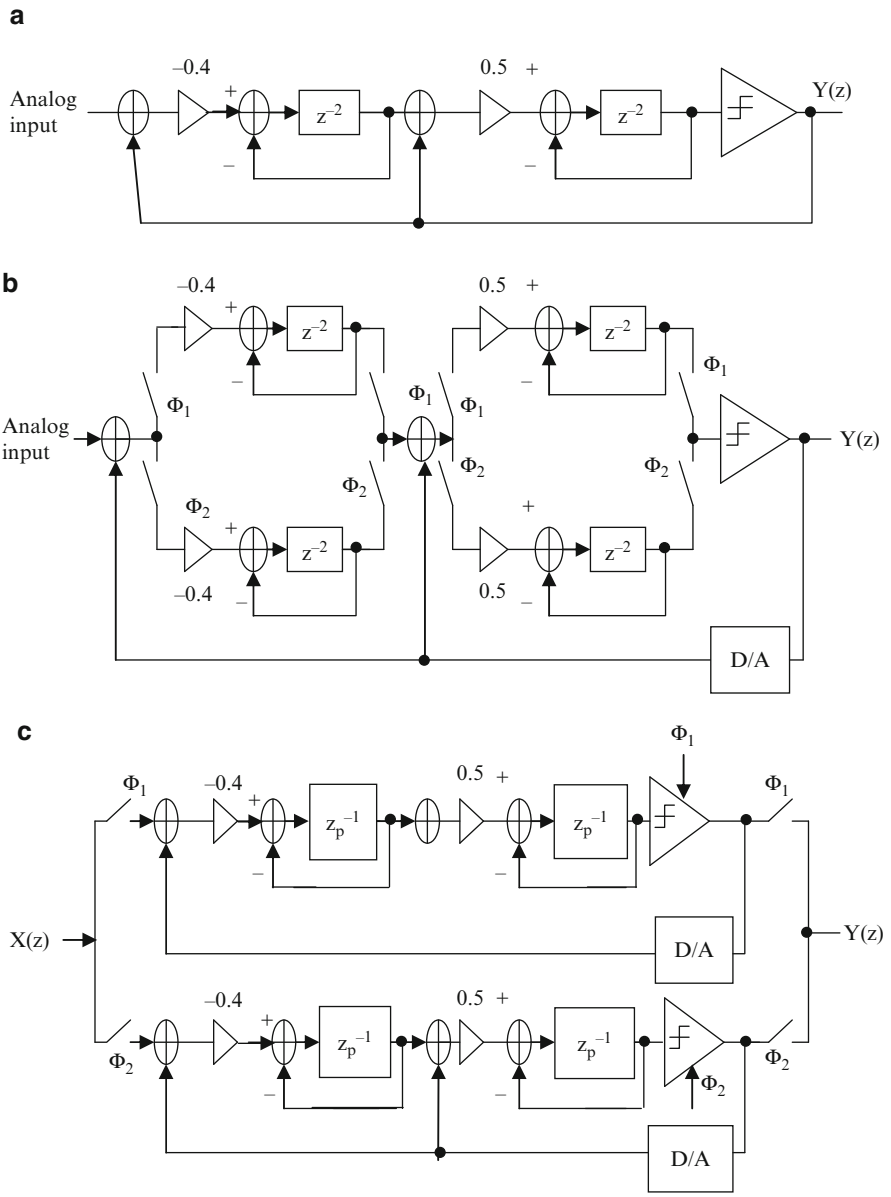


Fig. 4.84 (**a**) Fourth-order bandpass sigma-delta modulator, (**b**) implementation using a 2-path resonator, (**c**) partitioning of (b) into two separate paths, and (**d**) SC implementation of high-pass path filter (Adapted from [4.133] © IEEE 1997)

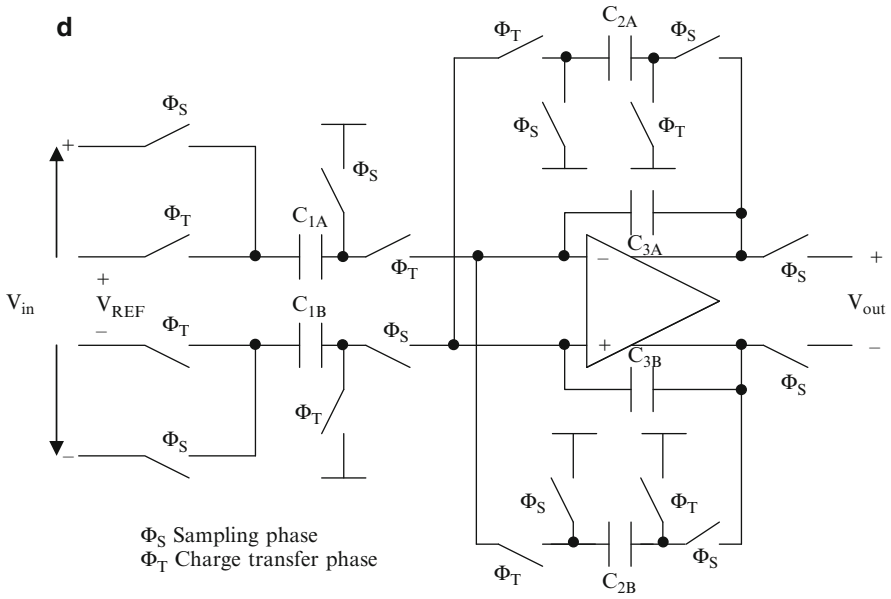


Fig. 4.84 (continued)

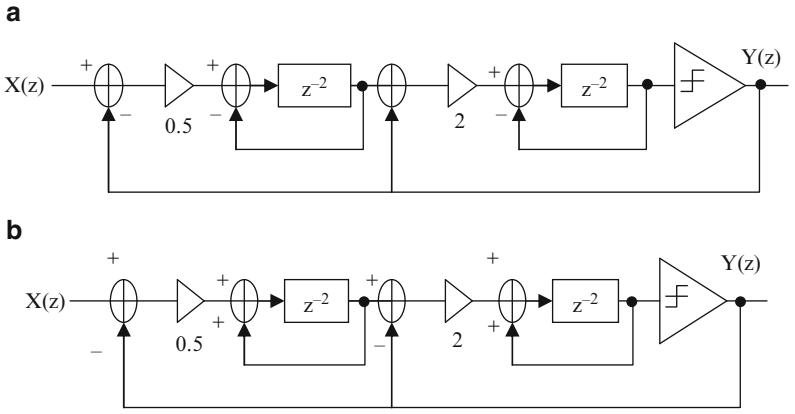


Fig. 4.85 (**a**) Song's fourth-order band-pass sigma-delta modulator architecture, and (**b**) modification to allow the use of integrators (Adapted from [4.139] © IEEE 1995)

opamps while realizing quadrature demodulation. The reader is referred to [4.139] for details on this approach.

Salo et al. [4.140] have described an interesting fourth-order band-pass sigma-delta modulator architecture. The block diagram of this is presented in Fig. 4.86a. The transfer function realized by this modulator is given by

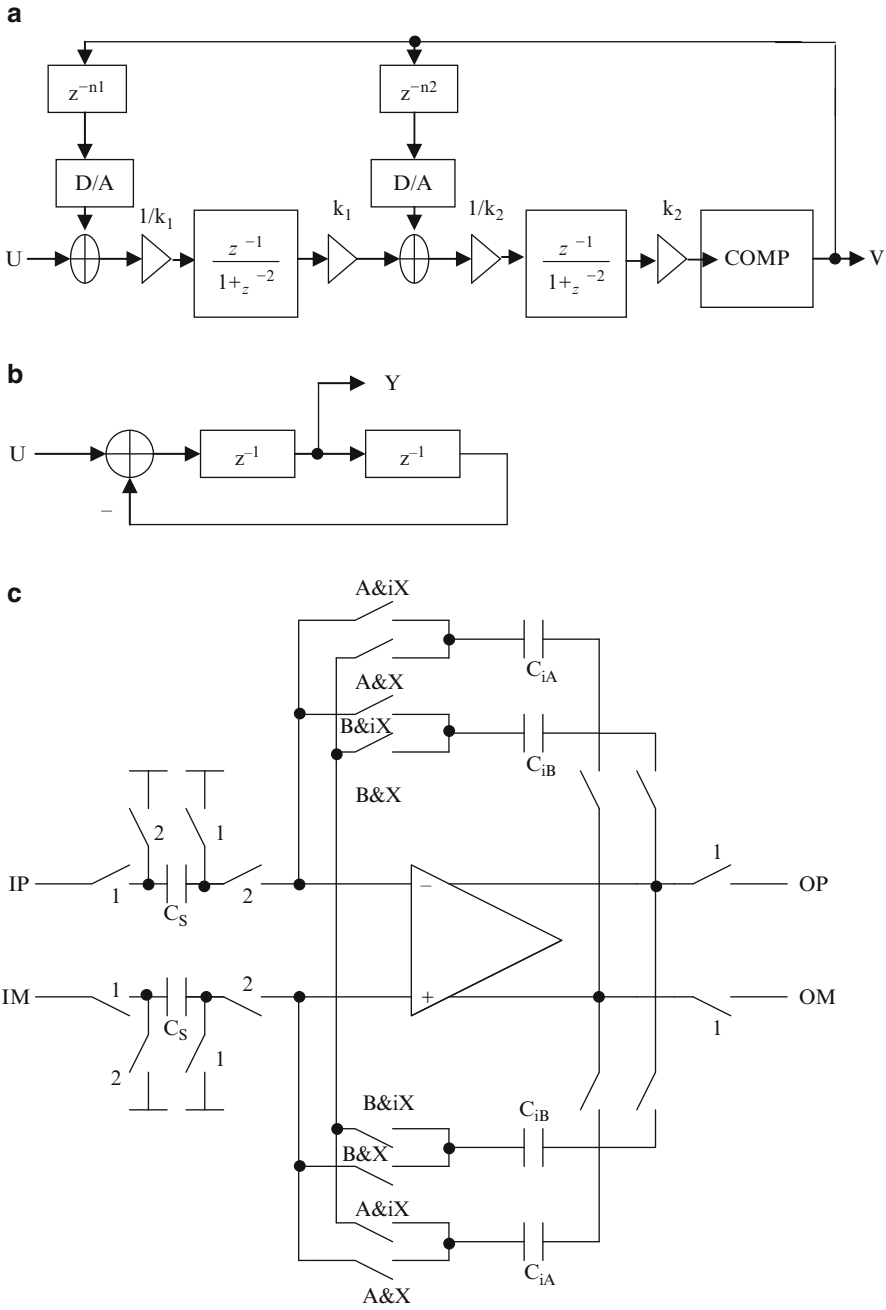


Fig. 4.86 (**a**) A fourth-order band-pass sigma-delta modulator, (**b**) resonator used in (a), (**c**) SC implementation, and (**d**) switching waveforms (Adapted from [4.140] © IEEE 2002)

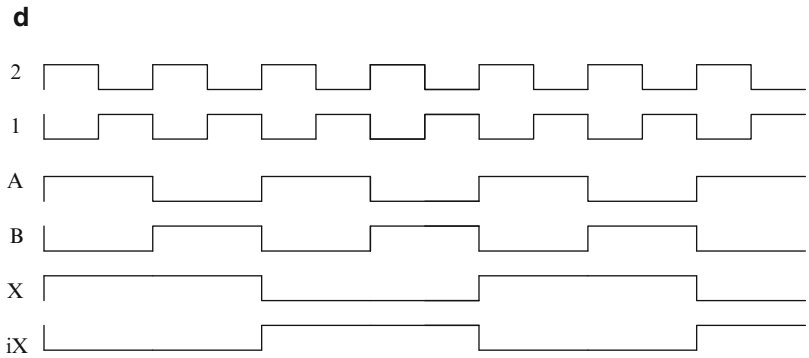


Fig. 4.86 (continued)

$$V(z) = \frac{z^{-2}\,U(z) + (1+z^{-2})^2\,E(z)}{1 + 2z^{-2} + z^{-4} - a\,z^{-(n_1+2)} - b\left(z^{-(n_2+1)} + z^{-(n_2+3)}\right)} \tag{4.190}$$

Two different choices are possible for n_1, n_2, a, and b given as follows: $n_1 = 0$, $n_2 = 1$, $a = 1$, $b = 1$ or $n_1 = 2$, $n_2 = 1$, $a = -1$, $b = 2$. Note that two separate DACs have been used. The block with transfer function $\frac{z^{-1}}{1+z^{-2}}$ (double-delay resonator) is realized as shown in Fig. 4.86b. The SC implementation is as shown in Fig. 4.86c together with the switching waveforms in Fig. 4.86d. Thus using two opamps, the fourth-order modulator can be realized. The operation of the resonator is as follows. In Phase 2, the charge in the sampling capacitance C_s is summed with the charge in either the integration capacitor C_{iA} or C_{iB}. In clock phase 1, a new sample is taken from the input and output of the resonator can be sampled by the following circuit. The delay of two clock phases is implemented by using two branches A and B in which the signal value is alternately integrated. The sample integrated two clock periods earlier is stored in the integration capacitance of the respective branch. The feedback factor of -1 is achieved by switching the integration capacitances alternately to the opposite nodes of the opamp. The center frequency of the resonator is $f_s/4$.

Kuo et al. [4.141] and Wang and Kuo [4.142, 4.143] studied the design of the single-loop sigma-delta modulator using a multibit quantizer in various configurations: (a) using a cascade of resonators with distributed feedback (CRFB), (b) cascade of resonators with feedforward (CRFF), and (c) low-spread cascade of resonators with feedforward (LSCRFF). The objective was to evolve a stable design needing minimum capacitor spread and minimum order for realizing a specified SNR. They consider the realization of inverse Chebychev type of noise transfer function while realizing a signal transfer function with only zeroes on the unit circle. The selection of the NTF is based on a figure of merit *noise power gain* which is given as $\frac{1}{\pi}\int_0^{\pi}\left(|NTF(e^{j\omega})|\right)^2 d\omega$ to examine the stability. Note that NTF

decreases when the order N is increased, SCR (sampling frequency to center frequency ratio) increases, or higher quantizer bits are used. The method has been used for band-pass sigma-delta modulators as well. The reader is referred to their work for more details.

4.19 Problems

P.4.1. Analyze the effect of opamp offset on the SC integrators of Figs. 4.5a and 4.6a. Analyze the effect of opamp dc gain as well noise of the opamp.

P.4.2. Multiphase SC circuits can be analyzed using z-domain equivalent circuits. Mulawka [4.144] has suggested the equivalent circuit of Fig. P.4.2a. Herein, as many sections as the number of phases exist. The opamp also gets split as n opamps. Draw a z-domain-equivalent circuit of Fig. P.4.2b and derive the transfer function. Derive by hand as well and compare the efficiency of both methods.

P.4.3. Derive a fifth-order SC filter based on component simulation technique from prototype LC ladder filter based on the approach of Fig. 4.17.

P.4.4. The LDI transformation is given by $s \rightarrow \frac{1-z^{-1}}{T z^{-1/2}}$. Thus, given an s-domain root, we can obtain two roots in the z-domain since this relationship is a quadratic in $z^{-1/2}$. One of these will be inside the unit circle and the other outside the unit circle. By choosing the roots mapped within the unit circle, a stable z-domain transfer function can be constructed [4.145]. Obtain a second-order digital filter transfer function from a second-order Butterworth filter with a pole-frequency of 1 KHz. Use a sampling frequency of 100 KHz.

P.4.5. SC filters can be obtained from active RC filters using p-transformation [4.146] defined by $s \rightarrow \frac{1-z^{-1}}{T}$. The procedure is to replace the resistors using series switched capacitors working in one phase, say even and isolating the capacitors so that charges flow in any one phase. An example is illustrated in Fig. P.4.5 derived from the Sallen–Key active RC filter. Derive the transfer function and confirm this fact. Evaluate δ and Q_p of the realized filter. What are the limitations to this method of deriving SC filters?

P.4.6. A SC circuit that can realize bilinear transformation [4.147] is shown in Fig. P.4.6. Determine the realized $\Delta Q(z) - V(z)$ relationship. Show that the SC resistor of Fig. P.4.6 realizes a bilinear transformed transfer function corresponding to the prototype Sallen and Key active RC filter.

P.4.7. Fried [4.148] described the application of the concept of switched-capacitors to filters first. Analyze the SC filter of Fig. P.4.7. When you interchange ground and input terminals (i.e., use complementary transformation), you can obtain another SC filter. Derive the transfer functions of both these circuits and comment on these circuits.

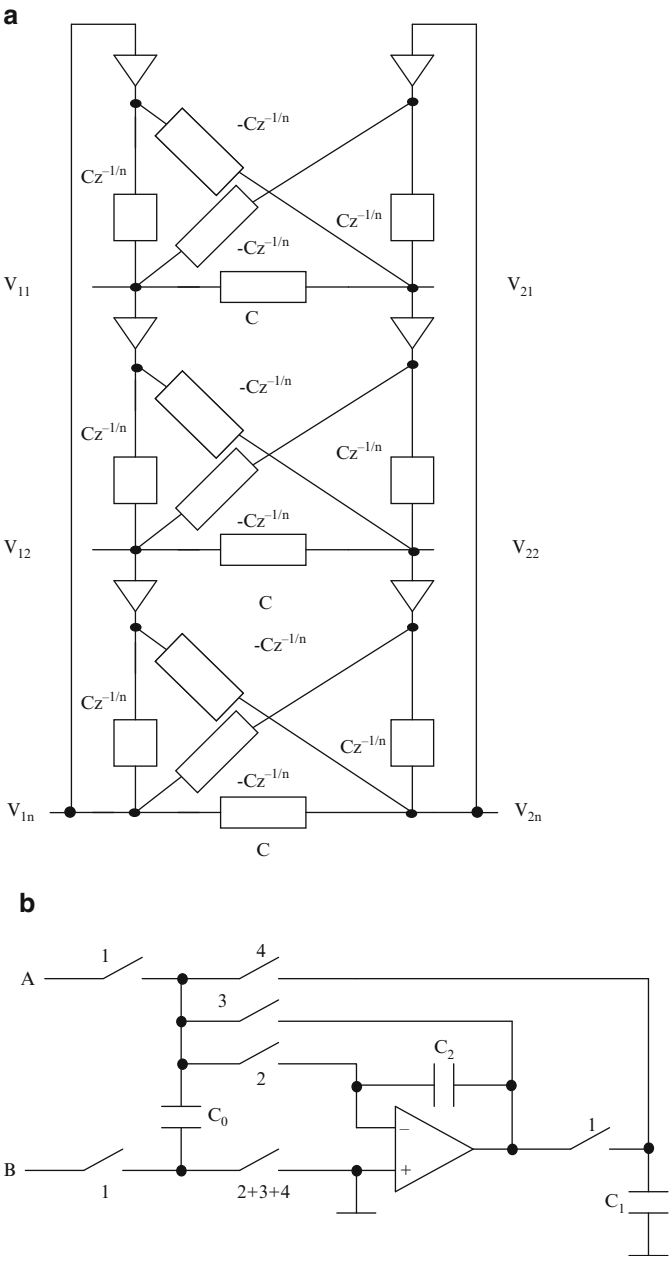


Fig. P.4.2 (a Adapted from [4.144] © Taylor and Francis 1980)

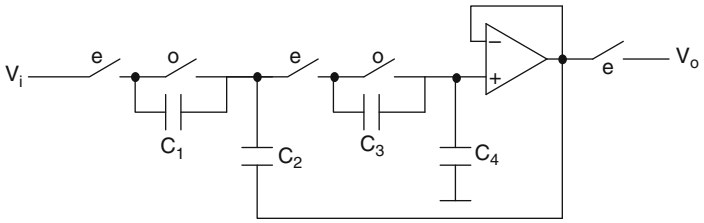


Fig. P.4.5

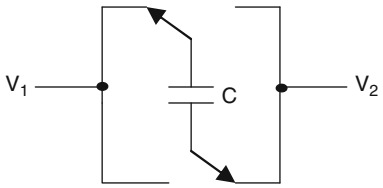


Fig. P.4.6 (Adapted from [4.147] © IEEE 1978)

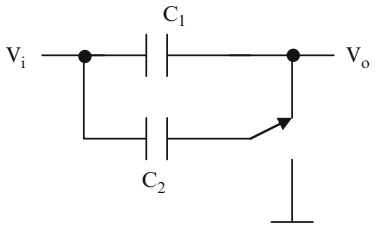


Fig. P.4.7 (Adapted from [4.148] © IEEE 1972)

P.4.8. Compare the various s to z transformations (a) $s \rightarrow \frac{1-z^{-1}}{T}$, (b) $s \rightarrow \frac{1-z^{-1}}{Tz^{-1}}$, (c) $s \rightarrow \frac{1-z^{-1}}{Tz^{-1/2}}$, (d) $s \rightarrow \frac{2(1-z^{-1})}{T(1-z^{-1})}$ regarding their mapping properties.

P.4.9. Analyze the effect of finite opamp gain on the circuits of Fig. 4.14a–d.

P.4.10. Show that the Q realized by the transfer function (4.75b) is $\frac{\pi}{6\ln(\beta)}$ [4.52].

P.4.11. Analyze the effect of offset voltage of the opamp on the circuit of Fig. 4.14a (see (4.38)).

P.4.12. Evaluate the dc gains taking into account the finite opamp gain A on the SC integrators of Fig. 4.44a–e.

P.4.13. Evaluate the dc gains taking into account the finite opamp gain A on the amplifiers of Fig. 4.46a–b.

P.4.14. Derive expressions for the change in pole frequency and pole-Q of a two-integrator loop in terms of the magnitude and phase errors of the lossless and lossy integrators (see (4.137a) and (4.137b)).

P.4.15. Analyze the effect of opamp finite gain on the sigma-delta modulators of Figs. 4.67a–d.

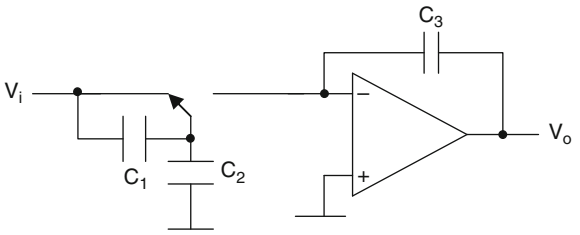


Fig. P.4.17

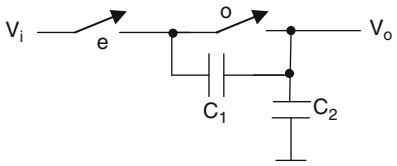


Fig. P.4.18

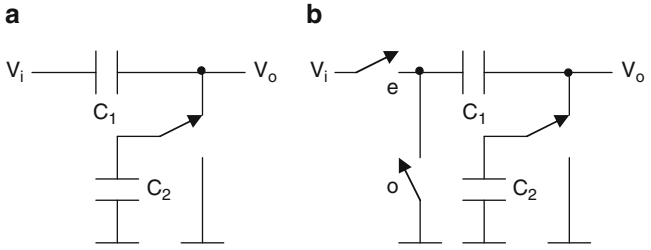


Fig. P.4.19 (Adapted from [4.158] © IEEE 1983)

P.4.16. Analyze the effect of capacitor mismatch on the Sigma-delta modulators of Fig. 4.67a–d.

P.4.17. Derive the transfer function of the SC integrator of Fig. P.4.17. Compare with other SC integrators of Fig. 4.6a, b, c with $C_3 = 0$.

P.4.18. Derive the transfer function of the SC circuit of Fig. P.4.18. and evaluate the performance.

P.4.19. Derive the transfer function of the SC filters of Fig. P.4.19a, b. Show that by choosing input properly, a LP filter can be realized from a high-pass filter.

P.4.20. Analyze the circuit of Fig. P.4.20 and derive the condition for realizing a bilinear integrator. Compare this circuit with other bilinear integrators.

P.4.21. Analyze the circuit of Fig. P.4.21. Determine the condition for realizing a bilinear integrator and compare it with other bilinear integrators.

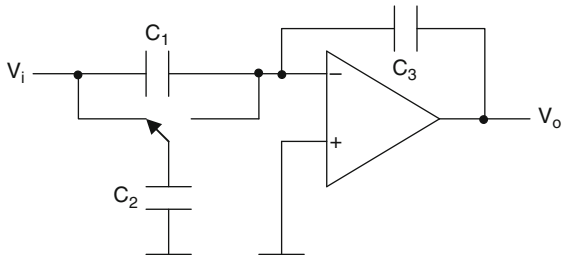


Fig. P.4.20

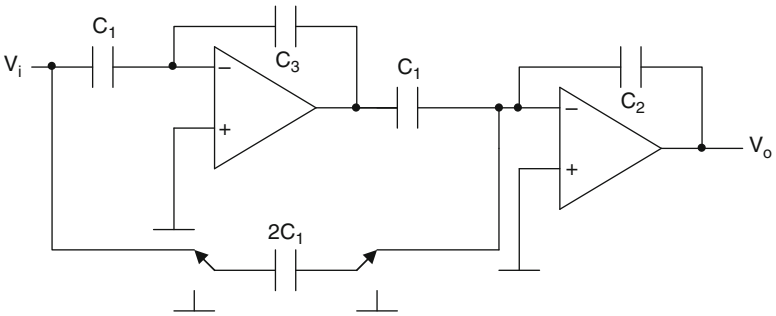


Fig. P.4.21

P.4.22. Analyze the general SC circuit of Fig. P.4.22 using Laker's equivalent circuit method. Derive the condition for having output held over a clock period.

P.4.23. Realize a fourth-order direct form filter using the three-phase delay of Enomoto (see Fig. 4.43b).

P.4.24. A parasitic-compensated differential integrator is shown in Fig. P.4.24. Derive the transfer function and obtain the condition for exact parasitic compensation.

P.4.25. Analyze the three Martin–Sedra SC biquads [4.4, 4.151] of Fig. P.4.25a–c. Compare them with the Fleischer–Laker SC biquad of Fig. 4.8a.

P.4.26. An electrically programmable SC filter [4.152] is shown in Fig. P.4.26. Analyze the circuit and derive expressions for pole-frequency, pole-Q, and gain. Discuss the limitations of this circuit.

P.4.27. Cox et al. [4.153] presented a programmable SC filter presented in Fig. P.4.27. Derive the design equations for various capacitor ratios for realizing the desired pole-frequency, pole-Q, and gain.

P.4.28. A programmable SC filter [4.154] is shown in Fig. P.4.28. Analyze the circuit and derive expressions for pole-frequency, pole-Q, and gain. Compare this with the two filters considered in P.4.26 and P.4.27.

P.4.29. Derive a stray-insensitive SC filter from Bach's active RC filter using p-transformation. Evaluate the design compared to the Fleischer–Laker biquad.

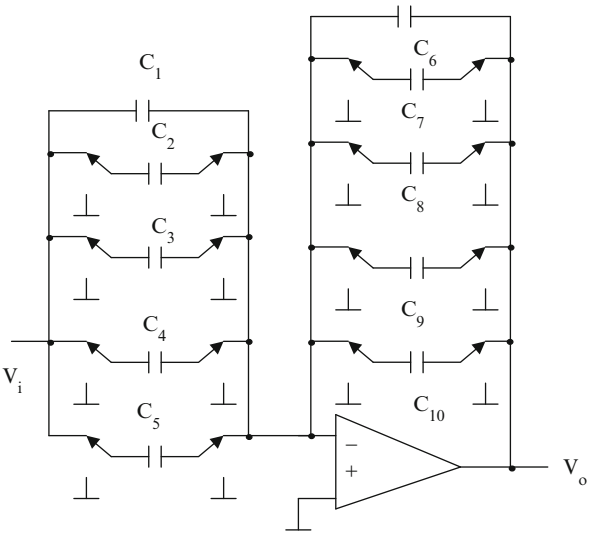


Fig. P.4.22

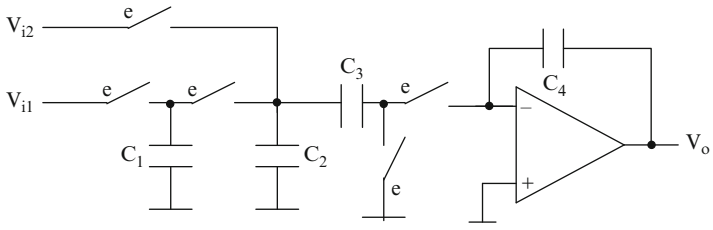


Fig. P.4.24

P.4.30. Derive a SC filter [4.159] from the Tarmy–Ghausi active RC filter of Fig. 2.25a. Discuss its advantages and limitations and derive the design equations.

P.4.31. Derive the expression for $\Delta Q(z) - V(z)$ relationships at the input port of the four-phase SC circuit of Fig. P.4.2b. Find the conditions under which a lossless floating inductance is realized.

P.4.32. Design a LDI-type SC ladder filter for a sampling frequency of 100 KHz and cutoff frequency of 11 KHz. The prototype with Chebychev 0.1 dB ripple is shown in Fig. P.4.32.

P.4.33. Design a bandpass filter from the third-order Chebychev prototype (see Fig. P.4.32) for 0.1 dB ripple, center frequency of 10 KHz, and bandwidth 1 KHz. Construct a leap-frog active RC implementation and SC implementation using bilinear transformation.

P.4.34. Derive an N-path SC filter from the two-phase SC filter of Fig. 4.6b using $z \rightarrow z^N$ transformation. Explain the operation and plot the frequency response.

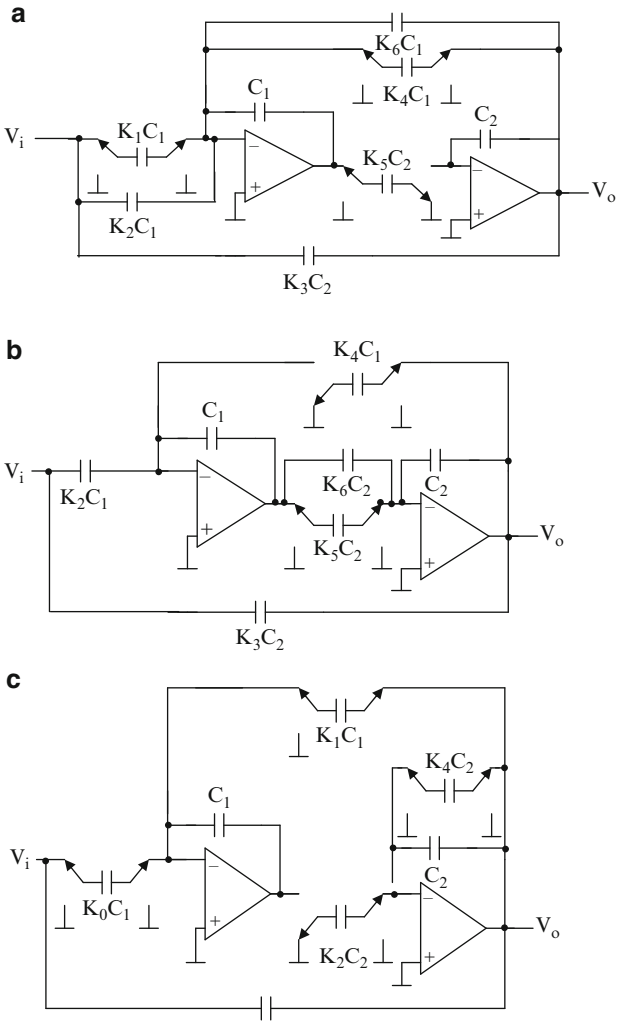


Fig. P.4.25 (Adapted from [4.4] © IEEE 1980)

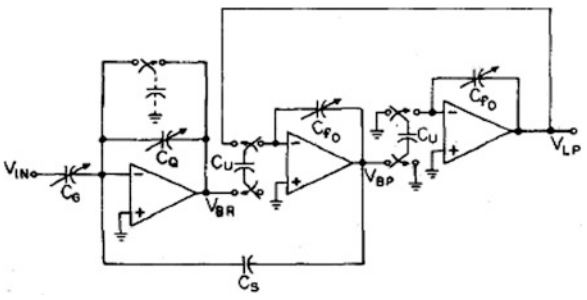


Fig. P.4.26 (Adapted from [4.152] © IEEE 1980)

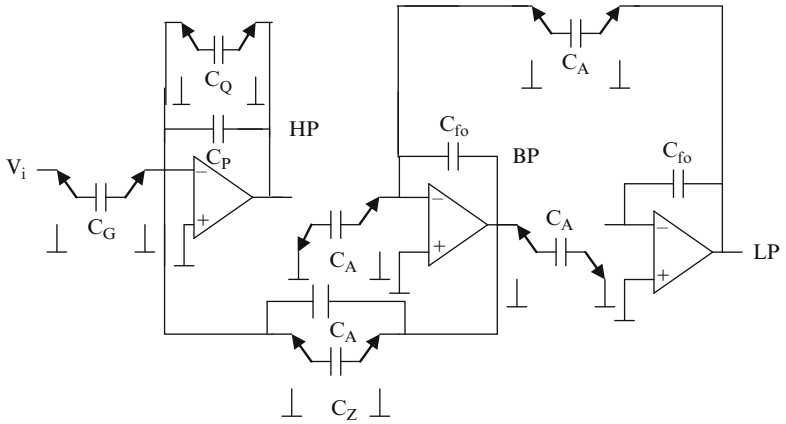


Fig. P.4.27 (Adapted from [4.153] © IEEE 1979)

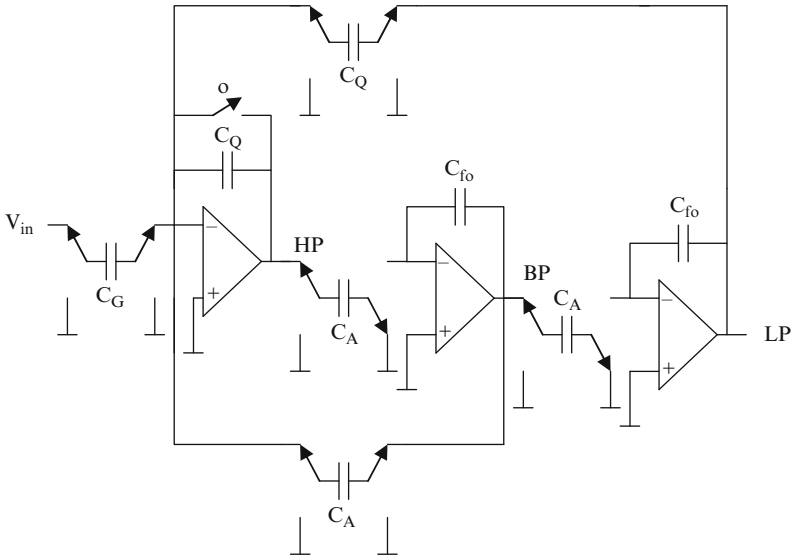


Fig. P.4.28 (Adapted from [4.154] © IEEE 1986)

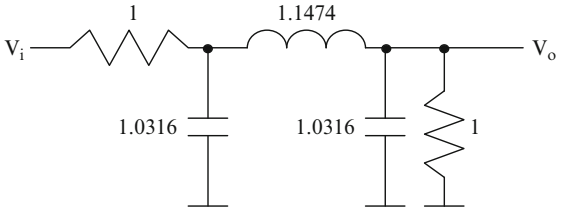


Fig. P.4.32

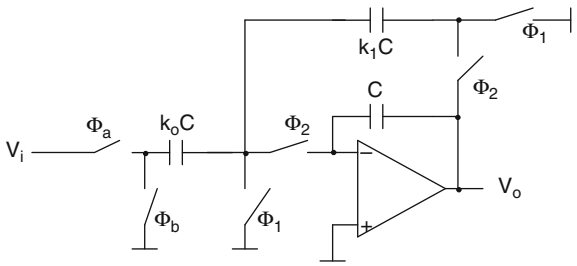


Fig. P.4.35 (Adapted from [4.10] © IEEE 1983)

P.4.35. A SC balanced modulator [4.10] is presented in Fig. P.4.35. Explain the operation of the circuit. Use a PSPICE program to obtain the time domain behavior.

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Chapter 5
Practical Designs of VLSI Analog Filters

In the previous chapters, design techniques for active resistance capacitor (RC), operational transconductance amplifier (OTA) capacitor (OTA-C), and switched-capacitor (SC) filters have been covered in great detail. In this chapter, we survey the state of the art of implementations. The objective is to bring to the attention of the reader how the various requirements such as low power, low voltage operation, high operating frequencies, and low area are addressed in practice. The evolution of contemporary design techniques has been continuing since the 1980s and many ideas developed have been employed and improved to meet the above-mentioned requirements. We present here work done more recently, since 2002. The figures of merit needed for comparing various design techniques, typical specifications, practical considerations, and tuning techniques are presented appropriately. We deal with active RC designs, OTA-C designs, and LC filters separately. Since Chap. 4 dealt with SC filters in great detail, and there has not been much recent development, we have not focused on those. We follow the description given by respective authors regarding total system design: filtering functions, tuning loops, programmability, and details of active device design since these diverse approaches cannot be easily unified.

5.1 Integrated Resistors and Capacitors

Double polysilicon capacitors offer good matching and low parasitic capacitance to substrate of 1% of the nominal value compared with 50–100% if metal layers are used. Polysilicon resistors exhibit good linearity of around 50 ppm/volt. For high linearity applications, passive components must be used for realizing time constants. Tunability of responses using passive components can be achieved by programmable resistor and capacitor arrays. The four types of programmable resistor and capacitor arrays are shown in Fig. 5.1a–d [5.1, 5.2]. Of these, (a) and (d) are preferable, taking into account the area requirements for a given tunability range. As an illustration for a five-bit control, considering a nominal value of the component C_{nom} or R_{nom} and

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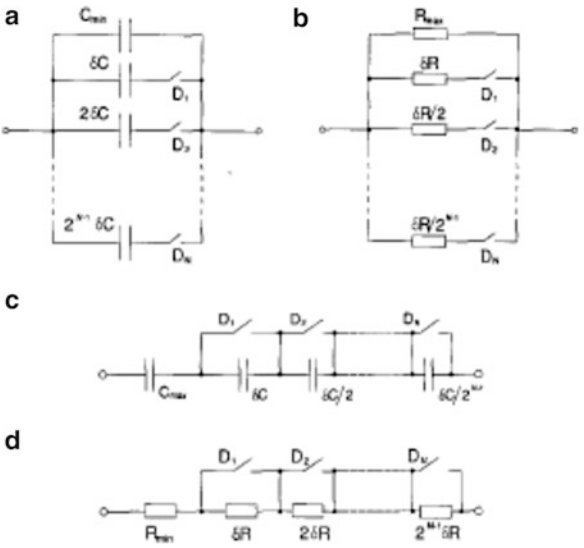


Fig. 5.1 (**a**) Parallel capacitor array, (**b**) a parallel resistor array, (**c**) a series capacitor array, and (**d**) a series resistor array (Adapted from [5.1] ©IEEE 1992)

Table 5.1 Design examples of four types of PCAs and PRAs (Adapted from [5.1] ©IEEE 1992)

Array	Design specification	C_{TOT} R_{TOT}	$\varepsilon^{+}_{max\,(\%)}$	$\varepsilon^{-}_{max\,(\%)}$
Parallel capacitive	$C_{max} = 40$ pF, $x = 50$, $N = 5$	59.38 pF	+3.13	−2.94
Series capacitive	$C_{max} = 40$ pF, $x = 50$, $N = 5$	1918 pF	+3.03	−3.03
Parallel resistive	$R_{max} = 80$kΩ, $x = 50$, $N = 5$	3836kΩ	+3.03	−3.03
Series resistive	$R_{max} = 80$kΩ, $x = 50$, $N = 5$	118.8kΩ	+3.13	−2.94

a 50% tuning range (i.e., $x = 50$), the area and quantization error limits are presented in Table 5.1. Evidently, designs (a) and (d) require the least area. Considering the switch parasitic capacitance and ON resistance, it can be shown that the parallel capacitive array has better performance than the series resistor array.

5.2 Active RC Filter Designs for Wireless Applications

The low-pass filter cutoff frequencies needed for various wireline and wireless standards within the 1- to 20-MHz range are presented in Fig. 5.2a.

Asalanzadeh et al. [5.3] have described a fifth-order reconfigurable power adjustable active RC low-pass filter to meet all these requirements. This can be

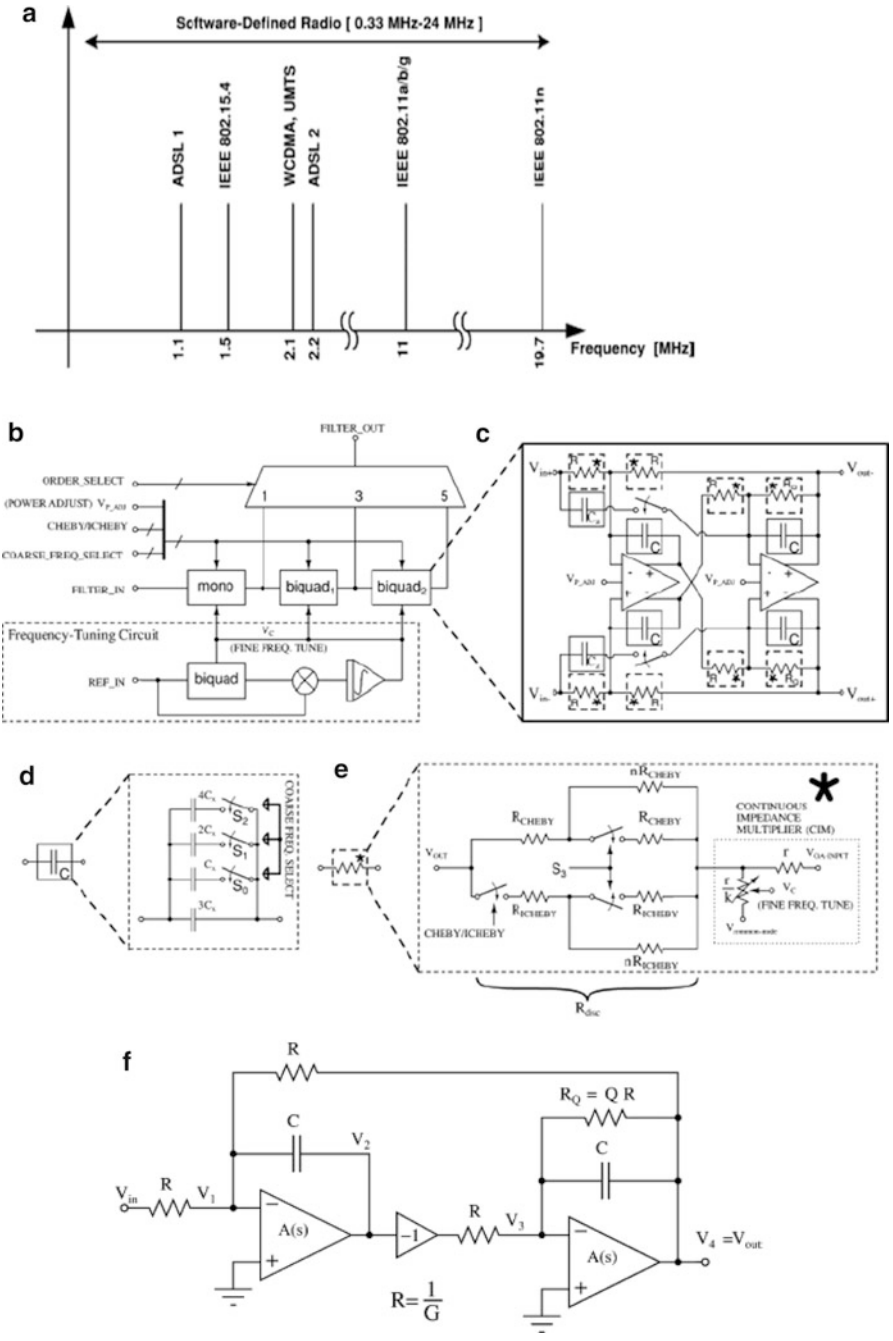


Fig. 5.2 (**a**) Diverse wireline/wireless applications with unevenly spaced cutoff frequencies, (**b**) top-level filter architecture, (**c**) biquad used in (**b**), (**d**) capacitor array for frequency selection, (**e**) continuous impedance multiplier (CIM), (**f**) biquad circuit used for analysis, (**g**) CIM, (**h**) opamp, and (**i**) CMFB loop schematic (Adapted from [5.3] ©IEEE 2009)

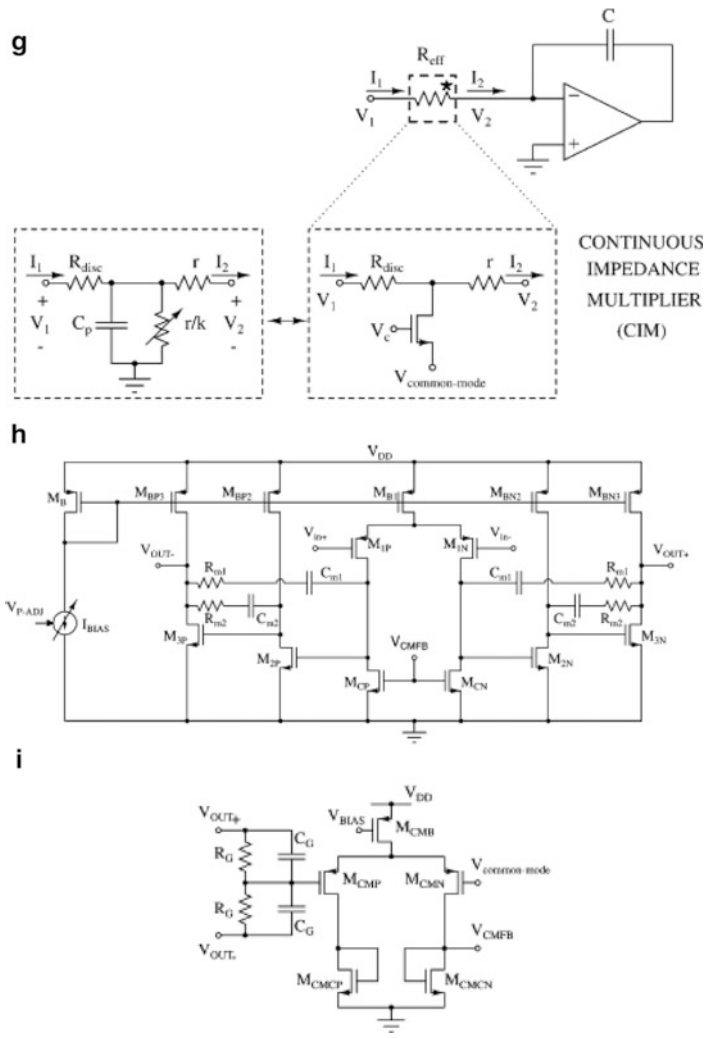


Fig. 5.2 (continued)

used for base-band filtering for a variety of applications needing cutoff frequencies in the range of 1–20 MHz. This architecture uses a first-order section followed by two second-order sections. A first-order, third-order, or fifth-order transfer function can be obtained by switching off the appropriate stages and taking the outputs at the first or second stage or after the third stage. The architecture of the fully differential filter is presented in Fig. 5.2b–e and the biquad circuit is shown in Fig. 5.2f. The frequency tuning is done in three ways. First, a Chebychev- or inverse Chebychev–type transfer function is selectable by the switch Cheby/ICheby (see Fig. 5.2c–e). Next, programmable capacitor arrays controlled by S_0, S_1, and S_2 together with the resistance

control of n using the switch S_3 are used to select the frequency band. Next, continuous change in pole frequency is feasible using a fixed value realized by the resistors R_{CHEBY}, R_{ICHEBY}, nR_{CHEBY}, nR_{ICHEBY} together with a continuous impedance multiplier (CIM). This uses a T network, whereby changing the k value, the total resistance can be changed. Note that this configuration is applicable only when the terminal B faces virtual ground. The resistance R/k is realized using a NMOS transistor with a continuously variable control voltage V_c (see Fig. 5.2g). The control voltage is obtained using a control loop, shown in Fig. 5.2b. In this technique, the input and output of a reference band-pass biquad implemented on the same chip are multiplied and the output signal is integrated using a low-pass filter to derive the dc control signal. Note that the phase difference ideally should be 90°. The control varies to satisfy this requirement.

The design also has a power adjustment feature. To maintain the stability margin while optimizing power, power is scaled to make ω_o/B constant when ω_o is reduced. Note that at high pole frequencies, high power consumption will exist. There is a tradeoff between phase margin and Gain Bandwidth Product (GBW) for a given ω_o and Q. The biquad realizes a sixth-order transfer function taking into account the first and second poles of the operational amplifiers. The authors define a parameter "minimum acceptable phase margin" and derive the condition for stability under different conditions. The power adjustment signal adjusts the bias currents of all the operational amplifiers (opamps) as well as that of the common-mode feedback (CMFB) circuit (see the complete opamp circuit in Fig. 5.2h, i) simultaneously. The opamps use three stages Since of the low supply voltage and moderately low load resistance. A CMFB circuit using an RC divider network is employed. The opamps used nested Miller compensation and all stages are inverting stages. Stability is ensured by proper choice of $R_{m1,\ 2}$ and ensuring that $C_{m1} \ll C_{m2}$.

Balankutty et al. [5.4] have proposed a zero-IF/low-IF receiver for 2.4 GHz ISM band applications. The architecture of this design in the 90 nm CMOS process is presented in Fig. 5.3a. The RF front-end consists of a single-ended low-noise amplifier (LNA) followed by a quadrature mixer to perform down conversion and single-ended to differential conversion. The local oscillator signals are derived from a 4.8-GHz fractional synthesizer operating from a 32-MHz reference clock. The LNA provides a 50-ohm input matching impedance at 2.4 GHz. Active polyphase buffers are used to provide the LO signal to the I and Q channel mixers. The variable gain complex band-pass filter rejects out of band channel blockers and provides programmable gain. The receiver caters to both Zigbee (802.15.4) and Bluetooth (802.15.1) applications. The radio specifications of Bluetooth and Zigbee are presented in Table 5.2. It can be seen that the channel filter for receiving Bluetooth signals in the low IF mode is 2 MHz and hence a band-pass filter is used. On the other hand, for Zigbee application using zero-IF mode, a base-band low-pass filter of a 1-MHz cutoff frequency is used. A three-wire serial interface is used to program and control the receiver.

To improve the linearity, in this design the filter precedes the variable gain amplifier. This requires that the filter noise be very low which leads to higher power consumption.

Interleaving gain and filtering will optimize the noise and linearity performance. Due to the low voltage operation, active RC circuits have been employed Since of their superior linearity performance. The authors' design is for a standard Bluetooth since the channel spacing is low for Bluetooth and hence has more stringent filtering requirements exist. A sixth-order Butterworth filter needs a maximum Q of 2 for any biquad section; therefore, it is preferred over a fourth-order Chebychev response.

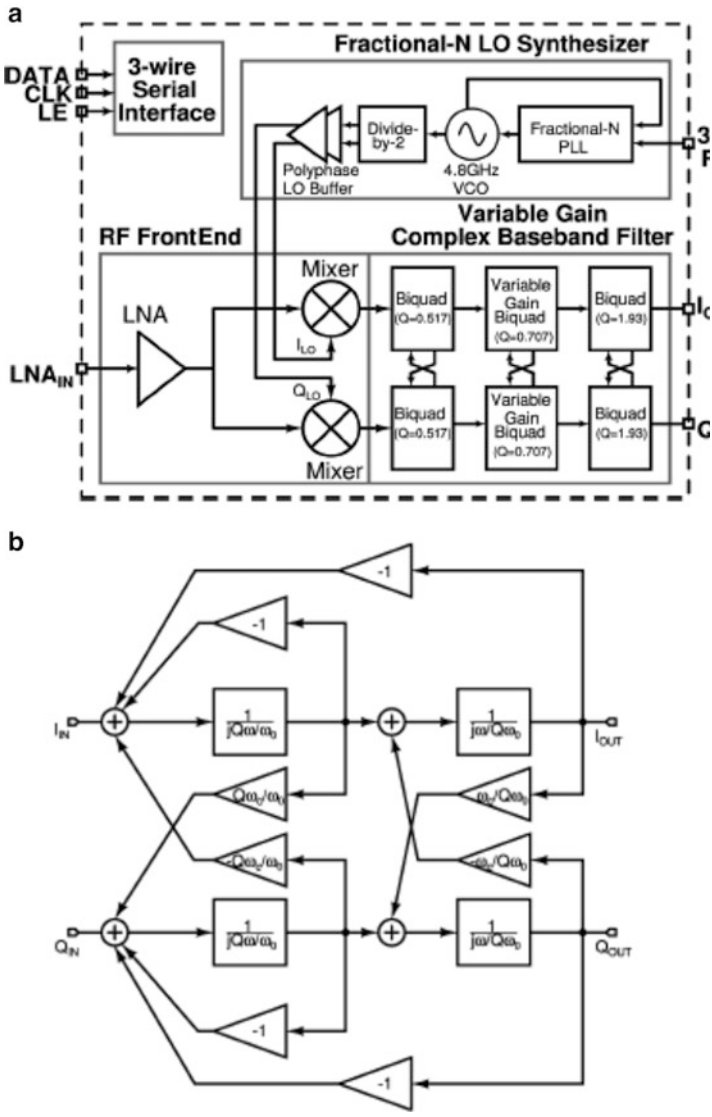


Fig. 5.3 (**a**) Block diagram of the dual-mode Zero-IF/low-IF 0.6 V receiver, (**b**) signal flow graph of a complex second-order active filter, (**c**) circuit implementation of (**b**), and (**d**) 0.6-V OTA schematic with circuit for operating the body bias (Adapted from [5.4] ©IEEE 2010)

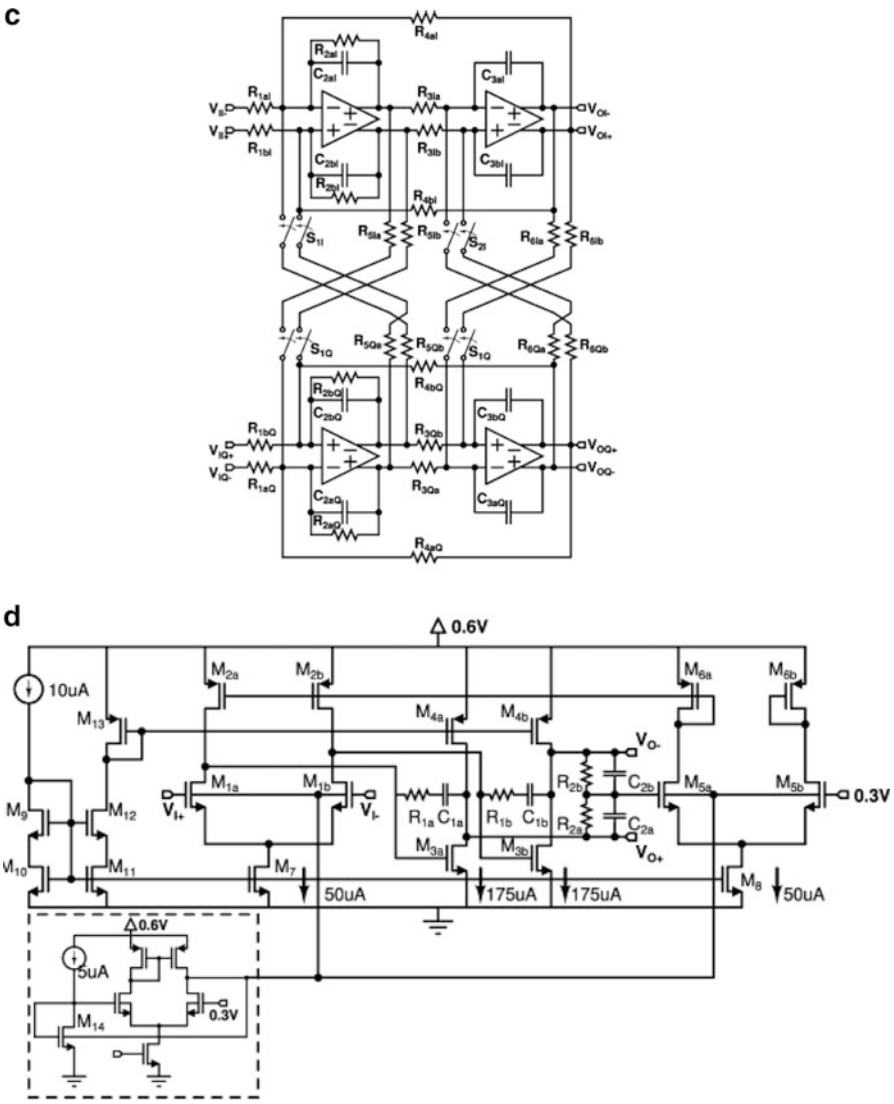


Fig. 5.3 (continued)

The design uses Tow–Thomas biquads. Due to the low pole-Q, the bandwidths of the OTAs can be lower.

In a complex first-order filter, a first-order transfer function $\frac{1}{1+\left(\frac{s}{\omega_o}\right)}$ is transformed to a band-pass transfer function $\frac{1}{1+\left(\frac{s-j\omega_c}{\omega_o}\right)}$. A second-order complex filter signal flow graph and active RC implementation are presented in Fig. 5.3b, c. In the zero-IF

Table 5.2 Radio specifications for Bluetooth (802.15.1) and Zigbee (802.15.4) operating in 2.4-GHz ISM band (Adapted from [5.4]©IEEE 2010)

		Bluetooth	Zigbee
Frequency band	[MHz]	2,400–2,480	2,400–2,483
SNR at demodulator	[dB]	15	7
Channel bandwidth	[MHz]	1	2
Data rate	[Mbps]	1	0.25
Min. receiver sensitivity	[dBm]	−70	−85
Receiver noise figure	[dB]	<28	<19
Channel spacing	[MHz]	1	5
Alternate channel rejection	[dB]	30	30
Receiver IIP_3	[dBm]	−21	−20
Received signal power	[dBm]	<−20	<−20
Synthesizer phase noise (@1 MHz offset)	[dBc/Hz]	−110	−88

mode, cross-coupling switches S_{1I}, S_{2I}, S_{1Q}, and S_{2Q} are opened to obtain a low-pass filter. The cutoff frequency is given by $\omega_c = \frac{1}{\sqrt{R_{3ab}\, R_{4ab}\, C_{2ab}\, C_{3ab}}}$. The capacitor and resistor values are set to realize the bandwidth of 1 MHz as well as to achieve low input referred noise of the filter (<3 nArms). In the low IF mode, the switches are closed and the filter characteristic shifts to a frequency ω_c, given by $\omega_c = \frac{1}{R_{5ab}\, C_{2ab}}$ $= \frac{1}{R_{6ab}\, C_{3ab}}$. Note that the filter capacitors are doubled in the low-IF mode to set the bandwidth to 1 MHz.

Since the GFSK spectrum used in Bluetooth has high energy at dc, a low IF architecture is preferred to avoid degradation due to $1/f$ noise. Since the bandwidth of the Zigbee signal is higher, the $1/f$ noise is of no consequence. A direct conversion receiver therefore is preferred for Zigbee.

The filter is tuned by using thermometer-coded and binary-weighted switched capacitors. The use of SCs helps to eliminate the nonlinearity of the varactors. In the low IF mode, the bandwidth can be tuned from 250 KHz to 2.2 MHz in steps of 40 KHz and in the zero IF mode, the filter bandwidth is tunable from 800 KHz to 2.1 MHz in steps of 30 KHz. The switches for tuning the filter bandwidth and cross-coupling switches are connected to the virtual grounds of the OAs since the signal swing that needs to be handled will be low. A nonminimum-length transistor with 600-mV forward body bias is used to reduce V_T so that the switch can be turned on stronger. The ordering of the pole-Qs of the biquads is $Q = .517$, $Q = .707$, and $Q = 1.93$ from the first to third stage, respectively. A variable gain of 0–24 dB is implemented in the input resistors of the second stage by using switched binary weighted resistors.

The OTAs (see Fig. 5.3d) are two-stage Miller-compensated types with input and output common mode voltage set to 0.3 V. Forward body biasing is used in the first stage to reduce the V_T of M_{1a} and M_{1b} to 150 mV (V_{gs} of 200 mV). Nonminimum-length devices are used to exploit the reverse channel effect. Second-stage transistors do not employ forward body bias because the biasing is more flexible in the second stage. The common mode rejection is achieved by the CMFB amplifier, which needs a bias current comparable to that in the first stage. The forward

body bias applied to transistor M_{1a} and M_{1b} is adaptive. The V_{GS} of the transistor M_{14}, which is fed with reference current, is compared with a fixed reference voltage and the error voltage is amplified to generate the needed body bias.

Shih et al. [5.5] have described a 250-MHz analog baseband chain for ultra-wide band (UWB) in 1.2 V 0.13 μCMOS process. A UWB receiver block diagram is shown in Fig. 5.4a. The RF front-end has a low gain so that the level of interferers is contained in the next analog baseband. The authors chose a current mode implementation since at low voltage, achieving high linearity with voltage mode circuits in deep submicron processes is very difficult. Voltage mode circuits also tend to have lower bandwidth at high closed-loop gains. A current mode Sallen–Key low-pass filter is used followed by programmable gain amplifiers (PGAs) and low-pass filters. At the output of the RF front-end, a large signal swing generates harmonics due to the nonlinearity of the MOS transistors used in mixers. Hence, translating the signal from the voltage domain to the current domain contains the signal swing. The WLAN 802.11a is only 700 MHz away from the 4.5-GHz channel, and therefore a single-pole low-pass filter is not adequate. Hence, this design uses a second-order current mode Sallen–Key filter. The complete baseband chain is presented in Fig. 5.4b. Following the Sallen and Key current mode filter, current mode programmable gain is realized in three stages. This is followed by a sixth-order voltage mode G_m-C filter, and again a chain of PGAs follows the G_m-C filter. An I/V converter is employed whose output is buffered to deliver the final output. The hardware is duplicated in the Q channel. The reader is referred to [5.5] for a detailed discussion on the current mode PGA. We restrict our attention here to the filtering subsystem.

A Sallen and Key current mode filter is presented in Fig. 5.4c. This can be obtained by applying the adjoint technique [5.6]. The realized transfer function taking into account the finite input resistance of the current amplifier can be derived as

$$\frac{I_o}{I_{in}} = \frac{s^2 C_1 C_2 R_1 r_i + sC_2 r_i - F}{s^2 C_1 C_2 (R_1 R_2 + r_i (R_1 + R_2)) + s(C_1 (R_1 + R_2) + C_2 (R_1 + R_2 (1 + F)) + 1} \tag{5.1}$$

Note that due to finite r_i, transmission zeroes are created. The notch frequency can be designed to lie in the range of 1.2–1.4 GHz to filter the interference signals, whereas the pole frequency is 250 KHz. Note that in this fully differential circuit, transistors M_1–M_4 form a series–series feedback-based current mirror with low input resistance. The currents are mirrored to generate FI_i as needed.

The sixth-order G_m-C filter is presented in Fig. 5.4d and is based on an LC ladder structure and is fully differential. The schematic of the G_m cell is shown in Fig. 5.4e. This uses the superfollower structure to improve the linearity. The G_m cell also has a common mode feedback loop as shown. The tuning of the G_m cell is carried out by having a calibration loop as shown in Fig. 5.4f. This consists of a G_m cell, a capacitor array, a comparator, and a digital controller. An accurate reference clock is used to control the switch across a voltage source V_2 and the output of the G_m cell to decide

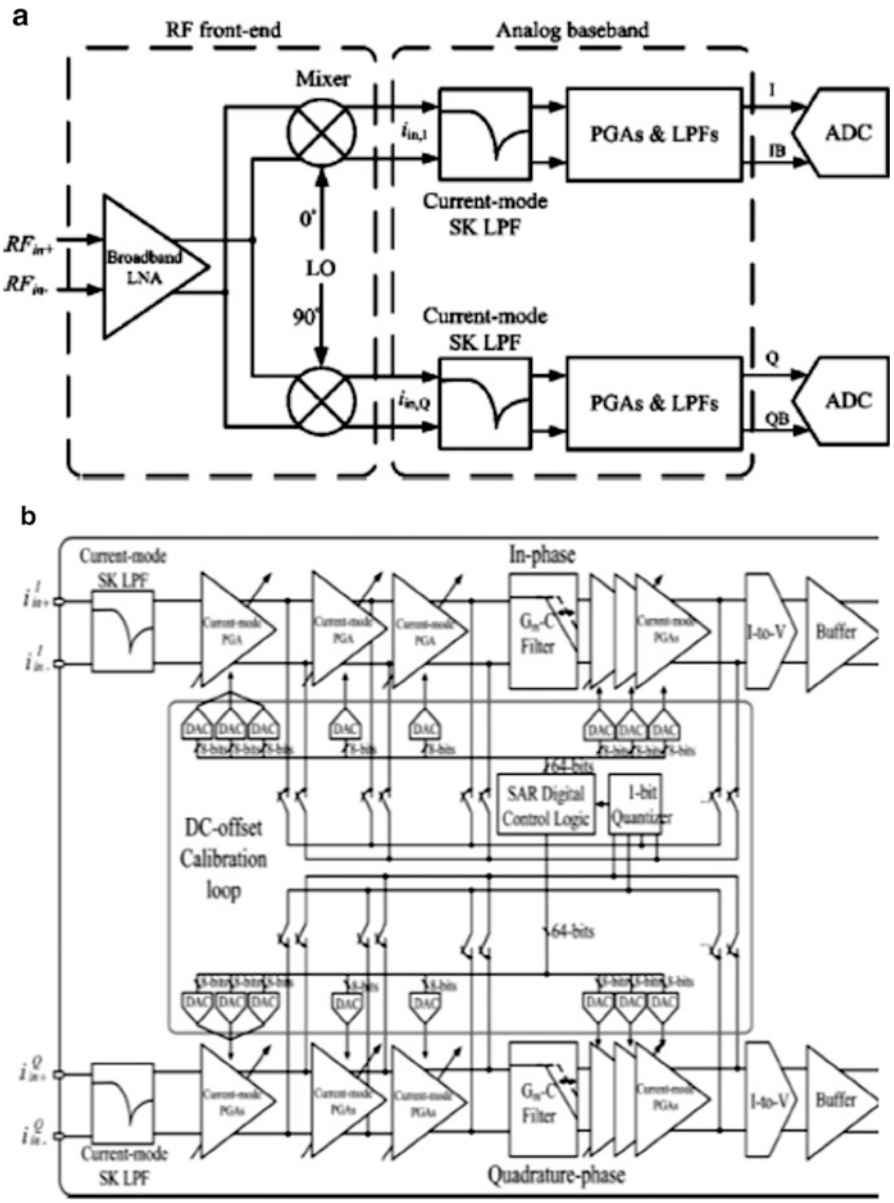


Fig. 5.4 (**a**) Architecture of a direct conversion receiver for UWB, (**b**) block diagram of the wideband wide dynamic range baseband chain, (**c**) current mode Sallen–Key LPF, (**d**) sixth-order G_m-C filter, (**e**) schematic of G_m used in (**d**), and (**f**) G_m-C calibration loop (Adapted from [5.5] ©IEEE 2010)

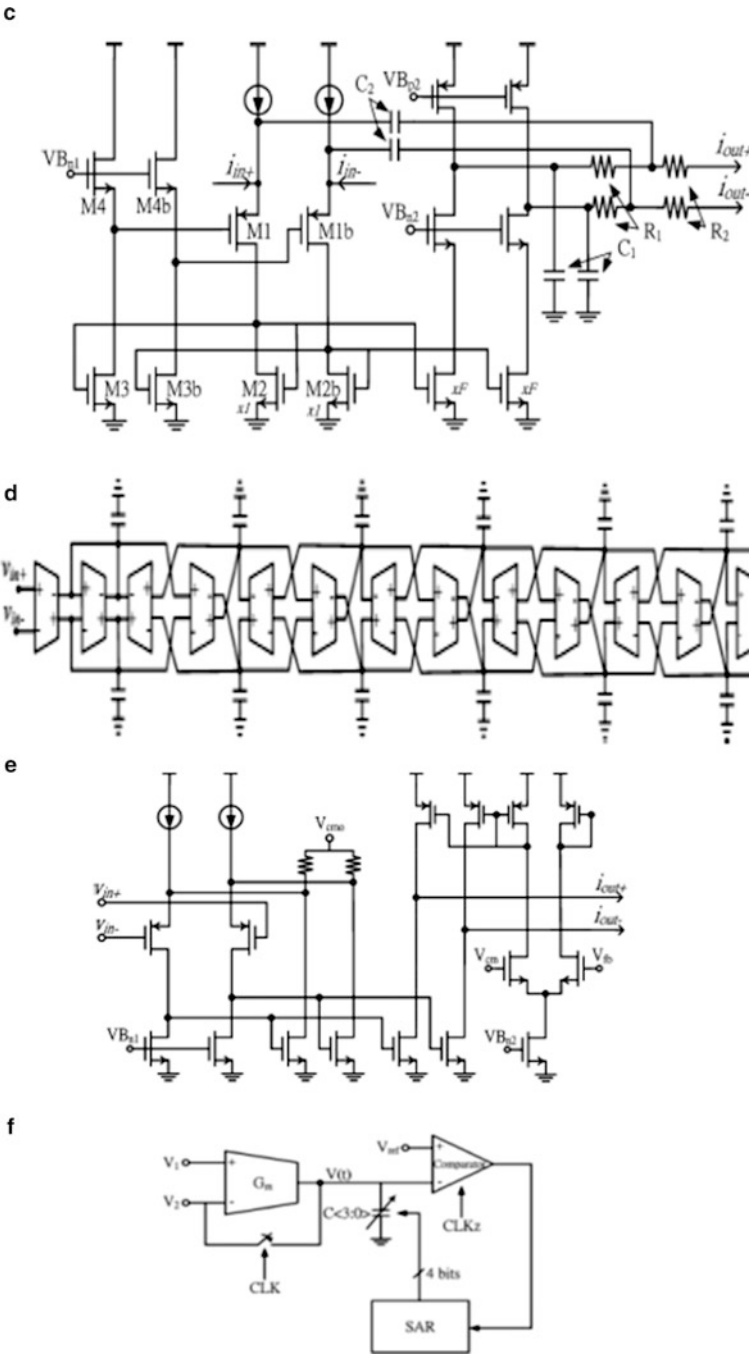


Fig. 5.4 (continued)

the charging time of the capacitor array. The output voltage of the G_m cell is compared with a V_{REF}. By using successive approximation search, the digital controller controls the capacitor array.

Vasilopoulos et al. [5.7] described a low-power, wide-band, reconfigurable integrated active RC filter. This realizes a fifth-order Chebychev or a third-order elliptic filter cascaded by a second-order delay equalizer. The cutoff frequency can be set either to 5 or 10 MHz. The active RC filter structure is presented in Fig. 5.5a and comprises a first-order filter cascaded by two biquads. In both cases the pass-band ripple is 0.1 dB and passband gain is 0 dB. Digital control signals are used to control the various resistors and capacitors using programmable arrays of the type shown in Fig. 5.5b, c. The structure of these can be controlled by one bit, as shown for typical resistance R_{1A} and capacitor C_{4C}. Each resistor in the configuration of Fig. 5.5d has three-bit control made up of a series-parallel connection of unit resistors. This has a constant part R_{con} together with a programmable part, yielding a total resistance of $R_{con} + \sum_{i=0}^{2} 2^i \frac{R}{2}$. The signal BAND controls the bandwidth of the filter. The variable part of the resistance is used for time constant compensation. All the switches are implemented using NMOS transistors with a driving voltage of 2.7 V derived from the 1 V power supply using a charge pump circuit.

The opamp employed is as shown in Fig. 5.5e, which uses two types of compensation: (a) R in series with C as well as (b) cross-coupling through the capacitors C_F. This technique has been found to increase the bandwidth of the opamp. The CMFB loop is also shown in Fig. 5.5e. The fully differential opamp uses a resistor in place of a current source for common mode rejection purposes at the expense of reduced CMRR since low voltage operation is desired. The voltage V_{CM} is typically 500 mV and is produced by the circuit, as shown. Note that V_{CM} is V_g of device M_{1a}. The transistors M_{5a} and M_{5b} pass the same current if their V_g is equal. The loop that closes through M_{5a}, M_{5B}, M_6, M_{7A}, and M_{7B} maintains the dc output voltage equal to V_{CM}. The capacitors C_1 and C_2 improve the loop phase margin so that common mode oscillations cannot be sustained.

The authors have used the RC oscillator of Fig. 5.5g together with the automatic tuning scheme of Fig. 5.5f for controlling the time constant variation. The nominal frequency of the oscillator is 500 KHz. A 32-MHz clock is used to clock a down counter preset to 32. The counter is enabled using the 500-KHz clock. The resistors of the oscillator are controlled by three bits. If the oscillator period is greater than the nominal, the down converter will reach a negative value. On the other hand, if the oscillator frequency is lower, the down counter will stop before it goes to zero. The down counter final value is added to the digital word that controls the register so that the resulting new digital word will be fed to the various resistors. Until a significant change occurs, the digital word remains the same.

The advantage of the tuning approach is that it corrects the oscillator frequency in one iteration of the algorithm.

Ghittori et al. [5.8] have described a multimode DAC+filter for reconfigurable transmitters for WLAN/UMTS and WLAN/Bluetooth application. Two devices have been proposed: (a) for WLAN IEEE 8012.11 a/b/g with a base-band width of 10 MHz and UMTS with a base-band width of 2.34 MHz, and (b) WLAN and

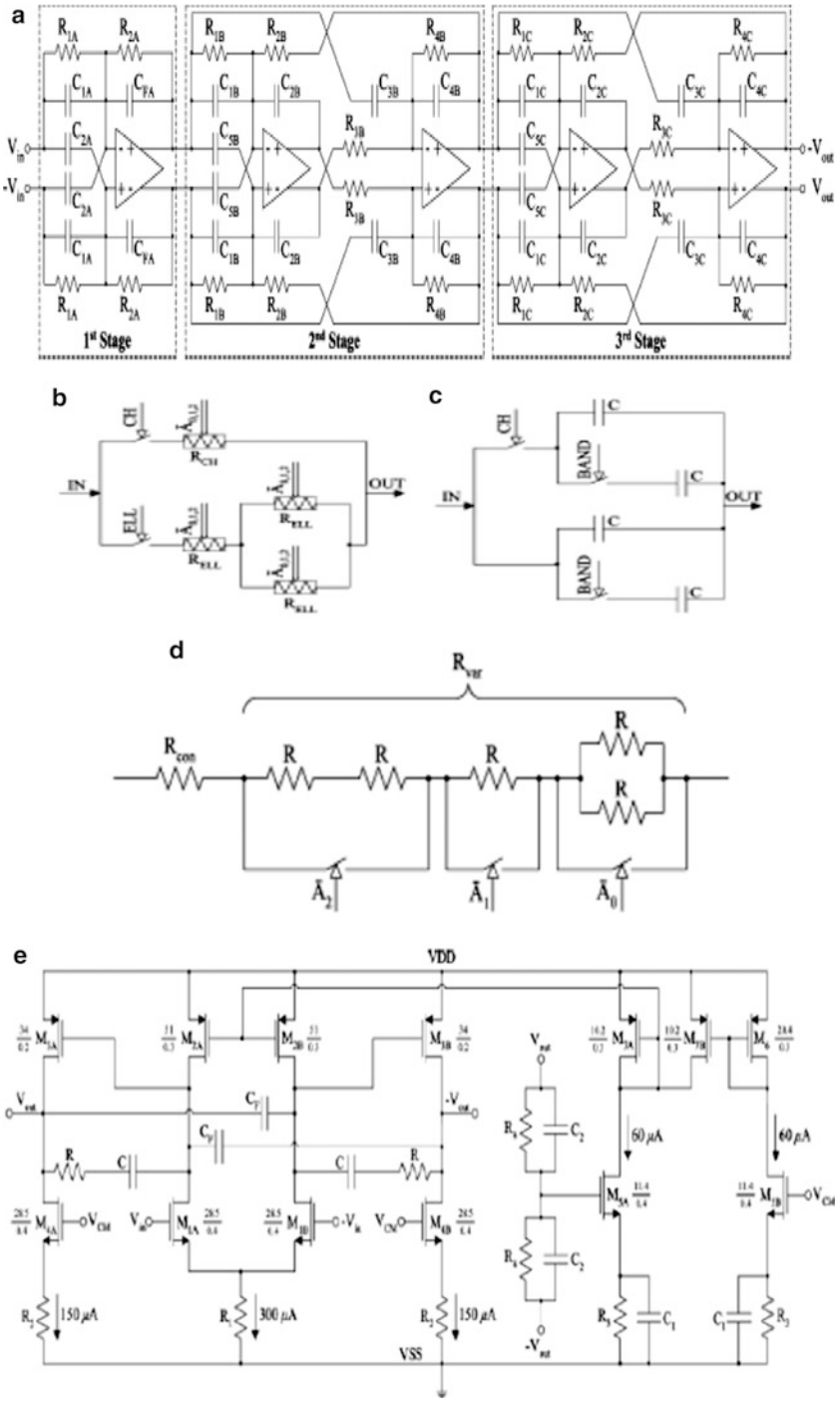


Fig. 5.5 (**a**) Topology of the filter, (**b**) structure of R_{1A}, (**c**) structure of C_{4C}, (**d**) structure of resistor used, (**e**) schematic of the operational amplifier, (**f**) conceptual control loop, and (**g**) relaxation oscillator (Adapted from [5.7] ©IEEE 2006)

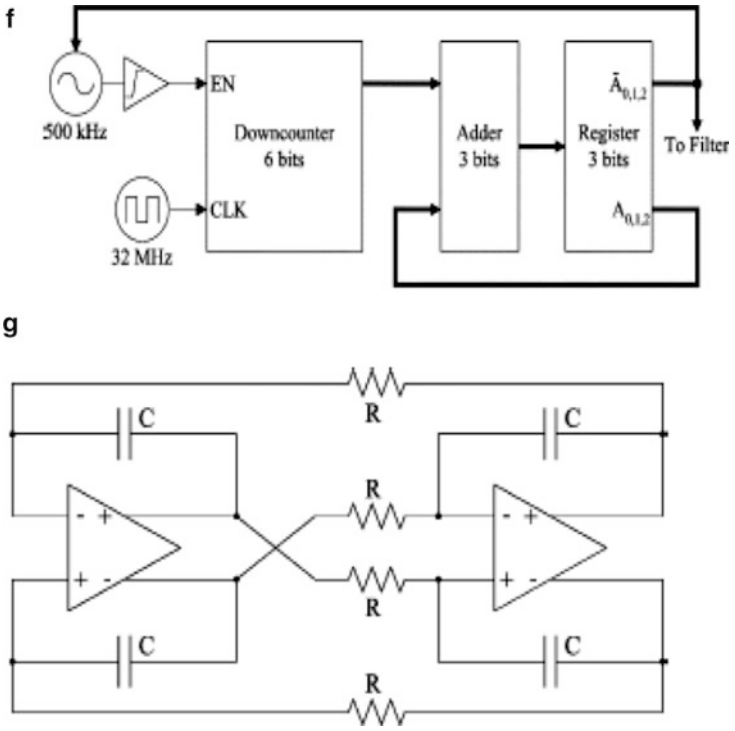


Fig. 5.5 (continued)

Bluetooth with 500-KHz base-band width. The architecture of the transmit chain is shown in Fig. 5.6a. The overall DAC and filter structure is shown in Fig. 5.6b. Note that the DAC is based on a current steering thermometer type. The programmable reconstruction filter is a fourth-order Bessel filter realized using a cascade of two Rauch (multiple feedback) low-pass filters. Note that the resistors can be selected using the bit BS. A 4-bit digital tuning circuit is provided since the tolerance needed to adjust the capacitor values is $\pm 35\%$. No cutoff frequency tuning was deemed necessary. The opamp bandwidth was 30 times the pole frequency. Fully differential Miller-compensated opamps have been employed. The opamp bandwidth is reduced for UMTS and Bluetooth modes because the needed pole frequencies are lower in this case. This is achieved by reducing the g_m of the first stage/bias current.

The current steering DAC has 255 unit current sources, each of which is implemented using a NMOS transistor in the saturation region. These are connected to a differential switching pair that diverts the current to a positive or negative output node depending on the digital control provided by the binary thermometer coder.

Kousai et al. [5.9] have described a fifth-order active RC Chebychev low-pass filter for meeting draft 802.11n next generation WLAN requirements. They have considered the nonidealities of the opamps, finite bandwidth, and nonidealities of

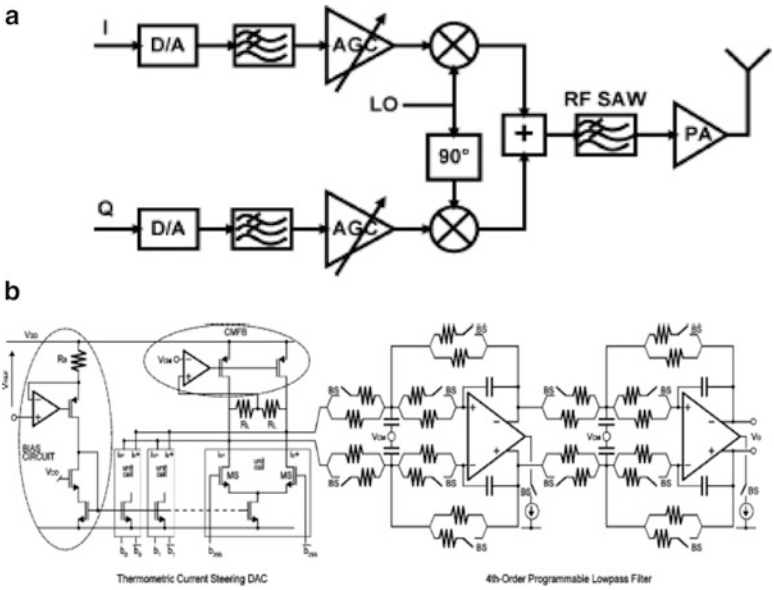


Fig. 5.6 (**a**) Direct conversion transmit chain, (**b**) overall DAC+filter structure (Adapted from [5.8] ©IEEE 2006)

programmable resistors. The variable resistor can be realized as shown in Fig. 5.7a or in the "one-hot" configuration shown in Fig. 5.7b. However, the latter has the advantage that one parasitic capacitance is at virtual ground of the opamp, whereas the other parasitic depends on the tap position. Due to the distributed parasitic capacitance, the equivalent pole-frequency of the resistor can be very low. As such, the authors use the configuration of Fig. 5.7c which also is a one-hot configuration and has the equivalent circuit as shown. An integrator using such a variable resistor can be compensated by using a resistance in series with the integrating capacitor as is well known.

The authors have realized a fifth-order ladder filter as shown in Fig. 5.7d. By switching the capacitors C_1, C_2, and C_3, the bandwidth can be changed between 19.7 and 8.9 MHz. Fine tuning of the bandwidth is possible using R_V between 19.3 and 20.1 MHz.

The second-order LPF replica shown in Fig. 5.7e is used to facilitate tuning the main filter of Fig. 5.7d. This replica filter is similar to the third factor (quadratic factor) of the fifth-order transfer function. The tuning procedure is illustrated in Fig. 5.7f. Using R_v, the pole-frequency can be tuned and next using R_{C4}, compensation can be achieved. The filter tuning system is presented in Fig. 5.7g which uses a clock of 40 MHz/20 MHz and generates 20 MHz/10 MHz. This will generate differential input signals for the replica filter and reference signals (see Fig. 5.7h). The signal is fed to the replica filter whose output amplitude is compared with the reference signal. Ideally, the amplitude should be 16 V_{in}/π.

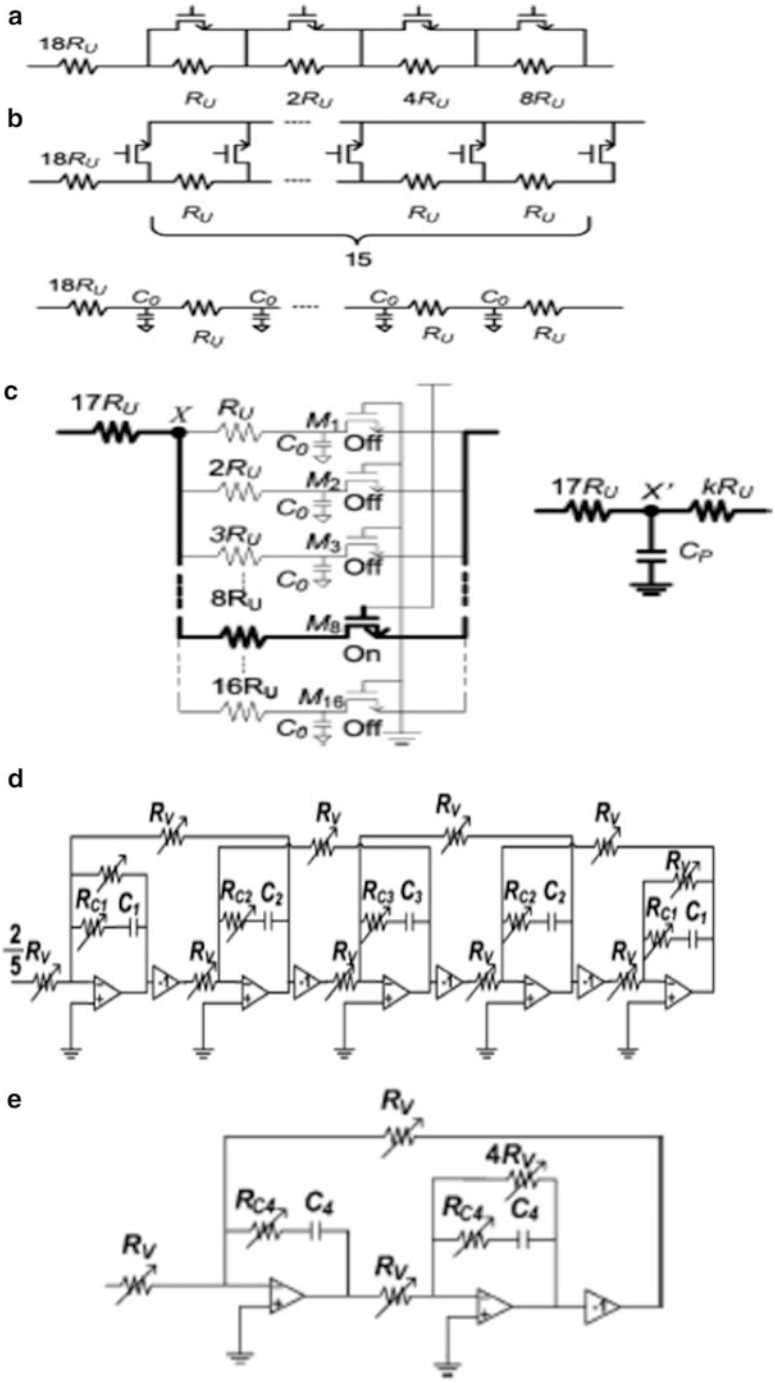


Fig. 5.7 (**a**) Binary-weighted resistor bank, (**b**) one-hot variable resistor and its equivalent circuit, (**c**) variable resistance implementation, (**d**) fifth-order filter schematic, (**e**) schematic of second-order replica filter, (**f**) filter tuning procedure, (**g**) block diagram of filter tuning system, and (**h**) schematic of reference signal generator (Adapted from [5.9] © IEEE 2007)

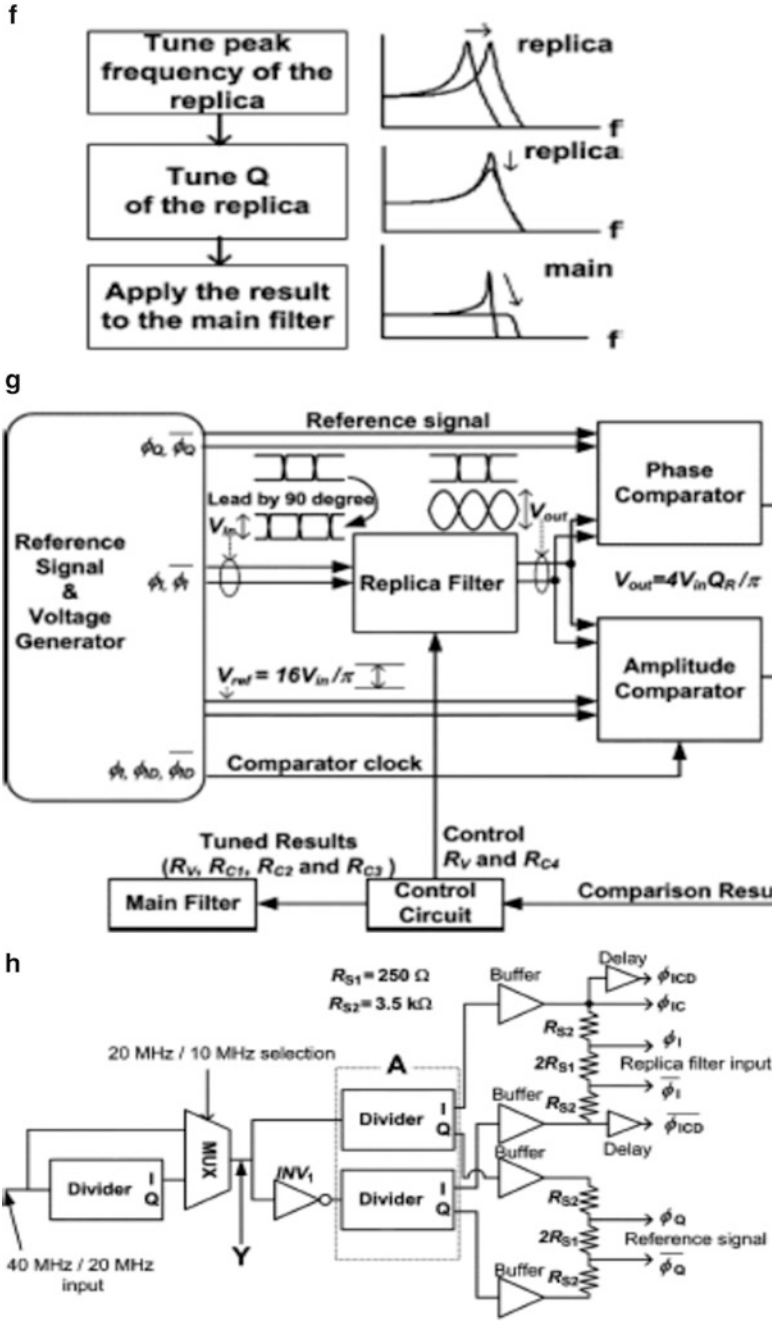


Fig. 5.7 (continued)

The amplitude comparator shown in Fig. 5.8a uses the SC technique. The control block adjusts R_V to minimize the phase difference due to the nonideal opamp bandwidth. Next, Q_R is tuned using R_C based on the amplitude comparator.

The schematic of the amplifier used is shown in Fig. 5.8b. It is a two-stage amplifier followed by a common source amplifier. The differential amplifier is a folded cascode type. The biasing circuit is shown in Fig. 5.8c where I_{CONST} and I_{PTAT} are temperature-independent current and current proportional to the temperature generated by a bandgap reference.

Yoshizawa and Tsividis [5.10] have proposed a channel select filter with agile blocker detection and adaptive power dissipation. In order to keep the power dissipation low, a detector circuit monitors the blocker levels and controls the bias currents of the filter. The block diagram of such a system is shown in Fig. 5.9a. This concept is applied to a first-order active RC filter as shown in Fig. 5.9b. The differential input signal of the opamp is nonzero due to the finite bandwidth of the opamp. A level detector monitors this signal and generates a bias voltage that can control the open loop gain of the opamp by controlling the transconductance.

To monitor the blocker signal level, it may be preferable to have a frequency selective characteristic before the peak detector circuitry. The circuit of the level detector is presented in Fig. 5.9c. The circuit performs preamplification, CM rejection, peak detection, and loop filtering. The input capacitors block the dc signal. An integrator is used as the loop filter so that the dc gain of the loop filter is large and hence small v_x can be sensed. Dynamic biasing in the loop filter helps fast ramp-up when a large blocker appears. Two differential pairs are used that are initially used to reduce the attack time. When P_o turns on, the 1 μA differential pair goes off. The operating current reduction makes the loop filter time constant larger. The amplifier used follows the scheme of Fig. 5.9d wherein the common mode path and signal path are different. The CM path is through TA2 and TA3 whereas the signal path is through TA1. Such separation ensures that the signal path bandwidth is more than that of the common mode feedback path.

The complete fully differential class AB output stage is shown in Fig. 5.9e. The current mirrors M_1 and M_2 provide quiescent current to the opamp. The cascaded PMOS pair M_3 and M_4 provide the error control current I_{CNT} (10–150 uA) through control by V_{CNT}. A class AB output stage is employed. The frequency compensation uses cascode Miller forward-type through two capacitors C_C and C_f (see Fig. 5.9f). At low frequencies, C_f is not effective. At high frequencies, the current through C_f cancels the phase shift caused by M_1 with C_{P1} (where C_{p1} is the parasitic capacitance at drain of M_1). Yoshizawa et al. [5.10] have applied the proposed technique for a fifth-order leap-frog type active RC ladder filter in the first and second stages as in the subsequent sections; the blocker level would have already been reduced (see Fig. 5.9g).

Hollman et al. [5.11] have described a dual-mode band-pass filter for PDC and WCDMA. In PDC mode, the cutoff frequency is 13 KHz and a third-order filter will be required whereas in the WCDMA case, a fifth-order Butterworth filter with cutoff frequency 2.1 MHz will be needed. The complete circuit of the filter is presented in Fig. 5.10a.

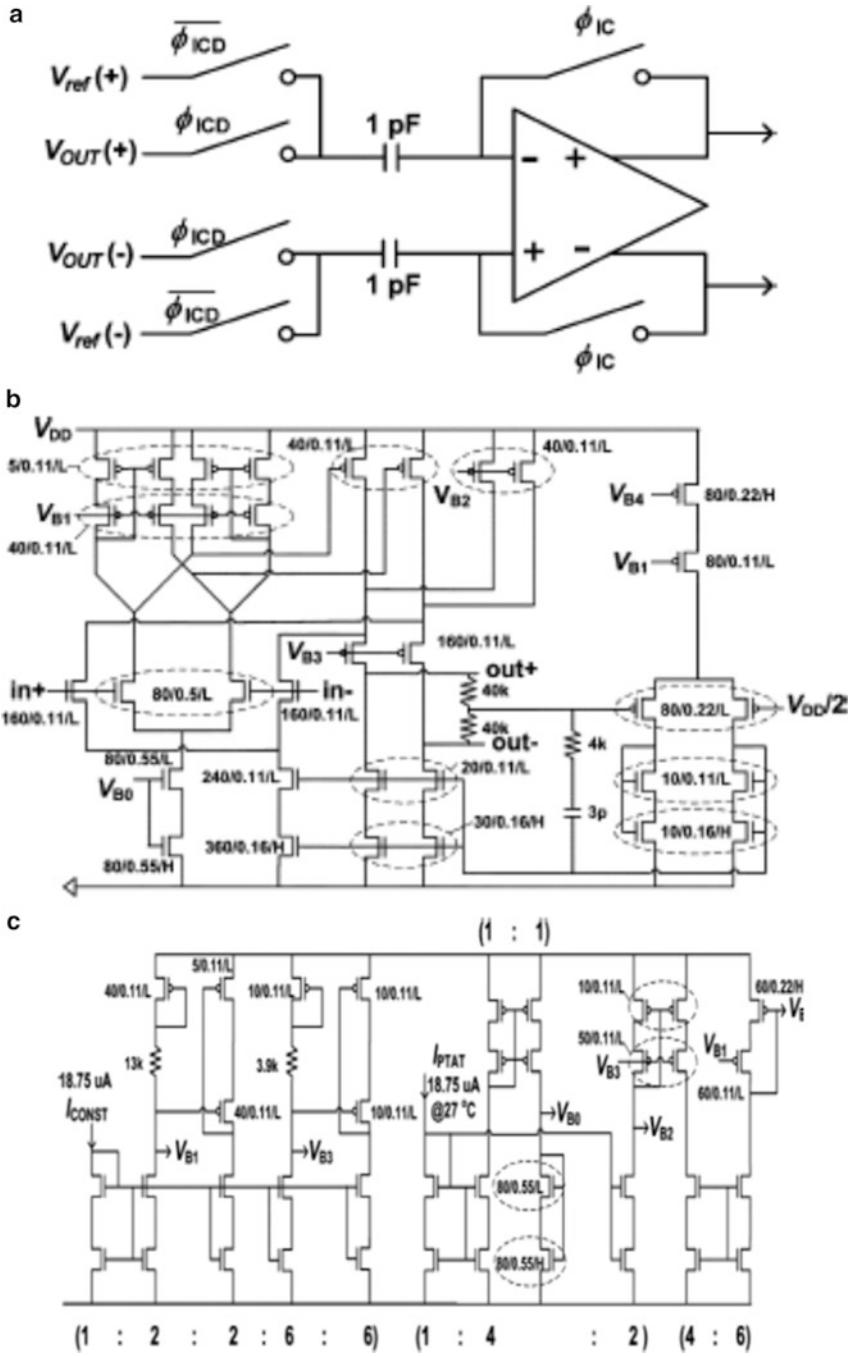


Fig. 5.8 (**a**) Amplitude comparator schematic, (**b**) schematic of the amplifier, and (**c**) schematic of the biasing circuit (Adapted from [5.9] ©IEEE 2007)

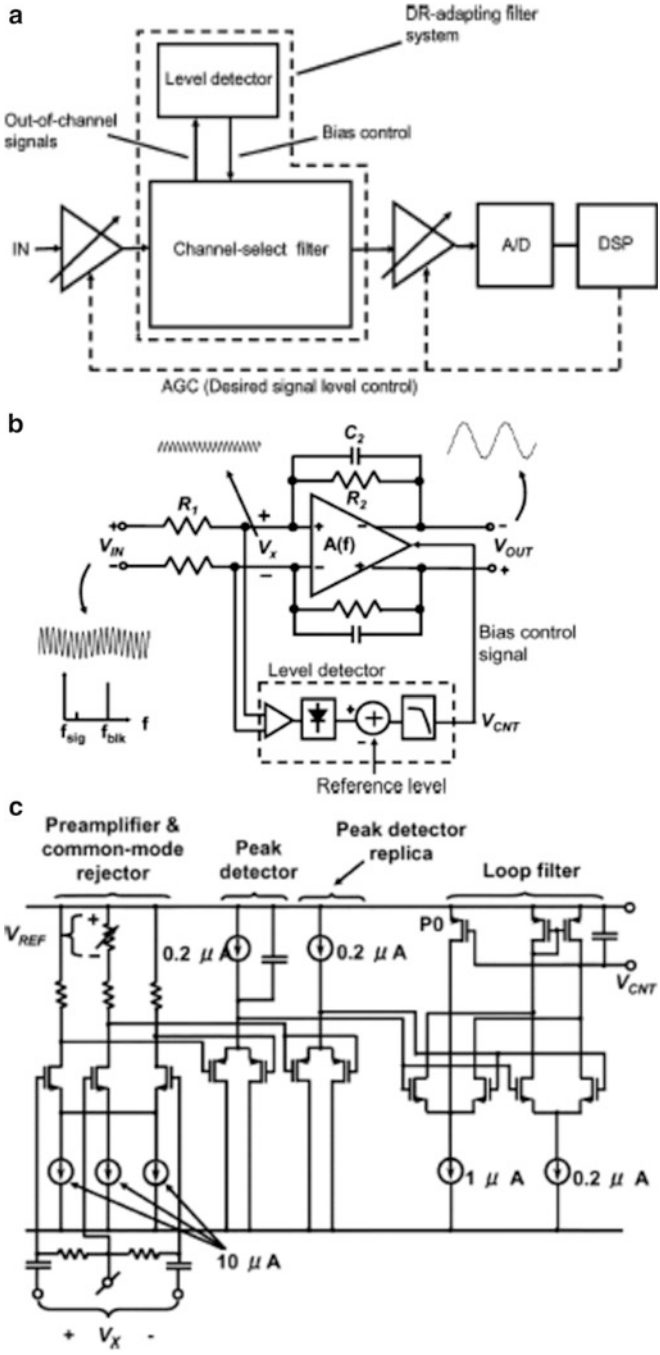


Fig. 5.9 (**a**) Dynamic range adapting channel filter system schematic, (**b**) first-order opamp RC filter with bias control loop, (**c**) level detector circuit, (**d**) opamp using Class AB output stage, (**e**) fully differential class AB output stage with variable bias current, (**f**) two-stage folded cascode amplifier with compensation network, and (**g**) fifth-order leap-frog opamp RC ladder filter (Adapted from [5.10]©IEEE 2007)

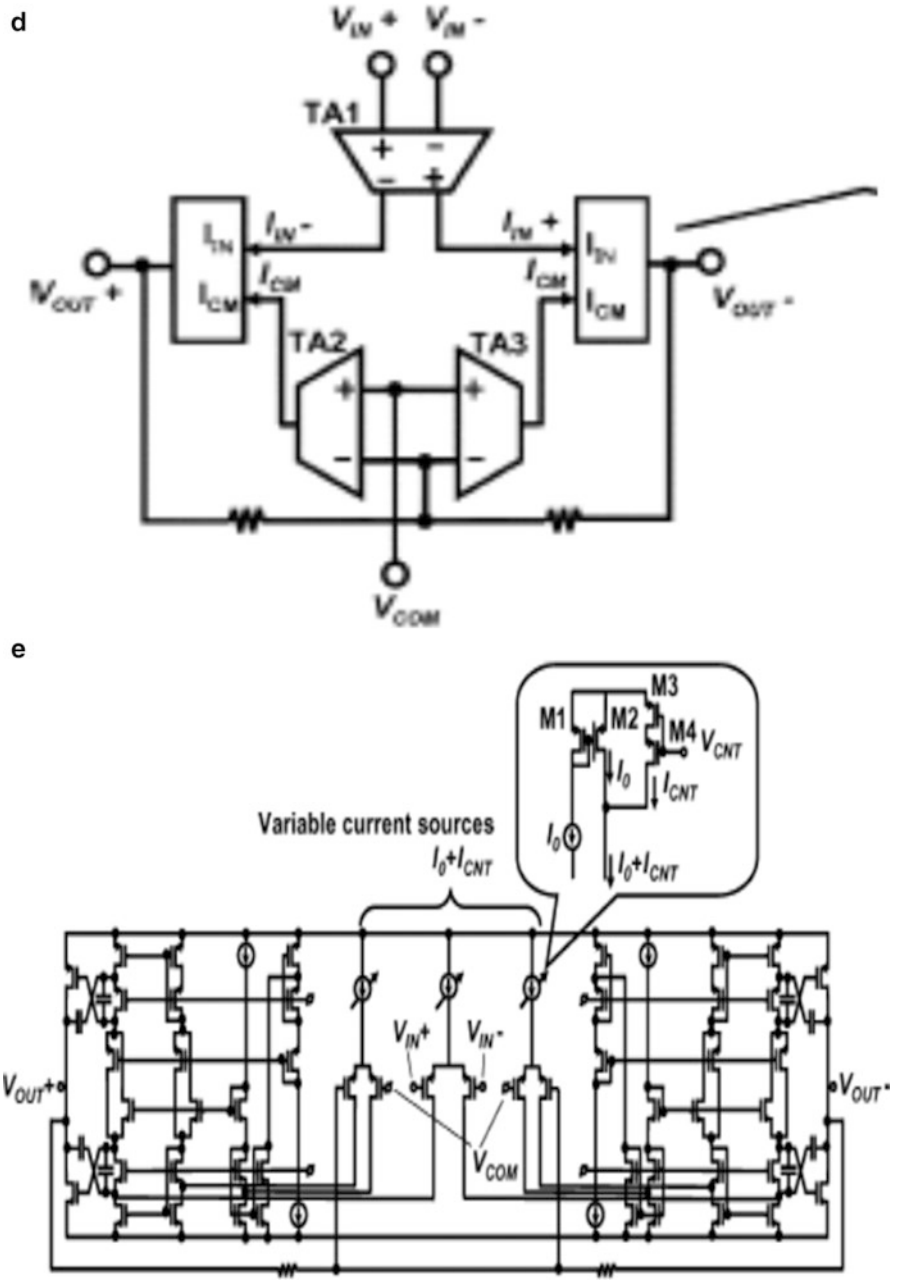


Fig. 5.9 (continued)

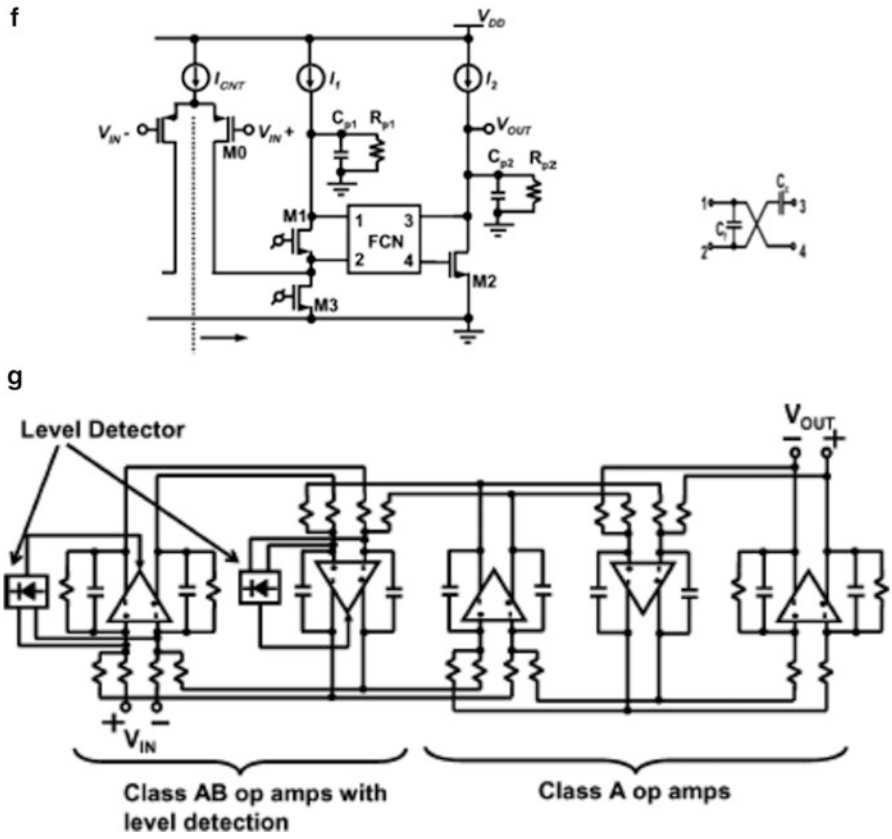


Fig. 5.9 (continued)

The filter is based on the leap-frog ladder technique. In PDC mode, the second and third opamps are disconnected and powered down. A gain of 18 dB was implemented in the filter. The first opamp bias current was twice that of the other opamps so as to reduce distortion. The opamp is presented in Fig. 5.10b with PMOS input transistors for low noise design. The opamp is Miller compensated with RHP zero nulling resistors realized using NMOS transistors. The GBW was made programmable. In the PDC mode, the bandwidth is lower and therefore the bias current can be reduced. This is done by switching the width of the PMOS current source transistors (see Fig. 5.10b). The corner frequency was made tunable using PCAs for capacitors. Five-bit tuning was used. The capacitors were shared between the two modes. As a consequence, the resistor spread will be higher between the two modes. Large resistors were realized using *T* networks.

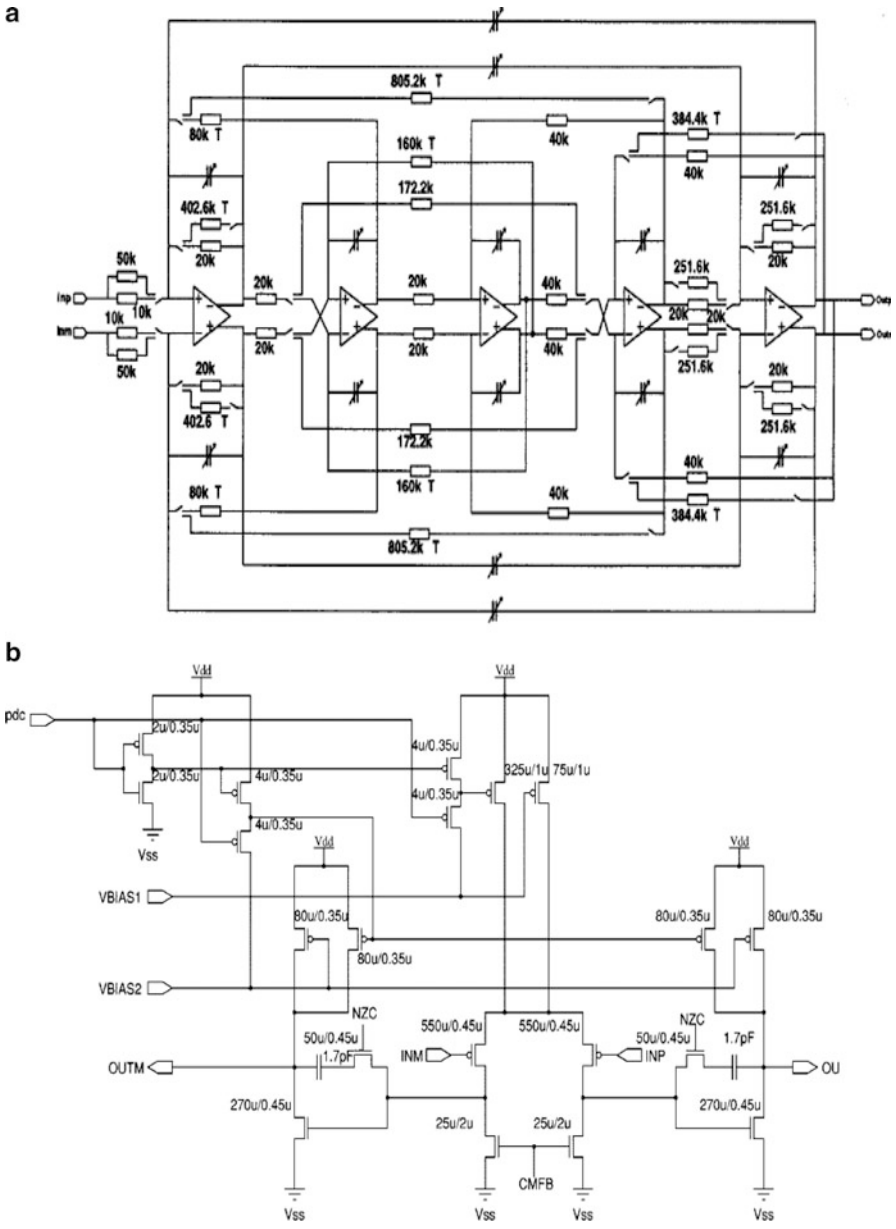


Fig. 5.10 (**a**) Dual-mode bandpass filter schematic, and (**b**) opamp used in (**a**) (Adapted from [5.11] ©IEEE 2001)

5.3 Active RC Filters for ADSL

A fourth-order Chebychev high-pass filter for asymmetric digital subscriber line (ADSL) and VDSL receivers in a 65 nm CMOS process has been described by Lin et al. [5.12]. The ADSL signal spectrum at the customer premises equipment (CPE) is shown in Fig. 5.11a. This uses frequency division multiplexing with DMT (discrete multitone) signaling. The upstream band exists from 25 to 276 KHz. The analog front-end architecture for ADSL/VDSL application is shown in Fig. 5.11b which contains a high-pass filter in the receive path to allow only the downstream frequency band. The long loop with bridged taps of about 15,000 ft. attenuates the receive in-band signal from the local transmitter. The front-end needs to perform echo cancellation for the signal from the local transmitter (25–138 KHz) signal which may be large due to the ineffective hybrid function. The presence of HPF reduces the echo signal. The high-quality LC filters conventionally used are costly whereas the low-quality LC filters generate noise pickup and are nonlinear. Moreover, this LC high-pass filter is not tunable to support various ADSL modes (Annex A, B, M) which have different frequency bands [5.13]. State-of-the-art systems use very high bit rate DSL (VHDL) which may extend up to 17-MHz frequency band for which a high-pass filter may not be necessary in the case where there is no transmission in the 28–138 KHz band. However, the passive high-pass filter cannot be bypassed. The active version of the HPF features low noise the same as that of the LC filter in the range 2–3 nV/$\sqrt{\text{Hz}}$ and cutoff frequency of 140 KHz.

The Lin et al. architecture [5.12] uses innovative techniques to reduce the noise. The evolution of their architecture is sketched in Fig. 5.11c. The top architecture uses integrators and resistive feedback. The architecture shown in the middle uses capacitive feedback so that the noise contribution of the resistors R_0, R_1, R_4, R_6, R_8, and R_{10} in topology 1 does not exist in this case. The topology in the bottom shown in Fig. 5.11c uses capacitive feedback and also feedforward in order to realize transmission zeroes. Scaling for minimum noise can be done by scaling the capacitors properly. The authors have shown that the third topology requires half the capacitance of topology 2 and one fourth that of topology 1.

The complete circuit of the fully differential filter is shown in Fig. 5.12a. Note that the gain of the filter is programmable from −12 to 30 dB with a 6 dB step by changing the capacitor ratio C_o/C_1. The four integrator resistors vary with the gain control to maintain the dynamic range. The corner frequency of the filter is variable from 160, 320, and 640 KHz and is also fine tunable from −30% to 40% with a 10% step to cover process variation. All tuning is done by programming R_3, R_5, R_7, and R_9. Filter dynamic range is programmable by varying integrator resistors and capacitors C_8 and C_{10} to support PAR (peak-to-average ratio) of 6.5–7.3. The summing amplifier (see Fig. 5.12b) is a two-stage amplifier. A combination of cascode compensation and Miller compensation has been used. Compensation capacitors track the changes in the programmable gain in order to maximize the closed-loop bandwidth. A PMOS input-type differential amplifier with a small gate area has been used to reduce the noise.

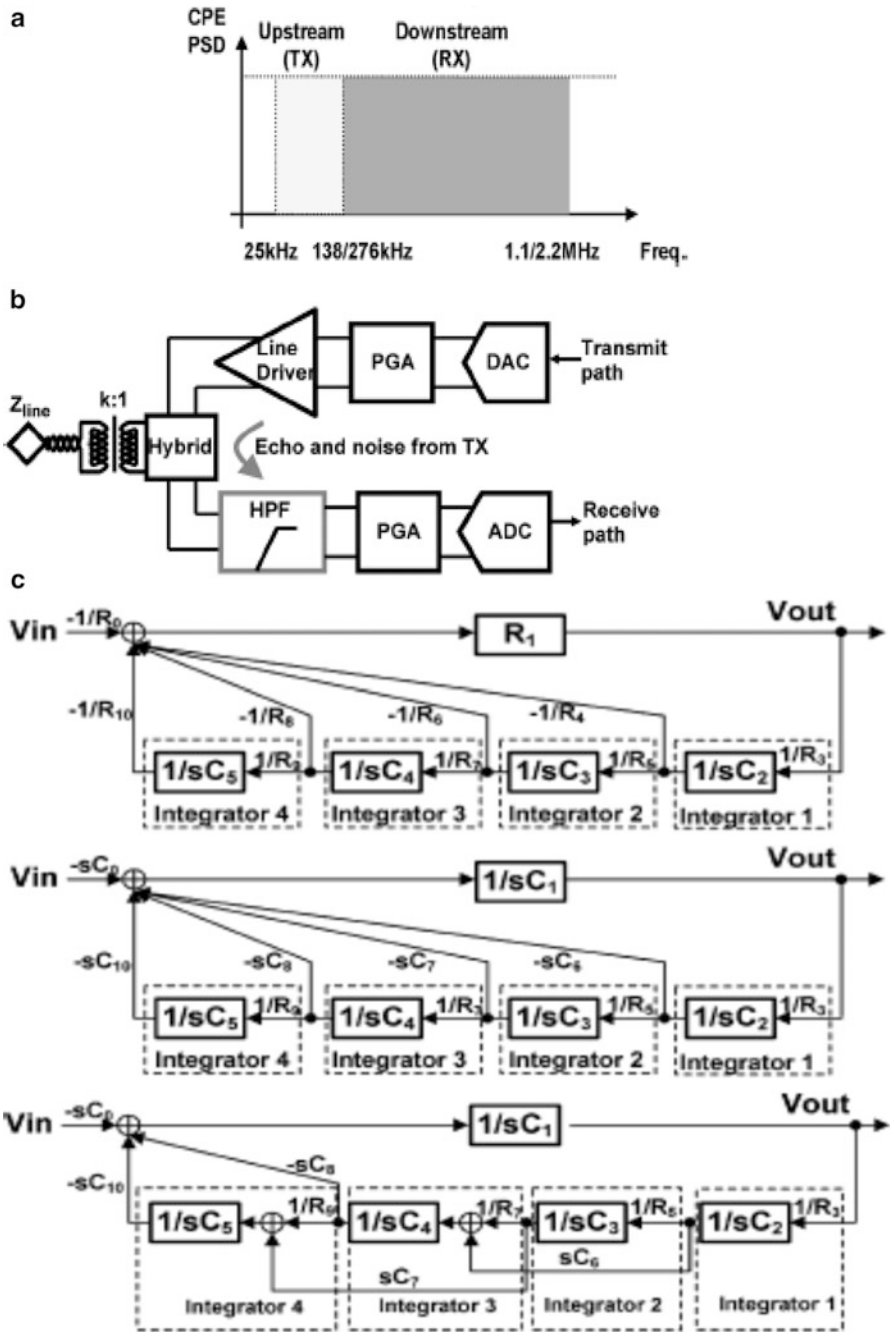


Fig. 5.11 (**a**) ADSL CPE frequency spectrum, (**b**) AFE block diagram, and (**c**) fourth-order single loop HPF topologies (resistive feedback, capacitive feedback, modified capacitive feedback) (Adapted from [5.12]©IEEE 2009)

The NMOS devices M_8, M_9, M_{19}, and M_{20} in the common mode feedback path use emitter degeneration to reduce their flicker noise.

The RC time constant variation by $\pm$ 30% over process and temperature is taken care of by having a frequency control loop. A relaxation oscillator shown in Fig. 5.12c is used to generate an oscillation frequency proportional to $1/R_oC_o$. These devices are matched with those in the filter. The resistors are tuned using a 3-bit control for a tuning accuracy better than 10%. The RC time constant is extracted and converted to digital form using a counter running at a known crystal oscillator frequency.

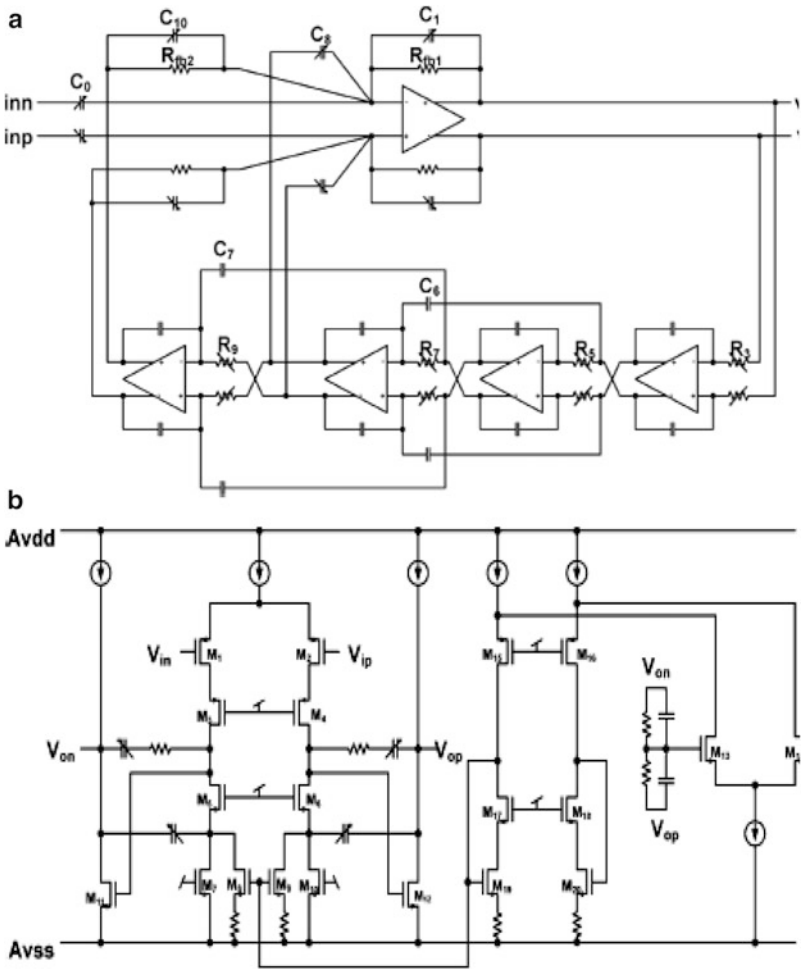


Fig. 5.12 (**a**) HPF top-level diagram, (**b**) summing amplifier schematic, and (**c**) RC-based relaxation oscillator showing timing of discrete resistor (Adapted from [5.12] ©IEEE 2009)

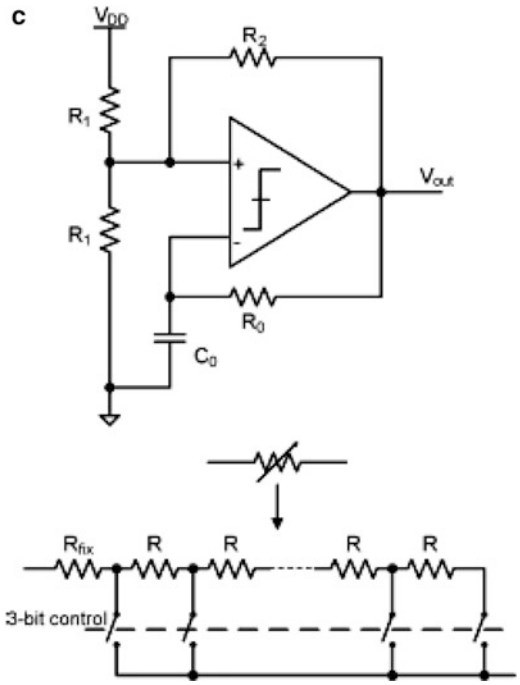


Fig. 5.12 (continued)

5.4 Active RC Filters for Software Radio

Giannini et al. [5.14] have described flexible base-band analog circuits for software radio front-ends. The architecture of their chip presented in Fig. 5.13a uses switchable opamps (SOA) shown in Fig. 5.13b which can be switched off and whose bandwidth can be programmed using a PCA for the Miller capacitor. Several SOAs can be connected in parallel to realize a flexible opamp. The common mode signal is obtained by using programmable resistors R_{cmfb} (see Fig. 5.13c). The flexible opamp (FLOA) features reconfigurable bandwidth, dynamic impedance scaling, and power scalability. A sixth-order filter comprising two active G_m-RC cells and one Rauch filter are used as shown in Fig. 5.13d. The Rauch cell improves the linearity whereas the active G_m-RC cells have a limited linearity due to the lack of virtual ground. The power will not scale with the change in cutoff frequency of the Rauch filter whereas in the active G_m-RC filter, the unity gain bandwidth scales with the cutoff frequency. The variable gain amplifier (VGA) is made up of two gain stages using programmable resistor arrays and one of the stages can be bypassed if needed (see Fig. 5.13e).

5.5 Active RC Filters for Other Applications

Tekin et al. [5.15] extended the well-known noise shaping techniques used in oversampled A/D converters to active filters. They observe that FDNR-based filters can be designed to shape the noise due to resistors and opamps so that the noise is high-pass in nature and lies outside the pass-band. The architecture of a third-order

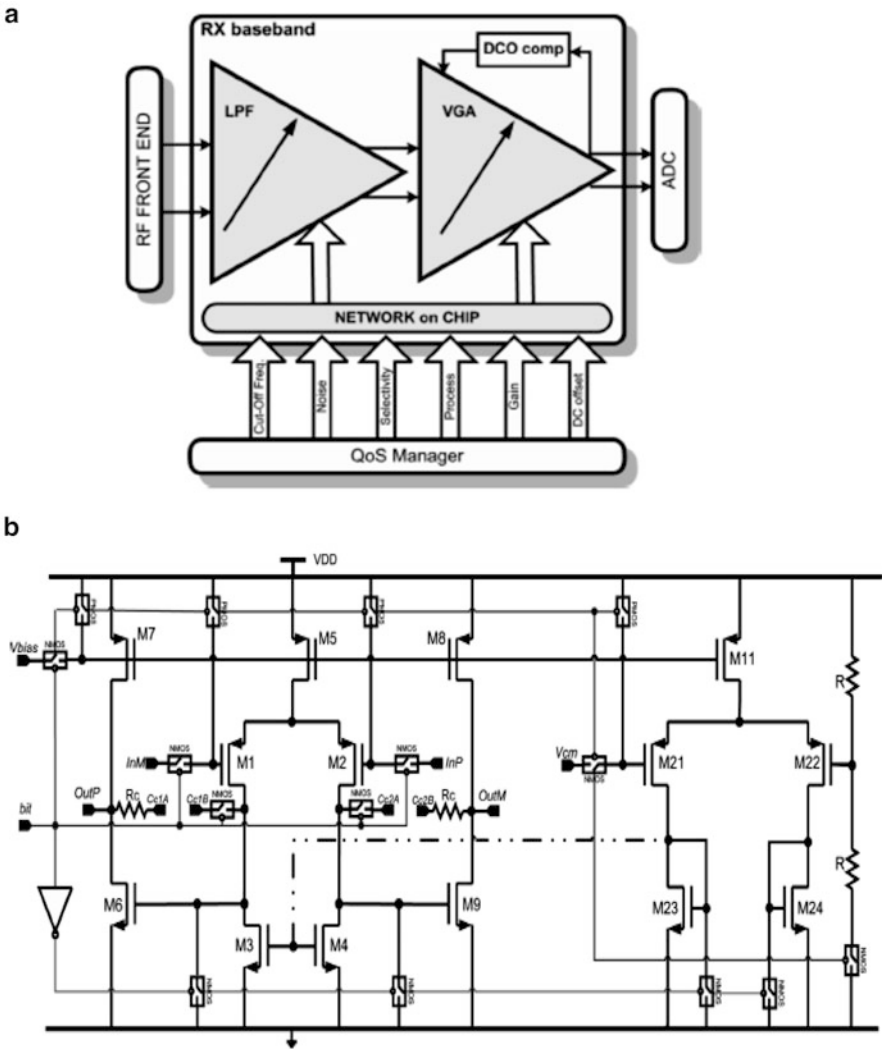


Fig. 5.13 (**a**) Analog base-band section for software-defined radio front-end, (**b**) switchable Miller opamp, (**c**) simplified structure of FLOA (flexible opamp), (**d**) flexible low-pass filter using G_m-R-C and active RC Rauch sections, and (**e**) variable gain amplifier (VGA) (Adapted from [5.14] ©IEEE 2007)

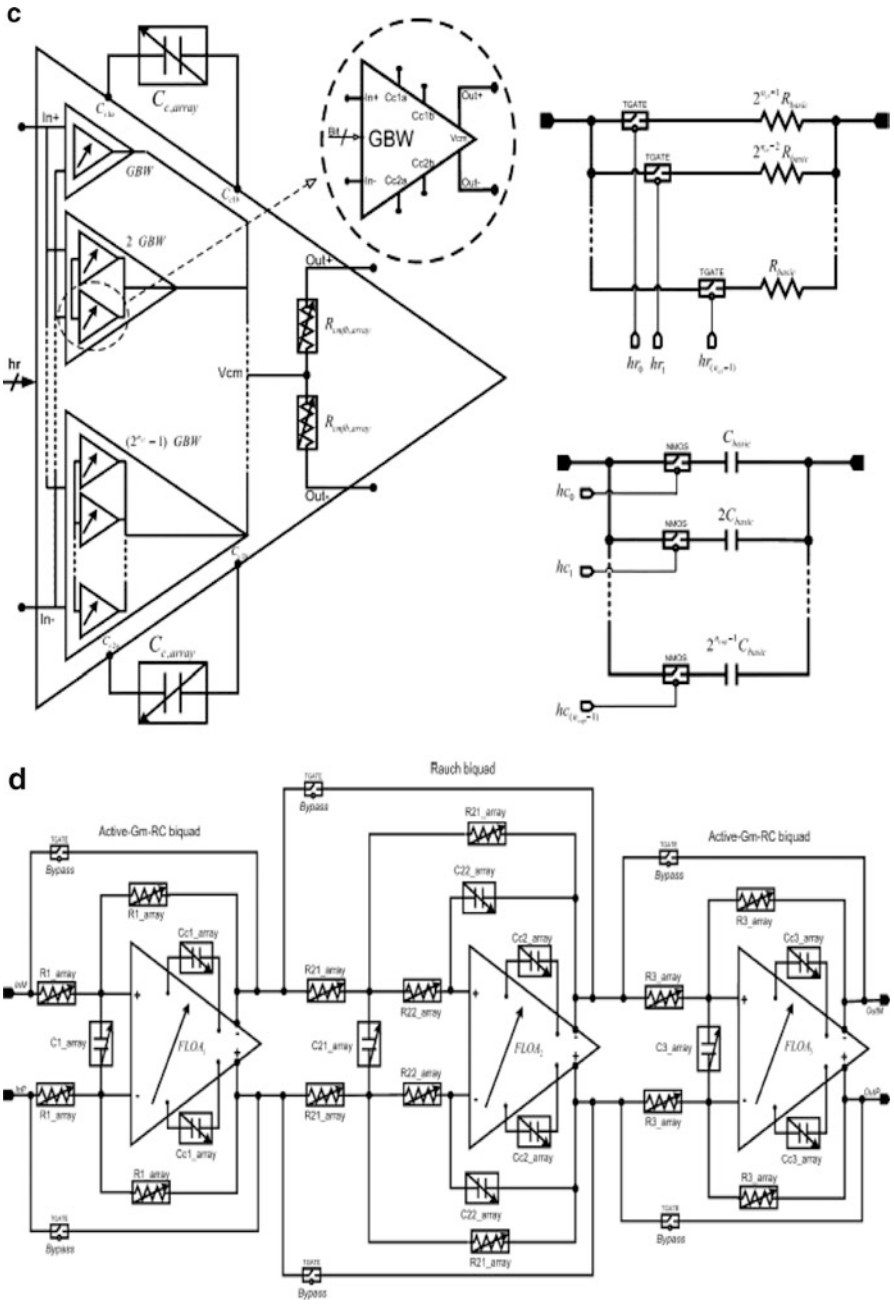


Fig. 5.13 (continued)

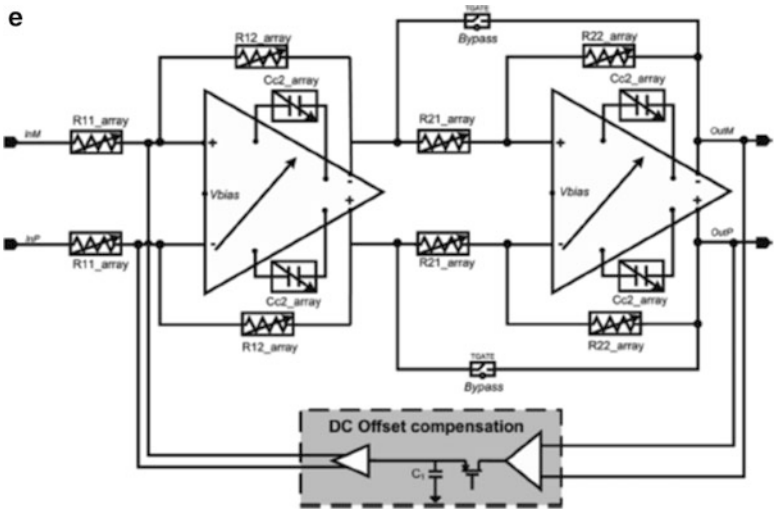


Fig. 5.13 (continued)

prefilter is shown in Fig. 5.14a which results in low noise and high dynamic range.

A mixer precedes the third-order elliptic filter in the receiver as shown in Fig. 5.14b. The resistor R_1 belongs to the mixer and also serves as part of the filter. The transfer function of this filter of Fig. 5.14b can be derived as

$$\frac{V_o}{I_{in}} = \frac{R_f\left(s^2 D R_z + 1\right)}{s^3 D R_z R_f C_f + s^2\left(D R_z + D R_f\right) + s R_f C_f + 1} \tag{5.2}$$

where $D = \frac{C_1 C_2 R_1 R_3}{R_2}$. It can be shown that the noise transfer functions of resistors R_1, R_2, and R_3 are high-pass-shaped. The noise of resistor R_z is second-order and hence can be ignored. The noise due to opamp1 and opamp2 are dominated by the "s" term in the numerator of the third-order transfer function. The total integrated noise can be reduced by choosing a small C_1 value. However, scaling for optimal dynamic range within the FDNR block so as not to saturate opamp1 and opamp2 necessitates a larger value of C_1. The advantage of noise shaping is that the design can use large resistors and reduce the capacitance leading to a low chip area.

The second stage—post-mixer amplifier (PMA)—uses the topology of Fig. 5.14c which is based on an instrumentation amplifier. In this, an asymmetric FDNR (AFDNR) is used. In this case, the current at one port satisfies the V–I relationship of a FDNR whereas the other port is connected to the opamp output as shown. This configuration helps to attenuate the blockers while still maintaining a low input referred noise for the PMA section. The transfer function of the instrumentation amplifier of Fig. 5.14d can be derived as

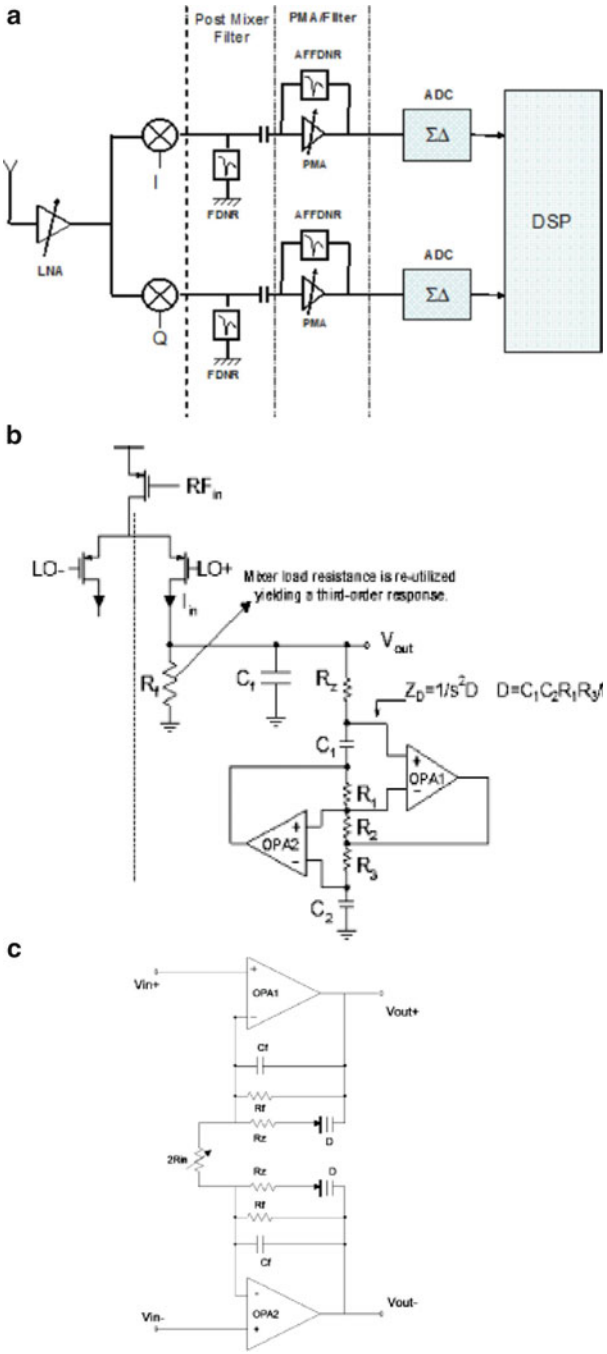


Fig. 5.14 (**a**) Block diagram of filter cascade employed in mobile TV tuner, (**b**) single-ended schematic of the third-order elliptic filter at the mixer output, (**c**) amplifier with AF(asymmetric floating) FDNR feedback, (**d**) fully differential implementation, and (**e**) folded cascode class AB opamp schematic (Adapted from [5.15] ©IEEE 2009)

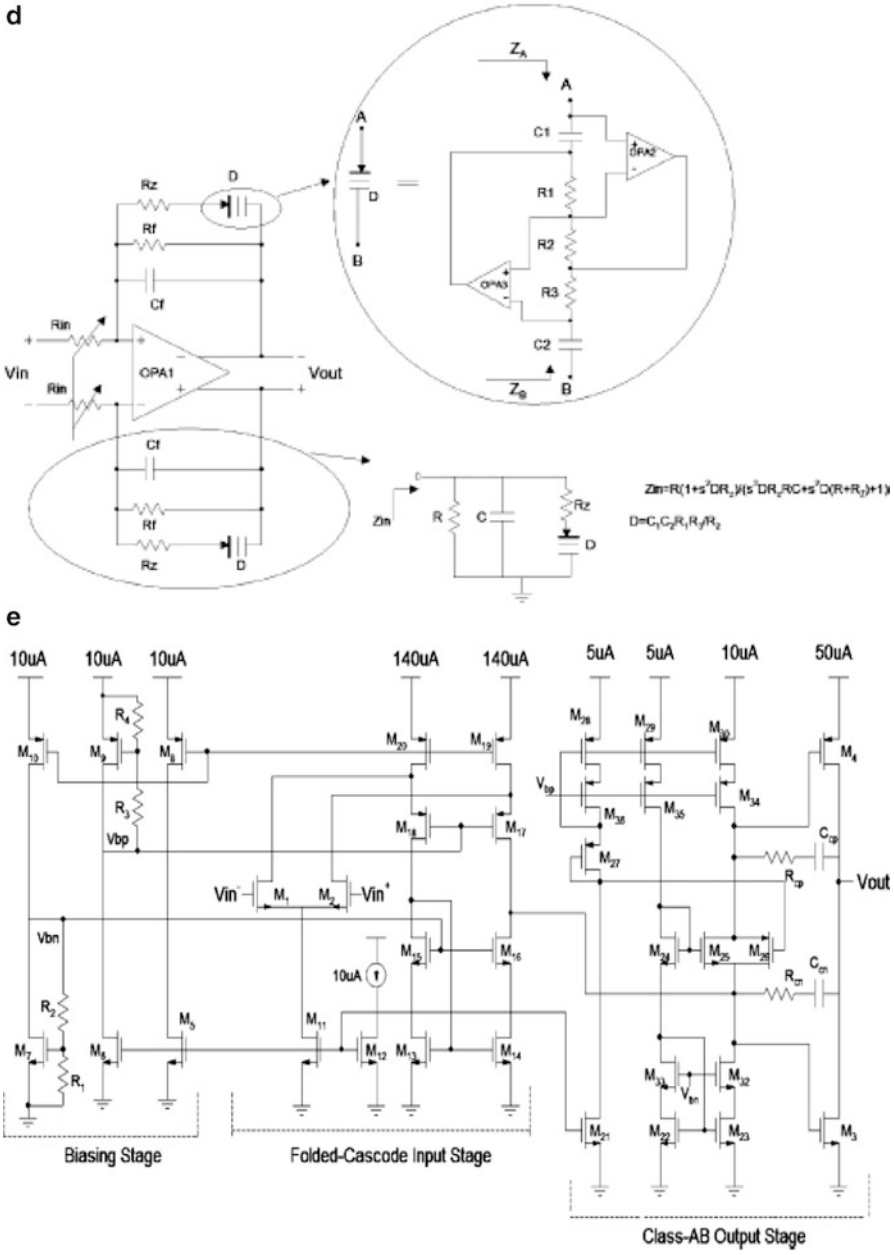


Fig. 5.14 (continued)

$$\frac{V_o}{V_{in}} = 1 + \frac{R_f\left(s^2 D R_z + 1\right)}{R_{in}\left(s^3 D R_z R_f C_f + s^2\left(D R_z + D R_f\right) + s R_f C_f + 1\right)} \tag{5.3}$$

At low frequencies, this reduces to 1 + (R_f/R_{in}). The folded-cascode based opamp schematic used in this design is presented in Fig. 5.14e which has a class AB output stage.

Ozgun et al. [5.16] have discussed techniques for power optimization of active filters and have suggested guidelines for designing filters for zero-IF receivers. Depending on the received input signal level, the power dissipation can be dynamically adjusted. Two filters can be optimized for different dynamic ranges and one of these can be selected. However, there can be transients during switching from one filter to another. Ozgun et al. [5.16] have suggested dynamic impedance scaling and dynamic biasing techniques that will ensure that the power is dissipated only at a level needed to process the signal at hand. They have considered impedance, noise, and power scaling.

Consider the single OTA-based circuit of Fig. 5.15 which can be realized using two g_ms in parallel. The result is increased supply current and increased transconductance but decreased input referred noise. Consider next, the first-order filter and its equivalent obtained after impedance and power scaling as shown in Fig. 5.16a, b. Thus, one can use the circuit of Fig. 5.16b to process low-level signals and switch to the circuit of Fig. 5.16a when the input signal is higher. Even though the load impedance of the OTA has been halved, the output linear range of the filter is not changed since the current driving capability is doubled by the parallel combination of the two OTA sections.

During the switching from the circuit (a) to (b), in the arrangement of Fig. 5.16b, it can be seen that by making the proper switching arrangement, transients can be avoided. The strategy (see Fig. 5.16c) is to switch off the lower circuit when the input signal is high. When the input signal is low, first φ_B is switched on so that the second circuit is functional and when the signal level is low, φ_C is switched on, thus connecting both filters in parallel. In a similar way, when the signal level becomes high, the lower one can be switched off. Note that the offset of each stage may be different leading to a voltage jump in the output. This demands that the offsets be cancelled before connecting the circuits.

Ozgun et al. [5.16] have extended this to many parallel paths using an *alternating divide and conquer technique*. This technique needs to be applied to the first stage. A GSM filter is considered which needs a fifth-order Chebychev 0.1-dB pass-band ripple and 100-KHz cutoff frequency using the leap-frog ladder technique. This filter is shown in Fig. 5.16d together with the new concepts implemented in the first stage. Note that two gain elements are used: one after the first stage and another in the feedback input to the first stage. This will ensure that the interferers would have been filtered enough in the first stage and hence the signal can be amplified thereafter. The dynamic impedance scaling in the first stage and the suitable interstage gain are implemented as shown in Fig. 5.16f. The upper forward path has a gain of +24 or −24 dB whereas the lower path has a gain of 0 dB. For weak and strong signals, the

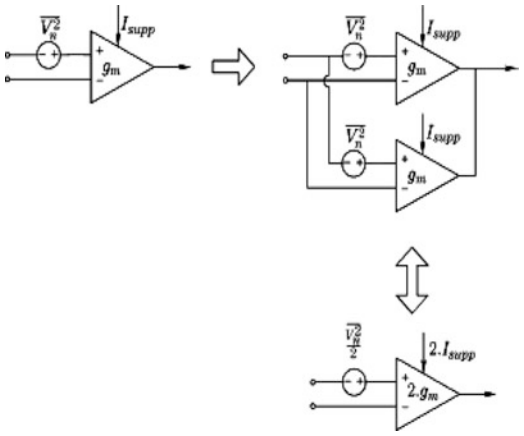


Fig. 5.15 Comparison of input referred noise of a single OTA and two OTA in parallel (Adapted from [5.16] ©IEEE 2006)

upper path is used and for medium signals, the lower path is used. Overall the first stage has 64 OTAs and different capacitor and resistance values. The OTA used is presented in Fig. 5.16e which is a fully balanced two-stage design. Transistors M_{1A}, M_{1B}, M_{2A}, M_{2B}, and M_5 form the first stage. A replica of this stage is used in the common mode feedback circuit comprising transistors M_8, M_{6A}, M_{6B}, M_{7A}, and M_{7B}. Note that the loads of the common mode feedback stage are diode connected. The gate source voltage of M_{7B} sets the biasing of the loads of the input stages M_{2A} and M_{2B}. The output stage is a common source stage formed by M_{4A}, M_{3A}, M_{3B}, and M_{4B} with Miller compensation using C_{CA}, C_{CB}, and transistors M_{CA} and M_{CB}. The common mode signal is detected using resistors R_{CMA} and R_{CMB} of 320 K ohms in parallel with two capacitors 50 pF. The output common mode voltage is set at 0.4 V. The input devices are large for reducing $1/f$ noise contribution of these devices.

Thyagrajan et al. [5.17] have described a class of active RC filters known as "g_m-assisted filters." The basic principle is similar to NIC-based compensation to achieve a real ground at the virtual ground terminal of the integrator. In the Thyagarajan et al. technique, currents are injected into the output terminal of the integrator block (see Fig. 5.17a) in order to make V_x zero. Analysis of the circuit taking into account the load resistance, input capacitance, and load capacitance (see Fig. 5.17b), we can obtain V_x as

$$V_x = \frac{G_1\left(G_L + s(C + C_L)\right)V_{in} - sC I_{assist}}{s^2\left(CC_L + C_x C_L + CC_x\right) + s\left(G_1\left(C + C_L\right) + G_L\left(C + C_x\right) + CG_{OTA}\right) + G_1 G_L} \tag{5.4}$$

Note that V_x can be made zero under the condition (numerator of (5.4) becoming zero)

$$I_{assist} = G_1\left(1 + \frac{C_L}{C}\right)V_{in} + \frac{G_L G_1}{sC}V_{in} \tag{5.5a}$$

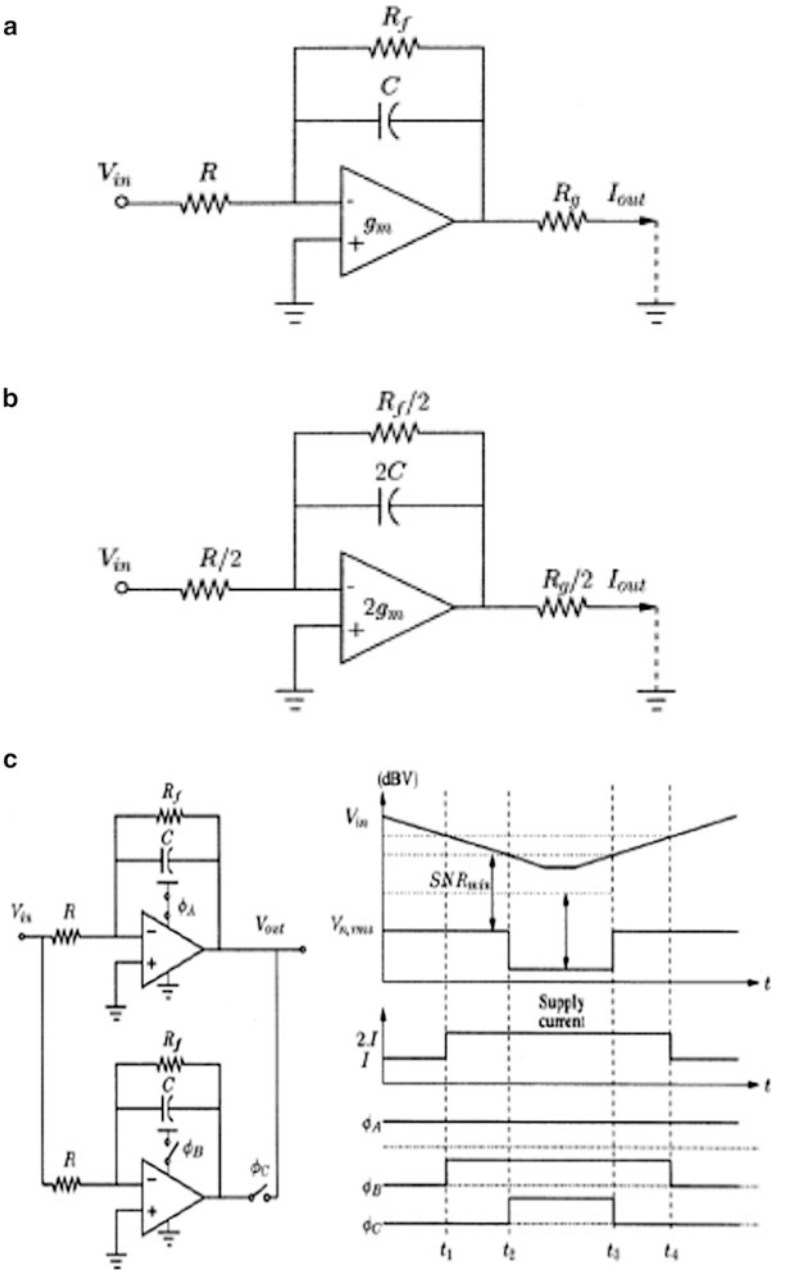


Fig. 5.16 (**a**) First-order active RC filter, (**b**) filter of (**a**) after impedance and power scaling, (**c**) switching procedure for dynamic impedance scaling in a first-order RC filter, (**d**) fully balanced active RC implementation of a fifth-order leap-frog Chebychev low-pass filter, (**e**) fully balanced two-stage OTA design with common mode feedback, and (**f**) filter system block diagram (sct means section) (Adapted from [5.16] ©IEEE 2006)

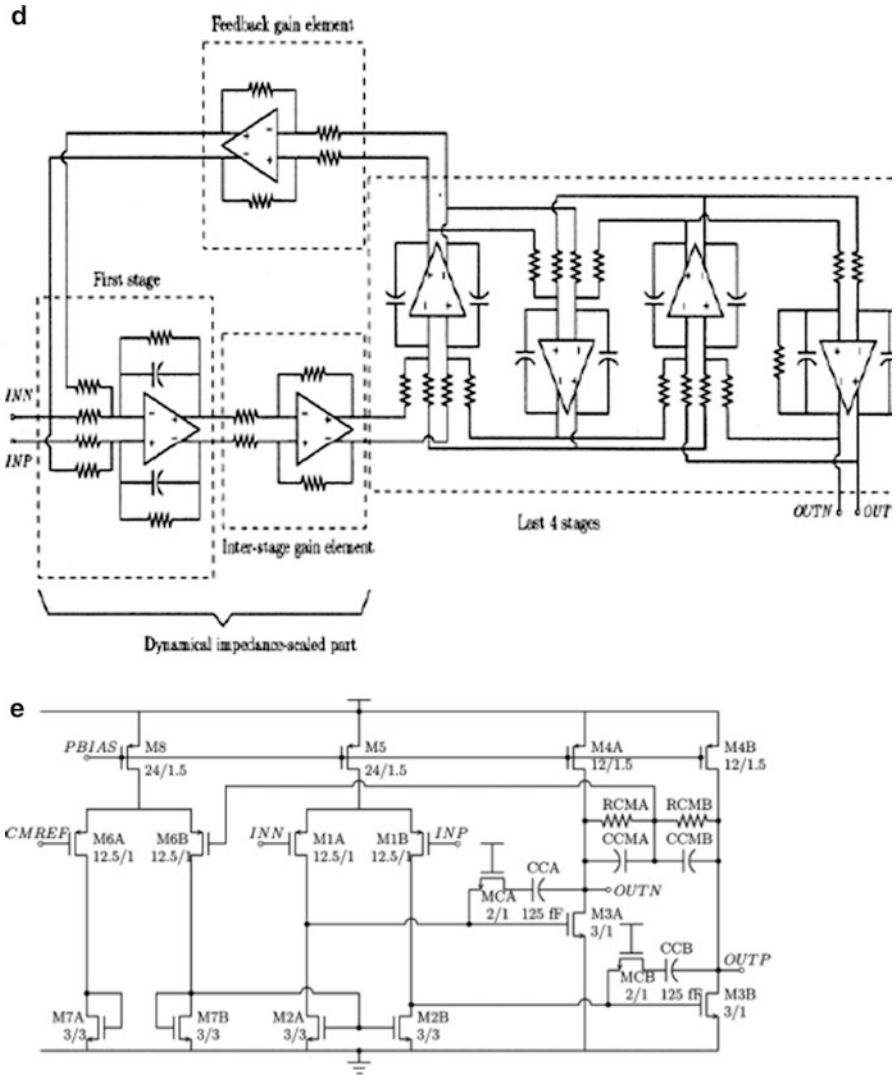


Fig. 5.16 (continued)

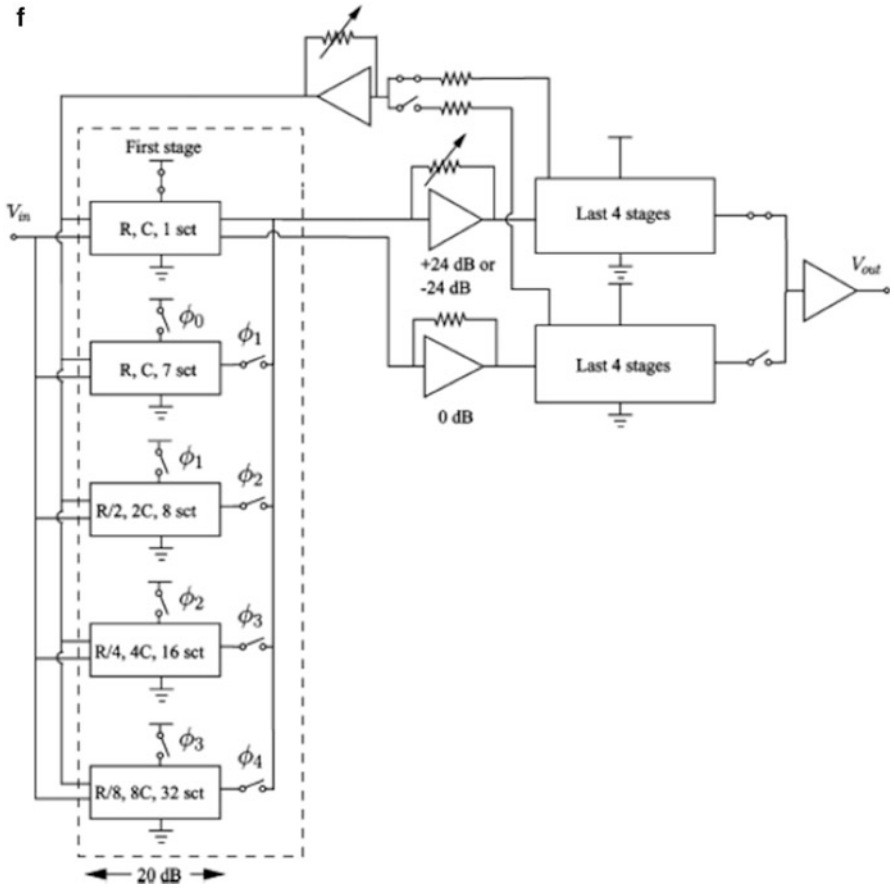


Fig. 5.16 (continued)

Noting that once V_x is zero, $V_o = -G_1/(sC)$, we have from (5.5a),

$$I_{assist} = G_1\left(1 + \frac{C_L}{C}\right) V_{in} - G_L V_{out} \tag{5.5b}$$

The transfer functions considering $I_{assist} = V_{in}\alpha - V_o\beta$ can be derived as

$$V_o = \frac{s(CG_1 - (C + C_x)\alpha) - G_1(G_{OTA} - \alpha)}{s^2(CC_L + C_xC_L + CC_x) + s(G_1(C + C_L) + (G_L - \beta)(C + C_x) + CG_{OTA}) + G_1(G_L - \beta)} \tag{5.6a}$$

and

$$V_x = \frac{s((C + C_L)G_1 - \alpha C) + G_1(G_L - \beta)}{s^2(CC_L + C_xC_L + CC_x) + s(G_1(C + C_L) + (G_L - \beta)(C + C_x) + CG_{OTA}) + G_1(G_L - \beta)} \tag{5.6b}$$

It is therefore necessary to generate the two currents using g_m blocks denoted as assistant transconductors. Thyagarajan et al. [5.17] have demonstrated that the linearity of the filters can be increased due to reduction in V_x. They have also observed that the noise contribution of the additional circuitry (assistant transconductors) is insignificant. The reader is referred to [5.17] for more detailed analysis.

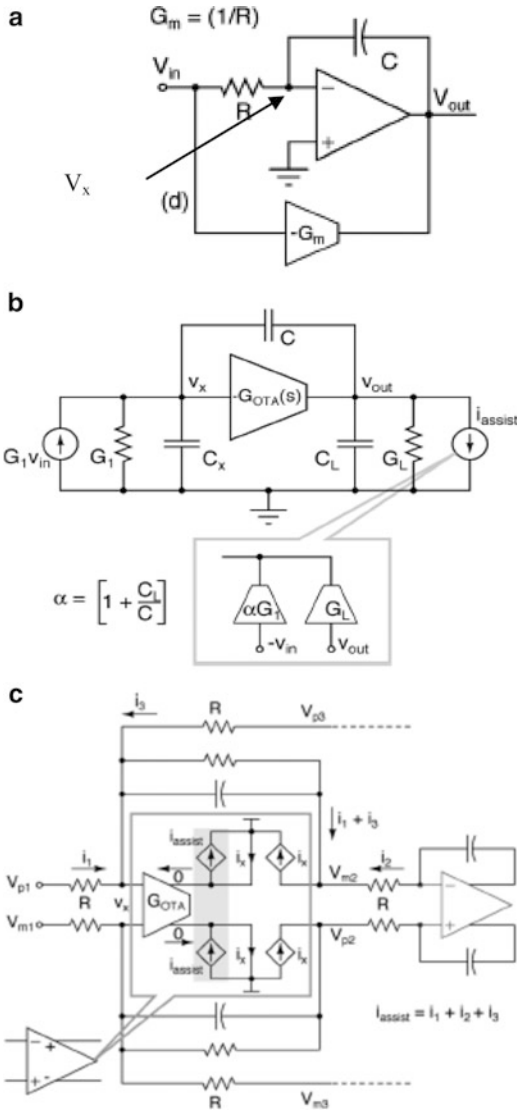


Fig. 5.17 (**a**) G_m-assisted Active RC section, (**b**) integrator using (**a**), (**c**) OTA embedded in active RC filter, (**d**) folded cascade OTA needed in (**c**), and (**e**) bias generator schematic that servos the transconductance of the assistant (Adapted from [5.17] ©IEEE 2011)

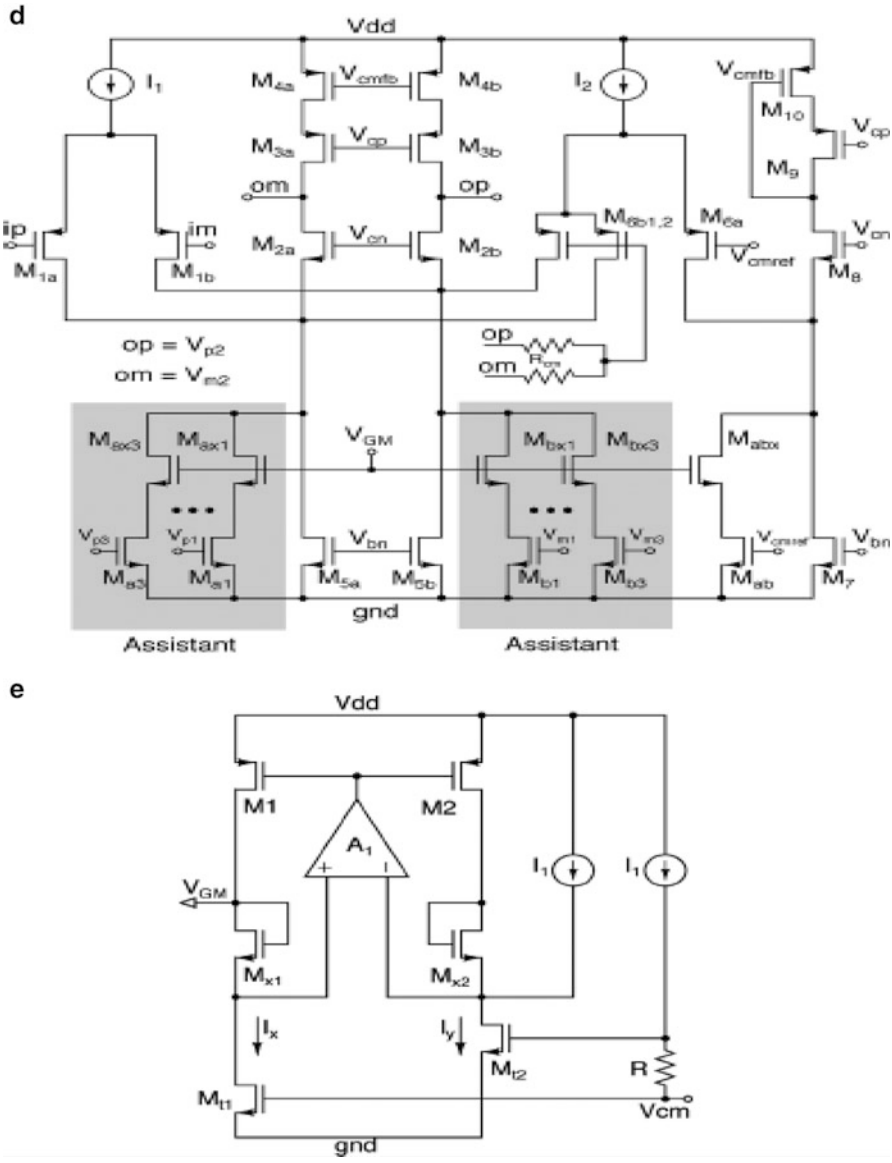


Fig. 5.17 (continued)

The opamp used is a single-stage folded cascode opamp with CMRR rejection circuit as shown in Fig. 5.17d. The cascode connection helps to increase the output swing capability. Note that in the biquad based on the two-integrator loop, a section of which is shown in Fig. 5.17c, i_1 and i_3 need to be summed at the virtual ground and the output of the opamp needs to drive i_2 to the next lossless integrator. Thus the assistant produces $i_1 + i_2 + i_3$. These assistant currents are generated by three

OTAs with transconductance $1/R$ excited by $V_{p1,m1}$, $V_{p2,m2}$, and $V_{p3,m3}$. The opamp uses the PMOS input stage in order to reduce the noise. M_2 and M_3 are NMOS and PMOS cascodes, respectively. The CMFB loop is formed by $M_6 - M_{10}$. A resistive common mode detector r_{cm} is used. The CMFB circuit injects currents at the sources of M_2 through $M_{6b1,2}$ and furthermore it varies the gate voltages of $M_{4a,b}$. The assistant OTAs are formed by M_{ax1}–M_{a1}, M_{ax2}–M_{a2}, M_{ax3}–M_{a3}, and M_{bx1}–M_{b1}, M_{bx2}–M_{b2}, M_{bx3}–M_{b3} pairs. M_{a1}–M_{a3}, M_{b1}–M_{b3} operate in the triode region and M_{ax1}–M_{ax3}, M_{bx1}, M_{bx3} operate in the saturation region. Note that M_{ab}, M_{ab4} add a current to the CMFB circuit so that M_9, M_{10} operate in a similar manner to that of M_3 and M_4. The g_m of M_{ax1} tracks R by deriving V_{GM} from a control loop that servos to make $G_{ma} = 1/R$. Note that the assistant currents are injected into the sources of M_2 so that they do not have low output impedance, otherwise needed, if we inject these into the output terminals of the opamp.

The resistor servo loop is shown in Fig. 5.17e. It can be seen that $I_y - I_x = I_1$ and $g_m(V_{gst2} - V_{gst1}) = I_1 R_{gma} = I_y - I_x = I_1$ thus making $Rg_{ma} = 1$. The transistors M_{x1}, M_{x2} are identical to M_{ax1} and M_{b1} so that V_{GM} generated in the bias generator of Fig. 5.17e can be distributed to all OTAs in the filter. The drain voltages of M_{t1} and M_{t2} are equal due to the high gain opamp A_1.

5.6 G_m-C Filters for Wireless Applications

Bagbahani et al. [5.18] described a variable bandwidth band-pass filter for a fully adaptive wireless local area network. The block diagram is presented in Fig. 5.18a. The pass-band is selectable—625 KHz, 2.5 MHz, or 10 MHz—with a stop-band that exceeds 100 MHz. The filter attenuates the incoming signals farther than 100 MHz away with 50 dB attenuation. In order to have a symmetric band-pass response, the authors use a fifth-order LP elliptic filter cascaded by a third-order Chebychev high-pass filter. The largest pole-Q thereby reduces to 6.9 in LPF and 1.3 in HPF whereas the LP–BP transformation type band-pass filter has a pole-Q of 7.8 for the pole pairs. The HPF fixes the lower edge whereas the LPF fixes the upper band edge.

A g_m of a MOS differential pair may be changed by bias current. But it does not provide high linearity and the tuning range is limited. A MOS resistor may be used for voltage-controlled degeneration but the available triode region limits the tuning range. For high linearity, a MOS transistor may be padded with a fixed linear resistor that limits the range of G_m variation. In a technique called "soft switching," a ladder of padded MOS degeneration widens the g_m tuning range while maintaining good linearity.

The g_m used is presented in Fig. 5.18b where $MN3$ operates in the triode region as a voltage-controlled resistor. For greater voltage headroom, the bias current source is removed at the expense of CMRR. The active load is a MOSFET. The dc gain voltage of the basic g_m can be boosted by connecting a negative conductance stage implemented by a cross-coupled g_m placed in parallel with the output of the main transconductor. The authors have used three types of conductances as

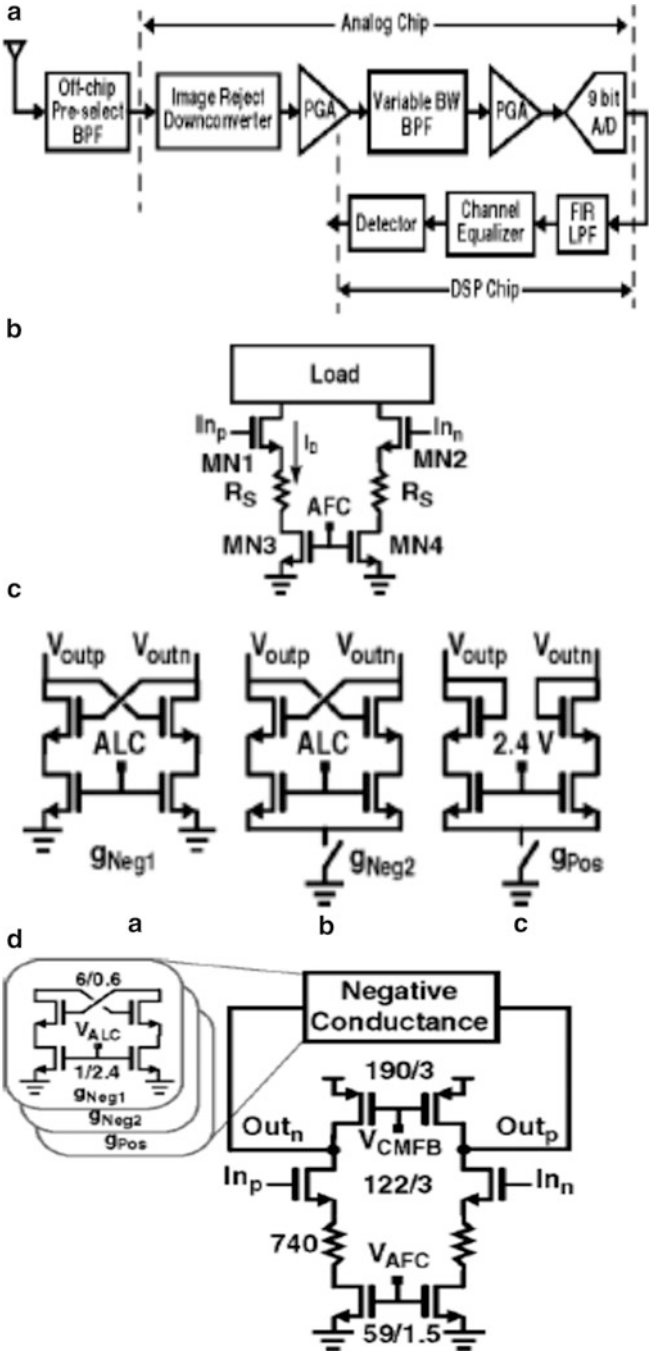


Fig. 5.18 (**a**) Block diagram of receiver, (**b**) variable transconductor based on degenerated differential pair, (**c**) negative conductance, auxiliary switched negative conductance, and switched positive conductance, (**d**) variable g_m used in low noise LPF, (**e**) variable g_m used in low power LPF and HPF, (**f**) prefilter AGC, (**g**) HPF using amplifier with LPF in the feedback path, and (**h**) details of HPF (Adapted from [5.18] ©IEEE 2000)

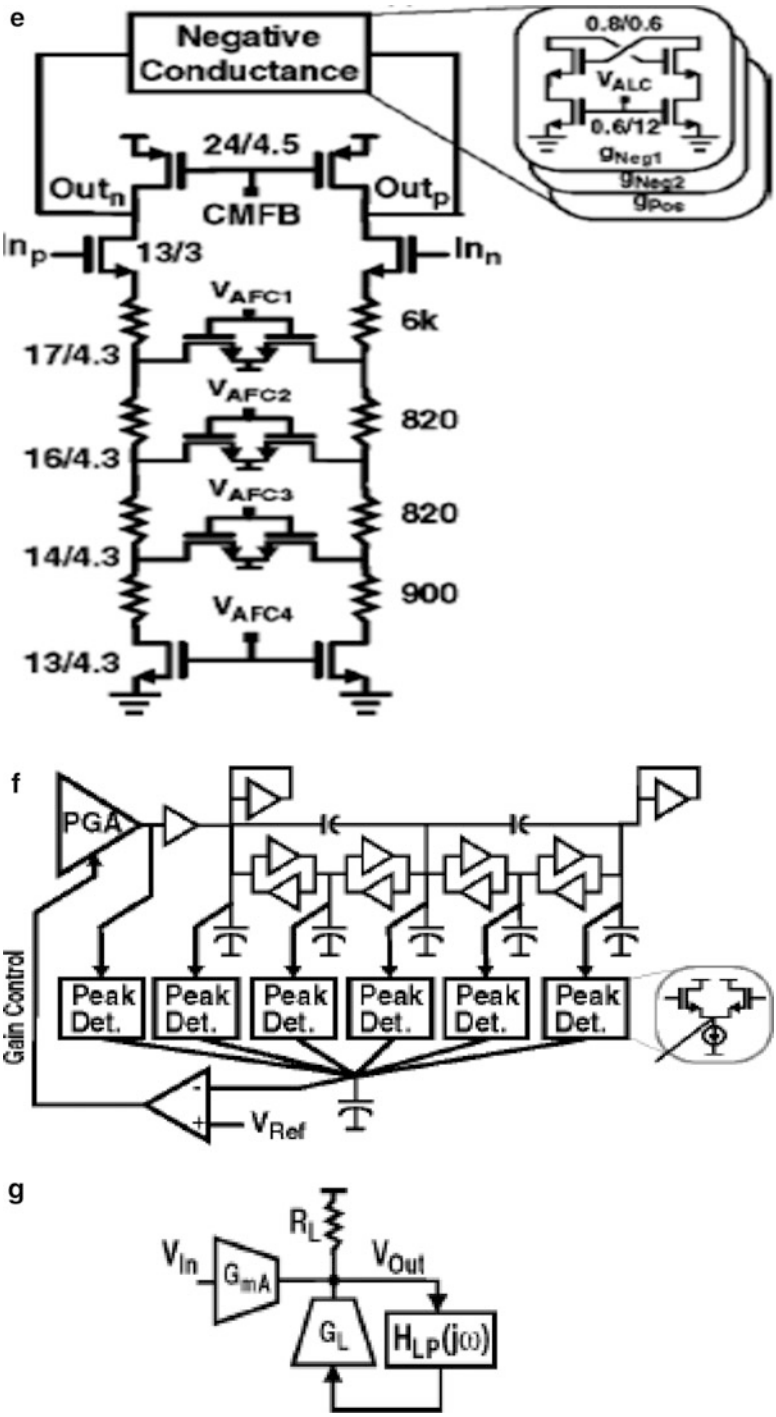


Fig. 5.18 (continued)

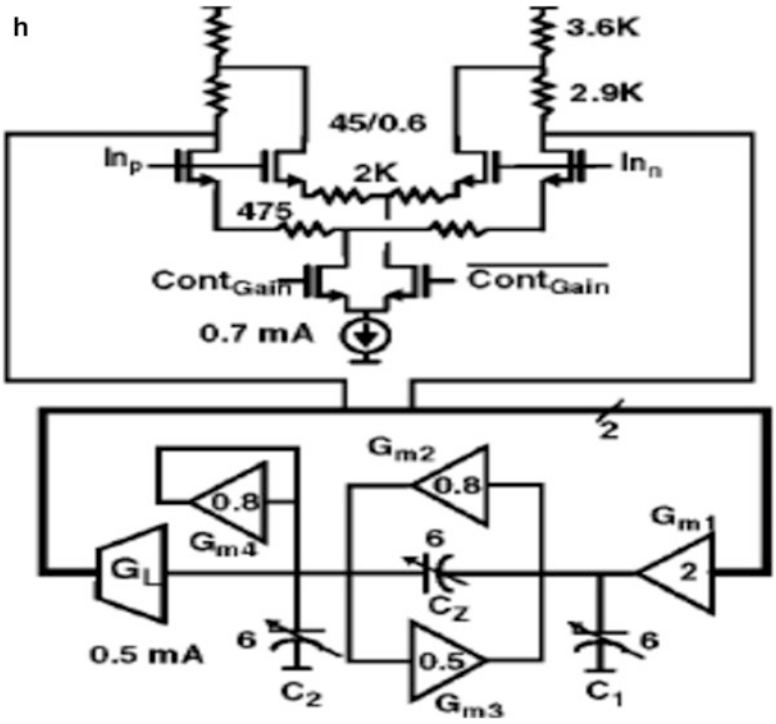


Fig. 5.18 (continued)

shown in Fig. 5.18c: (a) fixed negative resistance, (b) switchable negative resistance, and (c) switchable positive resistance.

The complete g_m circuit used in the low noise LPF ($G_{m,H}$) is shown in Fig. 5.18d and low power g_m ($G_{m,L}$) used in low-power LPF and HFP is shown in Fig. 5.18e. The latter has higher noise. The G_{mL} includes several stages of variable degeneration to expand the range without giving up linearity. At any time, only one MOSFET is on and its gain control varies from 1.6 to 3.3 V. The range of degenerated g_m overlaps so that a continuous sweep of 50% of g_m is realized. The LPF is based on a doubly terminated ladder filter with inductances realized using gyrators and capacitors. In order to optimize the noise performance, the authors suggest the scheme of Fig. 5.18f where all the signal peaks at all nodes are detected. If the peak value exceeds some limit, then the input gain is scaled through variable gain PGA. Noise scaling is done next by scaling up the g_ms and filter capacitors together with a bias current which proportionately decreases the noise spectral density. Both G_m and C are tuned so that the noise spectral density is constant with tunable frequency.

The HPF is realized using the configuration of Fig. 5.18g by putting a LPF in the feedback path of a 45-dB switchable gain stage. At high frequencies, there is no feedback and hence the gain is $g_{mA}R_L$. At low frequencies, the OTA g_L appears as a resistor $1/g_L$. When $R_L \gg 1/g_L$, the dc gain is smaller. Actually, the LPF is

second-order only. The capacitor C_Z creates a transmission zero so that an overall third-order response is realized as shown in the complete circuit of Fig. 5.18h.

The CMFB circuit is presented in Fig. 5.19a. The common mode signal is detected by *MN*5–*MN*6 and *MP*3 and compared with V_{ref} to amplify the error using *MP*3, *MP*4, and *MN*7–*MN*8. The CMFB output feeds all the PMOS load transistors. Note also that each OTA need not have a CMFB loop which may cause instability since in many places, outputs of G_ms are connected. Hence, all active nodes connecting to an output node are merged and driven by CMFB signal.

The chip contains frequency and Q tuning loops. The V_{AFC} biases the gates of the active degeneration FETs in the G_m block (see Fig. 5.19b) and sets the transconductance. The digital word from 5-bit U/D counter sets the PCA. The PLL is conventional with a phase frequency detector, charge pump, and a series RC filter for compensation. Note that V_{AFC} will increase until the upper limit, assuming that f_{VCO} is initially much less than the frequency output of the divider f_o. Then, the comparator trips and the logic decrements the PCA. The ALC (automatic level control) loop (see Fig. 5.19c) controls the oscillation amplitude by changing the negative resistance in the OTA.

Lo et al. [5.19] have described a G_m-C filter with a wide tuning range for a multimode direct conversion wireless receiver. The tuning encompasses Bluetooth (650 KHz), CDMA 2000 (700 KHz), wide-band CDMA (2.2 MHz), IEEE 802.11a/g (10 MHz), IEEE 802.11b (12 MHz), and IEEE 802.1n (20 MHz) wireless LAN applications. These specifications cover the range 650 KHz–20 MHz. A tuning ratio of G_m of 30 is required. However, taking into account all the tolerances and temperature variations, a tuning range of 50 is required. A high linearity transconductor with a wide transconductance range shown in Fig. 5.20a has been employed. In this, the linear V-I conversion is performed first using resistors R_{1a} and R_{1b} and then the transconductance is varied using the translinear loop formed by the current multiplier composed of transistors M1–M4, resistors R_{1a} and R_{1b} and the current source I_{tune}. Transistors M1 and M4 are biased in the weak inversion region. It can be shown that the transconductance is given as $G_{m,sat} = nV_T\frac{\sqrt{k_{3,4}I_{tune}}}{V_{cm}}$ where $k = \mu C_{ox}\frac{W}{L}$ and V_{cm} is the common mode voltage, V_T is the thermal voltage. It can be seen that the transconductance can be adjusted using the current I_{tune}. The complete transconductor is presented in Fig. 5.20b showing the CMFB circuit composed of transistors MF1–MF8. The feedback loop forces the output common mode voltage to the desired value. The block diagram of the third-order Butterworth filter is presented in Fig. 5.20c consisting of seven identical transconductors. The transconductance is programmable and has a nominal value of 50μS. Automatic tuning of frequency is not incorporated.

Saari et al. [5.20] have described a CT low-pass filter with variable gain in 65 nm CMOS for an UWB radio receiver. This used 1.2 V supply voltage which necessitated the use of a pseudo differential G_m-C technique in order to achieve a large bandwidth as well. The fifth-order filter architecture is shown in Fig. 5.21a which comprises a front-end first-order filter realized by R_1 and C_1 fed with input current. This is followed by a fourth-order low-pass filter based on a leap-frog ladder. The finite output resistance of the various G_ms has been taken into account for synthesizing the L and C values of the

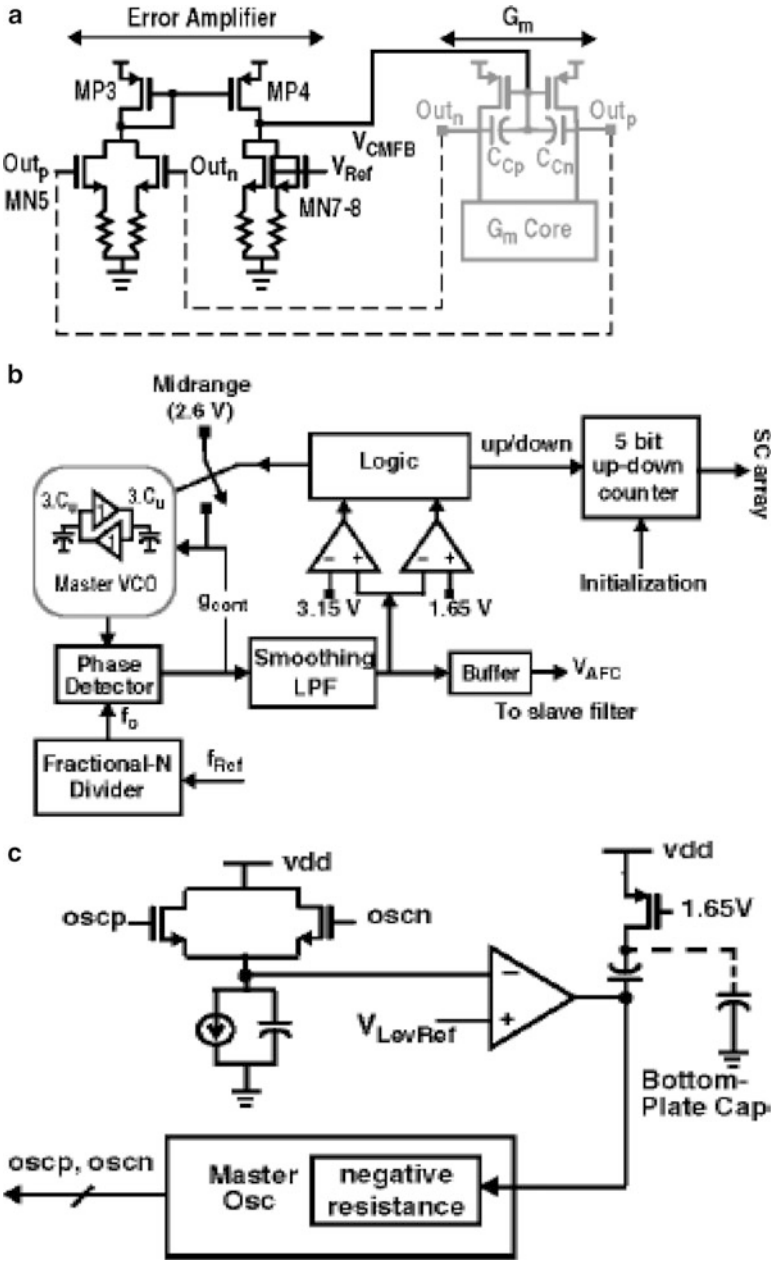


Fig. 5.19 (**a**) CMFB amplifier, (**b**) automatic frequency control loop, and (**c**) automatic level control loop (Adapted from [5.18] ©IEEE 2000)

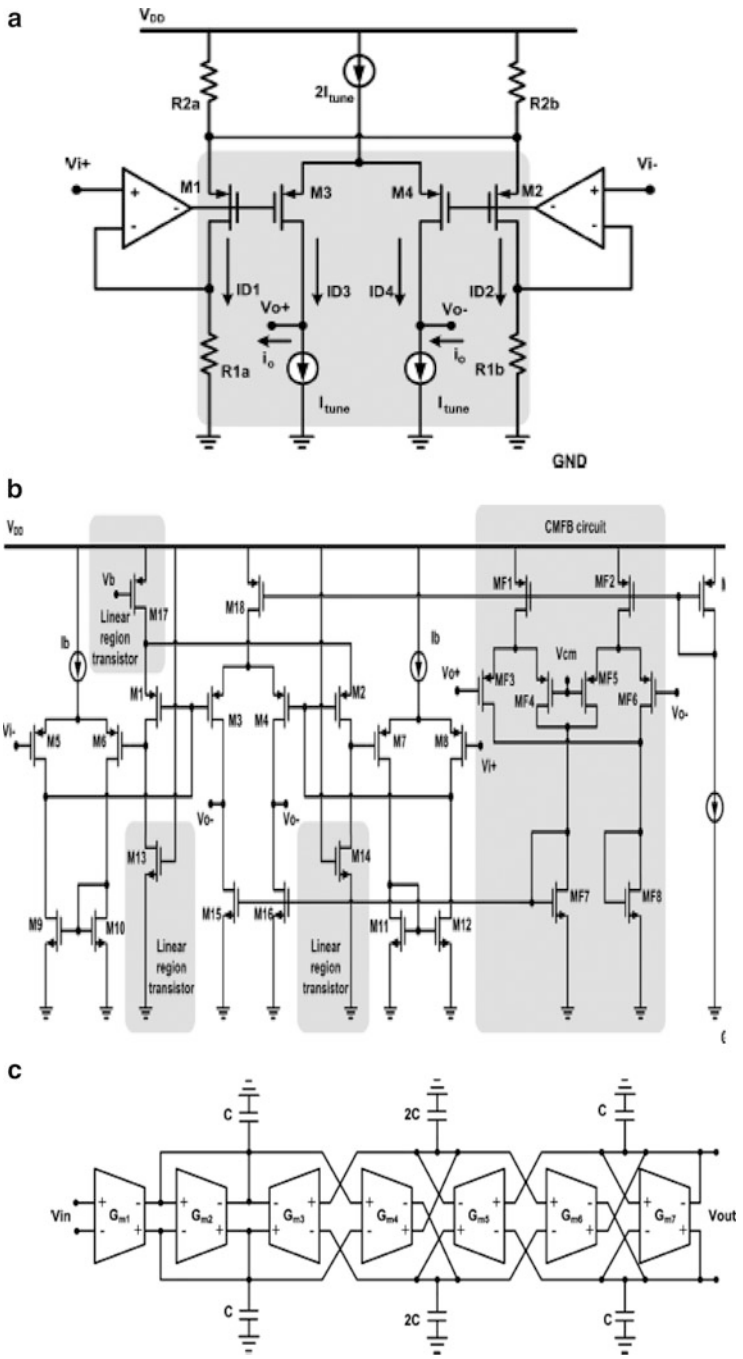


Fig. 5.20 (**a**) Wide tuning range transconductor conceptual diagram, (**b**) complete implementation of (**a**), and (**c**) third-order Butterworth filter (Adapted from [5.19] ©IEEE 2009)

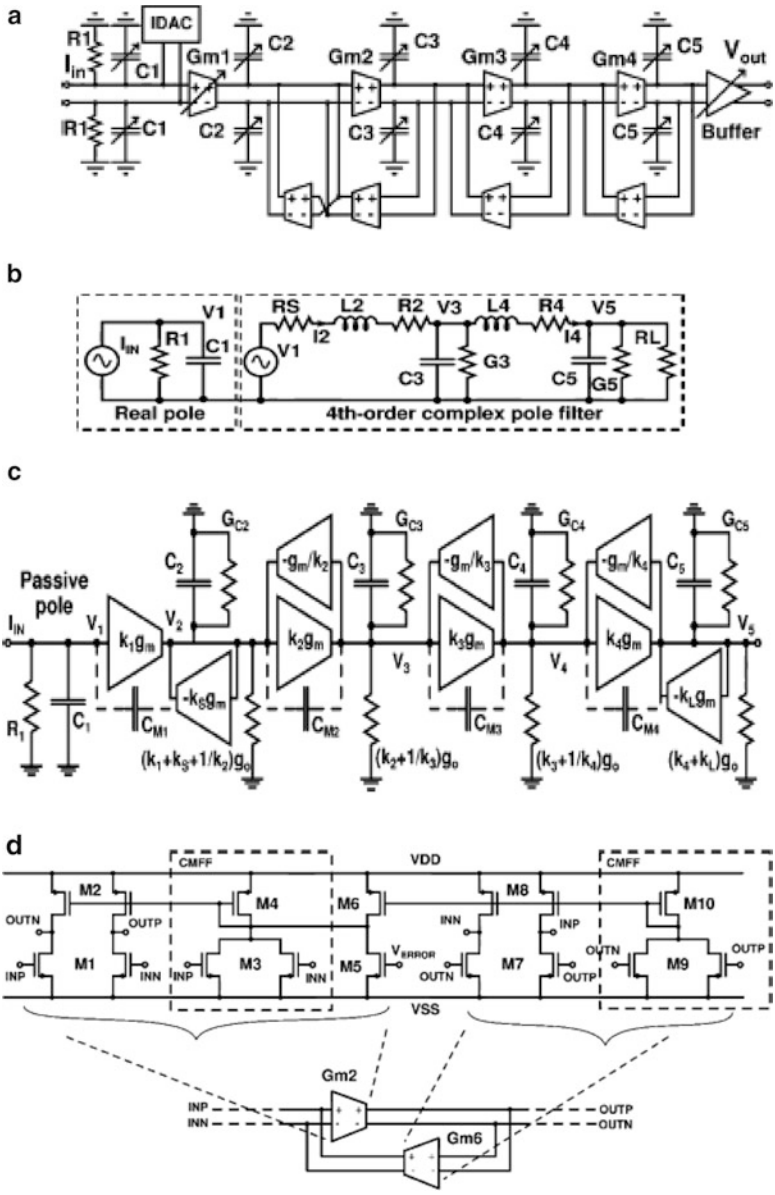


Fig. 5.21 (**a**) Fifth-order pseudo differential G_m-C low-pass filter, (**b**) prototype LC ladder filter with extracted real pole, (**c**) single-ended G_m-C filter with scaling factors k_i, (**d**) transconductors with CMFF and CMFB circuit, (**e**) gain control slice from the input transconductor G_{m1}, (**f**) bias circuit for error compensation, and (**g**) 5-bit switched capacitor matrix (Adapted from [5.20] ©IEEE 2009)

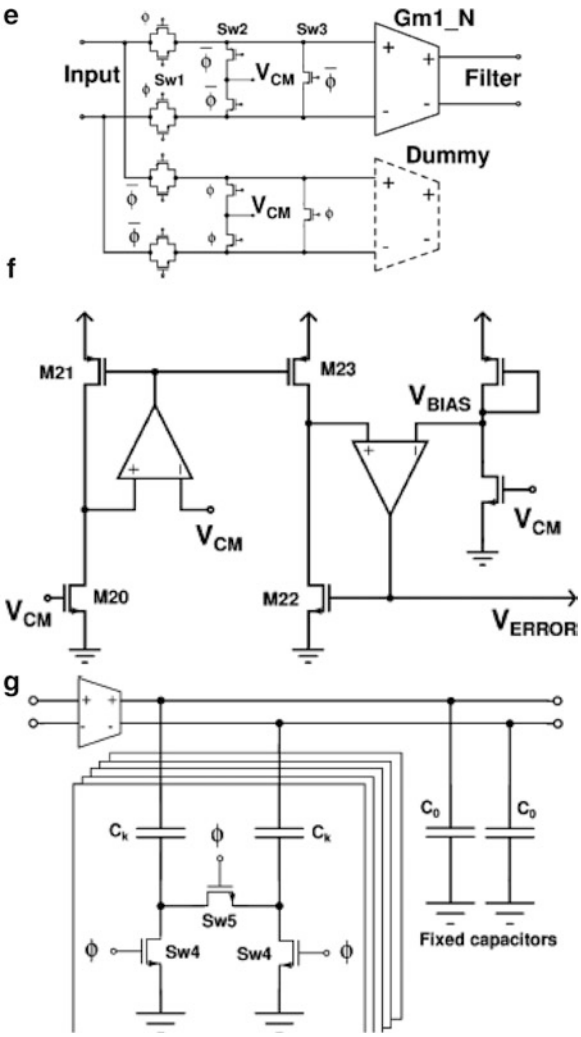


Fig. 5.21 (continued)

filter. The nonideal filter is as shown in Fig. 5.21b, c showing various parasitic losses. Note that all the integrators have a fixed gain of 26 dB. The pseudo differential OTA is presented in Fig. 5.21d. This has both input common mode feedforward and feedback compensation. This uses NMOS input transistors to reduce the parasitic capacitance at the input terminals. It employs PMOS current source loads. Grounded negative resistance has been connected at the output of each g_m so as to enhance the dc gain to the desired 26 dB in the presence of process variations. The transistors M_{11}–M_{14} realize the negative resistance. The tuning of these is accomplished by varying the gate-source voltage of the degeneration transistors M_{13} and M_{14}.

In order to achieve high-input CMRR, a transconductor formed by M_3 and M_4 replicates the input transconductor formed by M_1 and M_2 and subtracts current from that of the input transconductor formed by M_1 and M_2. The output CMFB injects current through the transistor M_6 to the input transconductor. The output CMFB employs the transistors M_7–M_{10} by again using replica-based error detection. The transistor M_5 is provided the common mode reference voltage. There can be mismatch in the PMOS current mirrors in the transconductor that can be taken care of by the circuit (see Fig. 5.21f) which generates the replica of the current mirror error and subtracts it from the transconductor output currents. The transconductors M_{20}, M_{21}, M_{22}, and M_{23} are copies of the transconductors in the transconductor core. The generated V_{ERROR} is fed to the transistor M_5 to obtain the correct current. The filter gain is controlled from 9 to 43 dB in 1 dB steps by using five 6-dB gain steps and five 1-dB gain steps. The transconductor G_{m1} (see Fig. 5.21a) includes the 6-dB gain steps whereas the 1-dB gain steps are implemented in the output buffer. The 6-dB gain steps are realized by using six binary weighted transconductors which can be appropriately switched. In order to keep the frequency of the pole the same, dummy G_ms are switched with the input disconnected (see Fig. 5.21e). In addition, the corner frequencies of the passive pole and fourth-order filter are tunable using capacitor arrays in place of each grounded filter capacitor. Five-bit tuning is possible for these binary weighted capacitor arrays (see Fig. 5.21g).

Oskooei et al. [5.21] have described a CMOS continuously tunable channel select filter for WLAN and WiMax receivers. This covers the frequency range 8.4, 11, and 11.2 MHZ for 802.11a, 802.11b/g (WLAN), and 802.16 (WiMax). As the supply voltage shrinks and the threshold voltage is not reduced at the same rate, the tuning range of MOSFET-C filters is lowered. G_m-C filters suffer from low linearity but they offer high cutoff frequencies and continuous tunability. UGB and cutoff frequency are the same in G_m-C low-pass filters and hence they consume less power than active RC or MOSFET-C filters. Hence, the authors have used the well-known two-integrator loop-based OTA-C biquad of Fig. 5.22a. They have used NMOS transistors to serve as the various G_ms due to which the parasitic poles occur only at very high frequencies where nonquasi-static behavior is significant. Power consumption also can be minimized. The complete circuit of the biquad is shown in Fig. 5.22b. Note that M_1 and M_2 realize G_{m1} whereas M_3 and M_4 realize G_{m4}. Both convert voltages into currents and pump into BPN and BPP nodes. The negative sign of G_{m4} is realized by cross-connecting the differential input signals. The transistors M_5 and M_6 are in common-gate configuration and present a resistance of $1/G_{m5}$ and $1/G_{m6}$ at BPN and BPP nodes analogous to G_{m2} in the circuit of Fig. 5.22a. They also drain the currents $G_{m5}V_{\mathrm{BPN}}$ and $G_{m6}V_{BPP}$ from the BPN and BPP nodes and buffer those to the output nodes performing the function of G_{m3} in Fig. 5.22a. Thus, one transconductor is eliminated thereby saving power. Evidently $G_{m2} = G_{m3}$ because of both of these are being realized by M_5 and M_6. The source followers M_{15} and M_{16} shift the dc level of OP and ON voltages. The devices M_{21}, M_{22}, M_{13}, and M_{14} implement the output common mode feedback loop. It can be shown that the pole-frequency, pole-Q, and gain are approximately given as

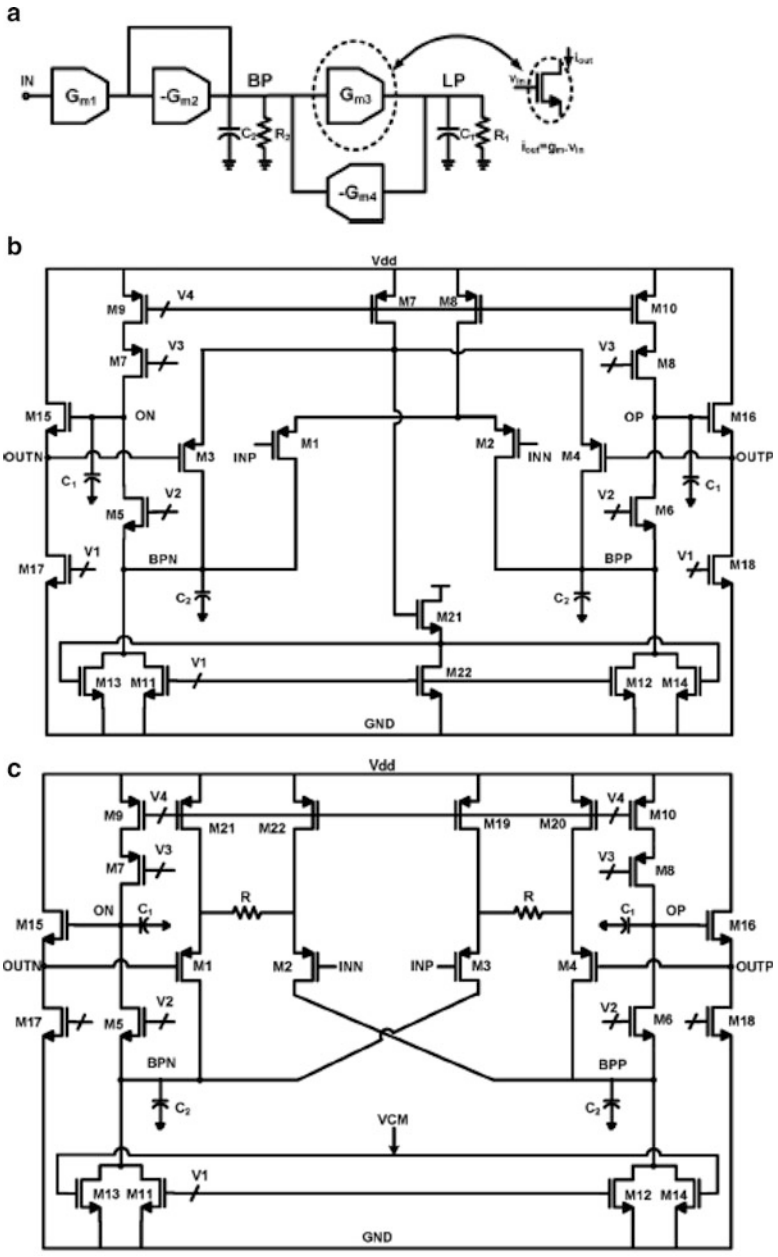


Fig. 5.22 (**a**) G_m-C low-pass biquad, (**b**) biquad circuit schematic, (**c**) schematic of linear biquad, (**d**) CMFB circuit, (**e**) capacitor arrays for C_1 and C_2, and (**f**) bias circuit of the filter (Adapted from [5.21] ©IEEE 2011)

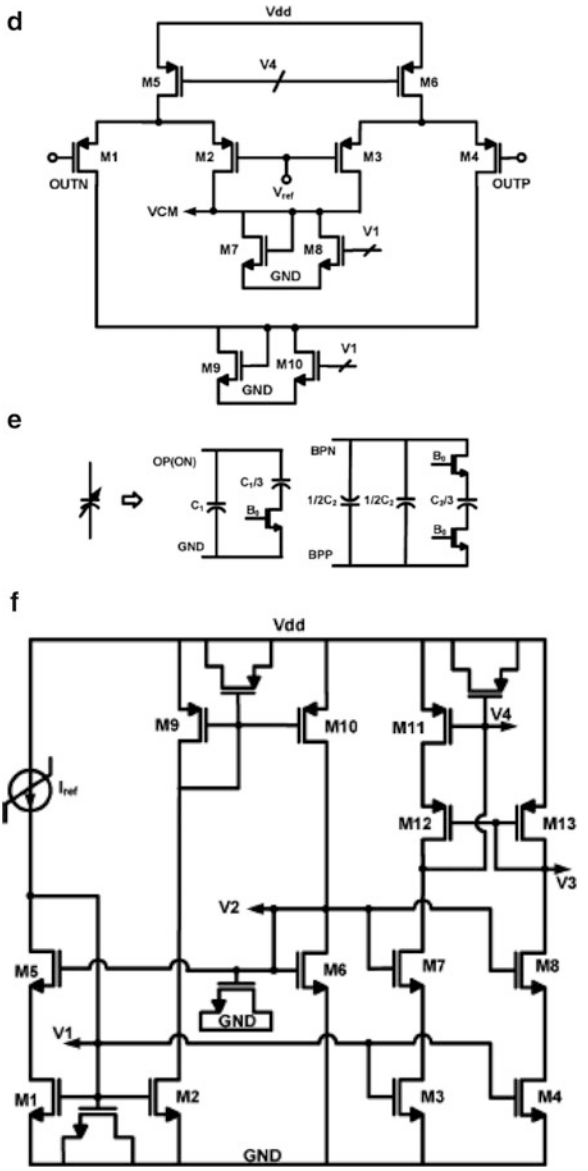


Fig. 5.22 (continued)

$$\omega_o^2 = \frac{g_{mf}\ g_{m6}}{C_1\ C_2},\ Q_p = \sqrt{\frac{g_{mf}\ C_2}{g_{m6}\ C_1}}\ \text{and}\ A_{dc} = \frac{g_{\min}}{g_{mf}} \tag{5.7}$$

where $G_{mf} = G_{m4}$. Due to sharing of the CMFB loop among all OTAs, considerable area and power can be saved.

Oskooeoi et al. [5.21] suggested a modification as shown in Fig. 5.22c that will help to improve the linearity. This is achieved in principle by bringing the differential pairs into the feedback loop. Note that the difference between Fig. 5.22b, c is in the connection of the input and feedback differential pairs. The common mode feedback circuit used in the configuration of Fig. 5.22c is shown in Fig. 5.22d. The input voltage swings of both differential pairs is smaller than that in the circuit of Fig. 5.22b. Note also that the resistors R provide additional degeneration so as to improve the linearity at high frequencies.

The cutoff frequency can be tuned coarsely by using programmable capacitors for C_1 and C_2 as shown in Fig. 5.22e. Note that to conserve area, the capacitors C_2 are connected in a differential mode. The fine tuning is carried out by the bias circuit shown in Fig. 5.2f which is used to change the transconductances G_{mf} and $G_{m5,6}$ by equal factors. This is achieved by changing the bias current I_{ref}.

D'Amico et al. [5.22] have suggested the use of source follower-based biquads for WLAN application. Such a biquad is shown in Fig. 5.23a. Note that the devices M_2 and M_3 provide positive feedback thus realizing complex poles. The small signal equivalent half circuit is shown in Fig. 5.23b from which the approximate transfer function can be obtained as

$$H(s) = \frac{1}{s^2 \frac{C_1 C_2}{G_m^2} + s\frac{C_1}{G_m} + 1} \tag{5.8}$$

considering the output conductances of the transistors are negligible compared to G_ms and choosing $G_{m1} = G_{m2} = G_{m3} = G_{m4} = G_m$. Thus a biquad with Q dependent on the ratio of capacitors can be realized. In order to meet the low power supply requirement, a folded version of the circuit of Fig. 5.23a is also used as shown in Fig. 5.23c which has increased power consumption due to additional current branches. A fourth-order Bessel filter based on the biquad of Fig. 5.23c is shown in Fig. 5.23d. The first and second cells are made up of PMOS and NMOS devices so that the input common mode voltage difference can be compensated.

Chamla et al. [5.23] have described a third-/fifth-order G_m-C band-pass filter with tunability for GSM as well as W-CDMA applications. The bandwidth for GSM application is about 115 KHz whereas for W-CDMA it is 2 MHz. A third-order and fifth-order low-pass filter will suffice for these applications. The authors use the topology of Fig. 5.24a based on gyrators that can share the same hardware so that the area can be minimized. The Butterworth implementation of a fifth-order filter needs capacitors of values 0.618, 1.618, 2, 1.618, and 0.618 whereas the third-order filter needs 1, 2, and 1. Hence by augmenting the third-order Butterworth filter values, the fifth-order filter can be realized. The wide ratio between bandwidths needed for GSM and W-CDMA applications of 25 requires the tunability of G_m over such a wide range. The authors use a MOS transistor in the triode region of operation for realizing the transconductor.

The basic transconductor principle is illustrated in Fig. 5.24b. The transconductance is realized by M_1 and its G_m is directly proportional to V_{DS}:

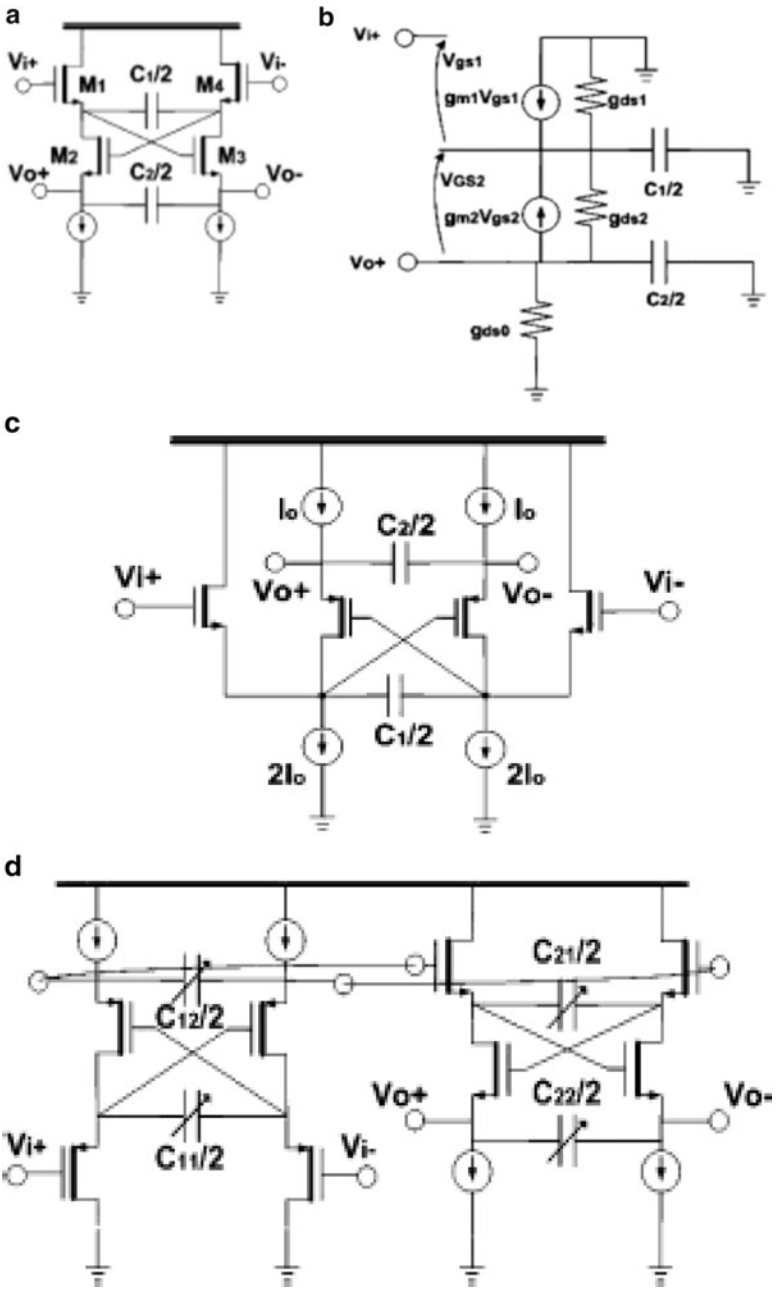


Fig. 5.23 (**a**) Biquadratic cell based on source followers, (**b**) half small signal equivalent circuit for the differential mode, (**c**) folded version of (**a**), and (**d**) fourth-order filter schematic (Adapted from [5.22] ©IEEE 2006)

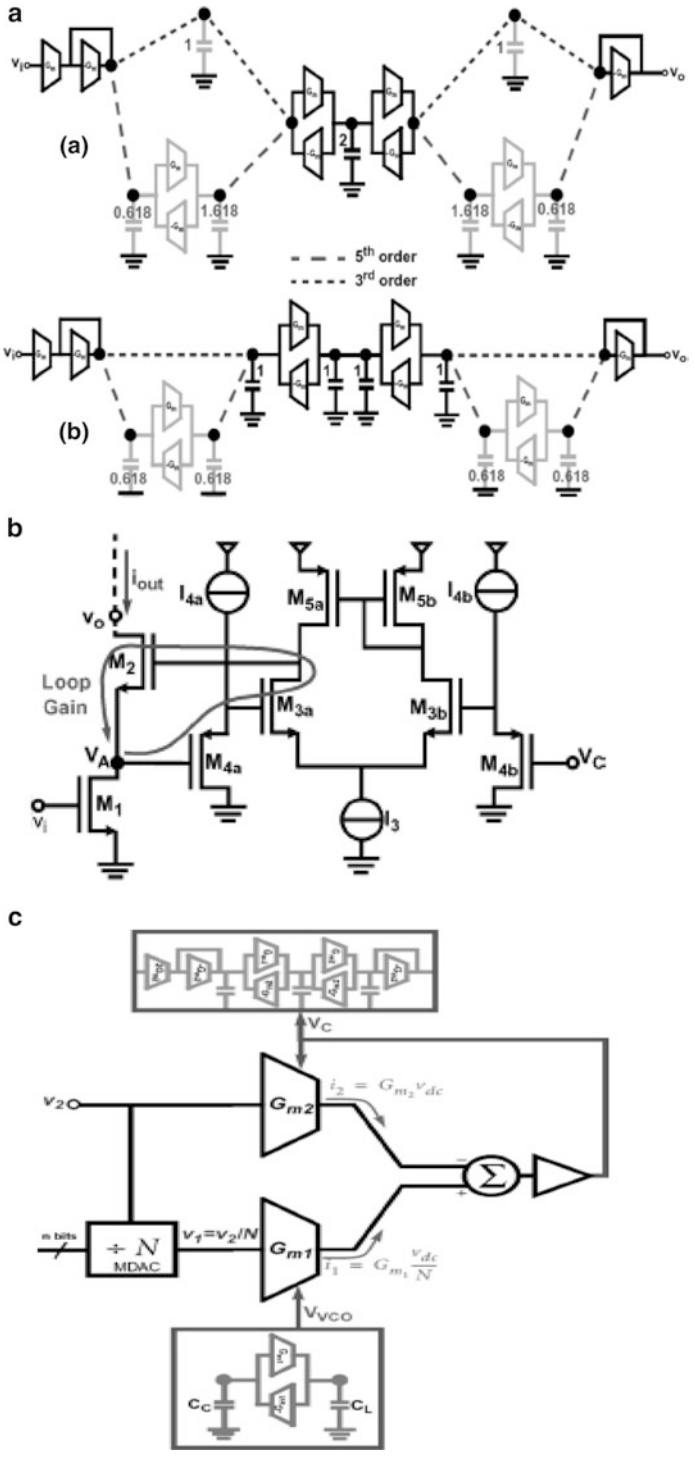


Fig. 5.24 (**a**) Third-/fifth-order switchable Butterworth G_m-C low-pass filter basic configuration (*top*) and optimized implementation (*bottom*), (**b**) principle of linear tunable transconductor, (**c**) implementation of accurate G_m ratio division, and (**d**) schematic of the VCO (Adapted from [5.23] ©IEEE 2007)

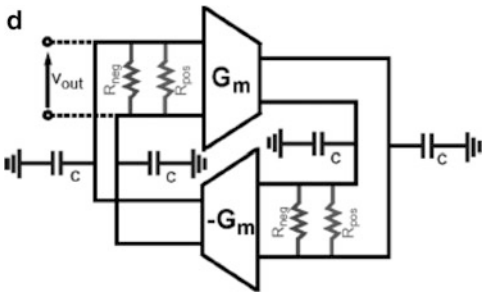


Fig. 5.24 (continued)

$$I_D = \mu_n C_{ox} \frac{W}{L}\left(V_{GS} - V_T - \frac{V_{DS}}{2}\right)V_{DS} \tag{5.9a}$$

$$G_m = \frac{\partial I_D}{\partial V_{GS}} = \mu_n C_{ox} \frac{W}{L} V_{DS} \tag{5.9b}$$

Thus, tuning V_{DS} necessitates V_{DS} going down to zero. M_2 acts as a cascode transistor that reduces the swing at V_A. The device M_4 acts as source follower and M_3s provide voltage gain. The control voltage is fed to M_{4b}. Assuming matching of all pairs of transistors, M_{3a} and M_{3b}, M_{4a} and M_{4b}, it can be observed that $V_A = V_C$.

The authors propose a master–slave tuning technique illustrated in Fig. 5.24c based on a *transconductance division scheme*. This uses two transconductors G_{m1} and G_{m2} one of which (G_{m1}) is matched to the transconductance in the VCO and another (G_{m2}) is matched to those in the G_m-C filter. A divider produces a voltage V_2/N from the input voltage V_2. A feedback loop makes $G_{m2}V_2 = G_{m1}V_2/N$ so that $G_{m1}/G_{m2} = N$. Thus division by N is achieved by using a MDAC. Note that the G_m variation as a function of input level as well as the offsets of both paths affects the accuracy of the tuning loop. The authors have used a10-bit MDAC. Thus for a maximum input of 500 mV, the offset needs to be less than a few mV. This is achieved by using large input transistors M_{3a} and M_{3b}. The VCO structure is based on the two-integrator loop as shown in Fig. 5.24d. The negative and positive resistances control the oscillation amplitude by compensating the finite output resistance of the OTAs. The VCO frequency used was 2.5 MHz.

D'Amico et al. [5.24] have proposed an active G_m-RC approach that exploits the opamp pole in the transfer function realization for dual mode base-band filter for WLAN (11 MHz) and UMTS (2.11 MHz) applications. This is based on a cascade of two second-order cells. The filter shares the capacitors and opamps in both modes thus saving area while maintaining the same linearity and low noise. A calibration circuit is employed to adjust the cutoff frequency deviation. The architecture of the cell (Fig. 2.26f) is redrawn for convenience together with the internal structure of the opamp and showing all the parasitics in Fig. 5.25a. Note than an adjusting circuit is required to set $G_{m1} = \frac{1}{k_g R_1}$ so that the filter parameters are dependent on

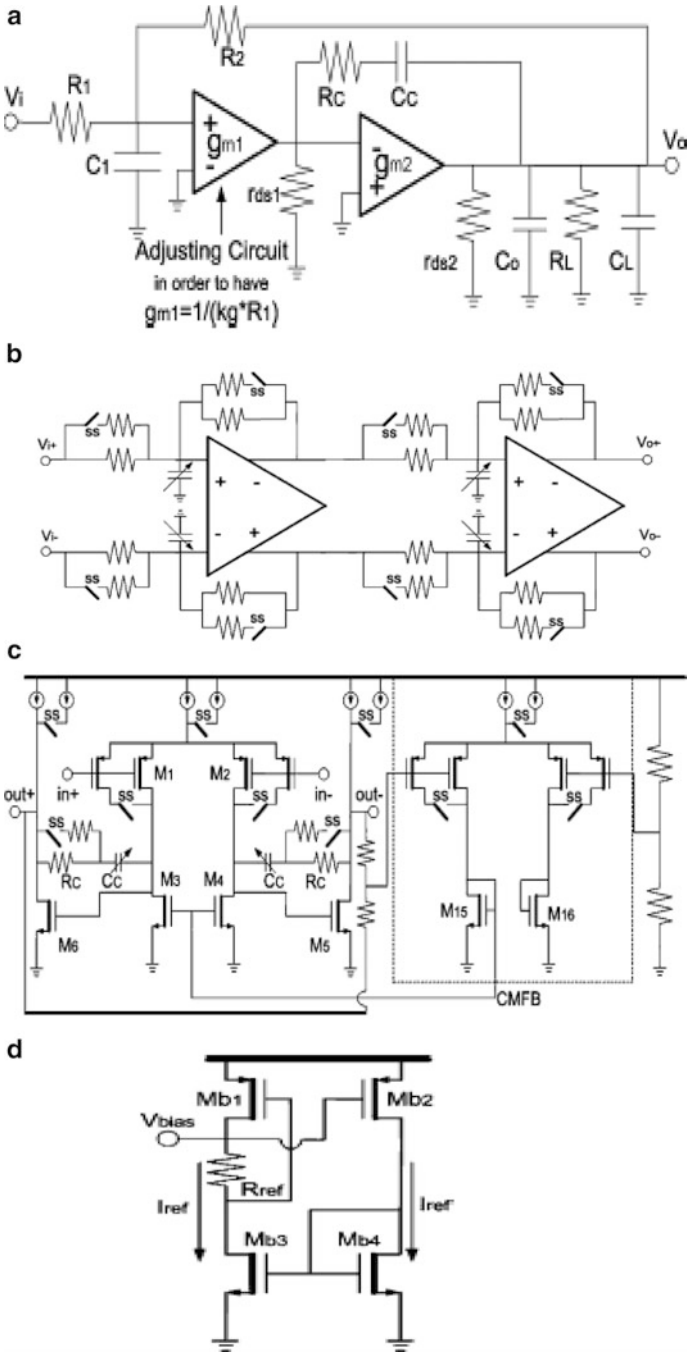


Fig. 5.25 (**a**) Active *Gm*-RC biquadratic cell with internal parasitics, (**b**) fourth-order reconfigurable filter structure based on (**a**), (**c**) opamp schematic, (**d**) schematic of adjusting circuit, and (**e**) calibration circuit (Adapted from [5.24] ©IEEE 2006)

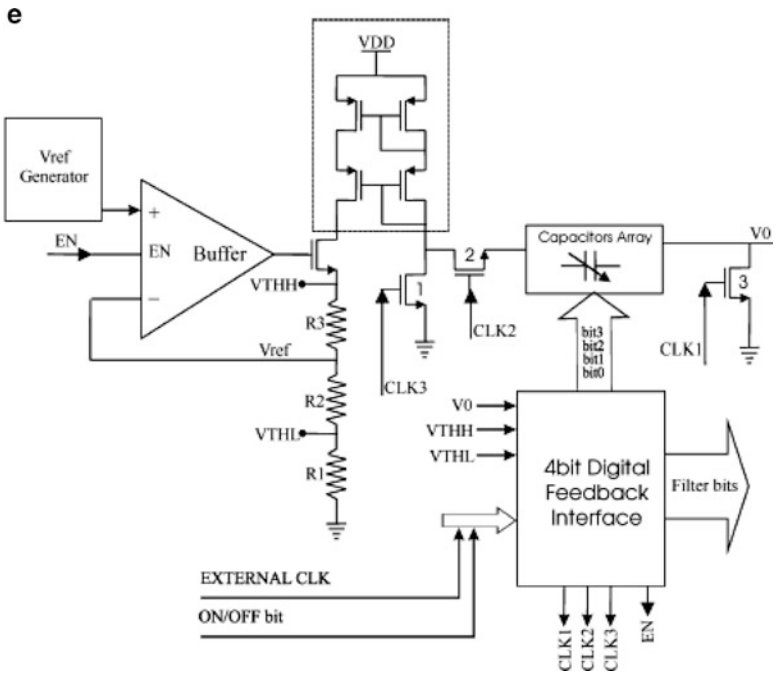


Fig. 5.25 (continued)

resistors R_1, R_2 rather than on G_{m1}. The transfer function of the low-pass filter can be derived as

$$\frac{V_o}{V_{in}} = \frac{\left(\dfrac{1}{k_g\ R_1^2\ C_1\ C_c}\right)}{s^2 + s\left(\dfrac{R_1 + R_2}{C_1\ R_1\ R_2}\right) + \dfrac{1}{k_g\ C_1\ C_c\ R_1\ R_2}} \tag{5.10}$$

The f_u/f_{LP} for this design is lower than 2 meaning that the opamp bandwidth need not be very high. This reduces the power consumption. The RC network filters the high level of out of band blockers. A tuning system is used to tune the opamp frequency response. The complete filter architecture is presented in Fig. 5.25b. Note that the filter can be reconfigured using the single selection bit "SS". The opamp implementation is presented in Fig. 5.25c. The transistors M_1 and M_2 form the input differential pair realizing G_{m1} and transistors M_5 and M_6 realize G_{m2}. The CMFB circuit is implemented using another differential amplifier as shown in Fig. 5.25c. A Miller compensation scheme using R_c and C_c is employed. The size of the input devices, current levels, R_c and C_c, are controlled by the standard selection bit in order to reduce the power consumption in the UMTS case. The adjusting circuit is shown in Fig. 5.25d. It correlates the transconductance variation of the input transistors G_{m1} with the variations in external resistances around the opamp.

It forces G_{m1} to be proportional to $1/R_{REF}$ by regulating the current of the input stage. The matching between M_{b1}, M_1, and M_2 is guaranteed. The resistance R_{REF} is matched with the resistances in the filter. Note that M_1, M_2 operate with same current density as M_{b1}. Thus the transconductance of M_1 and M_2 is proportional to $1/R_{REF}$. In addition, the process-related variations of R and C values may necessitate tuning which is carried out by using programmable capacitor arrays whose value is set by an on-chip calibration circuit shown in Fig. 5.25e. It is based on a comparison between an isolated time constant RC and a precise external clock period. A 4-bit code is used to be fed to all the PCAs. After calibration is performed, this circuit can be switched off to conserve power.

Matteirs et al. [5.25] have described a fourth-order analog base-band filter for telecomm applications (see Fig. 5.26b) that can operate with a 0.55 V dc voltage supply. This filter, denoted as an active-G_m-RC filter, is based on the amplifier finite pole. A second-order section uses minimum components: one opamp, one capacitor, and two resistors. At low supply voltages, the large overdrive needed for an open loop-type G_m-C filter is a disadvantage that limits the dynamic range. The relationship between supply voltage, MOS threshold voltage, and minimum channel length is shown in Fig. 5.26a. Hence, closed loop circuits have been recommended. The chosen active G_m-RC configuration of Fig. 5.25a exhibits good linearity and low noise.

The input common mode feedback technique shown in Fig. 5.26c is suggested to reduce the input common mode voltage to slightly less than $V_{DD}/2$. This uses two current sources formed by M_{B1} and M_{B2}. These force the virtual ground terminal voltage $V_{oa,dc}$ to a value lower than $V_{DD}/2$ while maintaining $V_{i,dc} = V_{o,dc} = V_{DD}/2$:

$$V_{oa,dc} = \frac{V_{DD}}{2} - I_1 \frac{R_1 R_2}{R_1 + R_2} \tag{5.11}$$

The authors use a Miller compensated 2-stage opamp as shown in Fig. 5.26d. The output CMFB loop is also shown in Fig. 5.26d which uses a PMOS differential pair. The common mode voltage is sensed by resistors R_{cm} and R_d that can be chosen large.

The input common mode voltage can be sensed at the source of the PMOS opamp input pair (by the V_{ICNTRL} node). The complete filter schematic is presented in Fig. 5.26e.

D'Amico et al. [5.26] described a multistandard base-band chain for Bluetooth, UMTS, and WLAN. The overall architecture of this system is presented in Fig. 5.27a. Since the cellular application is most stringent, the specifications of the reconfigurable baseband chain are summarized in Table 5.3. The design is tailored to meet cellular specification thus implying overdesign for Bluetooth and WLAN applications. The bandwidths of Bluetooth, UMTS, and WLAN are 1, 2, and 10 MHz, respectively. The RF sections use different power supply voltages (1.2 V and 2.5 V). A LPF selects the needed bandwidth and has a fixed gain of 4 dB, a restriction imposed by the tunability of the cutoff frequency. The two PGAs determine the gain in coarse and fine steps. The PGA is presented in Fig. 5.27b which uses a differential amplifier stage with resistor degeneration and is resistively loaded. For small input signals, R_G is minimum and R_L is maximum, thereby reducing the input referred noise. For large input signals, R_L is maximized

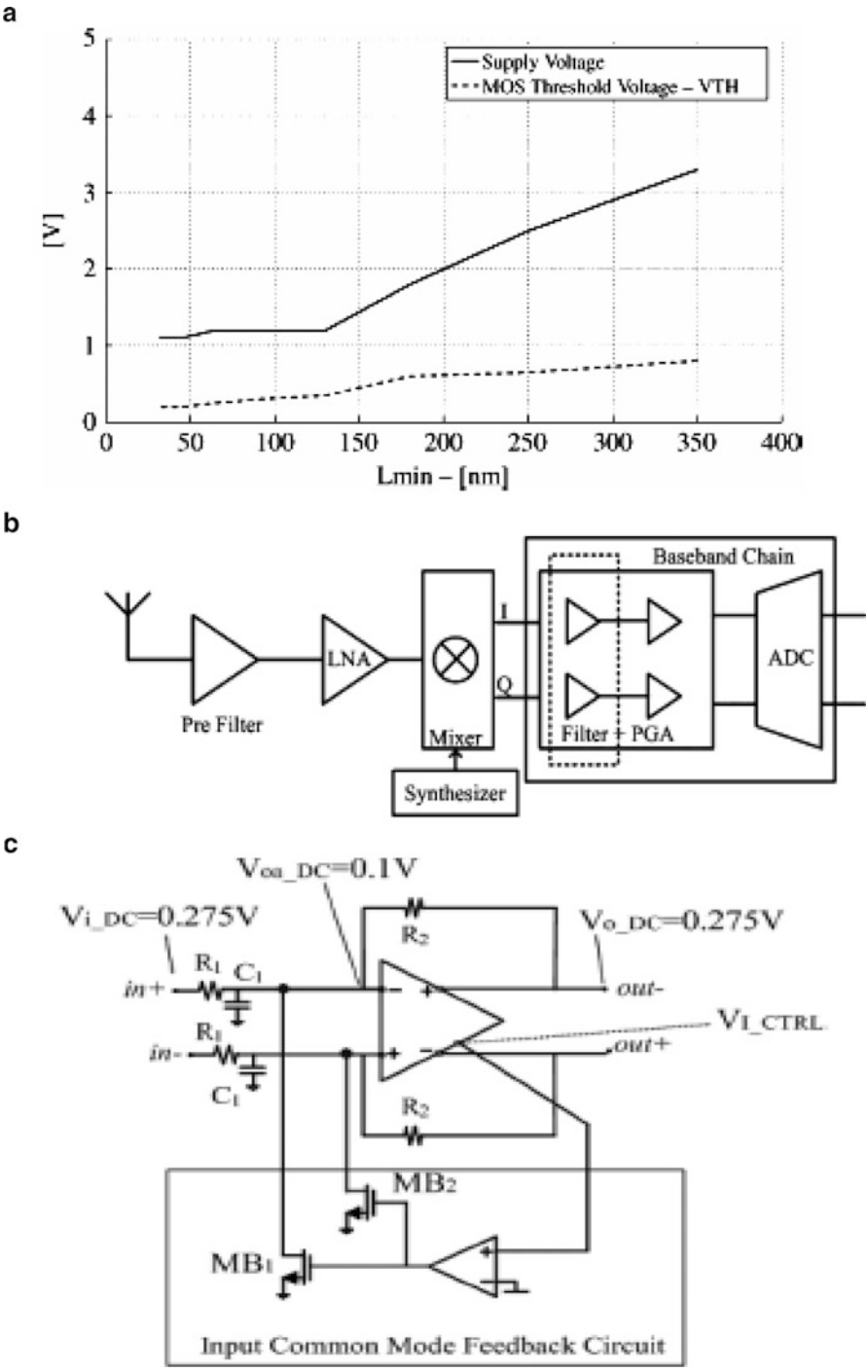


Fig. 5.26 (**a**) Supply voltage, MOS threshold voltage versus minimum channel length, (**b**) zero-IF receiver block diagram, (**c**) active G_m-RC cell with input CMFB, (**d**) opamp schematic, and (**e**) complete fourth-order filter (Adapted from [5.25] ©IEEE 2009)

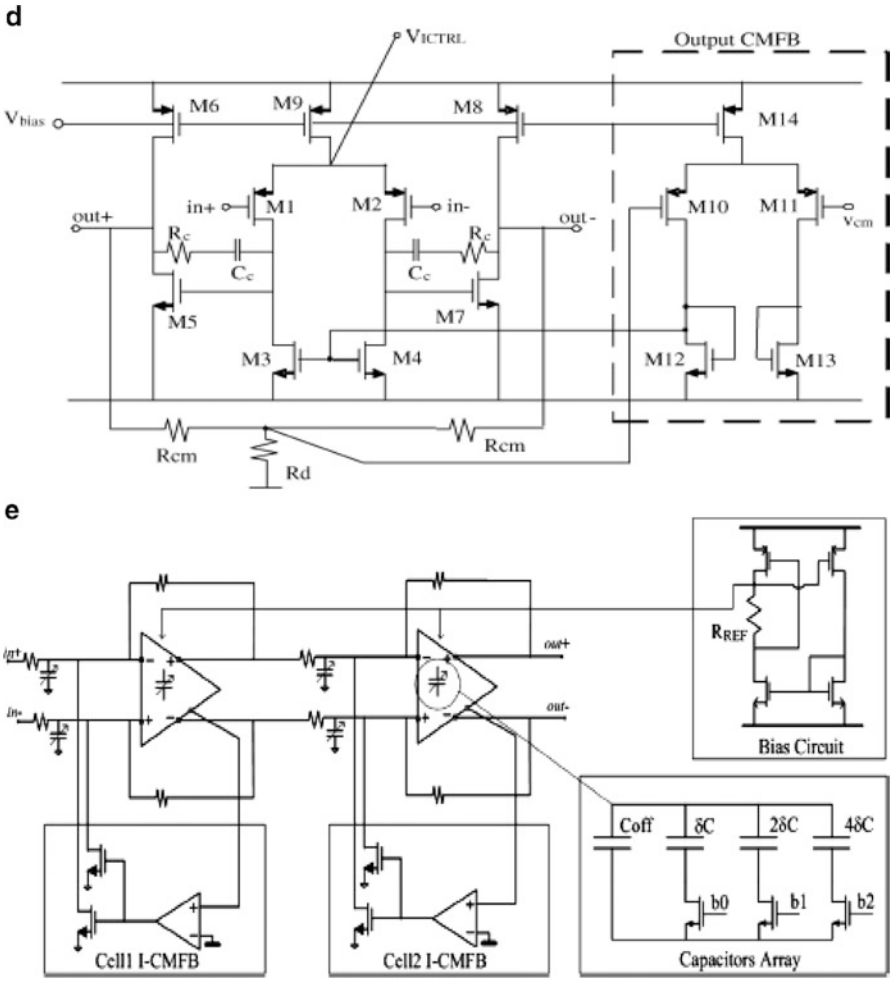


Fig. 5.26 (continued)

thereby decreasing the bandwidth decided by R_L and C_L. This will help to suppress the out-of-band tones. The input stage guarantees large in-band linearity. Transistors M_1 and M_2, opamps, and resistors R_G form a V–I converter. M_3 and M_4 form a level shifter. The input voltage is copied on the series impedance of transconductances G_{m1} (of M_1) and G_{m2} (of M_2) and resistors R_G. The linearity of G_m is improved by the large closed loop gain. The opamps in Fig. 5.27b are realized using the simple differential amplifier of Fig. 5.27c. Three bits are used to control the gain (two for R_L and one for R_G) (see Fig. 5.27d). The transistors M_9, M_{10}, and M_{11} act as switches and do not add parasitic capacitance to the drain and source nodes of M_1 and M_2. They are linear due to the reduced swing across them.

The LPF is based on two cascaded active G_m-RC cells described earlier (see Fig. 5.25a). The PGA2 configuration is shown in Fig. 5.27e. It uses resistors R_1 and R_2

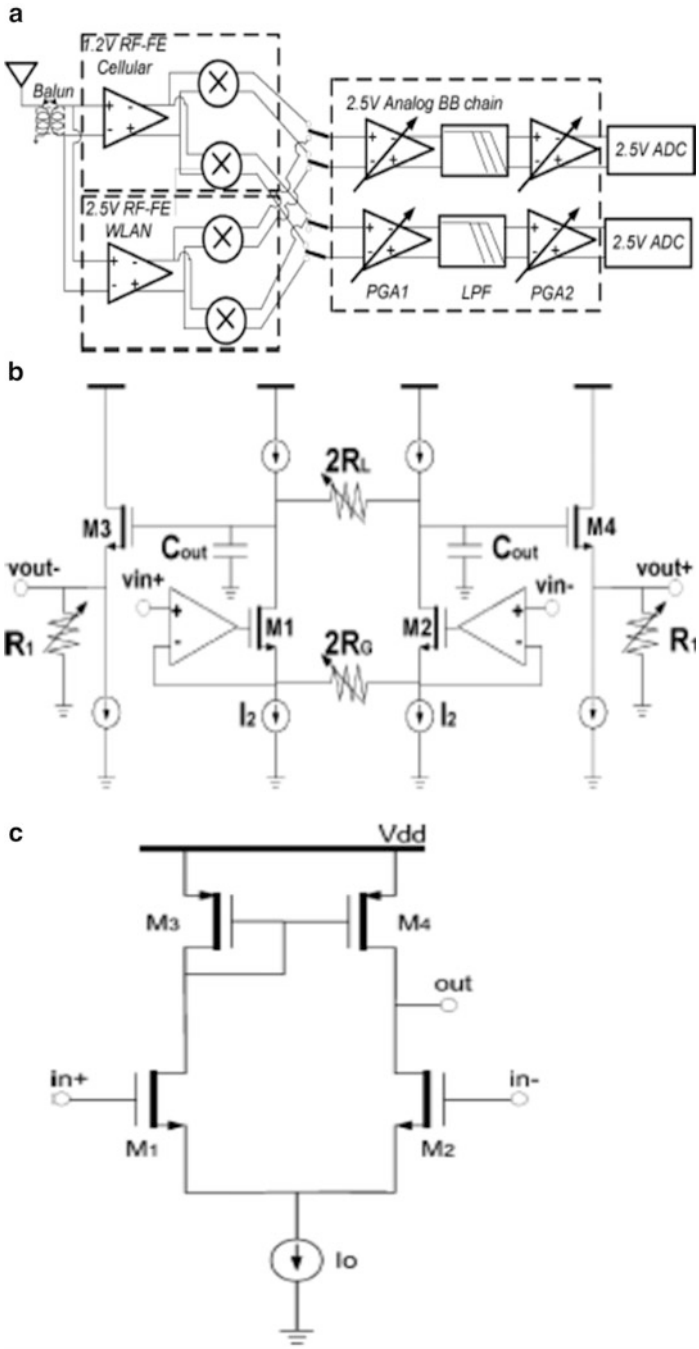


Fig. 5.27 (**a**) Overall receiver architecture, (**b**) PGA1 circuit, (**c**) input opamp, (**d**) gain control circuit, and (**e**) detailed block diagram of PGA2 (Adapted from [5.26] ©IEEE 2008)

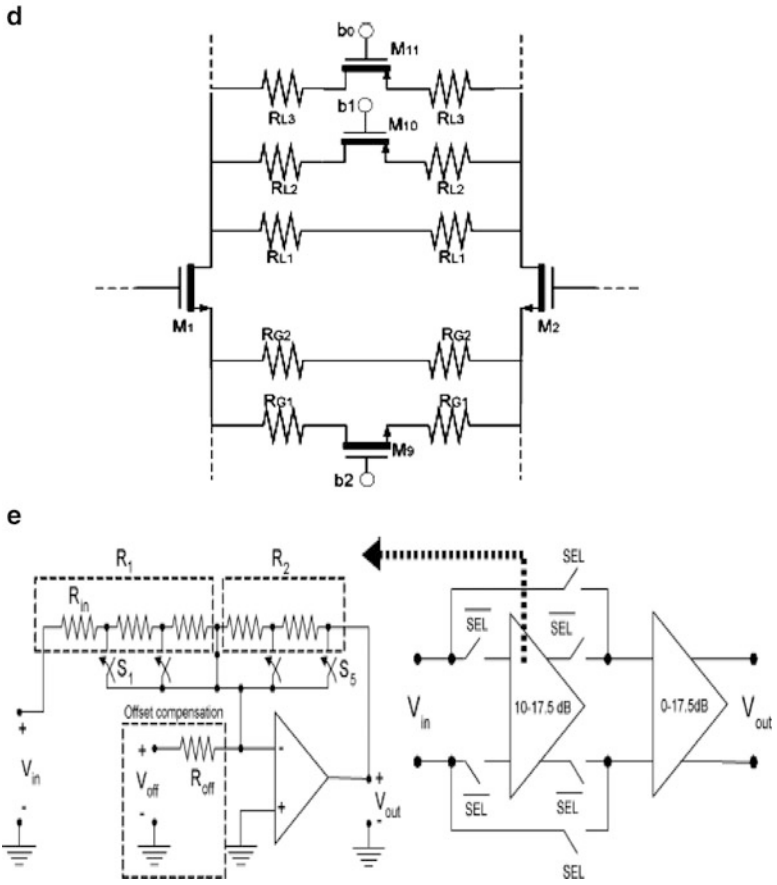


Fig. 5.27 (continued)

Table 5.3 Reconfigurable baseband chain main requirements (Adapted from [5.26]©IEEE2008)

	Bluetooth	UMTS	WLAN
IRN (nV/√Hz)	5		
DC-gain range (dB)	−6 + 68		
Bandwidth (MHz)	1	2	10
In=IIP3(dBm on 50Ω)	22		

which are programmable. The signal current does not flow through the switches thus avoiding the linearity and frequency response accuracy degradation. The two stages have gains programmable between (10–17.5 dB) and (0–17.5 dB) with a 2.5-dB step.

Chamla et al. [5.27] have described a third-order G_m-C Butterworth filter with a very wide tuning range from 50 KHz to 2.2 MHz to cover all the communication standards needed in practice. The commonly used specifications for the single-mode

Table 5.4 Analog baseband filters commonly used specifications in single-mode zero-IF receivers (Adapted from [5.27]©IEEE2005)

Parameter	GSM Spec.	Bluetooth Spec.	CDMA2000 Spec.	W-CDMA Spec.
Power consumption	3.5 mW	10 mW	7 mW	10 mW
Filter type	3th-order	3/4th-order	3/5th-order	3/5th-order
Cutoff frequency	fc = 115 KHz	fc = 650 KHz	fc = 700 KHz	fc = 2.2 MHz
IIP3	+10dBVp	+18dBVp	+15dBVp	+0dBVp
IIP2	+35dBVp	N/C	N/C	+35dBVp
Output DC offset	<10 mV	<15 mV	<15 mV	<20 mV
Output noise density	$400_N V/\sqrt{H_Z}$	$225\mu V/\sqrt{H_Z}$	$200\mu V/\sqrt{H_Z}$	$350_N V/\sqrt{H_Z}$
IQ mismatch (phase)	<1°	N/C	<2°	N/C
IQ mismatch (gain)	<0.3 dB	<0.5 dB	<0.5 dB	<0.5 dB

zero-IF receivers for these standards are presented in Table 5.4. The architecture is shown in Fig. 5.28a where the two parallel filters based on simulation of LC ladders are used as shown. They share the same grounded capacitors. The G_m values in the lower and upper filters are ratioed α:1. Hence by using the mode select control bit, B can be switched off. Defining $\chi_I = G_{max}/G_{min}$ and choosing the lower filter attainable highest frequency the same as the lower attainable frequency of the top filter, the cutoff frequency of the complete filter can change from $G_m/(2\pi C\sqrt{\chi})$ to $G_m \chi^{3/2}/(2\pi C)$ or $f_{max}/f_{min} = \chi^2$. Thus the OTA needs to have a spread of 6 if the desired f_{max}/f_{min} is about 30.

The transconductance used by Chamla et al. [5.27] is presented in Fig. 5.28b. Bipolar transistors have higher G_m than MOS transistors for the same bias current and hence have been chosen for the cascode transistors. The transistors Q_1 and Q_2 fix the drain voltages of M_1 and M_2 so that G_m is independent of V_{GS}:

$$G_m = \mu C_{ox} \frac{W}{L} V_{DS} \tag{5.12}$$

in the triode region of operation. The battery is realized using diode-connected transistor Q_3 in series with resistor R_{tune}. The CMFB loop is shown in Fig. 5.28c which uses folding allowing increase of V_{DS} upto 500 mV. M_3 and M_4 are also working in the triode region. The transconductor can be switched off by grounding node B and turning off the PMOS current sources.

Guthrie et al. [5.28] have described a low-IF filter for a dual mode Zigbee/Bluetooth application. They describe a complex filter using the OTA-C technique shown in Fig. 5.29b which is derived from the RLC ladder filter of Fig. 5.29a. The top and bottom blocks realize low-pass filters and the coupling through the gyrators realizes the complex filter. Effectively, the coupling through the gyrator performs the transformation $s \rightarrow (s - j\omega_o)$ leading to the shifting of the low-pass response of the prototype to a frequency ω_o. Thus real integrators will become complex integrators:

$$\frac{1}{s\tau} \rightarrow \frac{1}{(s - j\,\omega_o)\tau} \tag{5.13}$$

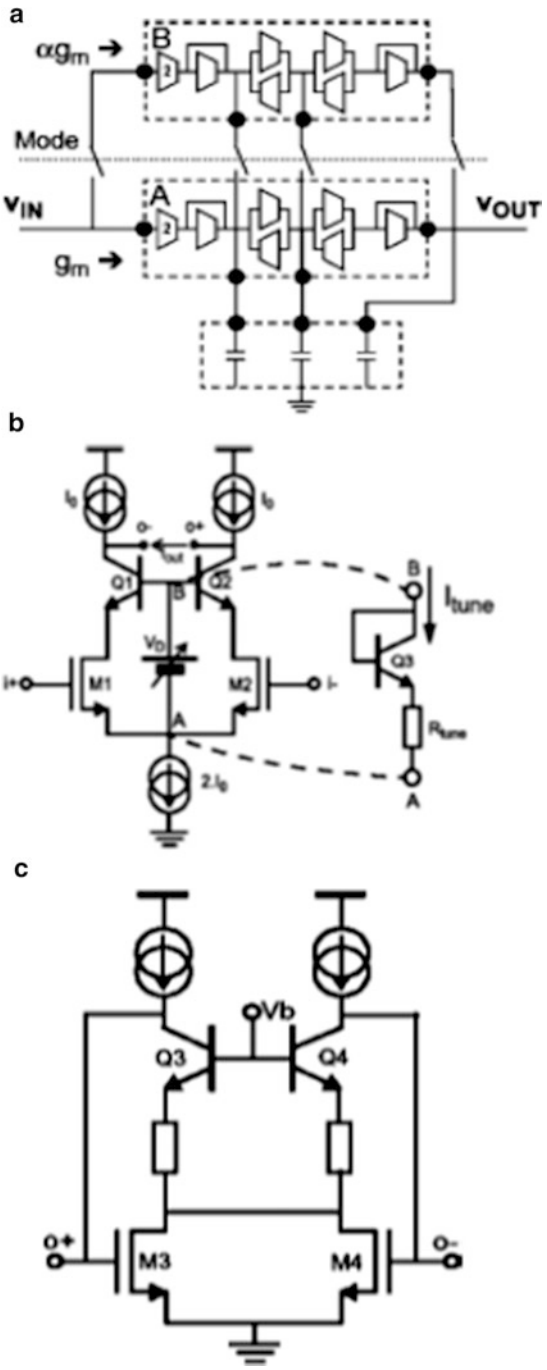


Fig. 5.28 (**a**) Multiple g_m reconfigurable low-pass filter structure, (**b**) schematic of transconductor cell and V_{DS} control, and (**c**) CMFB used for (**b**) (Adapted from [5.27] ©IEEE 2005)

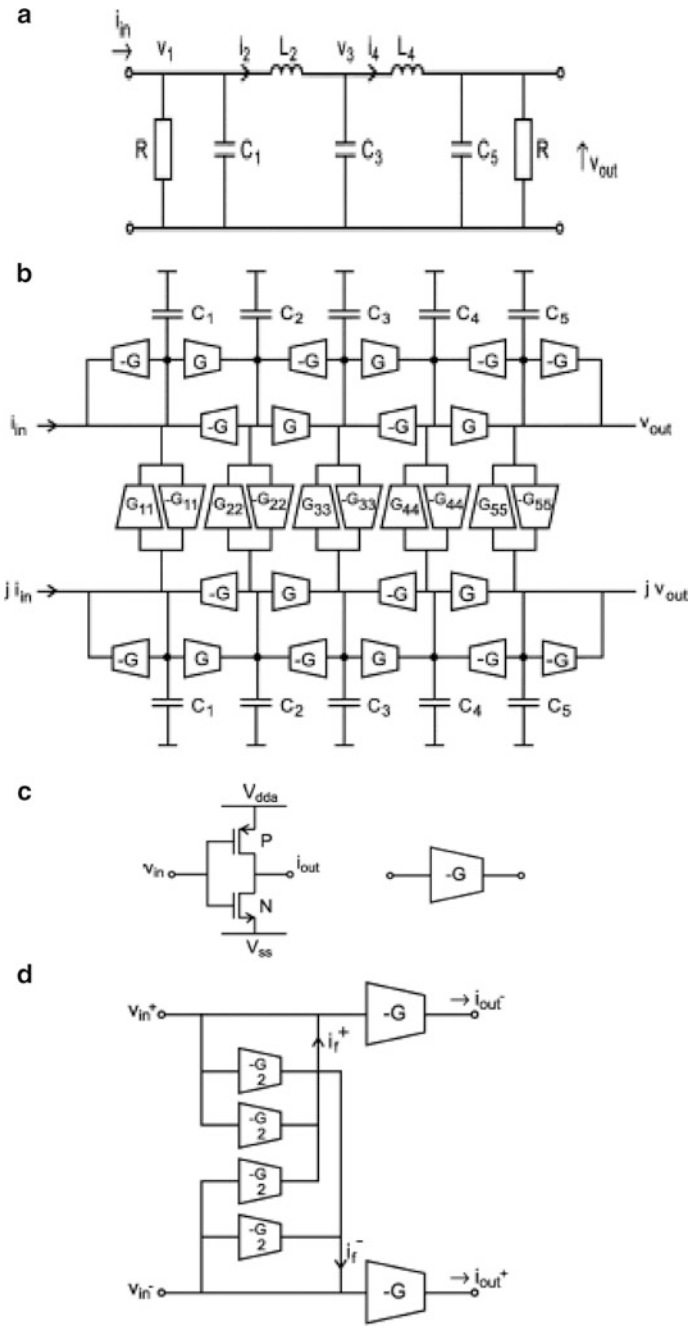


Fig. 5.29 (**a**) A fifth-order low-pass channel filter schematic, (**b**) gyrator-based complex band-pass filter derived from (**a**), (**c**) class AB CMOS single-ended transconductor, (**d**) balanced version of (**c**), (**e**) balanced gyrator loop of two transconductors with parasitics, (**f**) modified transconductor with capacitive feedthrough equalization, (**g**) preamplifier and postamplifier, (**h**) tuning control circuit, and (**i**) charge pump circuit (Adapted from [5.28] ©IEEE 2005)

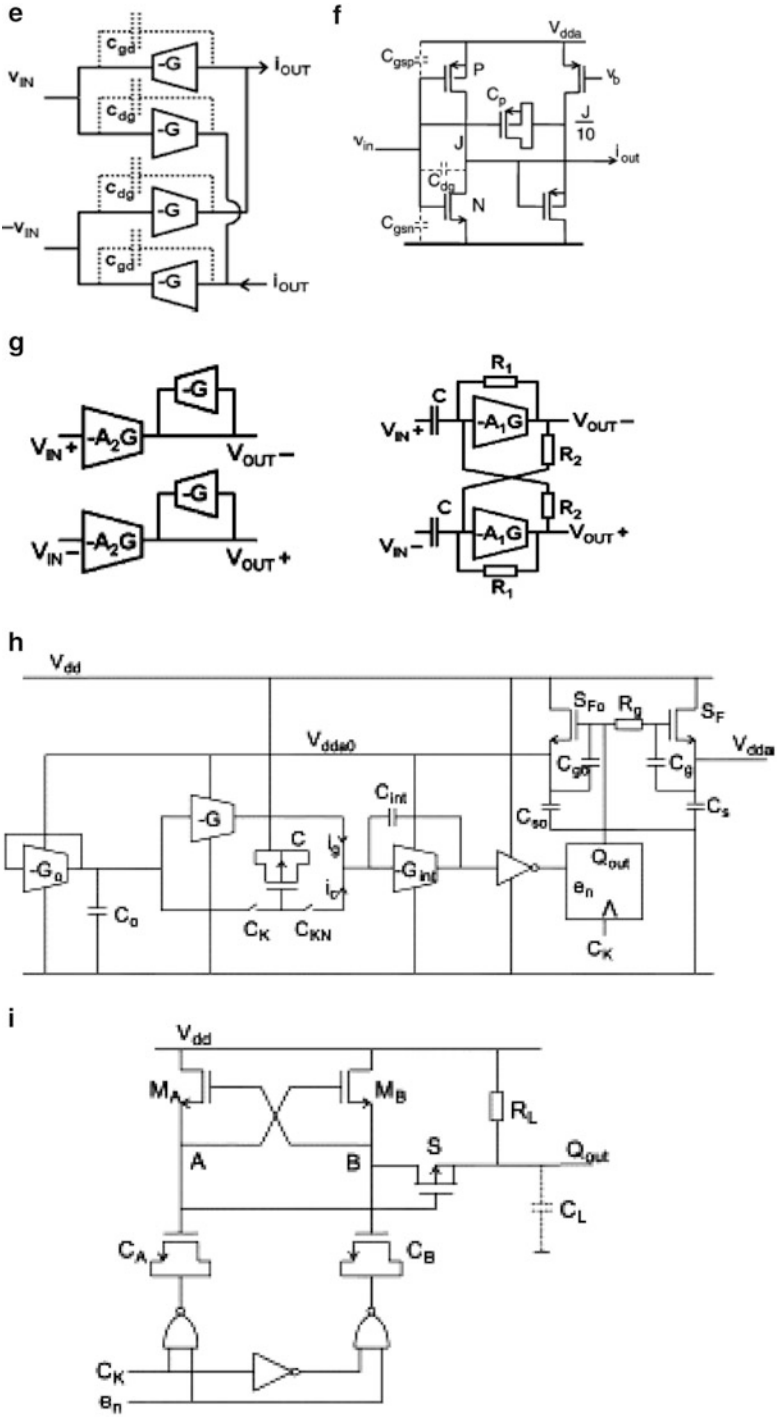


Fig. 5.29 (continued)

The design uses common sets of transconductors for Bluetooth and Zigbee application whereas the capacitor values are switched. The authors use balanced transconductors based on the Nauta class AB transconductor [5.29] shown in Fig. 5.29c. A balanced version of Fig. 5.29c is shown in Fig. 5.29d. By biasing the input at midrail voltage, the drain currents due to an input voltage V_{in} can be seen to be

$$I_n = J\left(1 + \frac{V_{in}G}{4J}\right)^2 \text{ and } I_p = J\left(1 - \frac{V_{in}G}{4J}\right)^2 \tag{5.14}$$

where J is the drain current with $V_{in} = 0$. Thus, $I_{int} = I_p - I_n = -GV_{in}$ showing that the transconductor is linear. It is important to note that the circuit is affected by the power supply voltage V_{dda} and power supply noise feedthrough.

The balanced gyrator loop is affected by the parasitic capacitance between the input and output terminals of the transconductor that are not reciprocal ($C_{gd} \neq C_{dg}$) (see Fig. 5.29e). This leads to undesirable peaking in the frequency response which can be solved by using the modified transconductor of Fig. 5.29f. A PMOS capacitor is connected between the output of the transconductor and output of the buffer following the transconductor. The postamplifier and preamplifier are shown in Fig. 5.29g. The preamplifier has common mode feedback through R_1 and R_2 which produces an effective feedback resistance of $R_1R_2/(R_2 - R_1)$. The capacitors block the dc input arriving from the mixer stage.

The frequency tuning loop is shown in Fig. 5.29h which uses a switched capacitor C, an integrator, a reference transconductor $-G$, an inverter, and a charge pump. The diode-connected transconductor $-G_o$ generates a quiescent voltage that is offset from that of the reference transconductor. Note that when the SC is set to G/F_{ck}, the loop stabilizes. The feedback loop adjusts the V_{ddao} of the reference transconductor which is buffered through S_{Fo} and S_F to provide V_{dda} for the complete filter. Note that R_g and C_g act as a filter to make V_{dda} ripple-free. The charge pump Q_{pump} [5.30] is shown in Fig. 5.29i.

Alzaher and Alghamdi [5.31] have described a CMOS band-pass filter for low-IF Bluetooth receivers based on the MOSFET-C technique. This uses current-followers (CF) and voltage buffers (VB). A CMOS CF is presented in Fig. 5.30a. The transistors M_9, M_{10} force equal current through M_1 and M_2 and hence the source of M_1 is at ground potential since the gate voltages of M_1 and M_2 are equal. The current into the x terminal is copied by M_6 and M_8 to the z output terminal. The level shifters M_3 and M_4 are used to adjust the standby current. The devices M_{11} and M_{12} provide biasing. The input impedance at the x terminal is reduced by feedback. M_3 and M_4 provide dc level shift to adjust the standby current. The VB circuit is presented in Fig. 5.30b. The voltage tracking is achieved by forcing same current through M_1 and M_2. Class AB negative feedback reduces the output resistance of this buffer stage.

The design of the filter uses MOSFET as a resistor. It is known that nonlinearity can be cancelled using the arrangement of Fig. 5.30c:

$$I_1 - I_2 = 2k(V_1 - V_2)(V_A - V_B) \tag{5.15}$$

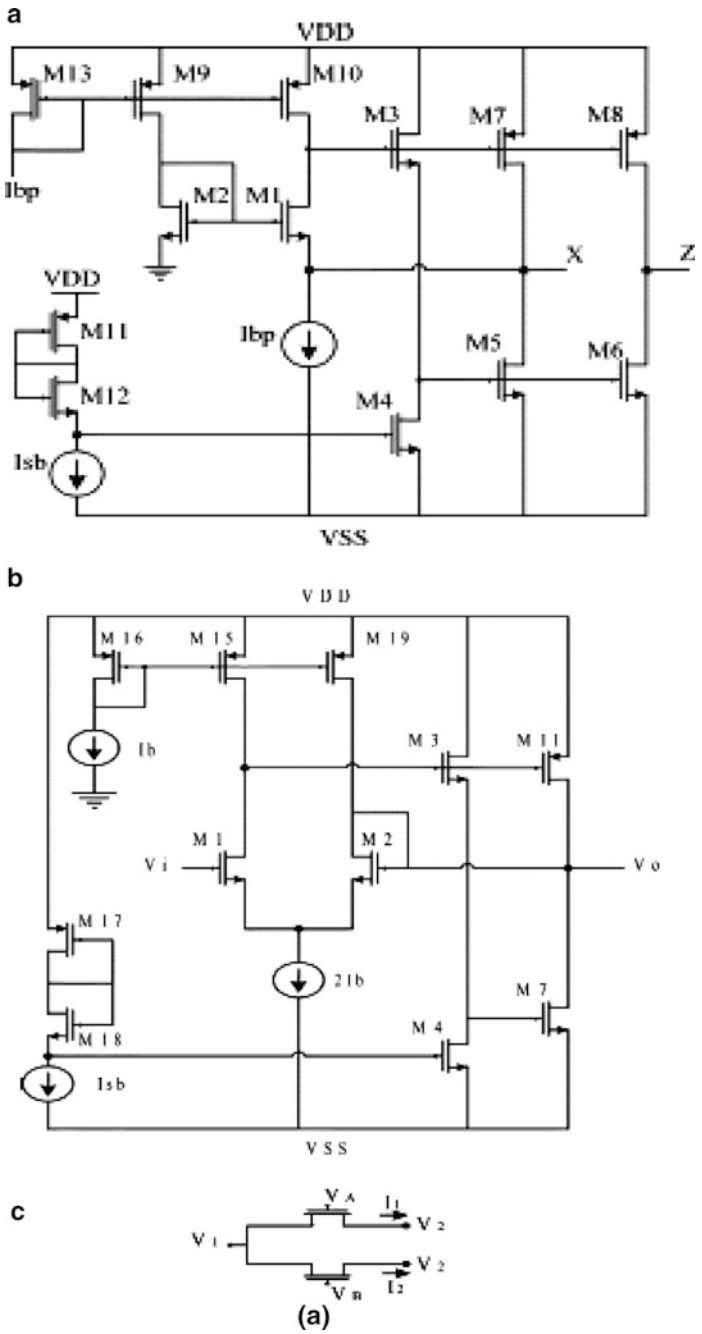


Fig. 5.30 (**a**) CMOS realization of a current follower, (**b**) CMOS realization of a voltage buffer, (**c**) nonlinearity cancellation of MOSFET using general method, (**d**) nonlinearity cancellation of MOSFET using CFs, (**e**) fully differential unity cell (UC), (**f**) Tow–Thomas biquad using UCs, (**g**) fully differential version of (**e**), (**h**) biquad with MOSFET nonlinearity cancellation, (**i**) optimized version of (**g**), and (**j**) automatic frequency tuning circuit (Adapted from [5.31] ©IEEE 2006)

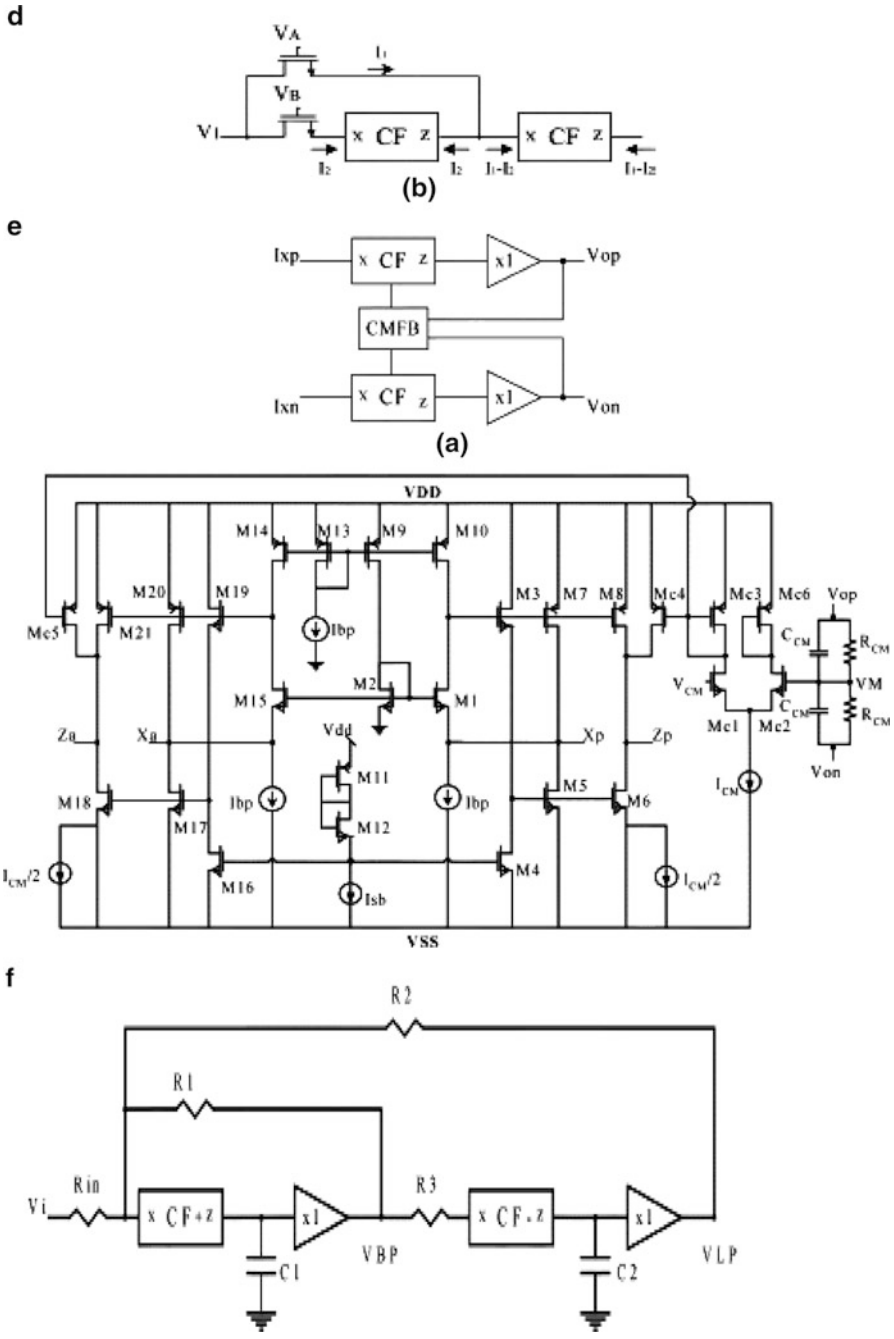


Fig. 5.30 (continued)

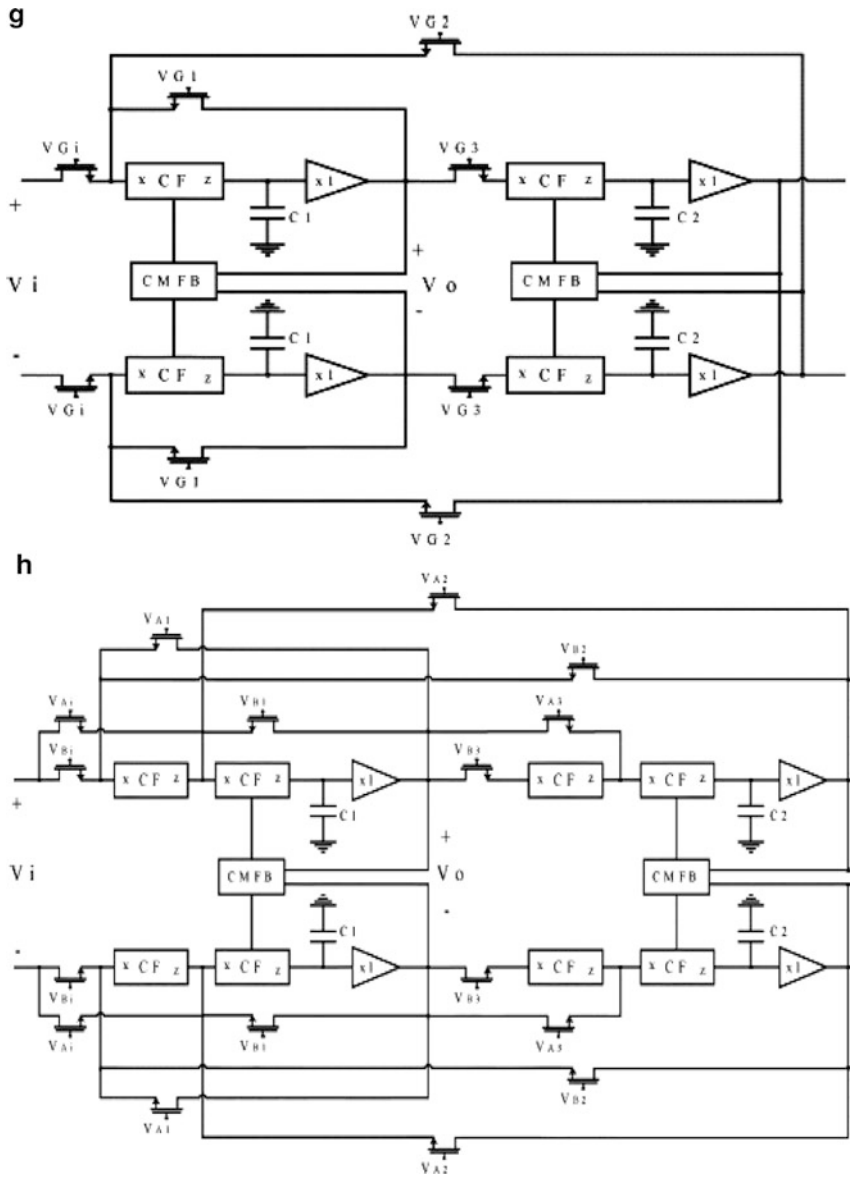


Fig. 5.30 (continued)

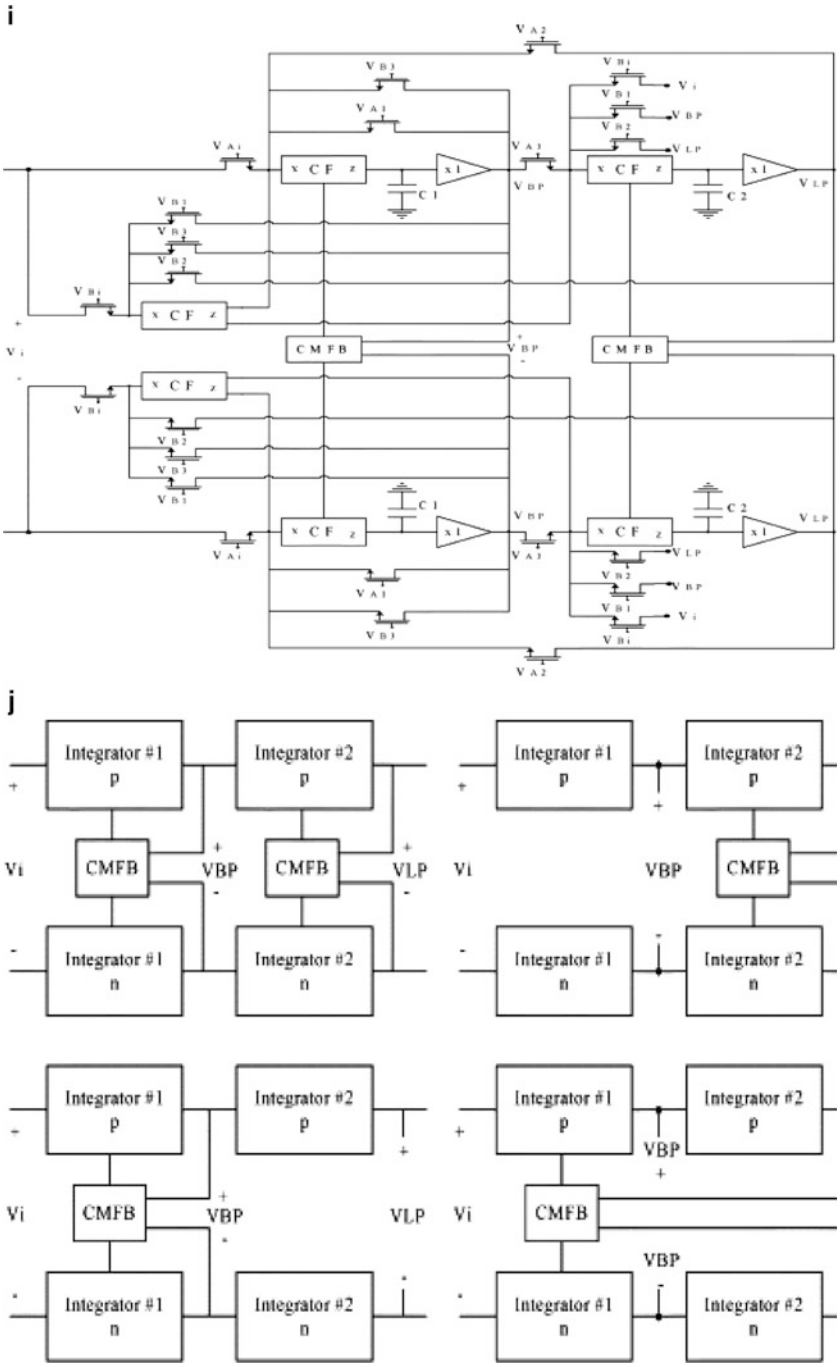


Fig. 5.30 (continued)

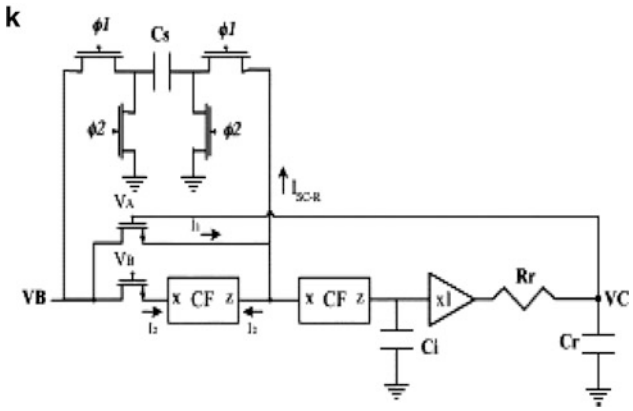


Fig. 5.30 (continued)

where $k = \frac{1}{2\mu C_{ox}} \frac{W}{L}$. Thus, a negative conductance can be attained by choosing $V_A = 0$. Using V_A and V_B, the resistor can be tuned. A virtual ground can be created to facilitate subtraction using the circuit of Fig. 5.30d while achieving nonlinearity cancellation.

A fully differential unity cell (UC) is realized as a cascade of CF and VB as shown in Fig. 5.30e. (Note that this is equivalent to a CFOA with y input grounded). The circuit of Fig. 5.30e has a CMFB loop. The RC network (R_{CM}, C_{CM}) generates the common mode voltage and compares it with V_{CM} and controls the currents through MC_3 and MC_5 and the voltages Z_p and Z_n.

The MOSFET-C biquad based on a two-integrator loop and using the UC is presented in Fig. 5.30f, g in single-ended and fully differential versions. Here, each CF and VB has its own CMFB loop. Note that even-order nonlinearity terms are removed due to the fully differential configuration. In the architecture shown in Fig. 5.30h odd-order nonlinearity cancellation can be achieved using the concept of Fig. 5.30d. Note that current summation can be done at the x terminal of the CF so as to reduce the number of CFs. A simplified version of Fig. 5.30h is presented in Fig. 5.30i with a reduced number of CFs, but some with dual outputs. The authors have shown that the IIP3 is improved by 6 dB for the realization of Fig. 5.30h and the power dissipation is more. On the other hand, the realization of Fig. 5.30i reduces the power consumption, area, and noise and improves the linearity. Note that two CMFB loops are needed: one each for integrator. Among the various alternatives possible shown in Fig. 5.30j, the topology (i) saves power. The topology (iii) gives good CMRR but has higher noise.

The authors have used an automatic tuning circuit shown in Fig. 5.30k that uses a frequency control loop with SC and continuous path. The loop settles when the resistance of the SC equals the MOSFET-C equivalent resistance.

Emira and Sanchez-Sinencio [5.32] have described a complex twelfth-order filter for Bluetooth application. The IF chosen was 2 MHz and the bandwidth of the filter is 1,060 KHz. The complex filter shifts the low-pass filter response to $j\omega_{IF}$ as can be seen from the mapping $s + \omega_{LF} \rightarrow s + \omega_{LF} - j\omega_{IF}$. Thus the input–output relation of a first-order complex filter can be written as

$$x_c = \frac{\omega_c}{s + \omega_{LF} - j\,\omega_{IF}}\, x_i \tag{5.16a}$$

where x_c and x_i are $x_c = x_{cI} + jx_{cQ}$ and $x_i = x_{iI} + jx_{iQ}$. Thus, we have

$$x_{cI} = \frac{\omega_o}{s + \omega_{LF}}\left(x_{iI} - \frac{\omega_{IF}}{\omega_o}\, x_{cQ}\right) \tag{5.16b}$$

$$x_{cQ} = \frac{\omega_o}{s + \omega_{LF}}\left(x_{iQ} - \frac{\omega_{IF}}{\omega_o}\, x_{cI}\right) \tag{5.16c}$$

The architecture of a first-order filter can thus be drawn as in Fig. 5.31a. An actual building block implementation is shown in Fig. 5.31b. An active RC implementation is presented in Fig. 5.31c. A OTA-C complex first-order filter is shown in Fig. 5.31d. Essentially, two paths will exist comprising a low-pass filter and the cross-connection of OTAs realizes the complex filter.

The authors have used pseudo differential OTAs shown in Fig. 5.32a. These need CM feedback loops or CM feedforward loops (CMFF) as shown in Fig. 5.32b, c. Note that CMFB is needed in the case where the output impedance of the OTA is high to bring the V_{CM} output impedance low. On the other hand, if the output impedance is small, then CMFF will suffice. The common mode detector (CMD) is shown in Fig. 5.32d, which is inverting so that its output can be connected to V_b of the OTA. In the case of CMFF, the noninverting control output are needed and can be derived as shown in Fig. 5.32d.

The conceptual complex biquad and complete circuit used in the I branch are shown in Fig. 5.33a and b. It can be seen that OTA1–OTA4 realize the biquad. The OTAs 5 and OTA 6 perform the linear frequency transformation. The OTA 1 has high output impedance and hence CMFB is used whereas OTA 2 is loaded by the resistance realized by OTA3 and hence CMFF is used. OTA3 does not need CMFF or CMFB and hence its bias voltage is connected to a fixed voltage. OTA4-OTA6 also use CMFF.

The frequency tuning is accomplished using the tuning circuit shown in Fig. 5.33c. A relaxation oscillator based on the OTA-C technique with transconductors of the same type used in the main complex filter is used. Its frequency is compared with a reference frequency (1 MHz). After reset, both counters start counting and once the reference counter reaches 64, the Up/Down counter counts or freezes depending on the difference between counts of the oscillator counter and reference counter. The contents of the U/D counter is fed to the DAC to generate a control voltage V_i. When the reference counter reaches 128, a new comparison cycle starts, this time with the updated oscillator frequency. For a $\pm 30\%$ process variation and a 7-bit DAC, the maximum frequency error is $\pm 0.23\%$ which leads to a 4.6 KHz error in the center frequency. The 7-bit DAC uses a resistor string. The relaxation oscillator is presented in Fig. 5.33d. It consists of OTA G_m and a current switch ($M_1 - M_6$), an integrating capacitor C_T, and a comparator and two switches. The CM input level V_c is changed to control the G_m. By applying a constant differential voltage ΔV to the OTA, the single-ended output current can be found as

$$g_m = \frac{k_n W}{L}(V_c - V_{Tn})\Delta V \tag{5.17}$$

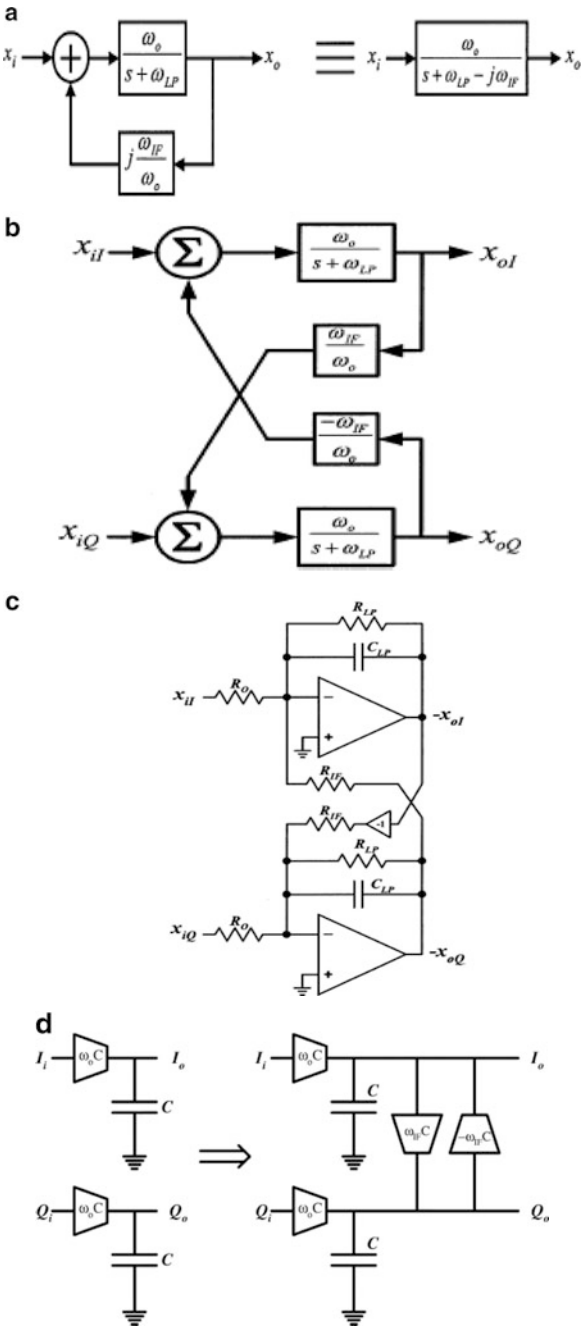


Fig. 5.31 (**a**) Conceptual complex LP filter, (**b**) actual building block implementation, (**c**) active RC implementation of (**b**), and (**d**) linear frequency transformation to convert LPF to complex BPF (Adapted from [5.32] ©IEEE 2003)

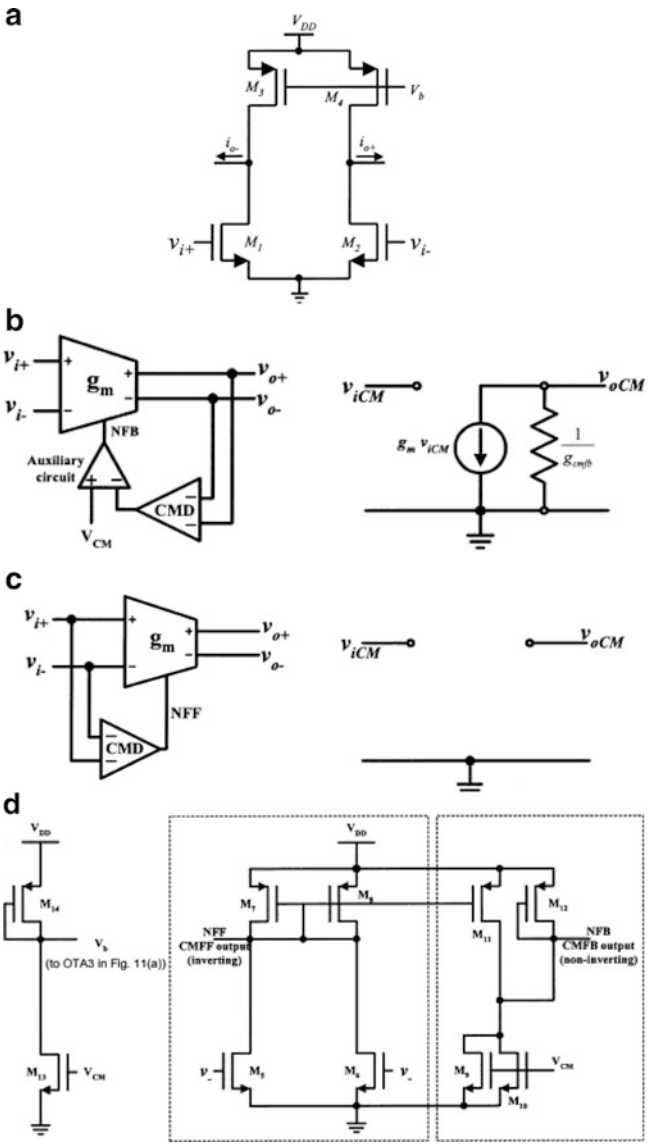


Fig. 5.32 (**a**) Pseudo-differential OTA, (**b**) CMFB loop and equivalent circuit, (**c**) CMFF circuit and equivalent, and (**d**) biasing circuit if no common mode control is used and CMD circuit (Adapted from [5.32] ©IEEE 2003)

which is mirrored to charge the capacitor C_T. The polarity is controlled by the differential pair. The slope of the triangular waveform across C_T is $G_m \Delta V$. The capacitor voltage is compared with V_{B1} and V_{B2} depending on the comparator output. The comparator output controls the differential pair transistors as well as the threshold voltage of the comparator. The frequency of oscillation is $f_{osc} = \frac{1}{4}\frac{g_m}{C_T}\frac{\Delta V}{\Delta V_B}$ where $\Delta V_B = V_{B1} - V_{B2}$. Note that V_{B1} and V_{B2} are obtained from the resistor string of the DAC.

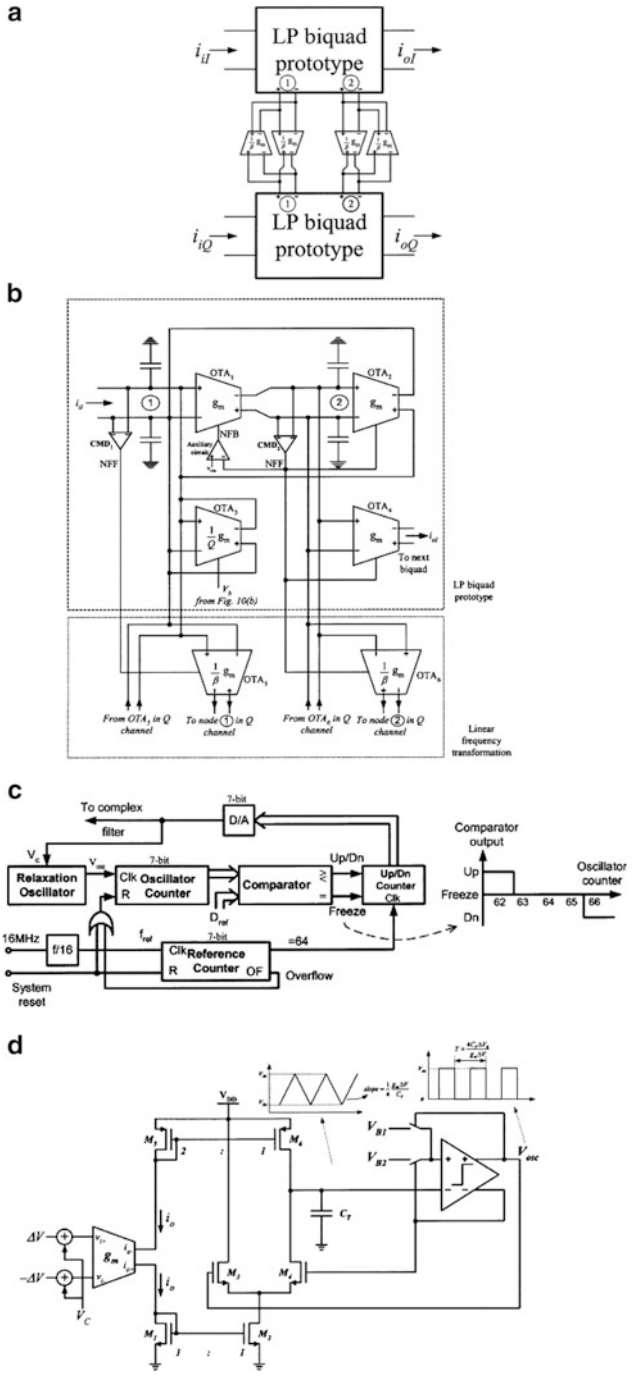


Fig. 5.33 (**a**) Conceptual complex biquad, (**b**) complete circuit of (**a**), (**c**) frequency tuning circuit for complex filter, and (**d**) relaxation oscillator (Adapted from [5.32] ©IEEE 2003)

5.7 G_m-C Filters for Optical Receivers

A 11.1 Gbps analog PRML (partial response maximum likelihood) receiver for electronic dispersion compensation of fiber-optic communications has been described by Elahmadi et al. [5.33]. The architecture of this IC is shown in Fig. 5.34a where a programmable continuous-time filter and a programmable FIR filter are used to implement the PR (partial response) equalization. The output of the FIR block is fed to a MLSE detector for data recovery. Precise clock and symbol timing are provided by the decision-directed clock recovery (CR) block. The block diagram is further elaborated in Fig. 5.34b. The optical signal affected by dispersion is converted to the electrical domain by the transimpedance amplifier and fed to a variable gain amplifier for amplitude normalization and enters the CTF. A five-tap discrete time FIR filter provides further equalization. The output is sampled in a time-interleaved fashion by splitting into two data streams A and B. The technology used was SiGe BiCMOS BBT with a f_t of 150 GHz. The Viterbi decoder contains the ACS (add, compare, and select) function and a survival sequence register (SSR). A multiplexer reassembles the error-corrected streams into a single stream. The CR block provides the necessary timing for FIR, ACS, and SSR as well as synchronization of other on-chip functions.

The AGC loop involving VGA, peak detector (PD1), and an AGC logic block facilitate coarse tuning of the CTF output signal swing. When the CR enters the phase-locked mode, the AGC control logic switches to the fine loop through the phase detector PD2 maintaining the output of the FIR filter equal to REF2. The VGA gain in the loop is controlled by the 7-bit ADC. An automatic offset correction feature is also available for cancelling out the offset introduced in the VGA and CTF.

A fourth-order G_m-C low-pass Bessel CTF is used consisting of two biquads and input V–I converter and an output I–V converter (see Fig. 5.34c). The cutoff frequency can be tuned from 1.5 to 3.5 GHz with a 4-bit granularity through a digital serial interface. The need for working at high frequencies with low power limits the architecture of OTA to the simplest differential pair using bipolar transistors as shown in Fig. 5.34d. A cross-connected differential pair ratioed at 1:5 has been used to obtain adequate linearity instead of using a resistor for increasing the dynamic range of the differential pair. The design takes note of the fact that although resistances may vary over process corners by more than 25%, g_m can be set virtually independent of PVT variation.

Temperature dependence of G_m can be decreased using the PTAT (proportional to absolute temperature) bias current. The circuit for PTAT reference producing currents proportional to both $1/R_{int}$ and $1/R_{ext}$ is shown in Fig. 5.34e. A constant bias voltage over temperature needs a bandgap current reference proportional to $1/R_{int}$. This is because of the reason that bias voltages are generated by setting up the currents through internal resistors. The bandgap current reference is shown in Fig. 5.34f.

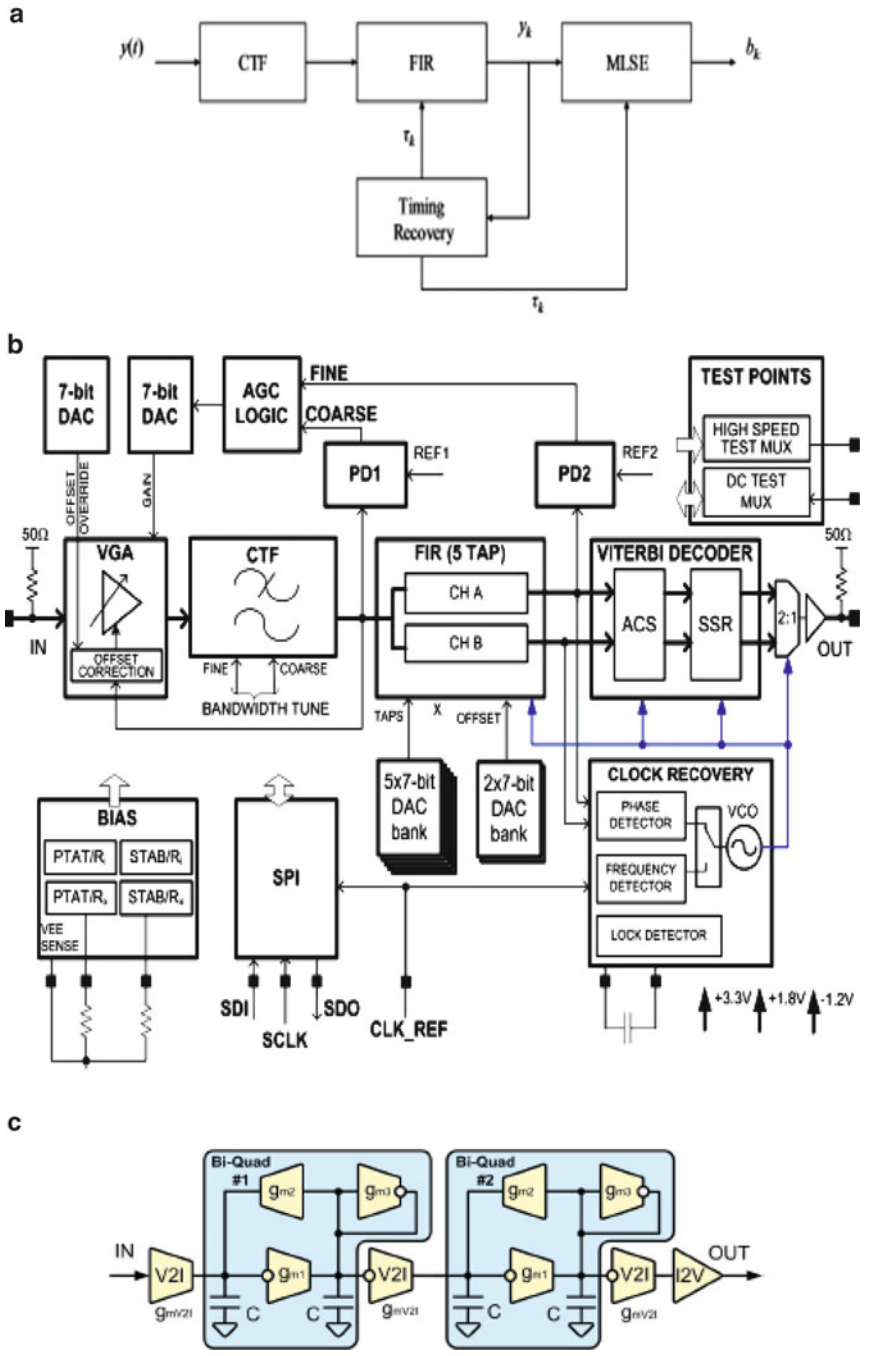


Fig. 5.34 (**a**) High-level architecture of a PRML receiver, (**b**) analog PRML receiver IC architecture, (**c**) continuous-time filter (CTF) block diagram, (**d**) linearized OTA, (**e**) current reference producing both PTAT currents proportional to $1/R_{int}$ and $1/R_{ext}$, and (**f**) current reference block producing the bandgap current proportional to $1/R_{int}$ (Adapted from [5.33] ©IEEE 2010)

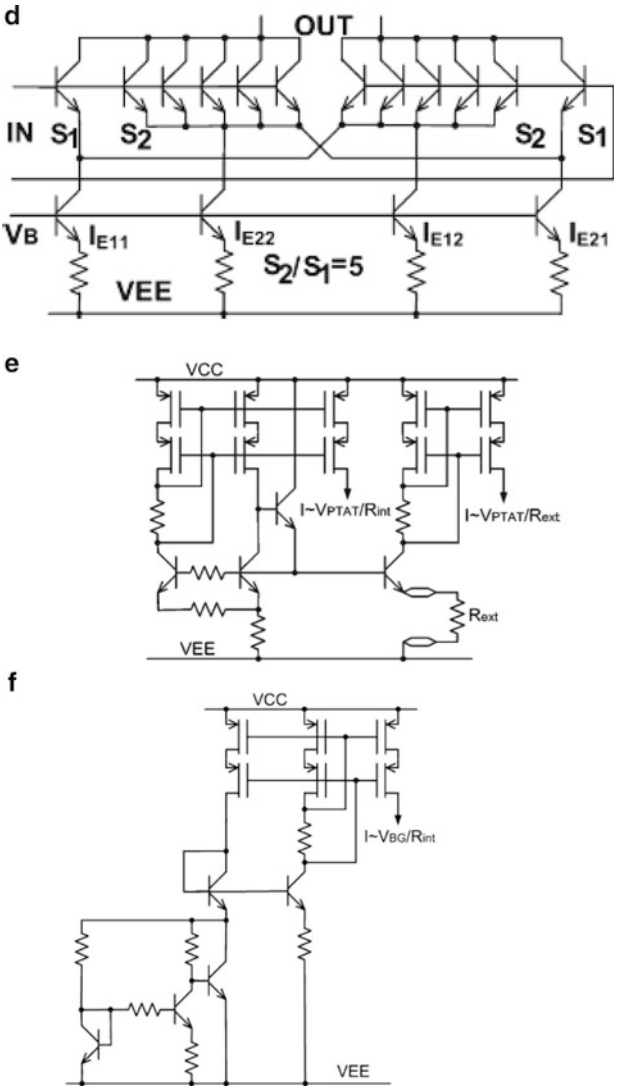


Fig. 5.34 (continued)

5.8 G_m-C Filters for Software Radio

Kilsunezuke et al. [5.34] have described a reconfigurable fourth-order LPF for software radio front-end applications. The block diagram of the analog base-band as shown in Fig. 5.35a comprises a programmable gain amplifier (PGA1) for coarse gain tuning followed by a fourth-order LPF. This is followed by another PGA2 for

fine gain tuning. The two cascaded second-order low-pass filters (see Fig. 5.35c) use discrete-time control of G_m values by switching off the G_m and switching on using variable duty cycle pulses as shown in Fig. 5.35b. The realized G_m is given by

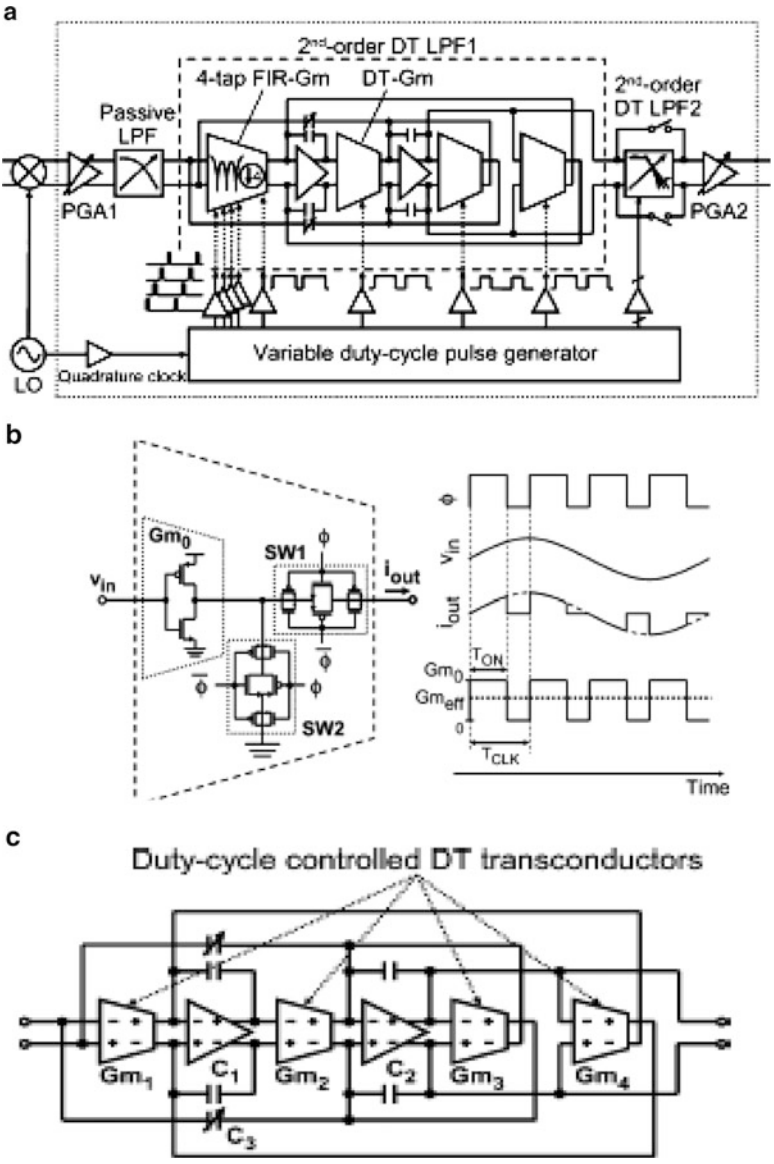


Fig. 5.35 (**a**) Block diagram of the analog baseband, (**b**) duty cycle controlled discrete-time transconductor, (**d**) antialiasing filter (passive filter +4-tap FIR filter), and (**e**) voltage input current output 4-tap FIR filter (Adapted from [5.34] ©IEEE 2009)

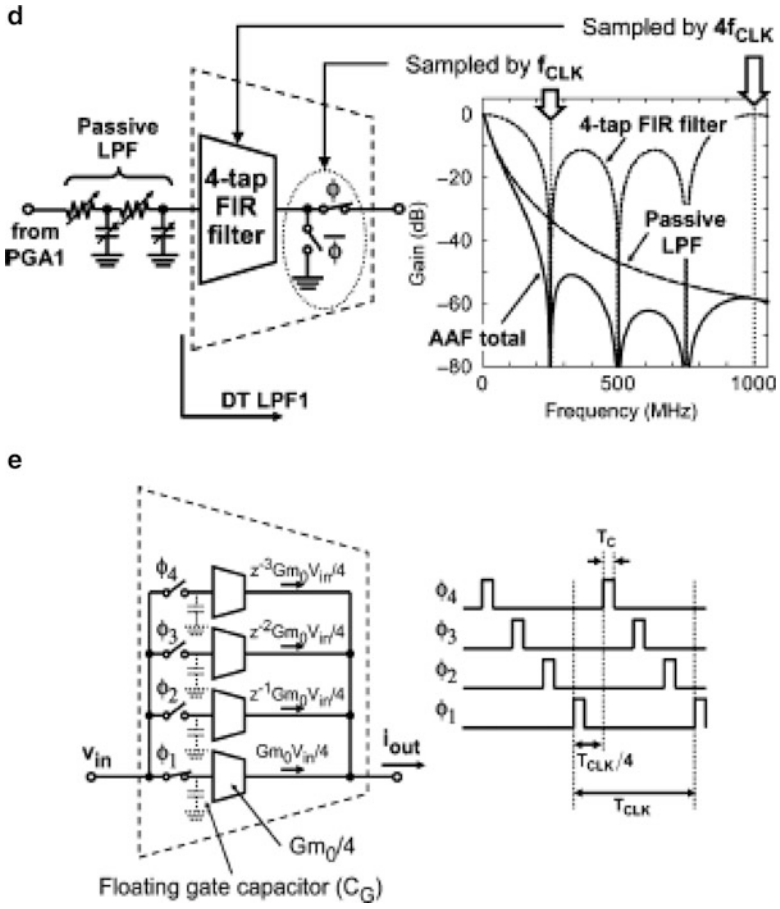


Fig. 5.35 (continued)

$G_{meff} = G_m(T_{ON}/T_{CLOCK})$. The G_m-C filters are based on the two-integrator loop and realize a transfer function

$$T(s) = \frac{s^2\left(\frac{C_3}{C_2}\right) + \frac{g_{m1}g_{m2}}{C_1C_2}}{s^2 + s\frac{g_{m3}}{C_1} + \frac{g_{m2}g_{m4}}{C_1C_2}} \tag{5.18}$$

A basic inverter is used as the G_m followed by two switches. The waveforms at various terminals are also shown in Fig. 5.35b. In Phase φ_1, the inverter output current flows to the load, whereas in Phase φ_2 , it flows to the ground. The advantage of such a design is that all OTAs can be the same size and use the same bias voltages realizing the same nominal value of G_m. Thus assuming that G_m/C is precisely tuned,

the design achieves a high tolerance to process fluctuations. An antialiasing filter is required due to the discrete time nature of the filter. This is realized by a second-order passive RC filter followed by a G_m-C-based DT FIR filter (see Fig. 5.35d). The FIR filter (see Fig. 5.35e) realizes a transfer function given by

$$G_{m,FIR}(z) = \frac{1 + z^{-1} + z^{-2} + z^{-3}}{4} G_{m,\,eff} \tag{5.19}$$

The variable duty cycle pulse generator comprises a 32-phase clock generator, a narrow pulse generator, a pulse decimator, and a switching matrix to generate the desired width pulses to control all the G_ms. The clock frequency used for the filter was 256 MHz derived from a master clock of 2 GHz. The chip has used a 90 nm CMOS process.

A low IF/zero IF configurable analog base-band IC has been described by Kitsunezuka et al. [5.35]. The software radio architecture and the analog base band are presented in Fig. 5.36a, b. The signal from the antenna is preamplified by a LNA and down-converted directly to IF by the quadrature mixer. The following analog filter attenuates the interferers and the PGA controls the gain. The IC features an I/Q phase imbalance cancellation scheme as shown in the block diagram of the analog base-band. The LO imbalance circuit needs four 25% duty cycle clocks derived from the external LO clock. The quadrature mixers can properly demodulate the input RF signal even if a few degrees of LO I/Q phase imbalance exist. The G_m-C filter following the mixer is duty cycle controlled followed by I/Q signal path rotators. This stage provides channel selection, antialiasing and image rejection. The DT G_m-C filter can be configured as a LPF in zero IF mode or BPF in the low IF mode. The filter control pulses are generated by a variable duty cycle pulse generator. The PGA consists of cascade-connected unit gain cells using two-OTA based amplifiers.

The circuit diagram of the OTA networks of a reconfigurable filter is shown in Fig. 5.36c which is applicable for both low-IF and zero-IF cases. As discussed earlier, a duty cycle control scheme is used to achieve reconfigurability. Each G_m is controlled by a variable duty cycle control pulse. By using two OTAs in parallel and switching them complementarily as shown in Fig. 5.36d, the effective G_m can be tuned. Note that the center frequency can be varied by varying G_{m5} in Fig. 5.36c.

5.9 G_m-C Filters for EEG Application

Casson and Rodriguez-Villegas [5.36] have described a 60 pW G_m-C continuous wavelet transform circuit for portable EEG systems. For portable and wearable electronics, extreme miniaturization is required. This limits the available battery size and power drain. The EEG needs to record the voltage between electrodes put on the scalp typically in the range 1–150 μV peak to peak over a 1–70 Hz bandwidth. The devices need to be discrete, lightweight, and comfortable for user

acceptance. These chips need real-time data reduction as well so that the transceiver power can be reduced.

The CWT (continuous wavelet transform) is suitable for low power implementations. The CWT of a signal $f(t)$ is defined as

$$W(a,b) = \frac{1}{\sqrt{a}} \int_{-\infty}^{\infty} f(t)\, \Psi^* \left(\frac{t-b}{a} \right) dt \tag{5.20}$$

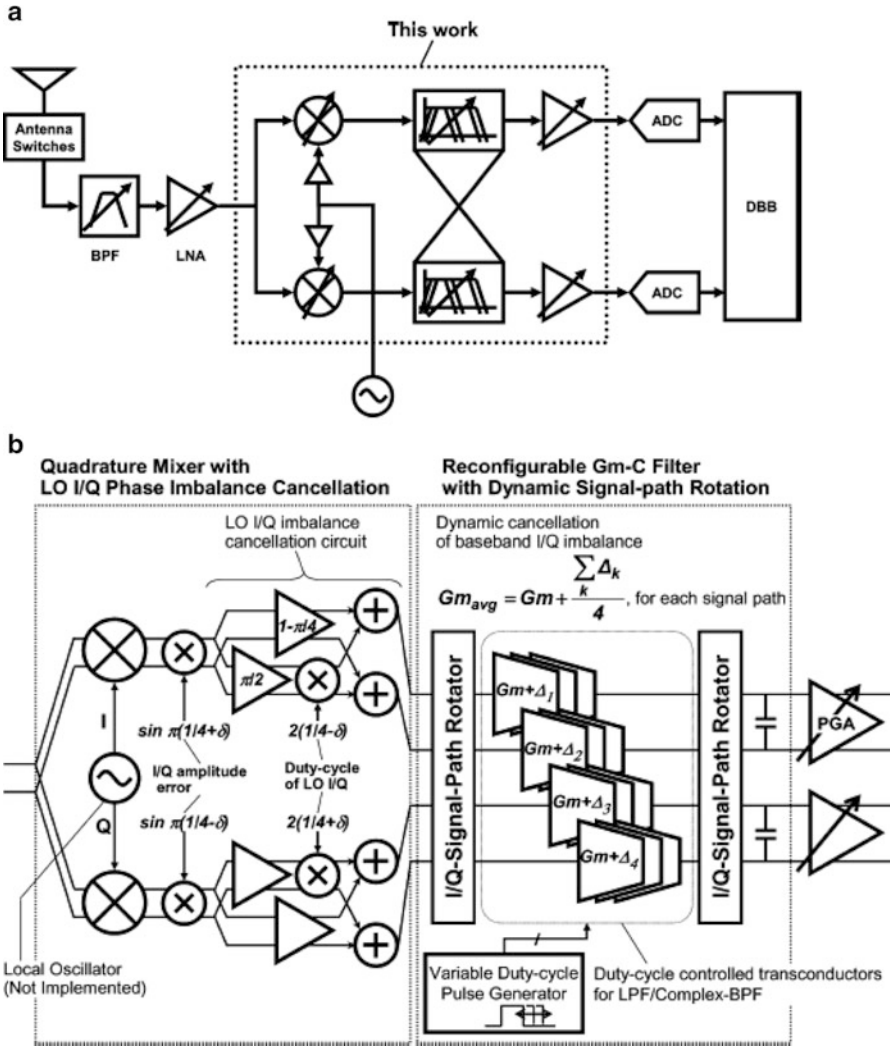


Fig. 5.36 (**a**) Architecture of software defined radio receiver, (**b**) block diagram of analog baseband, (**c**) transconductor networks of reconfigurable filters, and (**d**) duty cycle controlled transconductor and timing chart of control pulse (Adapted from [5.35] ©IEEE 2011)

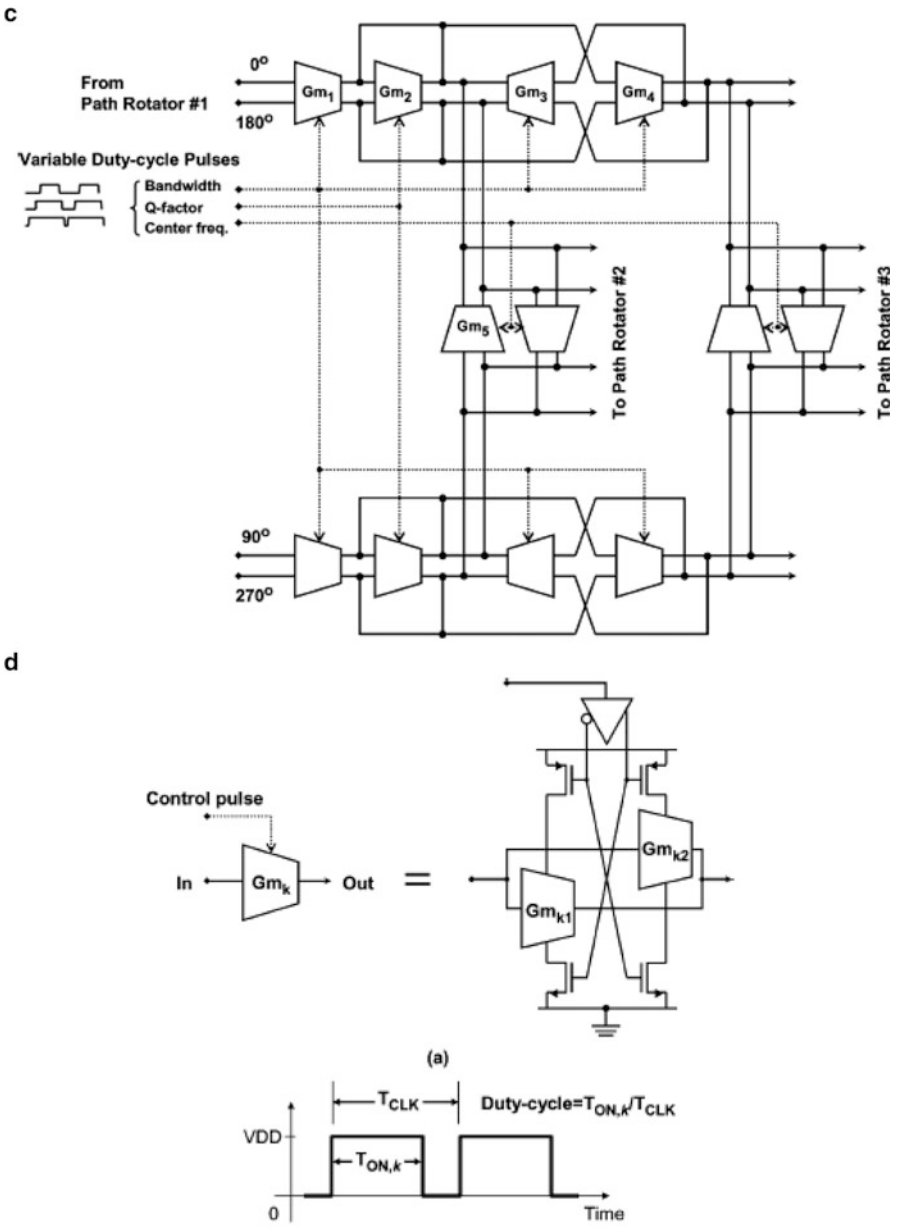


Fig. 5.36 (continued)

where $\Psi(t)$ is the mother wavelet, a is a dimensionless analysis scale, and b is the time at which the transform is taken. This corresponds to convolution of $f(t)$ with an impulse response

$$h(t) = \frac{1}{\sqrt{a}} \Psi\left(-\frac{t}{a}\right) \tag{5.21}$$

It has been found that $h(f)$ in (5.21) corresponds to a band-pass filter. The mother wavelet chosen was similar to the Mexican hat also called the low power CWT (LPCWT). A rational approximation to this can be found as the seventh-order transfer function

$$H(s) = \frac{-6.88X10^{-3}\, s^2}{2.34X10^{-8}\, s^7 + 1.34X10^{-6}\, s^6 + 3.7X10^{-5}\, s^5 + 6.79X10^{-4}\, s^4 + 8.67X10^{-3}\, s^3 + 0.075 s^2 + 0.40 s + 1} \tag{5.22}$$

The LPCWT mother wavelet function has the transfer function

$$H(s) = \frac{-\pi^{1/4}\sqrt{\frac{8}{3}\, a^5 s^2}}{1 + s\tau + \left(\frac{T^2 - a^2}{2}\right) s^2 + \left(\frac{T^3}{6} - \frac{T a^2}{2}\right) s^3 + \ldots.} \tag{5.23}$$

where the denominator is a truncated Maclaurin expansion of the term $e^{\left(sT - \frac{a^2 s^2}{2}\right)}$ and T is a delay introduced to ensure that $H(s)$ is open-loop stable. The impulse response is shown in Fig. 5.37a.

The G_m-C filter used is shown in Fig. 5.37c which is derived from the RLC prototype shown in Fig. 5.37b. The latter is obtained by replacing each grounded and floating inductor by a grounded and floating OTA-C-based inductance simulator, respectively. The authors have used the OTA of Fig. 5.37d which uses NMOS input transistors. The G_m realized in the weak inversion mode is

$$g_m = \frac{I_{bias}}{2n\, U_T} \tag{5.24}$$

where $n = 1.3$. Using a I_{bias} of 6.5 pA, a transconductance of 100 pS can be realized. The reader is urged to refer to [5.36] for an excellent treatment on issues related to deep weak inversion operation.

At extremely low currents, leakage current of the bond pads becomes significant. The linear range of a differential pair can be found as

$$V_{lin} = 1.5n\, U_T \sqrt{\tau(1 + i_f)} \tag{5.25}$$

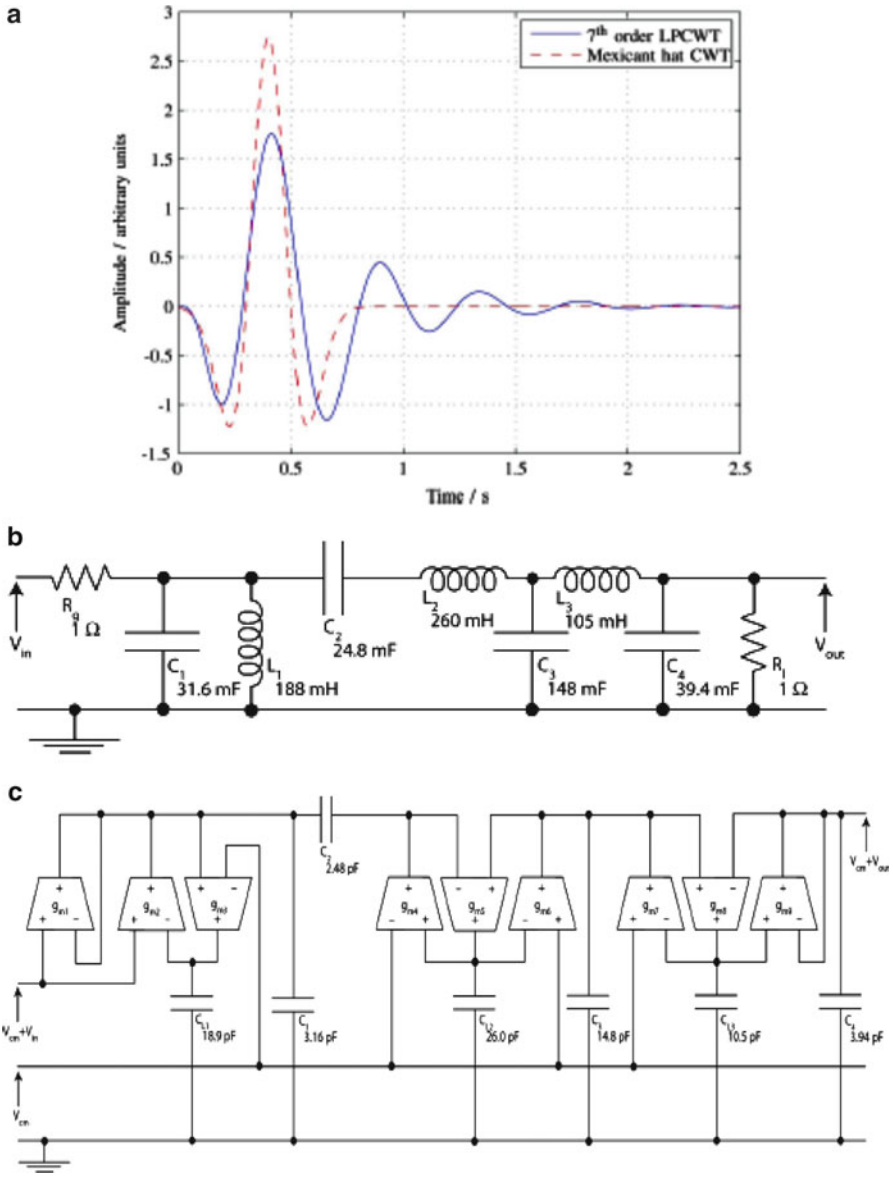


Fig. 5.37 (**a**) LPCWT (low power continuous wavelet transform) mother wavelet (a = 0.1 and T = 0.4 s) resembling Mexican hat (shown in *dotted lines*), (**b**) seventh-order LC ladder filter structure, (**c**) g_m-C implementation of (**b**), and (**d**) NMOS transconductor (Adapted from [5.36] ©IEEE 2011)

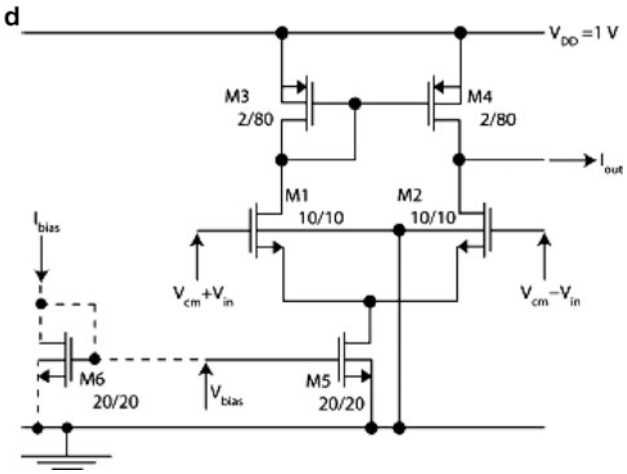


Fig. 5.37 (continued)

where τ is the allowable maximum difference between the ideal and actual nonlinear output current of the transconductor and $i_f = I_{DS}/I_S$. For deep weak inversion, $i_f \rightarrow 0$ and $V_{lin} = 10.9\,\text{mV}$ whereas for standard weak inversion, $i_f = 0.1$ and $V_{lin} = 11.4\,\text{mV}$. The authors have also pointed out that flicker noise corner frequency f is less than $\frac{KI_{DS}}{2qWL}$. Since I_{DS} is very low, thermal noise is predominant. Hence, NMOS transistors have been used. The lower V_T simplifies the operation using a 1 V power supply. The mismatch of transistors at the weak inversion region is about the same as that for deep weak inversion operation. The frequency response of the OTA is dominated by a zero. For the differential amplifier of Fig. 5.37d, the ω_o is 37 Hz. This introduces distortion in the frequency response that can be corrected by predistorting the value of capacitor C_2 (see Fig. 5.37a).

5.10 G_m-C Filters for HDD

Pandey et al. [5.37] have described a 140 mW fourth-order linear-phase low-pass filter for HDD read channel application. The architecture of the HDD front-end is shown in Fig. 5.38a. The real pole of the fifth-order filter is realized separately using R and C following the AGC block. The single-stage OTA employed in this design is based on complementary differential pairs as shown in Fig. 5.38b. The input signal is fed to both pairs thus increasing the effective transconductance. The power efficiency is increased since the biasing current sources can be shared by the two differential pairs. The CMFB loop is presented in Fig. 5.38c which minimizes the parasitic poles and thereby improves the stability. The simplified equivalent of the

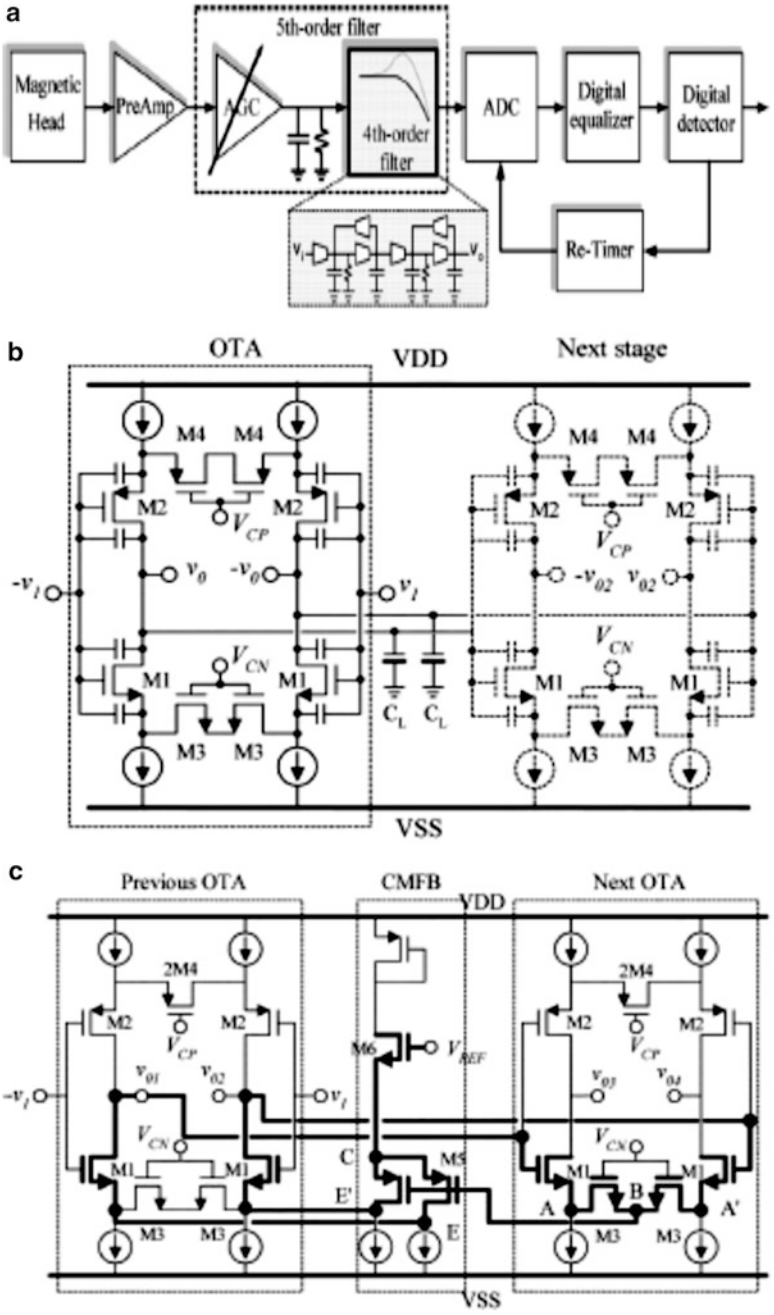


Fig. 5.38 (**a**) Schematic of HDD front-end, (**b**) single-stage OTA based on complementary differential pairs, (**c**) class AB CMFB system with enhanced loop stability, (**d**) simplified CMFB loop schematic, and (**e**) biquadratic section with CMFB (Adapted from [5.37] ©IEEE 2006)

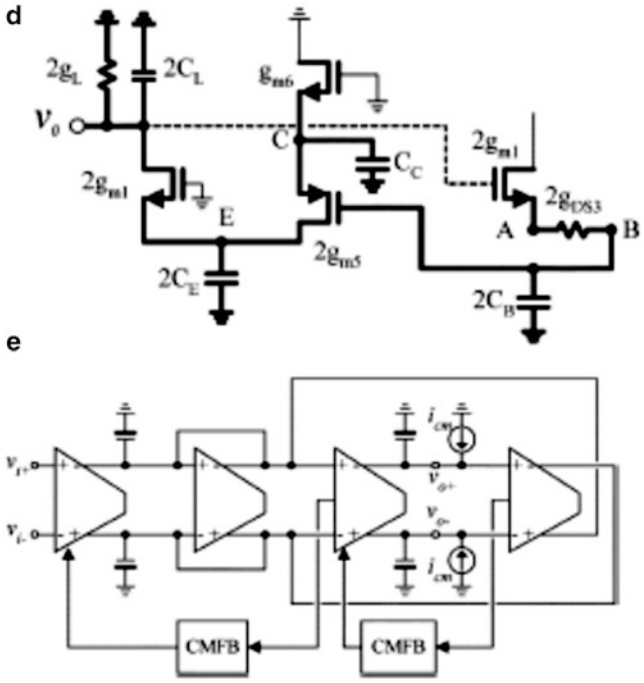


Fig. 5.38 (continued)

CMFB loop is shown in Fig. 5.38d. The fourth-order filter realized is presented in Fig. 5.38e wherein each stage has its own CMFB loop.

Read channel hard disk drives do not demand high linearity and high dynamic range (typically 40 dB for each parameter). However, very high speed is required and G_m-C filters are usually chosen since these use open loop structures. Bollati et al. [5.38] have described an eighth-order 0.05 dB equiripple linear phase filter using the G_m-C technique. This has a wide tuning range (30–120 MHz) and features a programmable boost. The eighth-order filter is realized as three biquads and two first-order cells. The highest pole-Q needed is 1.5. The equalization chosen is E^2PR4 realized through two opposite pairs of real axis zeroes. The numerator realized is $(1 - as)(1 + as) = 1 - a^2s^2$. The complete filter is presented in Fig. 5.39a which comprises a biquad and two third-order filters. The third-order filter is shown in Fig. 5.39b. Note that OTAs G_{m1} and G_{m5} realize a real zero as can be seen in the transfer function of the third-order filter:

$$\frac{V_o}{V_{in}} = \left(\frac{g_{m1} + sC_3}{1 + \frac{2sC_3}{g_{m5}}}\right)\left(\frac{1}{1 + \frac{sg_{m3}C_1}{g_{m2}g_{m4}} + \frac{s^2C_1C_2}{g_{m2}g_{m4}}}\right) \tag{5.26}$$

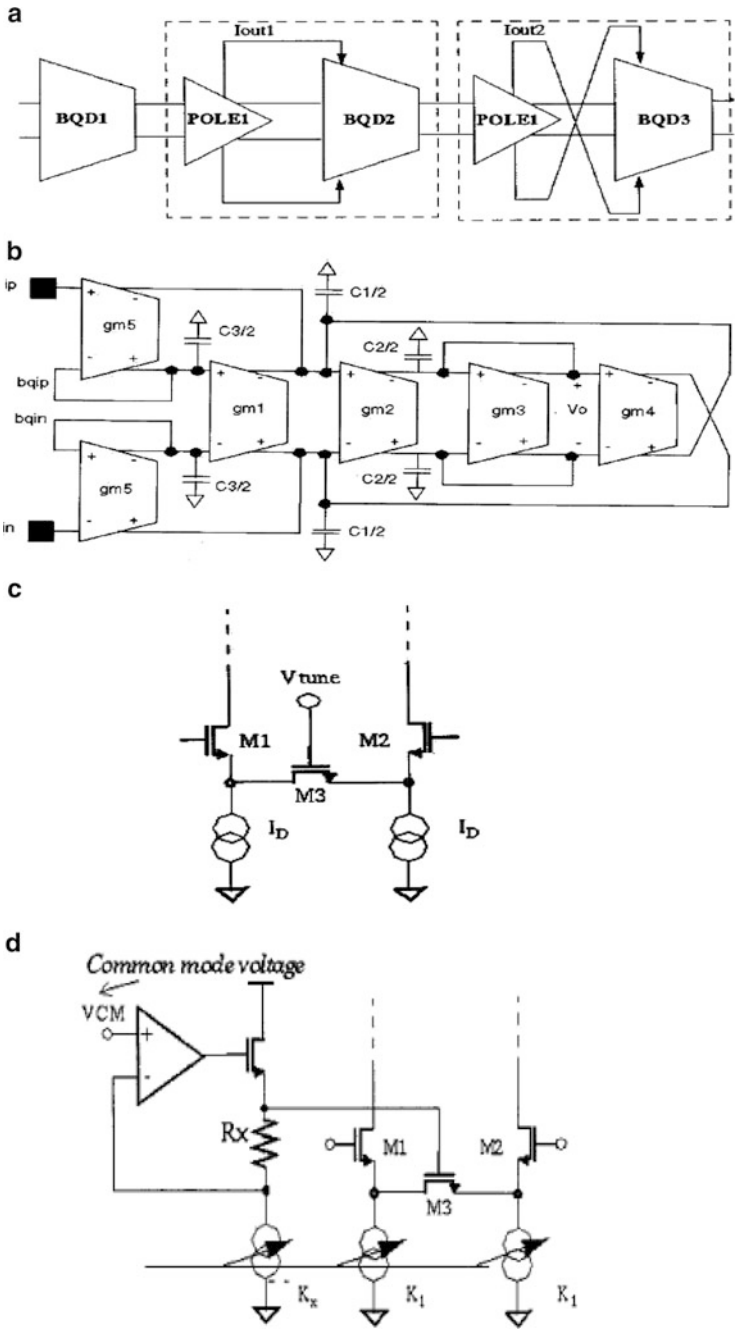


Fig. 5.39 (**a**) Block diagram of eighth-order LPF, (**b**) third-order filter block diagram, (**c**) degenerated differential pair used as a G_m, (**d**) V_{tune} control, and (**e**) complete G_m control scheme (Adapted from [5.38] ©IEEE 2001)

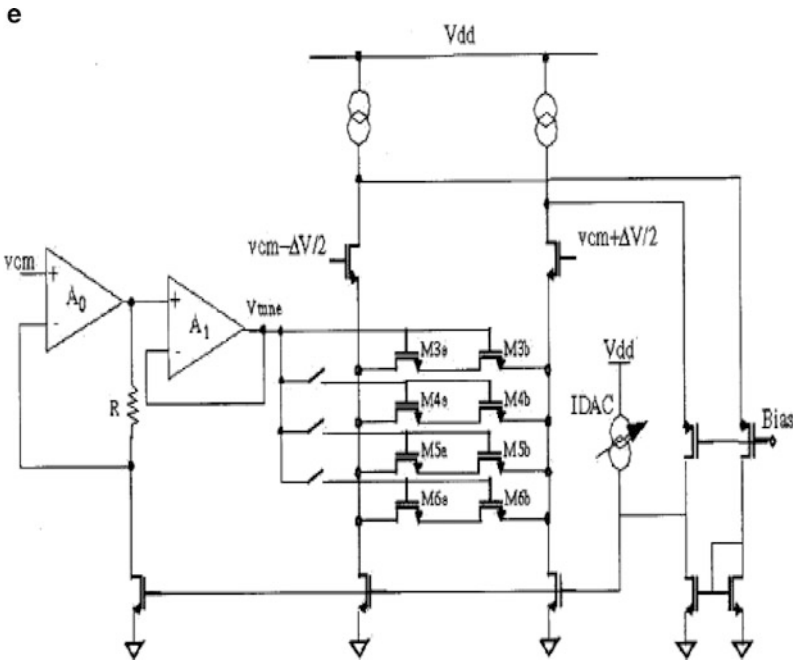


Fig. 5.39 (continued)

For the second biquad, the current outputs of the pole 1 stage are cross-connected as shown in the block diagram of Fig. 5.39b. The transconductor used is a degenerated differential pair using a MOS transistor as shown in Fig. 5.39c. The G_m is varied by two loops: (a) by varying the tail currents of the differential amplifier, and (b) by an auxiliary loop controlling the resistance $2R$ where $R = 1/2\ g_{ds3}$ through the voltage V_{tune} as shown in Fig. 5.39d. The MOS transistor is realized as several parallel resistors with each resistor comprising two MOS transistors (see Fig. 5.39e). The boost control needs a variable G_{m1} which is realized by connecting a programmable array of binary-sized transconductors. The complete G_m control scheme is presented in Fig. 5.39e. The G_m value is set using a servo loop so that G_m is inversely proportional to an external resistance R. The reference transconductor biases all the other transconductors. The reference transconductor is folded and its differential output is converted to single-ended output. The reference g_m is driven by a fixed voltage ΔV and its output current is forced to be equal to IDAC. Note that IDAC is derived from an external resistor on which ΔV is forced. The main loop adjusts the tail currents of the differential amplifier. The auxiliary loop controls the V_{tune}. This is realized using the opamp A_o, resistor R_x, and a current proportional to the tail current of the transconductor. Note that the auxiliary loop is faster than the main loop.

5.11 G_m-C Filters for Power Supply Applications

A very low offset rail-to-rail G_m-C filter has been described by Forghani-Zadeh and Rincon-Mora [5.39] for application in current sensing in switching power supply applications. The basic concept is illustrated in Fig. 5.40a, where the voltage across the inductor is measured using a G_m-C first-order filter. Since the equivalent series resistor of the inductor is very small (on the order of a few milliohms), low offset performance is required. The authors present an excellent review of offset cancellation techniques [5.40] using autozero (AZ) as well as chopper. The important features of both these are summarized in Table 5.5. The AZ technique extensively studied earlier in Chap. 4 measures offset and subtracts it in the processing phase. The chopper on the other hand changes the polarity of the offset every clock cycle and on average cancels the offset. A modulator and demodulator at the chopping frequency are placed before and after the filter. The signal is modulated to high frequencies but not the offset of the amplifier. Hence, the signal is demodulated back whereas the dc offset is modulated at high frequencies beyond the pass-band of the filter and can be removed by filtering. In power supply applications, autozeroing is preferred, since the inputs can extend up to a few MHz making the chopping frequency very large. Chopper schemes are continuous in time unlike in AZ, whereas in AZ schemes information is processed at discrete time instants.

Continuity can be achieved in an AZ scheme by using ping-pong or feedforward architectures. In ping-pong, while one amplifier is sensing and measuring the offset, another is processing the signal. There can be glitches during the transfer from one amplifier to another. In the feedforward technique, an error amplifier continuously cancels the offset thereby avoiding switching. The offset nulling amplifier is itself autozeroed and its output which tunes the main amplifier is sampled and held across a capacitor. The feedforward technique suffers from intermodulation effects between the AZ clock frequency and the input signal. Note that negative feedback is necessary to provide a sample of the offset across the input terminals without changing the connectivity. Table 5.6. summarizes the features of ping-pong and feedforward architectures.

The authors propose autozeroed ping-ponging dual-input summing transconductors, two offset programming capacitors for each OTA (C_{h1-}, C_{h1+}, C_{h2-}, C_{h2+}), a single bandwidth setting capacitor, and gain setting resistor R (see Fig. 5.40b). Note that an input differential pair is dedicated to the input signal and another to the offset. The advantage is that the offset holding capacitor is not in the signal path and hence not band-limiting the signal.

Note that in Phase1, the main input pair is short-circuited and the auxiliary pair is connected in the buffer configuration, thus charging the capacitor C_h with the overall offset of the opamp. In Phase2, this offset is subtracted from the input by breaking the unity gain feedback loop and connecting the stored offset across the auxiliary opamp. The input signal is simultaneously connected to the input pair. It can be shown that the offset is cancelled. Note, however, that the clock feedthrough and charge injection will cause a residual error to exist that is quite small. Note that

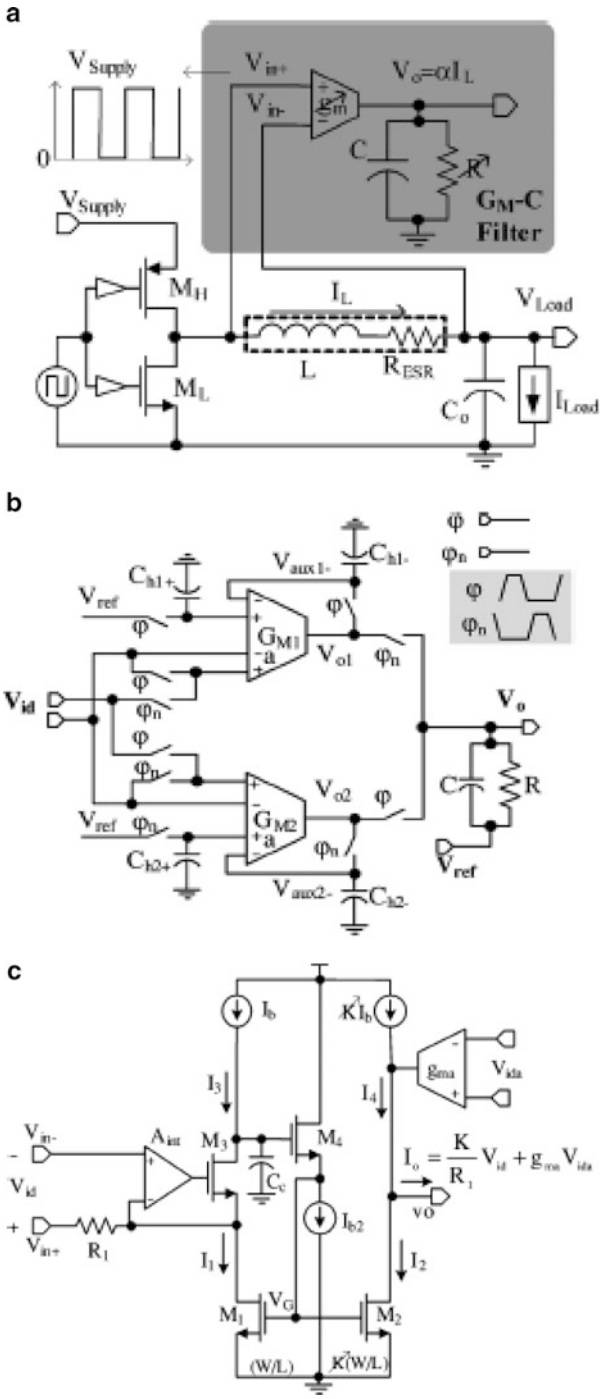


Fig. 5.40 (**a**) Programmable and continuous low offset G_m-C filter for current sensing in switching power supply applications, (**b**) ping-pong G_m-C filter with autozeroing summing transconductors, (**c**) linear dual-input rail-to-rail transconductance cell with tunable k, and (**d**) full schematic of the G_m cell (Adapted from [5.39] ©IEEE 2007)

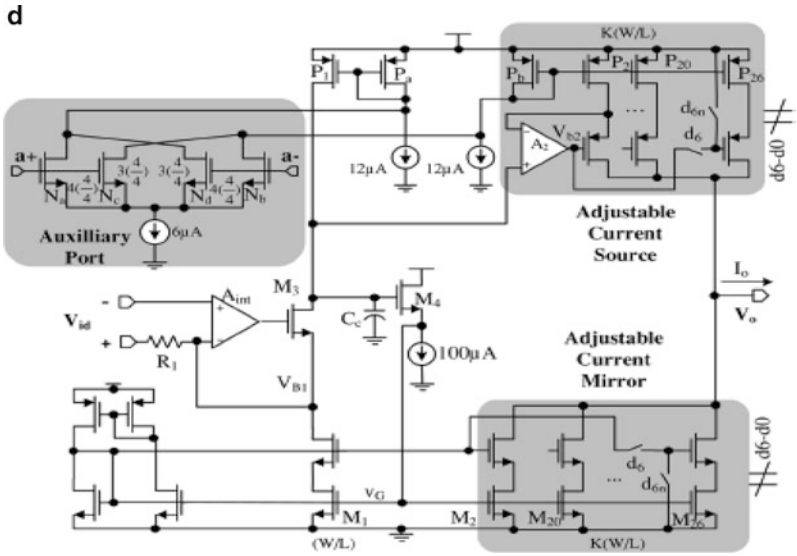


Fig. 5.40 (continued)

Table 5.5 Summary of dynamic offset cancellation technique (Adapted from [5.39]©IEEE2007)

Chopper	Auto zero
Modulates and filters Dc offset	Sample and subtract offset
Continuous	Discontinuous
Higher noise reduction	Lower noise reduction
Low bandwidth (BW<0.5f_{Chop})	High bandwidth

Table 5.6 Summary of continuous-time AZ techniques (Adapted from [5.39]©IEEE2007)

Ping pong	Feed forward
Higher glitch content	Lower glitch content
Used in open- and closed-loop amplifiers	Only used in closed-loop, negative feedback amplifiers
No intermodulation effect	Intermodulation effect

the bottom circuit performs a similar function in Phase φ_o. During transition from φ to φ_o, a few mV glitches will exist due to parasitic capacitances at the output of the transconductor.

The transconductance used is shown in Fig. 5.40c which is linear and provides rail-to-rail operation. Note that the G_m is a resistor-based current conveyor. The current I_{R1} is V_{id}/R_1 due to the opamp A_{int}. This current is mirrored to the output by current mirror M_1 and M_2 thereby defining the transconductance as k/R_1 where k is digitally programmable. The auxiliary transconductor G_{ma} is also shown in

Fig. 5.40d. Note that I_b and I_{b1} bias M_3 and M_4. The feedback loop forces the gate voltage of M_1 so as to sink I_b and I_{R1}. In other words, M_1, M_3, and M_4 form a current mirror. The full schematic of the G_m cell is shown in Fig. 5.40d. The bits d_6–d_0 control k using the cascode transistors M_{20}–M_{26}. The amplifier A_2 maintains the drain voltage of P_1 and P_2 equal to minimize channel length modulation errors and sets the bias voltages properly. The auxiliary pair consists of the current canceling differential pairs N_a–N_b and N_c–N_d realizing a low transconductance. The bandwidth of the filter is tuned using R realized as a programmable binary weighted polysilicon resistor. The offset achieved was < 210 μV.

5.12 G_m-C Filters for Other Applications

Mobarak et al. [5.41] have suggested a scheme for cancelling distortion due to OTA in OTA-C filters. Consider their scheme presented in Fig. 5.41a. In this, the auxiliary OTA generates a current $G_m V_{in}/2$ which is converted into voltage using the resistor $R = 1/G_m$ (and capacitor C_o representing the parasitic output capacitance and input capacitances of the OTAs). The difference between the input voltage and this voltage is converted into current by the OTA in the normal path. The current output of the OTAs can be expressed as the sum of linear and nonlinear components. The final output current is devoid of the nonlinear components as can be seen from the equations given in the inset of Fig. 5.41a. Note that the phase-shifter block is required to cancel the phase difference between the main and auxiliary paths. The G_ms need to be identical for good cancellation. A fully differential implementation follows the scheme of Fig. 5.41b. Note that the phase-shifter is a first-order filter with programmable resistance R_c. The reader is urged to verify the gain factors 2/3 and 1/3 needed to achieve perfect cancellation. Resistors R and R_c can be tuned with 6-bit resolution.

The G_m used in the realization is shown in Fig. 5.41c which uses a folded cascode configuration and is fully differential. The output common mode feedback loop also is shown in Fig. 5.41c. The input attenuation by k_1, $(1 - k_1)$ and k_2 is realized using capacitors by using floating-gate type input devices M_c. The schematic of the error amplifier is shown in Fig. 5.41d. Note that the series resistance R_z realizes transmission zero to ensure stability of the CMFB loop. The second-order low-pass filter based on the two-integrator loop realized by replacing each OTA with the circuit of Fig. 5.41b is presented in Fig. 5.41e. As is required in other G_m-C filters, a tuning loop is required. In this design, the authors use the distortion cancelling scheme as shown in Fig. 5.41f for realizing the tuning loop. It can be seen that the phase detectors $PD3$ and $PD4$ detect the phase difference between both inputs of both OTAs in the normal and auxiliary paths and derive a control signal for the resistors R_c. In a similar manner, the effective gain of the auxiliary path $k_2 G_m R$ is measured by comparing the phase difference between inputs and outputs using two phase detectors $PD1$ and $PD2$ and deriving a control voltage to vary R accordingly. Note the tuning is sequential and not adaptive, however.

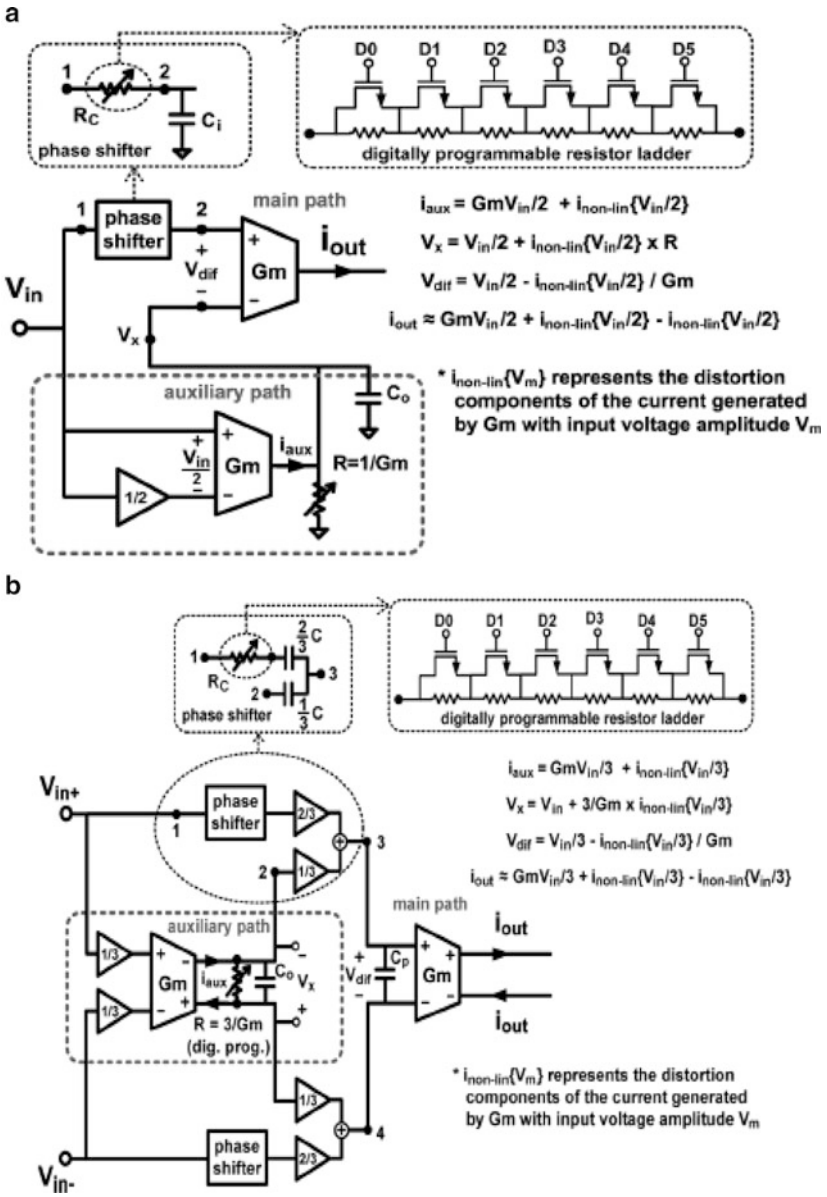
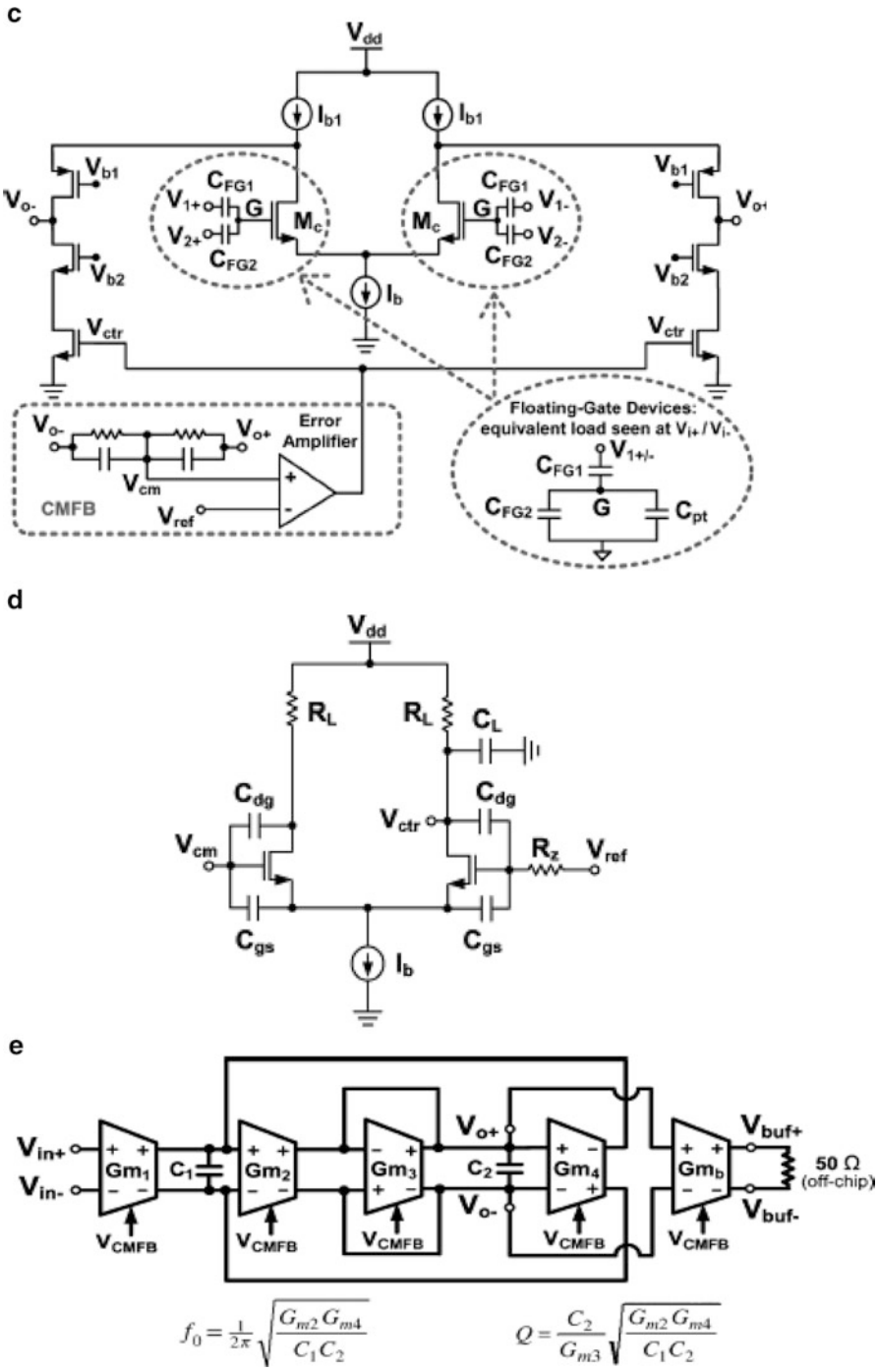


Fig. 5.41 (**a**) Attenuation predistortion linearization scheme, (**b**) application of (**a**) to a fully differential circuit, (**c**) folded cascode opamp, (**d**) error amplifier circuit in the CMFB loop, (**e**) fully differential second-order low-pass filter, and (**f**) automatc linearity tuning scheme (Adapted from [5.41] ©IEEE 2010)



$$f_0 = \frac{1}{2\pi}\sqrt{\frac{G_{m2}G_{m4}}{C_1C_2}} \qquad Q = \frac{C_2}{G_{m3}}\sqrt{\frac{G_{m2}G_{m4}}{C_1C_2}}$$

Fig. 5.41 (continued)

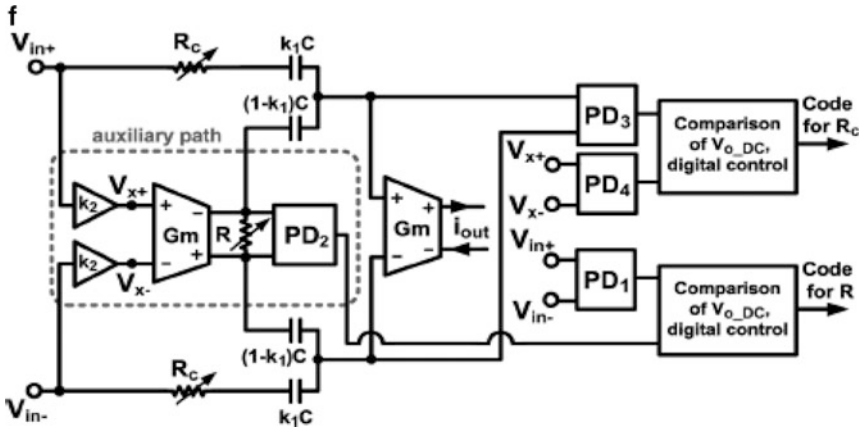


Fig. 5.41 (continued)

An IM3 improvement on the order of 22 dB has been found compared to realizations not using distortion compensation.

Acosta et al. [5.42] have unified the transconductor structures and derived a new architecture for realizing transconductors with large linearity. They observe that the linearity for transconductors should be based on the linearity of resistors. They suggest that CCII-based implementations have such a feature. Consider the CCII-based transconductor shown in Fig. 5.42a where in the input differential voltage is buffered by the unity gain amplifiers between the y and x terminals of both the CCIIs and is converted into current using two resistors R. This current is delivered at the z terminals of the current conveyors to flow into the output terminals. This configuration has very high input resistance. However, the input range is not rail to rail since the buffers need to track the input voltage. The voltages at the x terminals are complementary and the junction of resistors will be at signal ground for differential inputs equal to the common mode voltage. Hence a resistive divider can be used for output common mode voltage detection. An alternative architecture separates the signal ground as shown in Fig. 5.42b. Note that matching of resistors R will be required. This is a pseudo differential topology. The input common mode voltage needs to be sensed and applied via a buffer stage to signal ground. The third topology uses resistors in series with x inputs to convert the input voltage to current at the z terminals. The y terminals of both the CCs are connected to common voltage V_{cm}. This configuration is also sensitive to mismatch of resistors R. The input range can be rail to rail. However, the input resistance R is loading the previous circuit. The alternative circuit of Fig. 5.42d uses two transconductors of Fig. 5.42a and cross-couples them. The transconductance obtained is $1/R_1–1/R_2$. Thus, very small transconductances can be obtained.

Several alternative structures are possible for the voltage buffers. Some of these are presented in Fig. 5.43a–e. It is required that these buffers have provision to provide a copy of the output current at a separate terminal. In all the cases except Fig. 5.43c, the V–I converter serves as a resistor to sense the current. A source follower is presented

in Fig. 5.43a which is less linear, is simplest, and fast due to the absence of feedback. The current can be conveniently sensed at the drain of the transistor M_1. The output resistance can be increased by using a cascode connection but the power supply voltage needs to be larger. To increase linearity, the G_m needs to be increased needing a larger bias current and width of transistor M_1. The circuit of Fig. 5.43b needs a compensated opamp thus reducing the bandwidth and increasing the power consumption. However, the unity gain requirement is more easily satisfied than in the case of Fig. 5.43a due to the feedback reducing the dependence on V_{GS}. Another voltage follower is shown in Fig. 5.43c in which a folded cascade-type amplifier can be used yielding the circuit of Fig. 5.43d. The circuit of Fig. 5.43d leads to a higher power consumption and needs frequency compensation. The simplest implementation of an opamp in the circuit of Fig. 5.43c can be based on a single transistor as shown in Fig. 5.43e. It is faster and needs less power than the circuit of Fig. 5.43d. It provides the needed gain and linearity. The output current cannot be directly taken from the terminals shown in Fig. 5.43a–e but it is required to have a current mirror with high output impedance. Three current follower circuits are presented in Fig. 5.44. The circuit of Fig. 5.44a is based on a current mirror. Note that in the circuits of Fig. 5.43c–e, the current source in the source leg of the transistor can be the driver transistor of the current mirror thus simplifying the circuit. The circuit of Fig. 5.44b is a folding stage whereas the circuit of Fig. 5.44c is the well-known regulated cascode. The latter circuit has very low input resistance. Both the circuits of Fig. 5.44b and c are mismatch insensitive. But, the swing of Fig. 5.44c is lower due to the stacked transistors.

The tuning of the transconductors to an extent of 50% can be achieved in several ways as shown in Fig. 5.45. In Fig. 5.45a, the resistors R can be tuned using MOS transistors in place of resistors. However, this degrades the linearity of the transconductor. In the circuit of Fig. 5.45b, the current mirrors are tuned. This does not degrade the linearity of the core transconductor. Current scaling can be accomplished using transconductance multipliers [5.43]. In the arrangement of Fig. 5.45c, resistor dividers R_1 and R_2 realize attenuation without affecting the core. Furthermore, the accuracy depends on resistor ratios and not on absolute values of resistors as in Fig. 5.45a. The tuning resistors can be small so that voltage swings are less thus avoiding distortion. In the circuit of Fig. 5.45c, $\alpha = 1 + R_2/R_1$. Note also that complementary voltages are created at nodes A and B. As such, a signal ground is created at the junction of A and B equaling a voltage V_{BIAS}. In the alternative tuning scheme of Fig. 5.45d, resistive current splitting takes place leading to a dual-output transconductor. The price paid is the extra additive current followers and sensitivity to mismatch.

Acosta et al. [5.42] proposed a highly linear tunable transconductor based on the various buffer amplifiers, current mirrors, and tuning arrangements discussed above. They employ the modified tuning scheme of Fig. 5.45c, the voltage follower of Fig. 5.43c, the current follower of Fig. 5.44b, and the transconductor of Fig. 5.42a. The complete OTA schematic is presented in Fig. 5.46a. The buffers are realized by the pairs of transistors M_1 and M_2. The resistors R convert the voltage into current. The current is sensed at the sources of the buffer amplifiers and delivered to

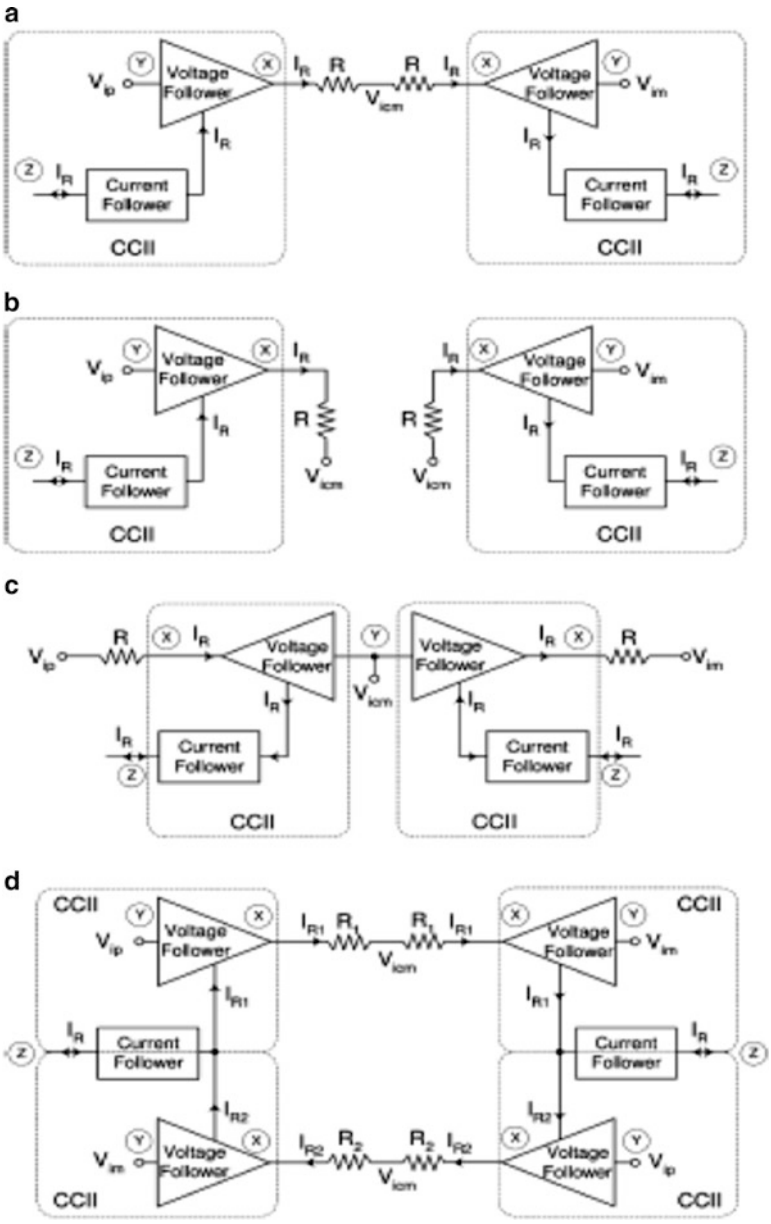


Fig. 5.42 CCII-based transconductor topologies: (**a**) with high input resistance, (**b**) alternative of (**a**), (**c**) with high input range, and (**d**) modification of (**a**) using two cross-coupled transconductors (Adapted from [5.42] ©IEEE 2009)

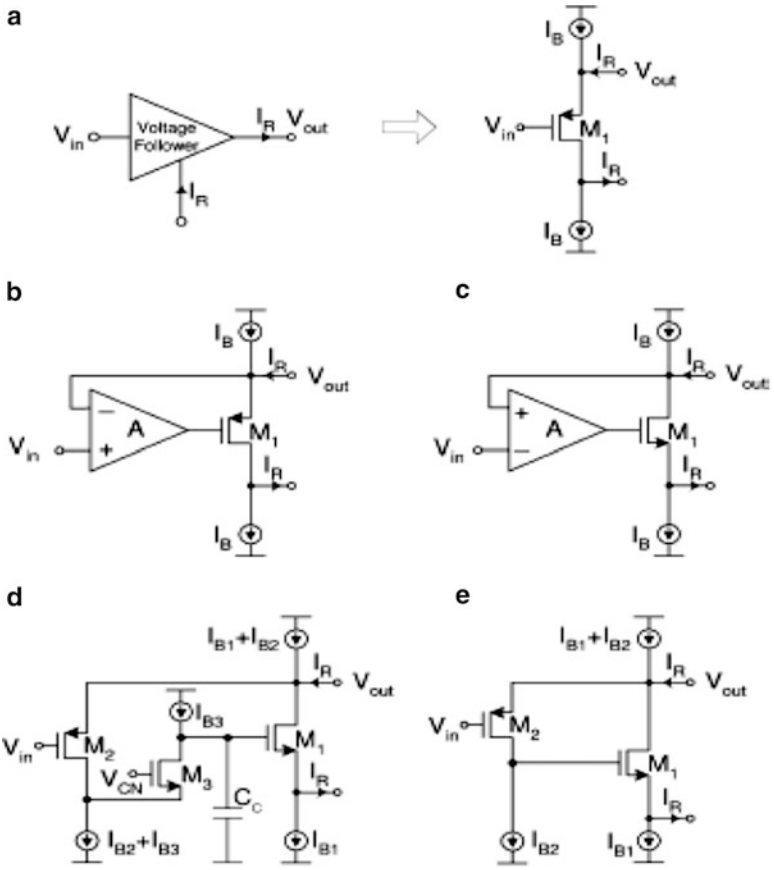


Fig. 5.43 Voltage follower implementations: (**a**) simple source follower, (**b**) super-G_m stage, (**c**) alternative servo loop, (**d**) implementation of (**c**) using folded cascode amplifier, and (**e**) implementation of (**c**) using common-source amplifier (Adapted from [5.42] ©IEEE 2009)

the output through the transistors M_{CN}. The resistor network provides tuning. Acosta et al. [5.42] suggest simplification as shown in Fig. 5.46b by noting that αI_R can be tapped at the source of transistor M_{CN} thus not necessitating the use of resistors R_2 in Fig. 5.46a. This will help to reduce the swing at nodes A and B. The detailed implementation of Fig. 5.46b is presented in Fig. 5.46c including the biasing current sources. A third-order G_m-C low-pass filter for VDSL applications has been realized. The low-pass filter schematic is presented in Fig. 5.47. The resistor $2R_N$ has been implemented using a MOS transistor M_{P1} controlled by the programming voltage V_{PROG}.

Le-Thai et al. [5.44] have proposed a bandpass filter based on coupled resonators and a G_m-C technique using a low distortion transconductor. They have reviewed the various linearization techniques of transconductors presented in Fig. 5.48. The G_m of the transconductor of Fig. 5.48a use resistive degeneration at the expense

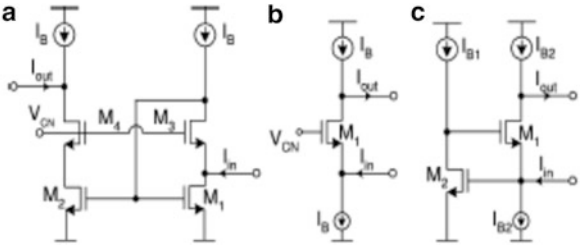


Fig. 5.44 Current followers (**a**) using current mirrors, (**b**) folding stage and (**c**) regulated cascode stage (Adapted from [5.42] ©IEEE 2009)

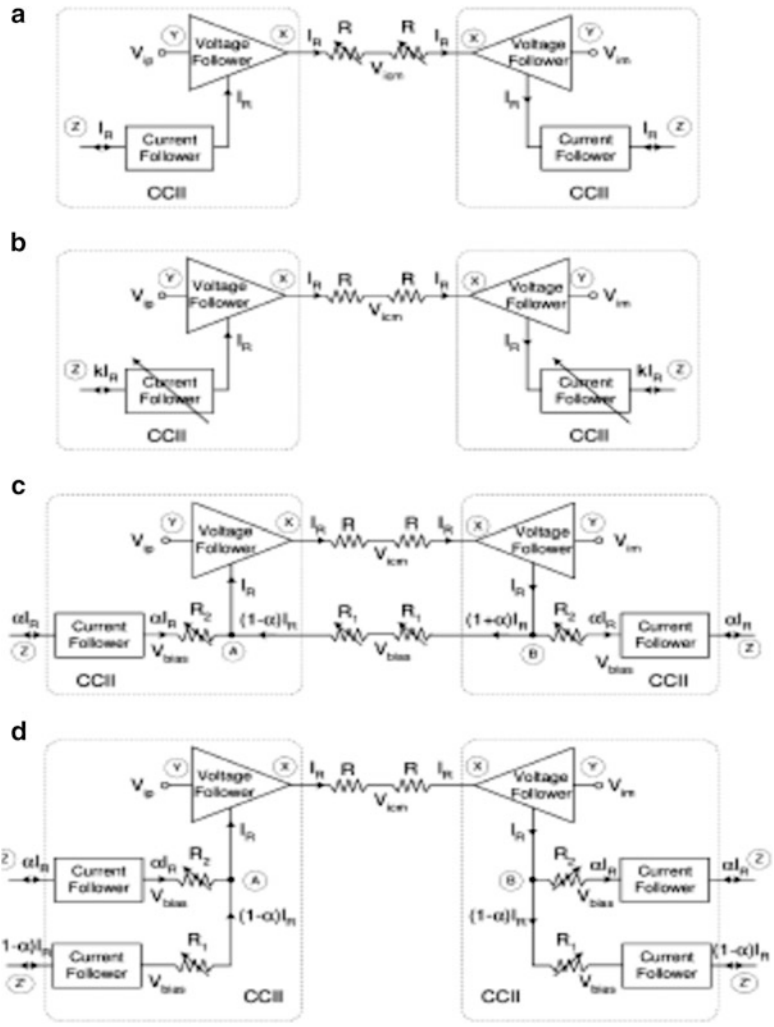


Fig. 5.45 Transconductor tuning techniques: (**a**) using resistors used for V–I conversion, (**b**) scaling the output current, (**c**) using resistor current division, and (**d**) using resistive current splitting (Adapted from [5.42] ©IEEE 2009)

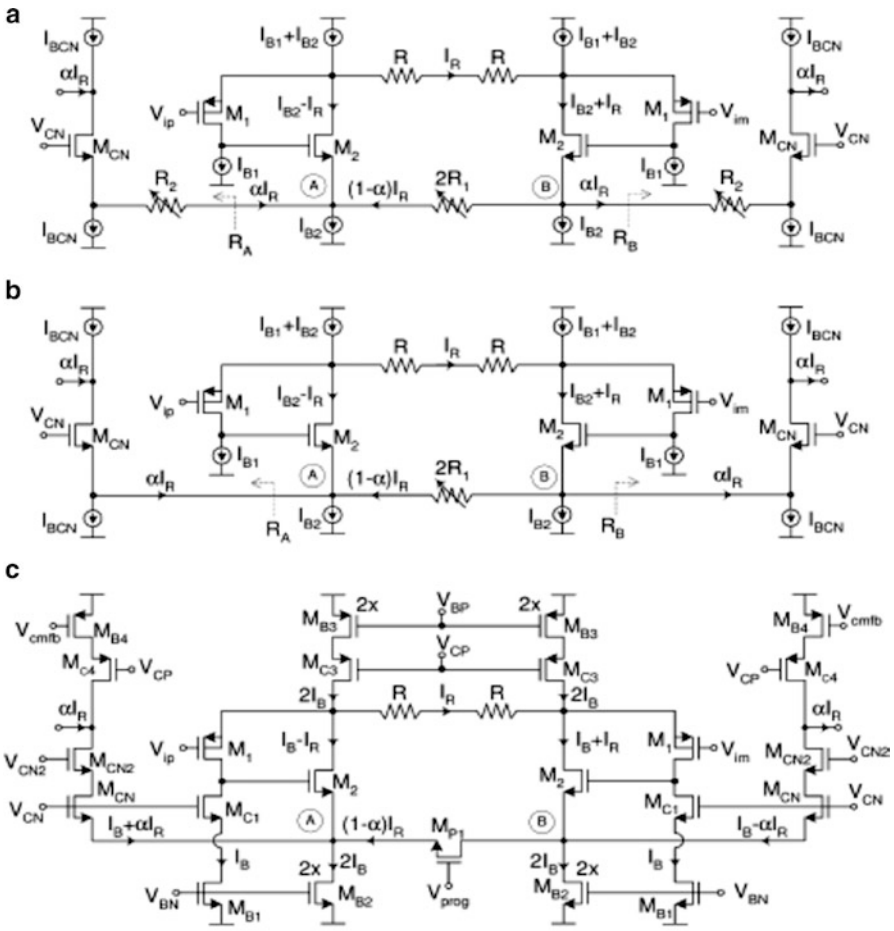


Fig. 5.46 Evolution of transconductor (**a**) starting topology using the tuning technique of Fig. 5.45(c), (**b**) modified tuning strategy, and (**c**) detailed circuit (Adapted from [5.42] ©IEEE 2009)

of more power consumption and are very linear. An improved version of Fig. 5.48a is shown in Fig. 5.48b which uses dynamic source degeneration wherein the resistance is adapted based on the amplitude of the input signal. The range of input voltages over which the G_m is linear is broadened but the variation of G_m in this range is still high. Another technique shown in Fig. 5.48c uses tunable feedback. The alternative technique of Fig. 5.48d uses both dynamic source degeneration and tunable feedback. This needs higher power while achieving good linearity. The transconductor of Fig. 5.48e uses bias feedback using four additional transistors M_3–M_6. These keep the total current flowing through the transistors M_1 and M_2 balanced.

Furthermore, the mismatch of the main differential amplifier and the adaptive biasing block affects the performance. However, all the techniques of Fig. 5.48 are not attractive for low power supply voltages.

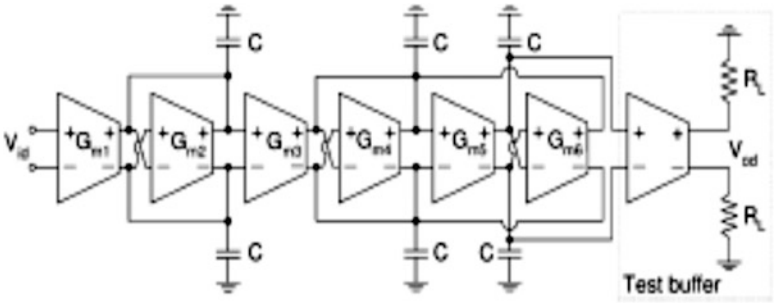


Fig. 5.47 Schematic of third-order low-pass filter (Adapted from [5.42] ©IEEE 2009)

The linearization technique presented by Le-Thai et al. [5.44] realizes a superposition method to reduce the nonlinear components. The basic principle is presented in Fig. 5.49a which uses superposition of two types of structures with opposite nonlinearity behavior. The three transistor pseudo differential arrangements M_1–M_3 and M_7–M_9 are different. These use, however, the same self-cascode structure using transistors M_1, M_2, and M_7, M_8, respectively. It can be shown that the G_m is flat and the first derivative of G_m is kept nearly zero over a large range of input signals. The THD is found to be better than all other structures: conventional differential pair (CDP), dynamic source degeneration (DSD) of Fig. 5.48b, or bias feedback pair (BFP) of Fig. 5.48e. The complete transconductor circuit is presented in Fig. 5.49b where the devices M_5–M_6 form the active current sources. The CMFB loop is presented in Fig. 5.49c using a resistive common mode detector for achieving good linearity. The capacitors C_o prevent the phase margin degradation of the CMFB due to distributed capacitance of 100 K ohm resistances R_o. The design also features a CMFF loop since the circuit is pseudo differential. The CMFF loop is formed by transistors M_{11}–M_{13}. The output impedance of the transconductors can be increased by using negative resistance shown in Fig. 5.49d.

The authors have described a 80 MHz IF bandpass filter using the coupled resonator-type structures. These are presented in Fig. 5.50a, b. Denoting $\omega_1{}^2 = \frac{1}{L_1C_1}$ and $\omega_2{}^2 = \frac{1}{L_2C_2}$ the transfer function of the structure of Fig. 5.50a can be written as

$$\frac{V_o}{V_{in}} = \frac{\left(\frac{g_{m1}g_{m2}}{C_1C_2}\right)s^2}{\left(s^2+\omega_1^2\right)\left(s^2+\omega_2^2\right)} \tag{5.27}$$

The bandwidth and the pass-band flatness are sensitive to process and temperature variations in this configuration. In the structure of Fig. 5.50b, the transconductor $-G_{m3}$ introduces negative feedback and the resulting transfer function can be derived as

$$\frac{V_o}{V_{in}} = \frac{\left(\frac{g_{m1}g_{m2}}{C^2}\right)s^2}{s^4+2\,s^2\left(\frac{1}{LC}+\frac{g_{m2}g_{m3}}{2C^2}\right)+\left(\frac{1}{LC}\right)^2} \tag{5.28}$$

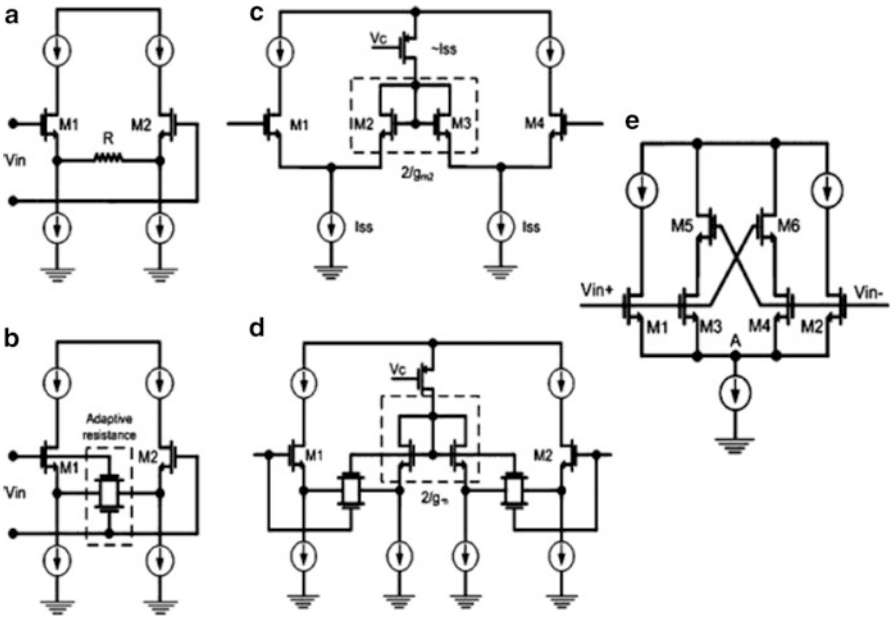


Fig. 5.48 Various linearization techniques for G_m cells: (**a**) resistive source degeneration technique, (**b**) dynamic source degeneration technique, (**c**) tunable feedback technique, (**d**) source degeneration tunable feedback combined technique, and (**e**) bias feedback technique (Adapted from [5.44] ©IEEE 2010)

Comparing the denominators of both (5.27) and (5.28), we can see that $\omega_1{}^2\ \omega_2{}^2 = \left(\frac{1}{LC}\right)^2 = \omega_o^4$ and $\omega_1{}^2 + \omega_2{}^2 = 2(\omega_o{}^2 + \omega_\Delta{}^2)$ where $\omega_\Delta{}^2 = \frac{g_{m2}\ g_{m3}}{2C^2}$. The bandwidth of the filter can be seen to be

$$BW = \omega_2 - \omega_1 = \sqrt{2}\,\omega_\Delta = \sqrt{\frac{g_{m2}\ g_{m3}}{C^2}} \tag{5.29}$$

showing that the bandwidth is dependent on G_{m3}. Since $\frac{BW}{\omega_o} = \sqrt{\frac{g_{m2}\ g_{m3}}{g_m^2}}$, it is independent of process and temperature variations. Note that $\omega_o = \frac{g_m}{C}$. The complete filter structure is presented in Fig. 5.50c. The LC resonators are designed using G_m-C integrators. The ratio G_m/C determines the center frequency of the filter.

A widely tunable cutoff frequency G_m-C filter with scalable power dissipation due to Tajjali and Leblebici [5.45] is considered next. The authors propose a new approach for improving the linearity of biquadratic G_m-C filters based on a two-integrator loop. The conventional fully differential biquad topology is shown in Fig. 5.51a. The currents flowing through the capacitors C_m and C_o can be written as

$$I_M = g_{m1}\left[(V_{IP} - V_{IN}) - (V_{OP} - V_{ON})\right] \tag{5.30a}$$

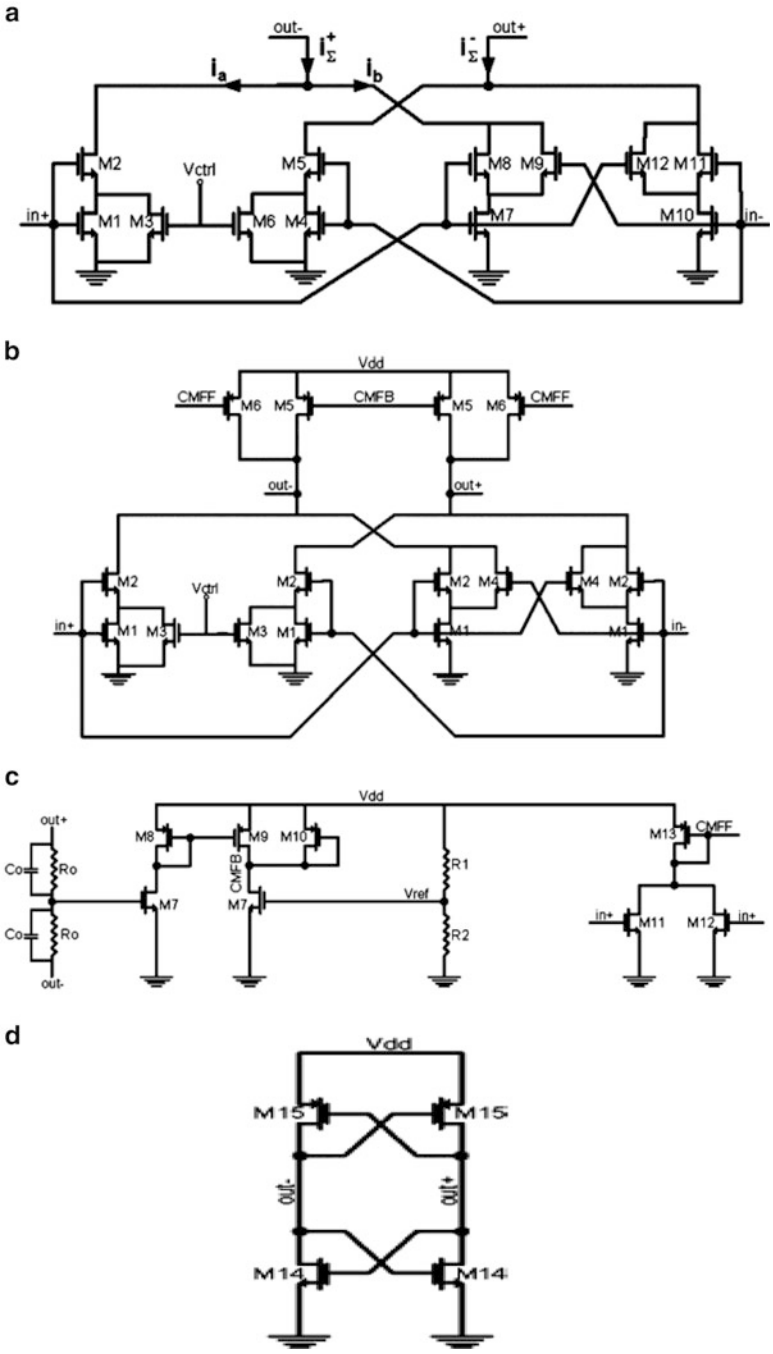


Fig. 5.49 (**a**) Core structure of the CMOS transconductor, (**b**) overall design of the transconductor, (**c**) CMFB and CMFF technique, and (**d**) negative resistance circuit (Adapted from [5.44] ©IEEE 2010)

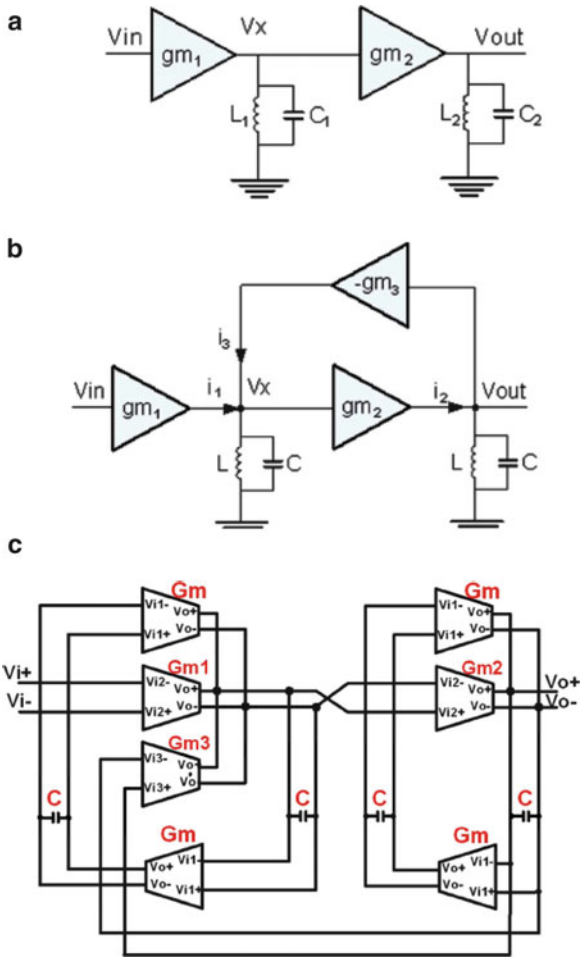


Fig. 5.50 Two filter structures using: (**a**) cascaded resonators, (**b**) resonant coupling, and (**c**) complete filter circuit (Adapted from [5.44] ©IEEE 2010)

$$I_o = g_{m2}\left[(V_{MP} - V_{MN}) - (V_{OP} - V_{ON})\right] \tag{5.30b}$$

Each OTA converts a differential voltage into current and then sums these currents, for realizing each equation. When the input signal is large, the linearity problem arises since the OTA needs to convert these large swing signal voltages into currents. However, Tajalli and Leblebici [5.45] suggest rewriting Equations (5.30) as

$$I_M = g_{m1}\left[(V_{IP} - V_{OP}) + (V_{ON} - V_{IN})\right] \tag{5.31a}$$

$$I_M = g_{m2}\left[(V_{MP} - V_{OP}) + (V_{ON} - V_{MN})\right] \tag{5.31b}$$

Thus, although the transfer functions do not change, each OTA needs to convert the difference of two signals that are in phase resulting in a much smaller input voltage swing. The implementation of this idea is as shown in Fig. 5.51b. Note, however, as the frequency increases, due to the increasing phase difference between V_i and V_o and V_M and V_o, degradation of linearity enhancement takes place. However, the performance is still better than that of Fig. 5.51a. The linearity performance is better when the devices are biased in weak, moderate, or strong inversion as well. The schematic of the folded-cascode OTA used in this design is presented in Fig. 5.51c. This consumes more power than conventional differential amplifiers. However, it can provide a wider input common mode range. The tuning range achieved was 50 Hz to 2 MHz for bias currents of 10 pA to 10 μA. Note that this technique is applicable when V_i and V_o do not differ much. The authors have realized sixth-order Butterworth filters in 0.18 μ CMOS technology with constant linearity over the entire tuning range.

A fully integrated 1.5–15 Hz low-pass filter with a linear tuning law has been described by Bruschi et al. [5.46]. This uses triode-based transconductors. A second-order low-pass filter shown in Fig. 5.52a has been realized using $C_{F1} = 70$ pf and $C_{F2} = 35$ pF. The important feature of the circuit is that although low G_m is realized, the input common mode range is comparable to a conventional differential pair in the saturation region. The transconductor used by the authors is shown in Fig. 5.52b which uses a triple input amplifier (TIA) to keep V_{DS} of the transistors M_1 and M_2 at a fixed value that keeps them in the triode region. The TIA is presented in Fig. 5.52c which has three inputs: inputs V_A and V_B and a terminal V_S which is a reference for input common mode voltage. The differential output stage is formed by M_{2A}, M_{3A}, M_{2B}, and M_{3B}. Note that $V_A - V_S = V_B - V_S = RI_B$ where R is a fixed resistance of value 50 K ohms. The TIA is cascaded to a fully differential common source stage formed by M_3 and M_4 whose loads are the transistors M_1 and M_2. Thus, a two-stage differential amplifier is formed with its inputs connected to the outputs in a negative feedback loop. The reader is referred to [5.46] for exhaustive design information. The G_m realized can be shown to be $G_m = k_2\, k_3\, \beta R\, I_{tune}$ where $k_3 = \frac{\beta_5}{\beta_3} = \frac{\beta_6}{\beta_4}$, $k_2 = \frac{\beta_{12}}{\beta_{11}}\, k_1 = \frac{\beta_0}{\beta_{11}}$, $\beta = \mu_n\, C_{ox}\, \frac{W_1}{L_1}$ and $\beta_{\beta i} = \mu_n\, C_{ox}\, \frac{W_i}{L_i}$. Note that all the bias currents are obtained from I_{tune}.

It is possible to realize programmable G_m-C filters [5.47] by using fixed G_m and programmable capacitors or having fixed capacitors and programmable G_m as shown in Fig. 5.53. The circuit of Fig. 5.53a is used as reference for evaluating these two options shown in Fig. 5.53b, c. The power dissipation is proportional to G_m and noise current spectral density due to OTA can be written as $4kT\gamma G_m$. Thus, the noise of the circuit of Fig. 5.53a is $\eta kT/C$. The "constant-C" design of Fig. 5.53c retains the same noise whereas the power dissipation is decreased for realizing $f_c = f_{\text{cmax}}/n$. On the other hand, for the " constant-G_m" design of Fig. 5.53b, the noise is decreased whereas the power dissipation is same. Figure 5.53 summarizes these results. The constant-C approach is preferable since lower power dissipation can be obtained for lower frequencies.

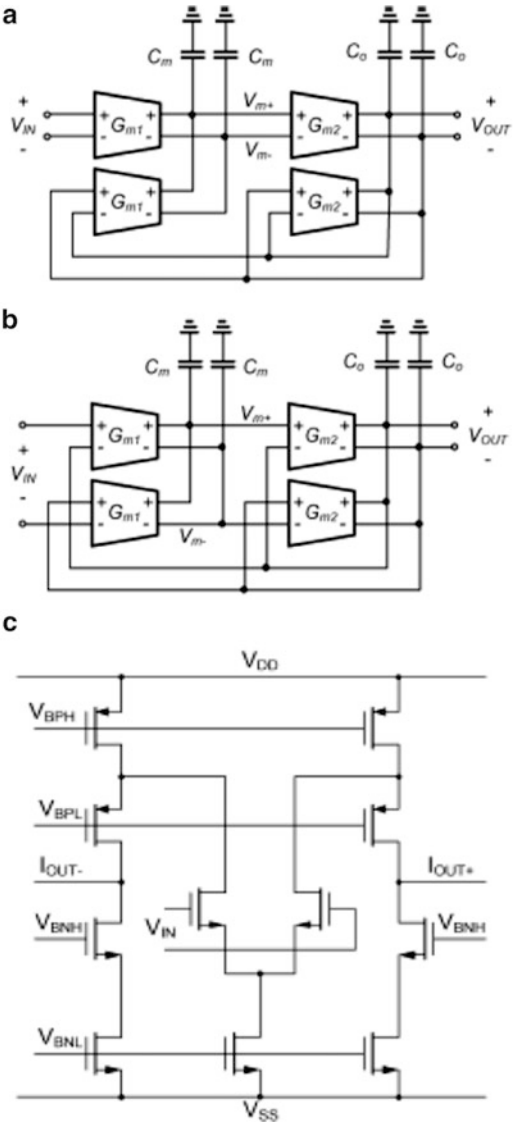


Fig. 5.51 Biquadratic G_m-C filters: (**a**) conventional implementation, (**b**) topology with improved linearity performance, and (**c**) folded cascode transconductor used to implement (**b**) (Adapted from [5.45] ©IEEE 2011)

The desired g_m can be composed using several unit G_ms in parallel. In such an arrangement, it is relevant to consider the effect of parasitic capacitances. As an illustration, in the G_m-C second-order filter of Fig. 5.54a, if transconductances are switched, several parasitics vary thus changing the pole-frequency and pole-Q (see Fig. 5.54b). On the other hand, if the parasitics are fixed, although the G_ms vary, the pole-frequency change will be proportional to the G_m change and Q will be fixed (see Fig. 5.54c).

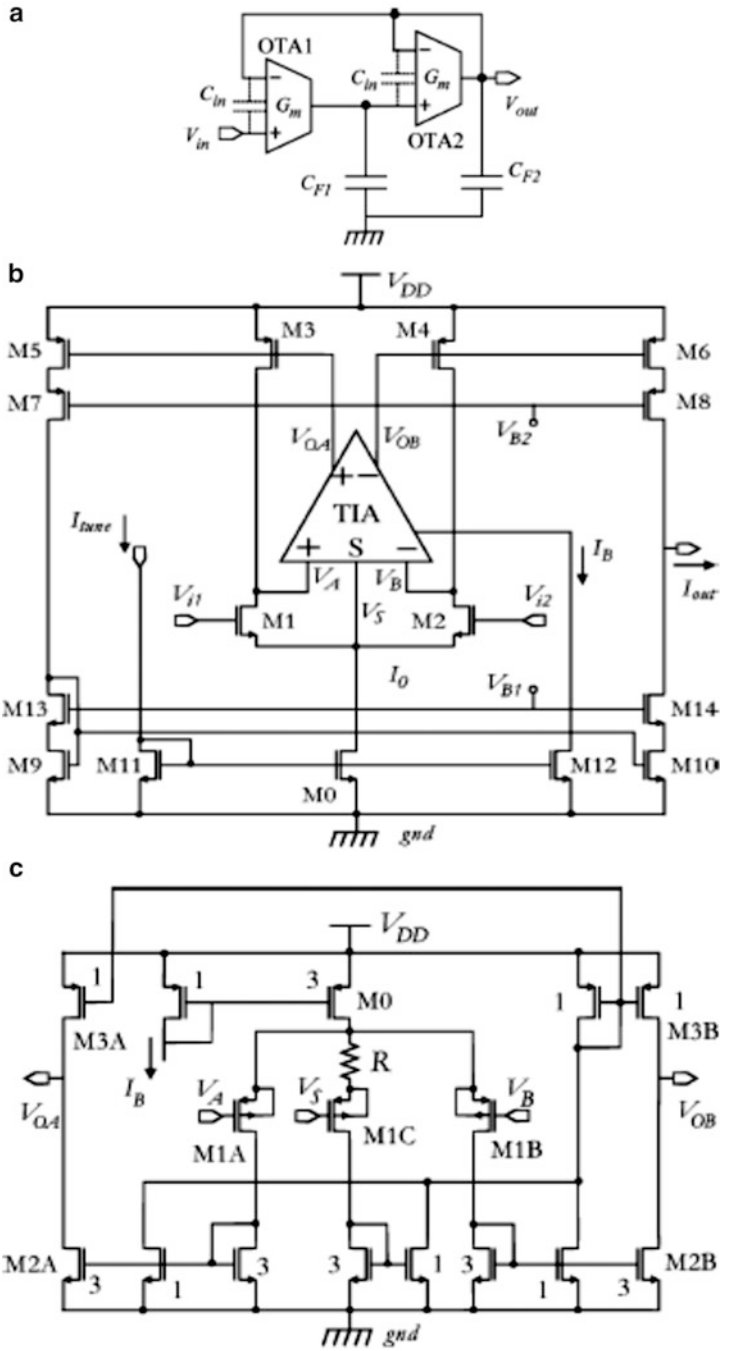


Fig. 5.52 (**a**) Second-order G_m-C low-pass filter, (**b**) topology of transconductors used in (**a**), and (**c**) three-input amplifier (TIA) simplified schematic (Adapted from [5.46] ©IEEE 2007)

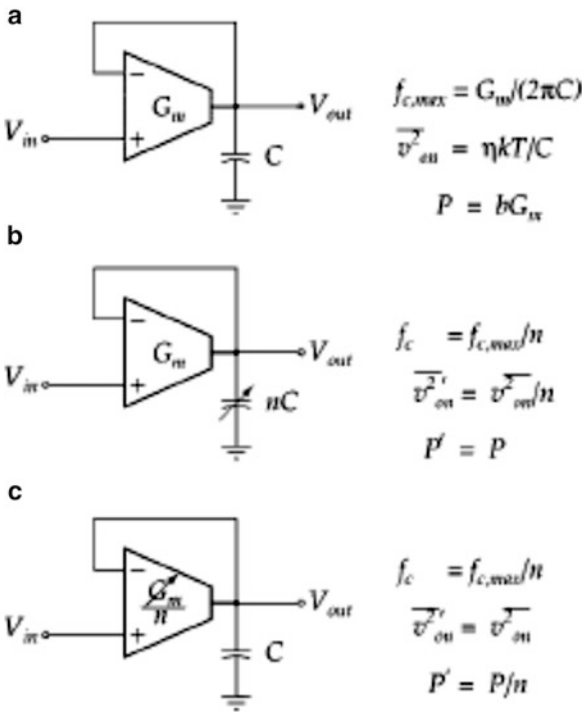


Fig. 5.53 (**a**) First-order G_m-C filter and lowering the cut off frequency using (**b**) variable capacitor and fixed G_m, (**c**) fixed capacitor and variable G_m (Adapted from [5.47] ©IEEE 2000)

The constant capacitance scaling can be shown not to increase the harmonic distortion. The unit transconductance element is shown in Fig. 5.55a. M_1 and M_2 form the differential amplifier whereas M_3 and M_4 form a dummy differential pair. M_5, M_6, M_7, and M_8 form the current sources for these two differential pairs. When M_7 and M_8 are supposed to act as current sources (i.e., $b = 1$), their gates are connected to V_{tune}. Otherwise, the gates are shorted to ground through a pass transistor and gates of M_5 and M_6 are connected to V_{tune} so that one of the differential amplifiers is always connected to the input. Thus, the input capacitance is independent of "b". M_{11} and M_{14} operate in the triode region and are used to switch off the load current sources. M_9–M_{12} are cascode devices that enhance the output impedance of the PMOS current sources. Note that the total power dissipation is constant and independent of "b". Several G_ms can be connected in parallel to realize a programmable G_m with constant input capacitance as shown in Fig. 5.55c for a 4-bit programmable element,. The various properties of the two transconductor parallel connection (see Fig. 5.55b) are as shown. The 4-bit programmable transconductor shown in Fig. 5.55c realizes a maximum G_m of $19G_{mu}$. A fourth-order Butterworth filter realized using a cascade of two biquads is shown in Fig. 5.55d which has pole-frequency programmable from 60 to 350 MHz.

The CM feedback circuit is shown in Fig. 5.55e. M_{c1} and M_{c2} form the common mode detector. M_{C5} is a PMOS source follower stage. M_{c3}, M_{c4}, M_{c11}, and M_{c12} form a servo amplifier. M_{c10} is a source follower. The device M_{c9} operates in the triode region and this transistor together with capacitor C_B forms a crossover network. M_{cs1} and M_{cs2} are similar to M_{11}, M_{14} in the transconductor (see Fig. 5.55a).

The tail currents of all the OTAs are varied by using the bias circuit of Fig. 5.55f which generates a current. Note that M_{b3}, M_{b4} form a current mirror and M_{b1}, M_{b2} together with R realize the condition

$$\frac{2I}{V_{GSb1} - V_T} = \frac{1}{R} = G_{m,Mb1} \tag{5.32}$$

Thus, the G_m of the transistor M_{b1} is $1/R$. The transistors M_{b5}–M_{b11} ensure that M_1 and M_2 and M_{b1} operate in exactly the same manner. The common mode voltage reference is fed to the M_{b6} gate. The reader may verify that the voltage at Y is the same as that at X. Since the G_m of M_{b1} is maintained at $1/R$ so is the transconductance of M_1–M_2.

Lo and Hung [5.48] have described a wide tuning range G_m-C filter based on the transconductor shown in Fig. 5.56a. When the transconductor operates in weak inversion region, it can be shown that

$$I_o = \frac{I_{c1}}{I_{c2}} \frac{(V_1 - V_2)}{R_{eq}} \tag{5.33}$$

Note that R_{eq} is chosen larger than V_T/I_{c1}. The drain current of the transistor can be written as

$$I_D = I_{DO} \frac{W}{L} \exp\left(\frac{V_{GS}}{n V_T}\right) \tag{5.34}$$

where n is the subthreshold slope factor. On the other hand, when the transconductor is operating in the strong inversion region, it can be shown that

$$I_o \cong (V_1 - V_2) \frac{\sqrt{\frac{2I_{c2}}{I_{c1}}}}{R_{eq} + \sqrt{\frac{2}{kI_{c1}}}} \tag{5.35}$$

Thus, in both cases, the transconductance can be changed by tuning I_{c2}/I_{c1}. The tuning range can be extended by designing the transconductor so that it can switch from weak inversion region to strong inversion region continuously. Thus, the input stage remains in weak or strong inversion, however, the output stage can move from weak to strong or vice versa.

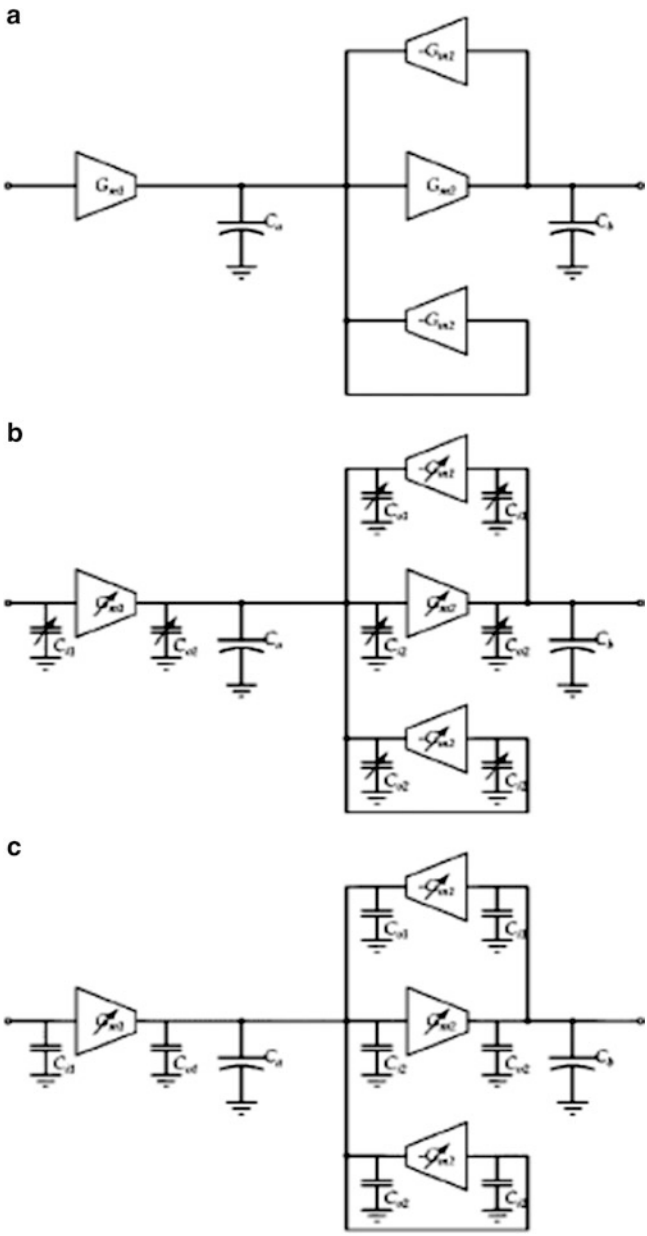
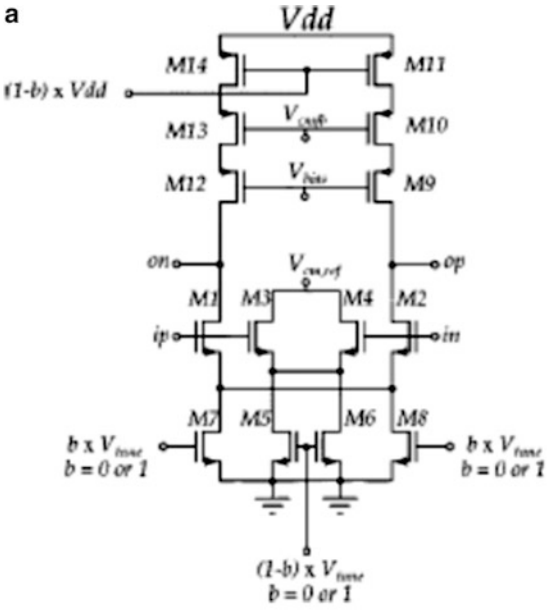
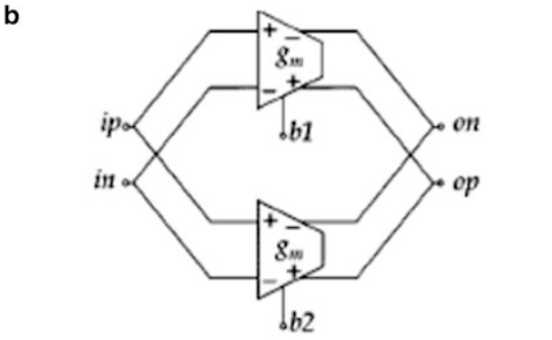


Fig. 5.54 (**a**) A second-order G_m-C filter, (**b**) programmable version of (**a**) using variable G_m and variable parasitics, and (**c**) programmable version of (**a**) using variable G_m but fixed parasitics (Adapted from [5.47] ©IEEE 2000)

The resistor R_{eq} is realized as shown in Fig. 5.56b which comprises a parallel connection of a large resistor and a small resistor. The large resistance is realized by the output impedance of four parallel connected transistors in the saturation region, when V_{mode} turns off M_{RS}. On the other hand, when M_{RS} turns on, the resistance is that of M_{RS} working in the triode region.





$b1$	$b2$	G_m	G_o	C_i	C_{ov}	C_o	DC Gain
0	1	g_m	g_o	$2c_i$	$2c_{ov}$	$2c_o$	g_m/g_o
1	1	$2g_m$	$2g_o$	$2c_i$	$2c_{ov}$	$2c_o$	$2g_m/2g_o = g_m/g_o$

(b)

Fig. 5.55 (**a**) A unit transconductance element, (**b**) parallel connection of two transconductors, (**c**) 4-bit programmable constant capacitance transconductor, (**d**) fourth-order G_m-C filter using transconductors of (**c**), (**e**) common mode feedback circuit, and (**f**) bias circuit for transconductance (Adapted from [5.47] ©IEEE 2000)

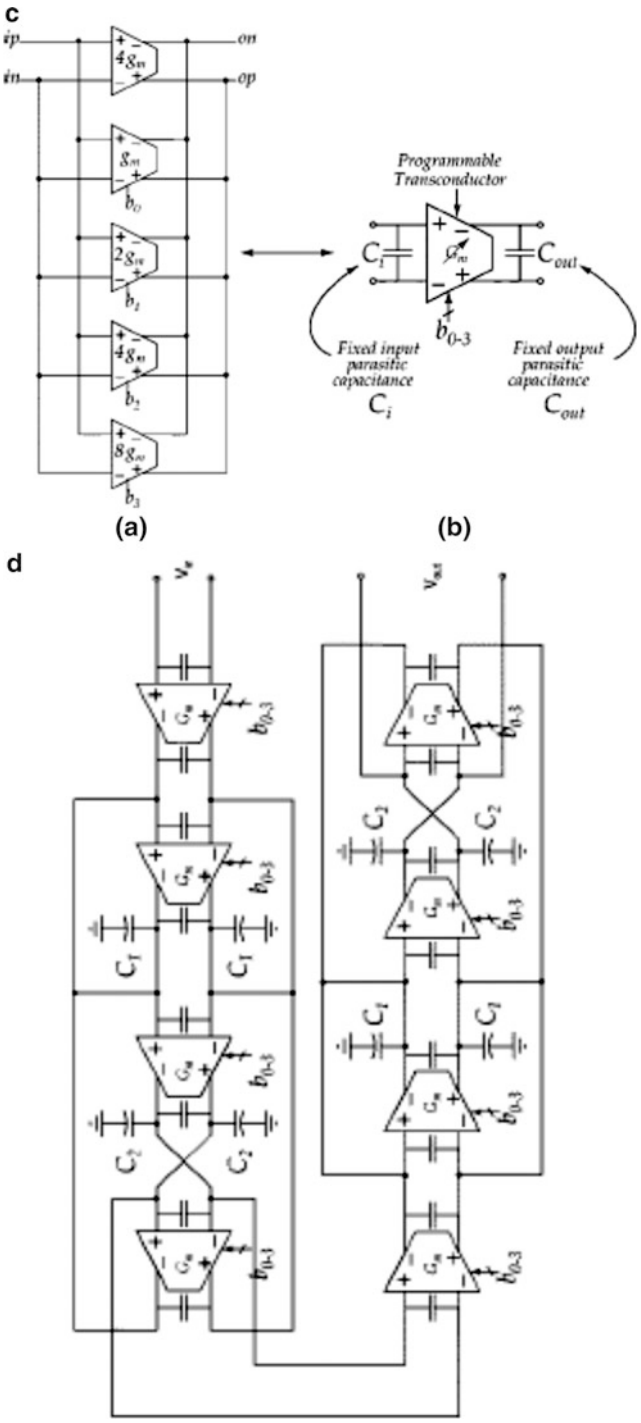


Fig. 5.55 (continued)

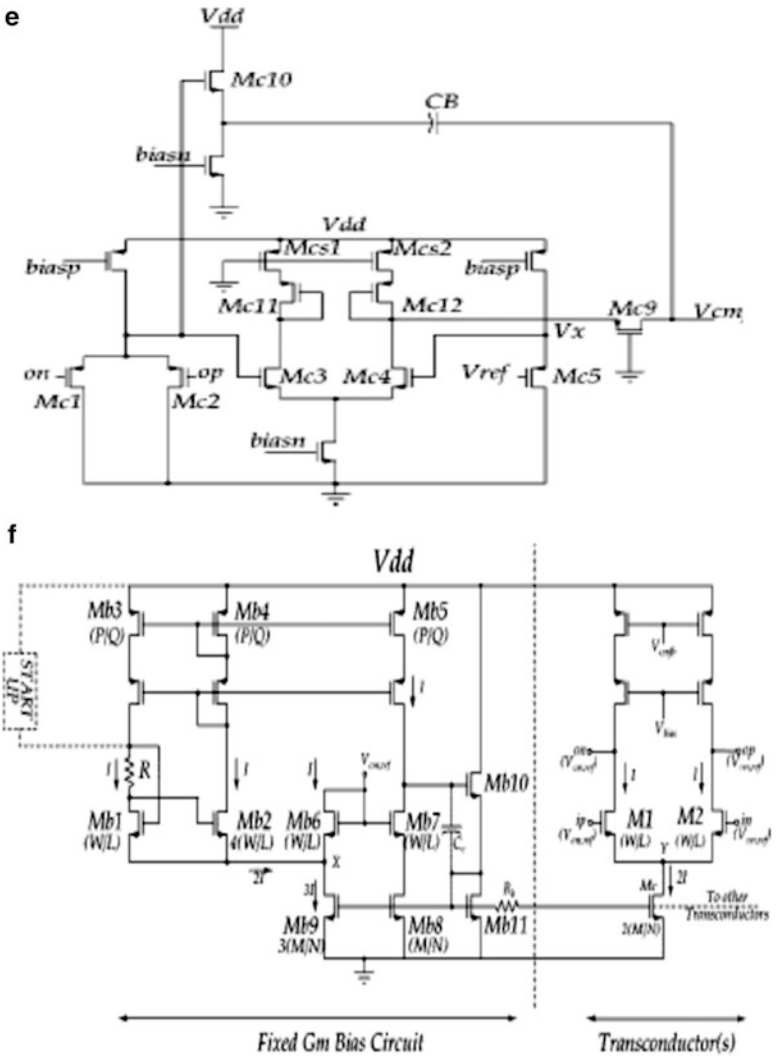


Fig. 5.55 (continued)

The complete circuit of the transconductor is shown in Fig. 5.56c. The mode can be selected by the circuit of Fig. 5.56d. If the gate voltage of MIC_{13} is greater than V_T, V_{mode} is set to "1" using the chain of inverters. Otherwise, it is set to zero ground voltage. The authors have implemented a fifth-order elliptic low-pass filter. The cutoff frequency was suggested to be tuned by changing the bias current of the OTA which, however, is not implemented by the authors.

Chen et al. [5.49] have described a fourth-order OTA-C linear-phase filter with automatic frequency tuning. The pseudo-differential OTA used in their design is

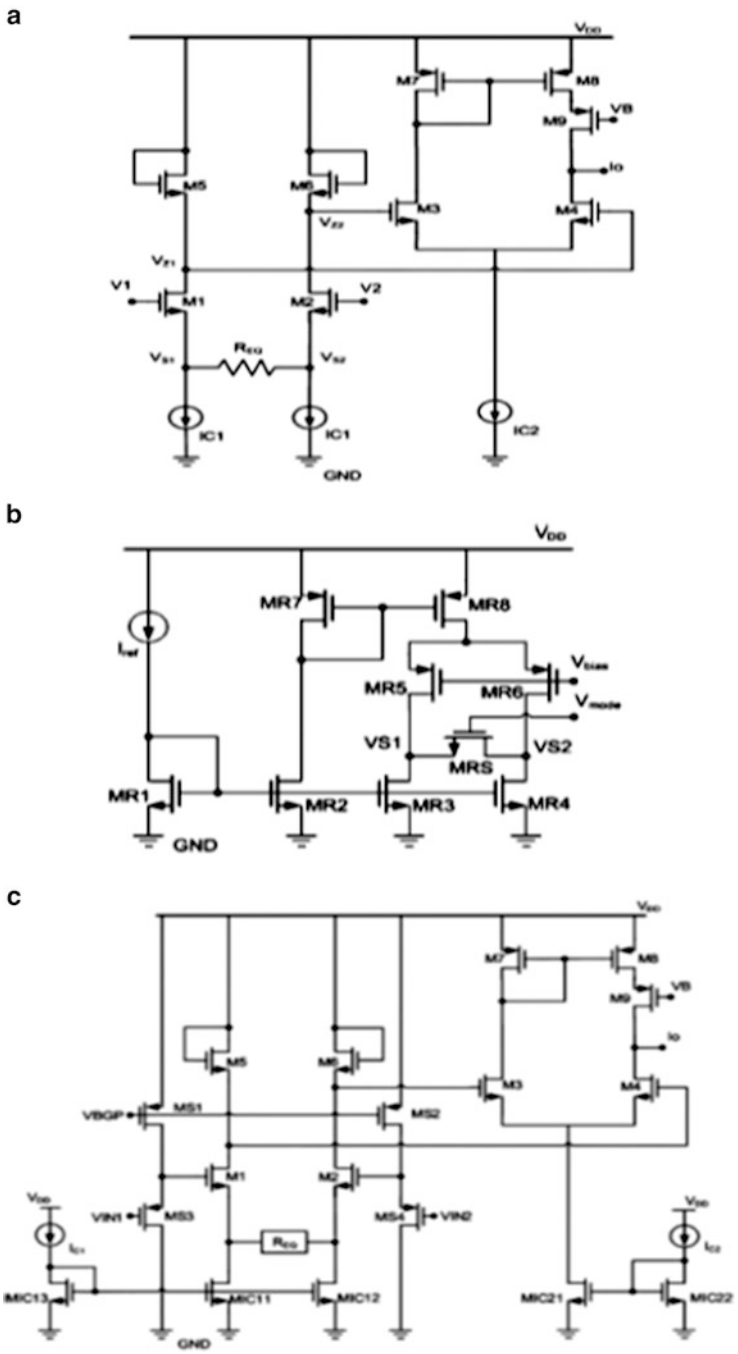


Fig. 5.56 (**a**) Transconductor with wide tuning range, (**b**) equivalent resistor circuit, (**c**) complete implementation of the transconductor, and (**d**) V_{mode} switching circuit for the transconductor (Adapted from [5.48] ©IEEE 2007)

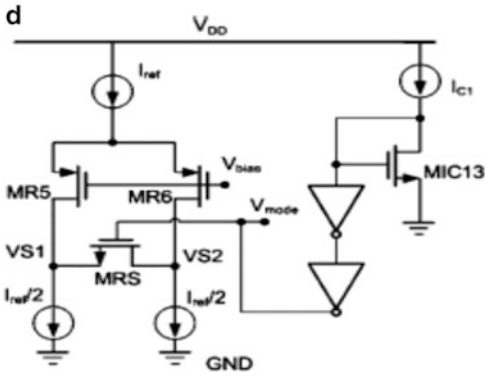


Fig. 5.56 (continued)

presented in Fig. 5.57a. Note that M_3 and M_4 operate in the saturation region and M_1 operates in the triode region. The transistor M_2 and opamp form a RGC (regulated gain control) loop to fix the drain voltage of M_1 to V_{tune} independent of the input signal level. The OTA uses CMFF, adaptive biasing as well as CMFB as shown in Fig. 5.57b. The CMFF/bias circuit shown on the right is a replica of a single branch of the OTA of Fig. 5.57a except that the transistor M_1' is split in two connected to the input voltage. The left circuit comprises a CMD. Transistors M_5 and M_5' work in the deep triode region to improve the linearity of the CMFB. The circuit compares V_{ref} with V_o and generates the CMFB correcting current which is added to that of CMFF to provide overall control to the transconductor. Transistors M_6 and M_6' are driven by the output of the OTA and CM reference voltage, respectively. The equivalent circuit of the CMFB is shown in Fig. 5.57c. Note that three parasitic poles exist at nodes A, B, and C of which the pole at C is dominant.

A fourth-order filter is shown in Fig. 5.57d in which six OTAs use a CMFF/CMFB /bias whereas the Q determining OTAs have only CMFF/bias due to the low output impedance. The automatic tuning system is shown in Fig. 5.57e. Note that G_m and C integrate V_{REF}. The difference between the input and integrator magnitude is compared to generate a control signal to tune the integrator's unity gain frequency to the desired value.

Pankiewicz et al. [5.50] have described a field-programmable analog array (FPAA) for CT OTA-C filter applications. This consists of 40 configurable analog blocks arranged as five rows and eight columns. In addition there are three buffers. Three different filters can be realized simultaneously. The CAB structure is shown in Fig. 5.58a which has several switches around each CAB (see Fig. 5.58b) to facilitate connection to other CABs using 12 switches. In addition the OTA has variable G_m using 5 bits and a capacitor array has 5-bit control. Thus overall, 22 bits are used to configure the CAB (configurable analog block). A total of 880 bits can configure the complete FPAA. The OTA has controllable G_m whose structure is shown in Fig. 5.58c. This is based on two cross-coupled differential pairs. The programmable

current mirrors G_1 and G_2 can facilitate changing the I_{out}. It can be shown that the output current is given as

$$I_{out} = K V_b A V_{id} \tag{5.36}$$

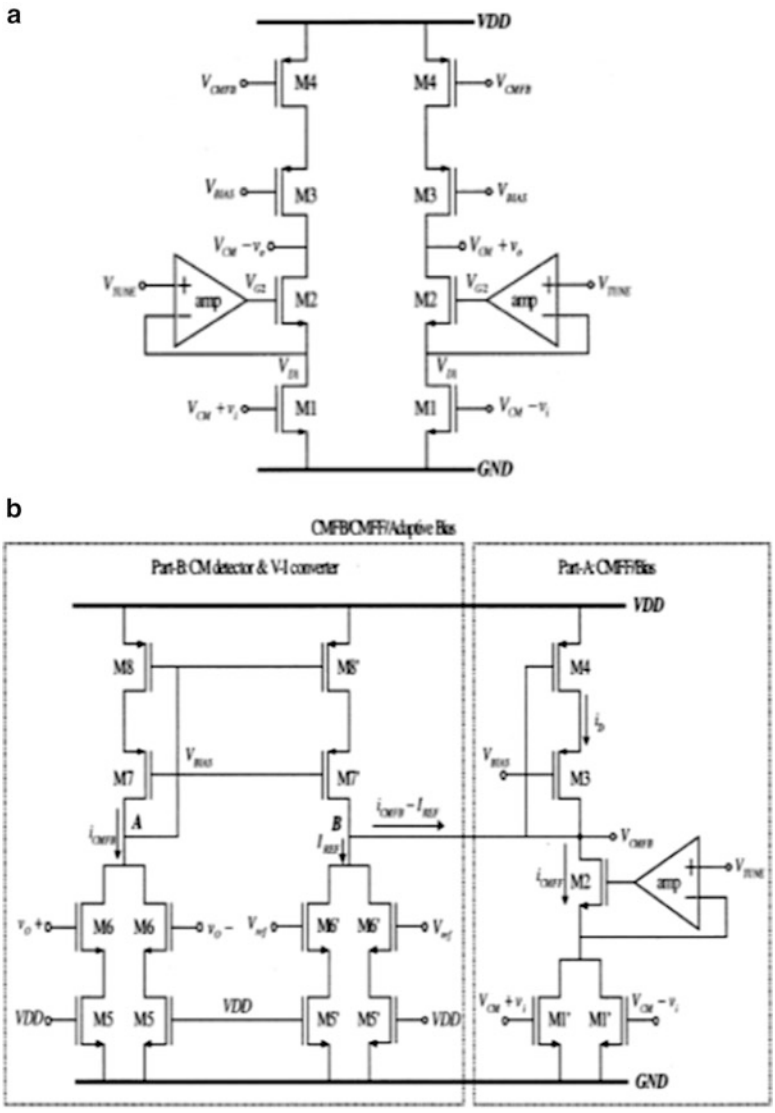


Fig. 5.57 (**a**) Pseudo differential OTA, (**b**) common mode control circuit, (**c**) simplified CMFB equivalent circuit, fourth-order equiripple linear phase filter, and (**e**) block diagram of the automatic tuning system (Adapted from [5.49] ©IEEE 2003)

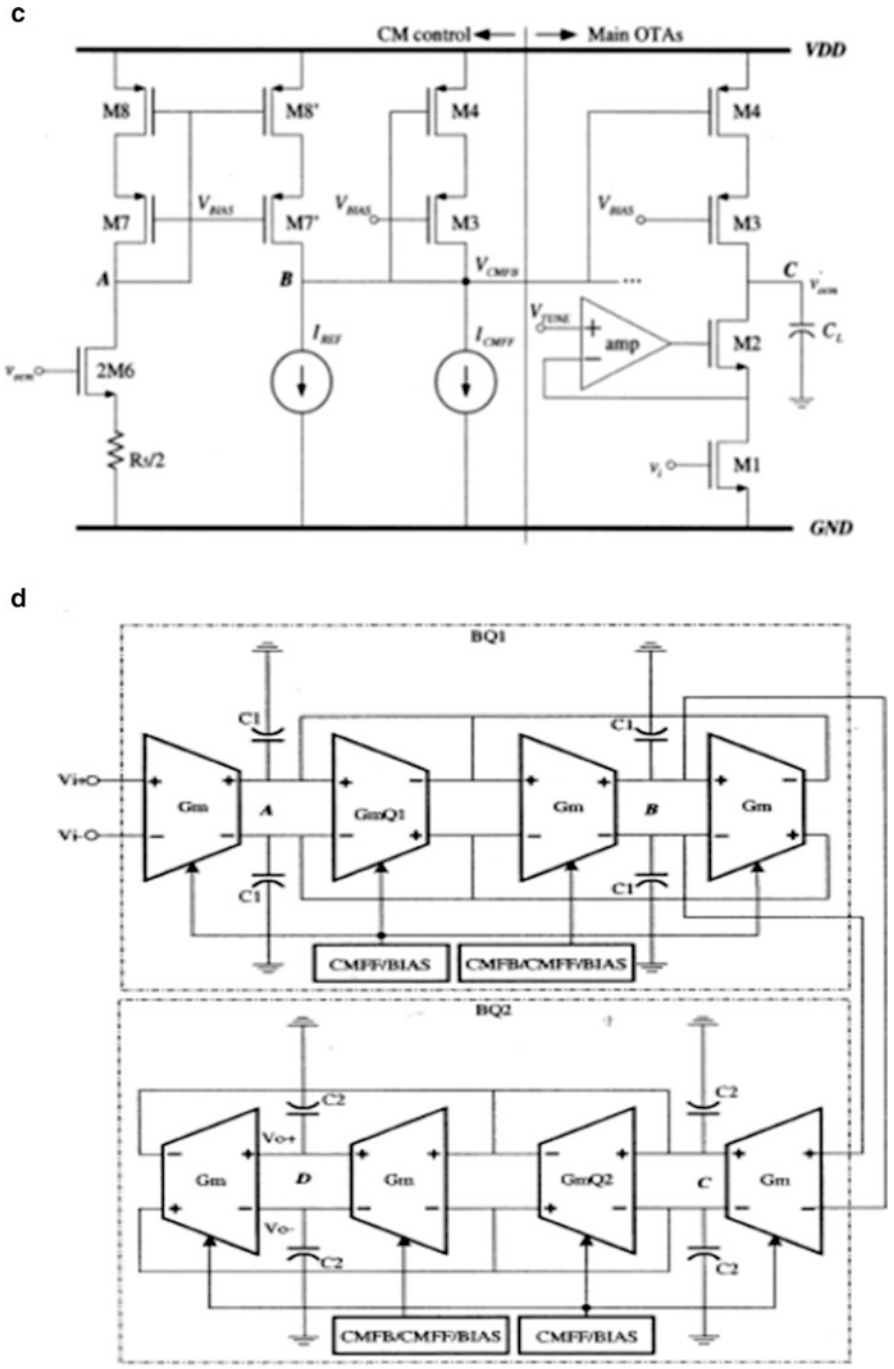


Fig. 5.57 (continued)

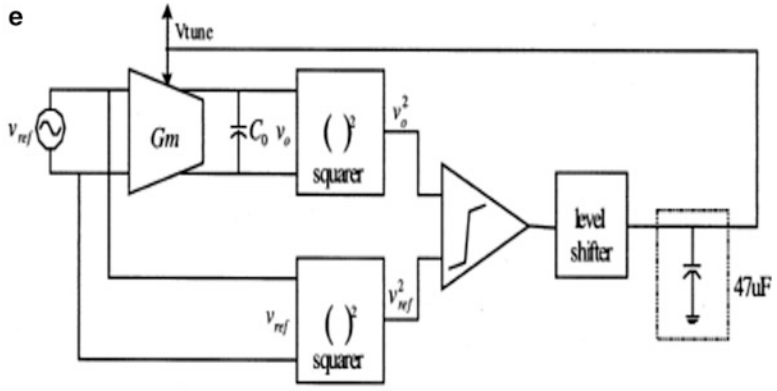


Fig. 5.57 (continued)

where $K = 0.5\ \mu C_{ox}W/L$ and A is the gain of the current mirror. Thus A or V_b or both can be used to program the G_m ($= KV_bA$). The current mirror used is shown in Fig. 5.58d which uses 31 cascode current mirrors connected appropriately using switches. When a current mirror is not selected, its switches are used to connect its gate of the lower transistor M_{ia} to ground. The authors have suggested a tuning technique shown in Fig. 5.58e. The reference is a cascade of four first-order filters with a overall gain of 4. At the cutoff frequency, the total phase shift is 180 degrees and the gain is 1. The output is compared with the input by a phase detector which gives a control voltage to adjust the g_m of the OTA. The reader is referred to [5.50] for a complete description including the floating voltage source V_b.

Lewenski and Silva-Martinez [5.51] described a fifth-order low-pass elliptic filter based on the RLC ladder filter. The OTA used is highly linear. The basic principle of the OTA is illustrated in Fig. 5.59a. Note that an adaptive nonlinear resistance is used between the sources of the differential pair using source degeneration. This is realized using the cross-connected transistors in the ADP (auxiliary differential pair) block. This reduces the third-order nonlinearity. The cross-coupled transistors introduce a negative resistance that increases with input voltage, thus effectively controlling the degeneration resistance. Cancellation of THD is possible under the condition $G_{mP}R \ll 1$. The authors realize the condition $nG_{mN}R = 1$ using a feedback loop as shown in the calibration circuit in Fig. 5.59b, where n is the desired scaling factor. The high loop gain adjusts the tail current I_{TBN} until the condition $V_R = V_{REF}$ is met. The complete transconductance is presented in Fig. 5.59c together with the common mode feedback loop. The CMFB loop does not use adaptive degeneration. A fifth-order LP elliptic filter (see Fig. 5.59d) was realized for powerline communications with 30 MHz bandwidth. The termination resistances were realized using polysilicon resistors. OTAs of fixed G_m were used and capacitor arrays were used for frequency tuning of the filter.

Chen et al. [5.52] described the design of OTA-C filters using linearized OTAs. A linearized cross-coupled differential pair based OTA is shown in Fig. 5.60a

which uses source degeneration. The cross-coupling yields polynomial cancellation. They have shown that HD_3 can be completely cancelled under ideal conditions. However, the parasitic capacitances, mismatches between resistors and transistors will limit the accuracy of cancellation. In addition, the OTA excess phase also affects performance. The authors have also considered using FGMOS (floating gate MOS) transistors in place of M_1 and M_2 as shown in the complete circuit in Fig. 5.60b. The FGMOS transistor including all capacitances is illustrated in Fig. 5.60c which results in input attenuation. The transistors M_6 and M_7 perform

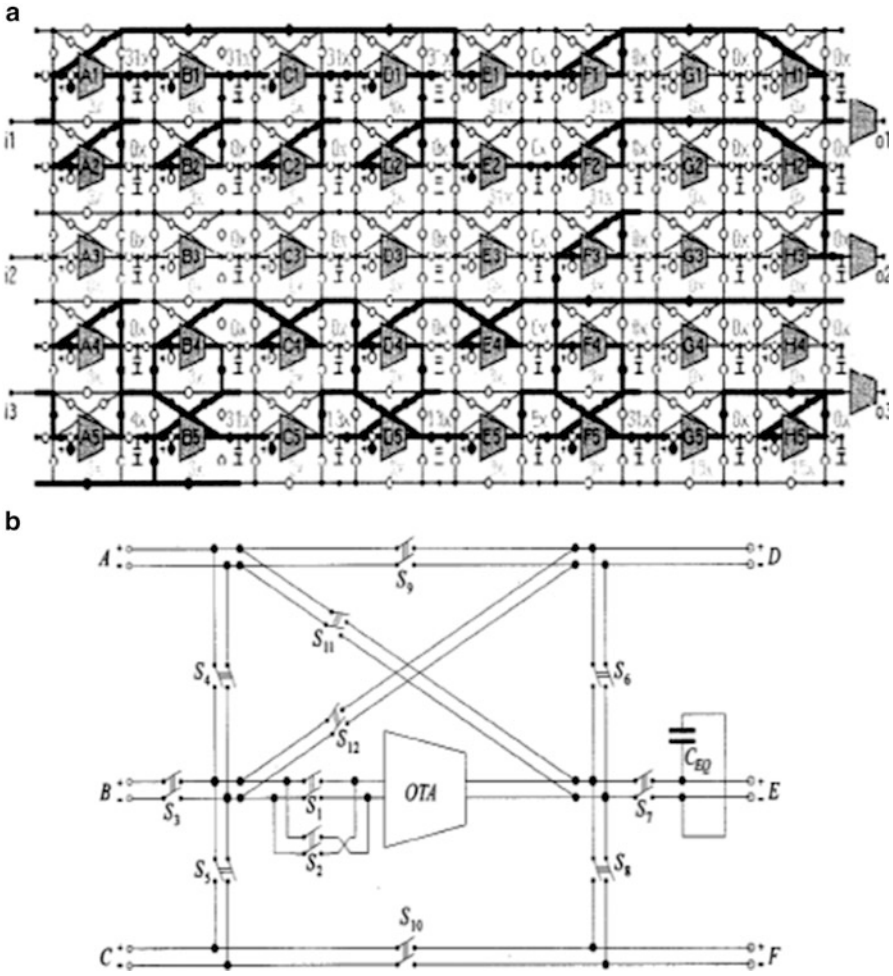


Fig. 5.58 (**a**) Field-programmable analog array structure, (**b**) structure of configurable analog block (CAB), (**c**) simplified schematic of CMOS programmable OTA, (**d**) simplified schematic of programmable current mirror, and (**e**) schematic of tuning circuit (Adapted from [5.50] ©IEEE 2002)

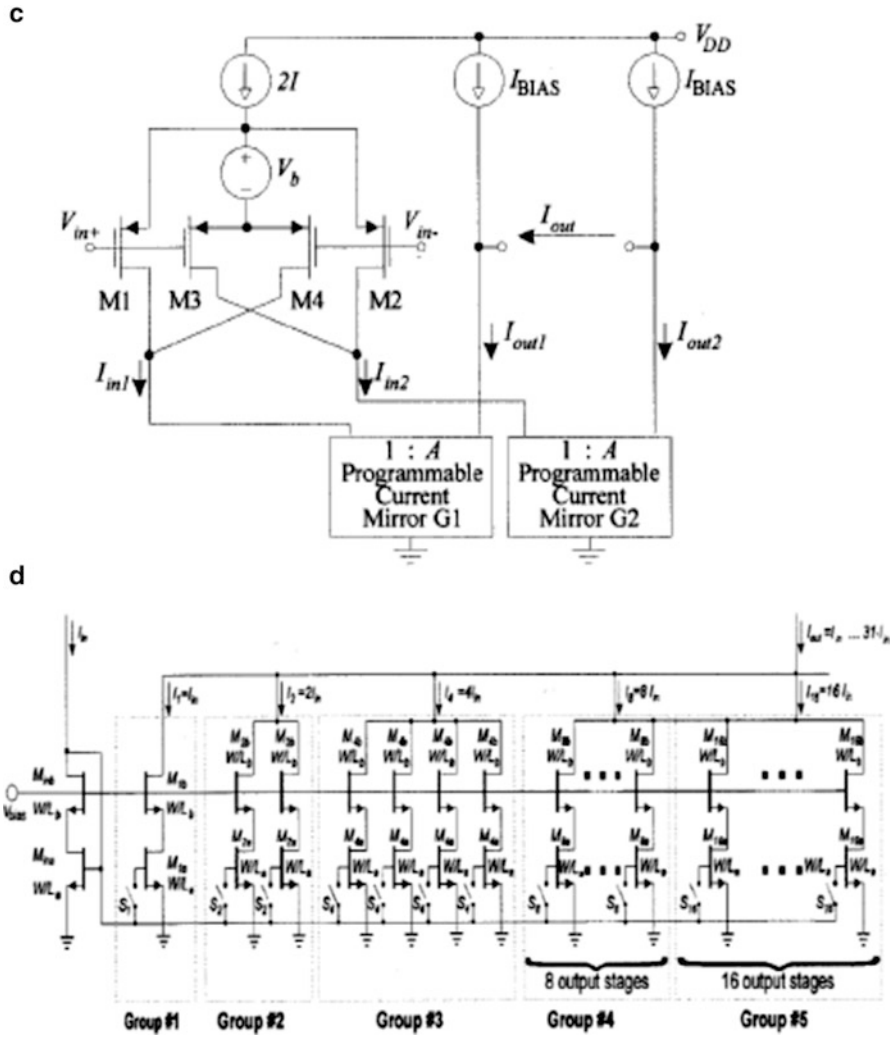


Fig. 5.58 (continued)

current division and facilitate tuning of the transconductance without changing core OTA biasing conditions. Note that the common mode signal can be obtained at the junction of resistors R_1 (V_{CM}). It has been shown that the FGMOS type of OTA improves linearity up to 10 dB at 20 MHz when compared to equivalent OTA not using FGMOS input transistors. The reader is referred to [5.52] for more information.

Silva-Martinez et al. [5.53] have described a seventh-order linear phase OTA-C filter with on-chip automatic tuning. The OTA is based on complementary differential pairs as shown in Fig. 5.61a. Note that degeneration is provided by transistors

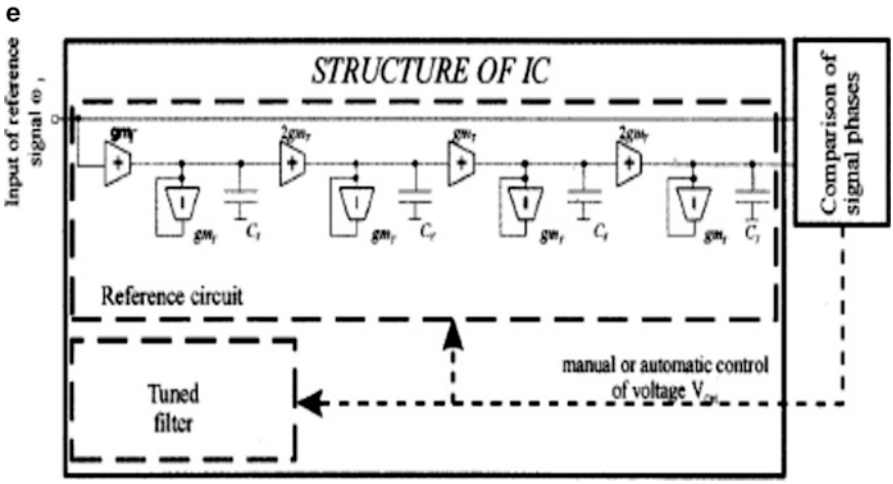


Fig. 5.58 (continued)

M_{RN} and M_{RP} for the n channel and p channel differential pairs, respectively. The transistor M_{RN} is split to obtain the CM signal. The even harmonic components are cancelled whereas the third harmonic components still exist. The OTA can be designed in two ways: (a) $V_{DSAT1} = V_{DSAT2}$, $I_{D1} = I_{D2}$ and $N_P = N_N$ where $N_N = g_{m1}/2G_{oR}$ where G_{oR} is the small signal transconductance of M_R; and (b) using the same dimensions for p and n channel input devices in which case V_{DSAT2} will be larger than in the previous case. Hence nonlinear components are dominated by an n-channel differential pair. The CMFB arrangement is presented in Fig. 5.61b which has three parasitic poles. The stability can be improved using the OTA circuit of Fig. 5.61c where capacitors C_L provide a shorter path for high-frequency signals. The authors describe an automatic tuning system shown in Fig. 5.61d where the input amplitude and output at the unity gain frequency of an integrator are compared to provide a control signal to node $V_{T,n}$ in Fig. 5.61a for adjusting f_u by tuning G_m. The squarer is realized using the circuit shown in the inset of Fig. 5.61d.

Chatterjee et al. [5.54] have presented techniques for designing 0.5 V supply-based filters. They exploit the use of forward biasing the body source junction of transistors for reducing the V_T of the devices. They consider two structures: (a) with input to body and (b) with input to gate. A body-input fully differential OTA with local common mode feedback is shown in Fig. 5.62a. Inputs are applied to the bodies of PMOS devices M_{1A} and M_{1B} and their G_{mb} provides the transconductance. These are loaded by M_{2A}, M_{2B} which act as current sources. The transistors M_{3A} and M_{3B} form a cross-coupled pair realizing a negative resistance thereby boosting the differential gain. The common mode signal is detected by R_A and R_B which is fed to the gates of devices M_{1A}, M_{1B}, M_{3A}, and M_{3B}. The purpose of M_4 is to create a small dc shift between the output common mode voltage 0.25 V and the gate bias of 0.1 V. A cascade of two stages as shown in Fig. 5.62b realizes the two-stage OTA. The OTA is stabilized by adding Miller compensation capacitor C_C with series resistors R_C.

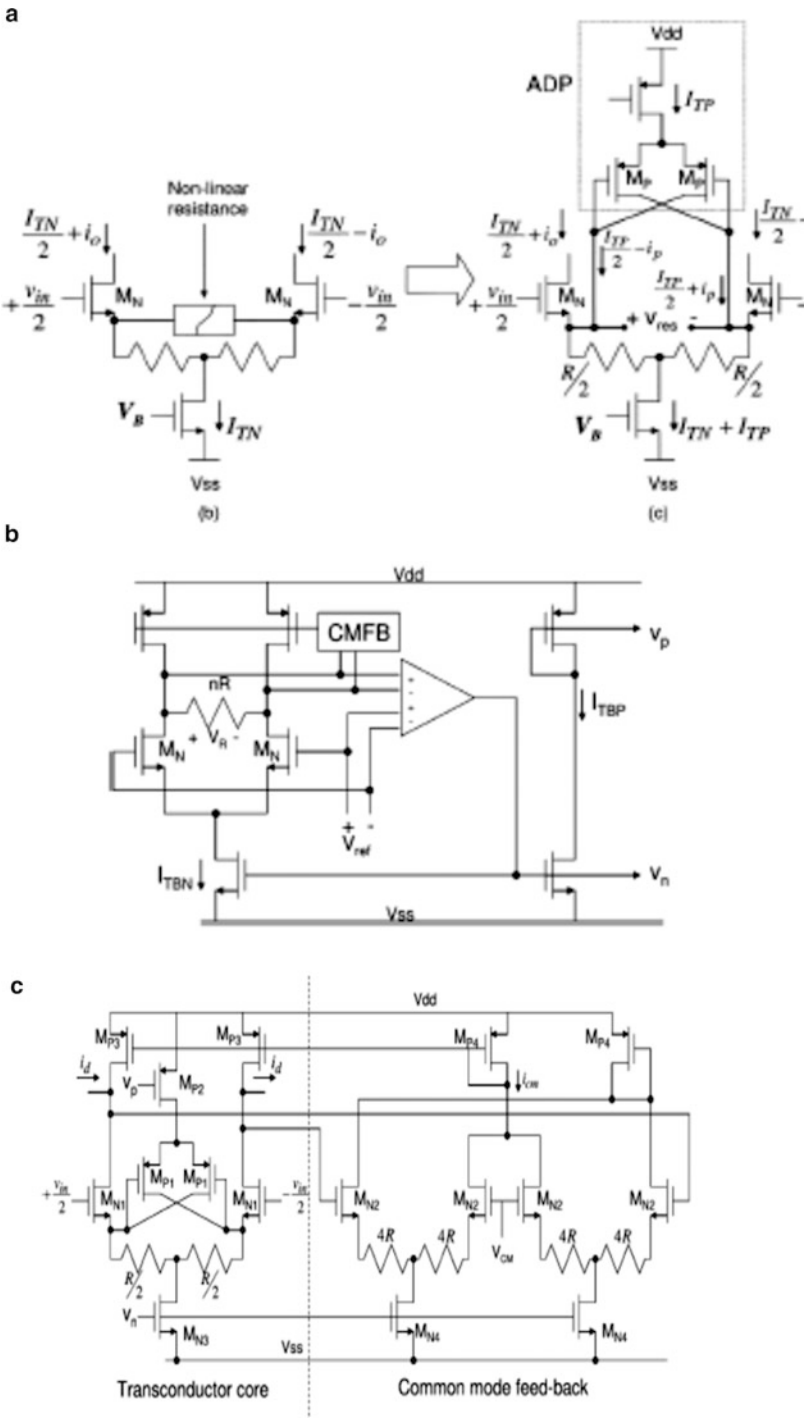


Fig. 5.59 (**a**) Technique for linearity enhancement of OTA, (**b**) self bias circuit (**c**) complete transconductor with CMFB and (**d**) a fifth-order elliptic filter implementation (Adapted from [5.51] ©IEEE 2007)

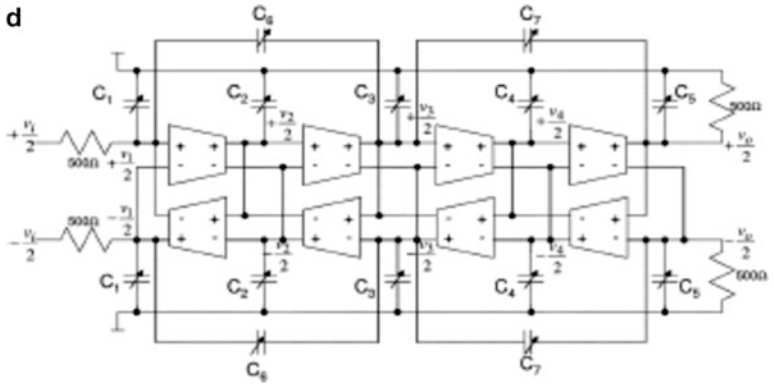


Fig. 5.59 (continued)

The gate input OTA is presented in Fig. 5.62d which is based on the basic configuration of Fig. 5.62c. The body terminal is used for biasing. The input differential pair is formed by M_{1A}, M_{1B} and active loads M_{2A}, M_{2B}. The resistors R_{1A} and R_{1B} provide common mode feedback through the active loads. A level shifting current I_L develops a 0.15 V drop across R_{1A} and R_{1B} so that M_{2A} and M_{2B} operate in the moderate inversion. The bodies of M_{2A} and M_{2B} are connected to the gate to reduce their V_T. The devices M_{4A}, M_{4B} realize a negative resistance for further enhancing the gain. The body voltage of this cross-coupled pair is controlled by the bias voltage V_{NR}. A common mode feedforward path is added through M_{5A}, M_{5B}, M_6, M_{3A}, and M_{3B}. The two-stage OTA based on the structure of Fig. 5.62d is shown in Fig. 5.62e. Note that in the second stage, M_{11A} and M_{11B} realize the negative resistance with their body voltage controlled by the low common mode voltage at the output. The OTA is stabilized through the Miller capacitors across the second stage.

The OTA of Fig. 5.62e requires three biasing voltages V_{bn}, V_L, and V_{NR}. The authors use replica circuits extensively to generate these bias voltages. An error amplifier based on inverters is shown in Fig. 5.63a. The inverter compares its switching threshold voltage with $V_{DD}/2$. The stability of the feedback loop is ensured through the compensating resistor R_{ea} and capacitor C_{ea}. The generated V_{amp} is used to derive the level shifting voltage V_L using the circuit of Fig. 5.63b. The voltage V_L is generated by the resistors R_{1c} and the current source realized by NMOS transistor. The voltage V_Y is 0.25 V and the voltage across R_{1c} is 0.15 V. This voltage drop is ratioed and transferred to the level shifter. Next, the V_{bn} is generated by the circuit of Fig. 5.63c. The output common mode voltage of the front-end opamp is compared with 0.25 V and the difference is amplified to control V_{bn}. Finally, the cross-coupled pair of devices M_{4A} and M_{4B} generating negative resistance (see Fig. 5.62d, e) are biased by V_{NR} generated by the circuit of Fig. 5.63d. A Schmitt trigger oscillator formed by OTA, R, and C oscillates at a frequency given by

$$f_o = \frac{1}{2RC}\frac{1}{\ln\frac{1+\beta}{1-\beta}} \tag{5.37}$$

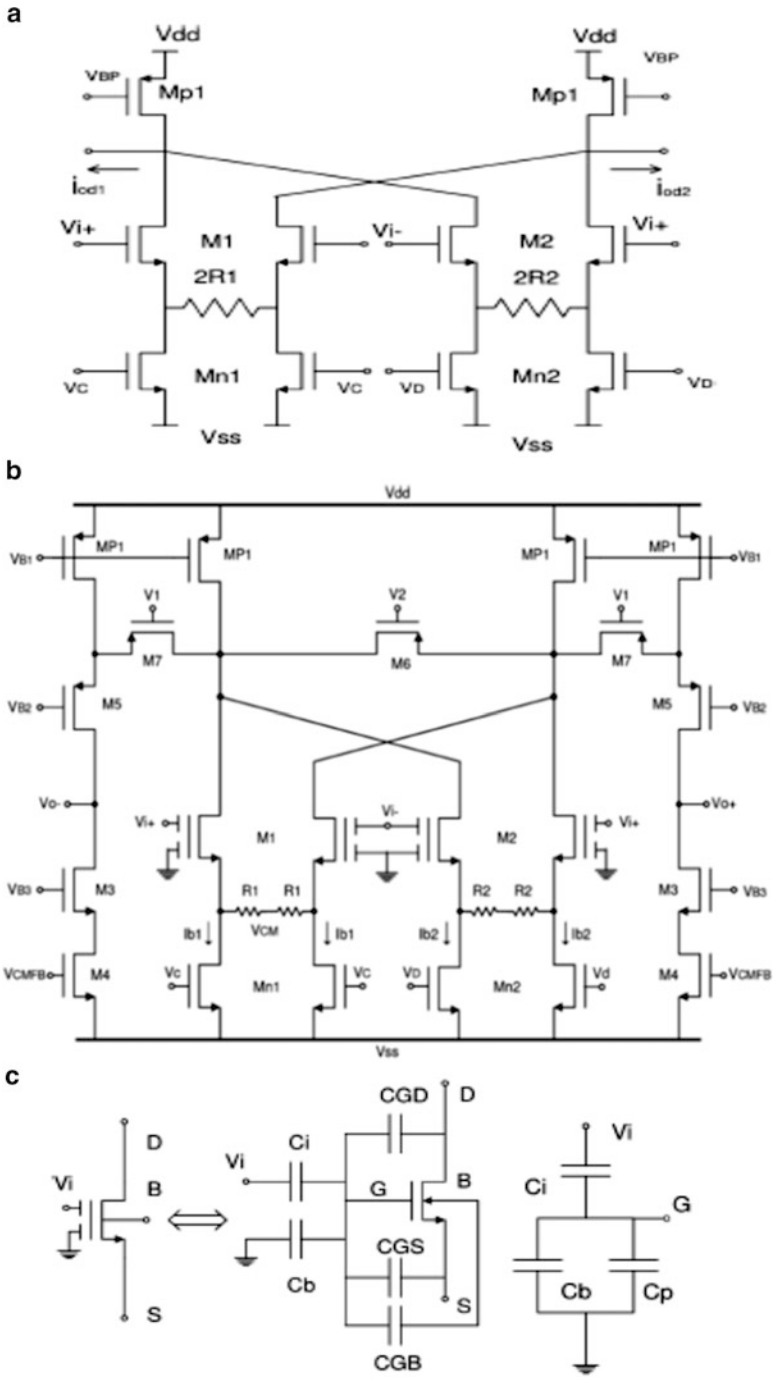


Fig. 5.60 (**a**) OTA based on cross-coupled differential pairs with degeneration resistors, (**b**) schematic of FGMOS OTA, and (**c**) FGMOS transistor with all capacitances and equivalent seen from V_i (Adapted from [5.52] ©IEEE 2006)

where $\beta = \frac{V_{hyst}}{V_{HL}}$ with V_{hyst} is the difference between trigger voltages for rising and falling edges and V_{HL} is the difference between the two output levels of the Schmitt trigger. When oscillations are present, the output of the XNOR gate decreases. Otherwise, the output increases, thus controlling the oscillator.

The OTAs are used to realize tunable damped integrators using the circuit of Fig. 5.64a which use three terminal varactors based on weak inversion MOS capacitors. The tuning voltage is applied to the body and source and drain are connected together. The capacitance is between gate and source. The resistors at the input to V_{DD} maintain the voltage at virtual ground of 0.4 V. A fixed capacitance is also connected across the varactor.

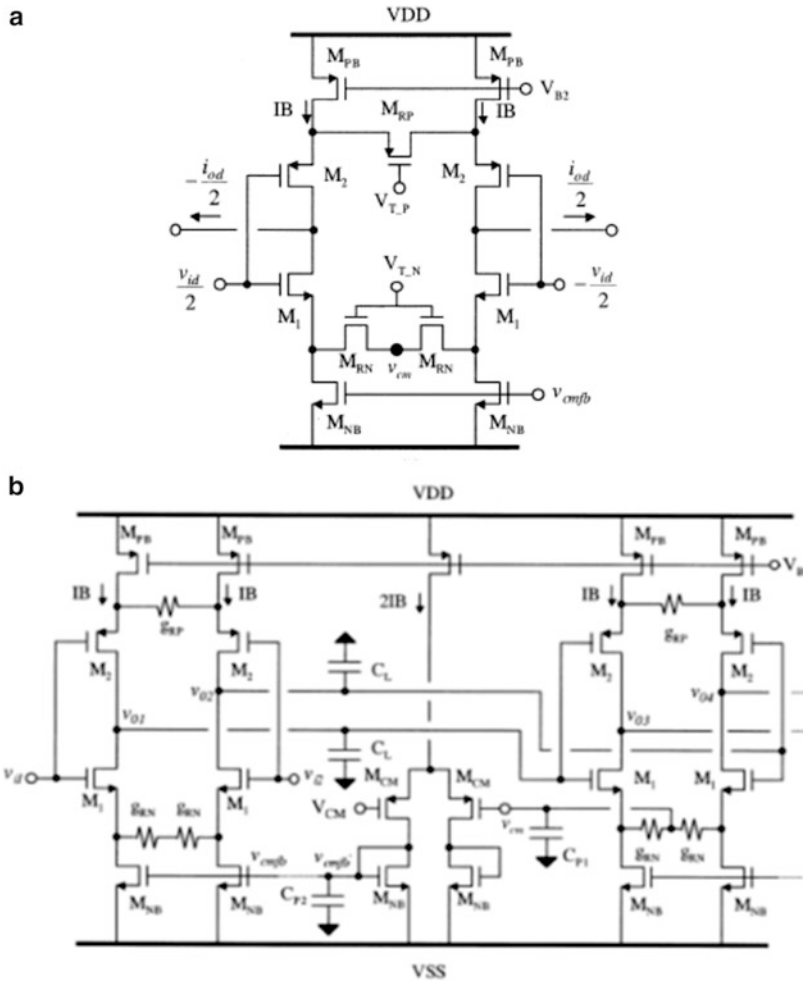


Fig. 5.61 (**a**) OTA based on complementary differential pairs, (**b**) CMFB arrangement exploiting direct connection of OTAs, (**c**) OTA with load capacitors used for stabilization of CMFB loop, and (**d**) frequency tuning loop together with squarer shown in inset (Adapted from [5.53] ©IEEE 2003)

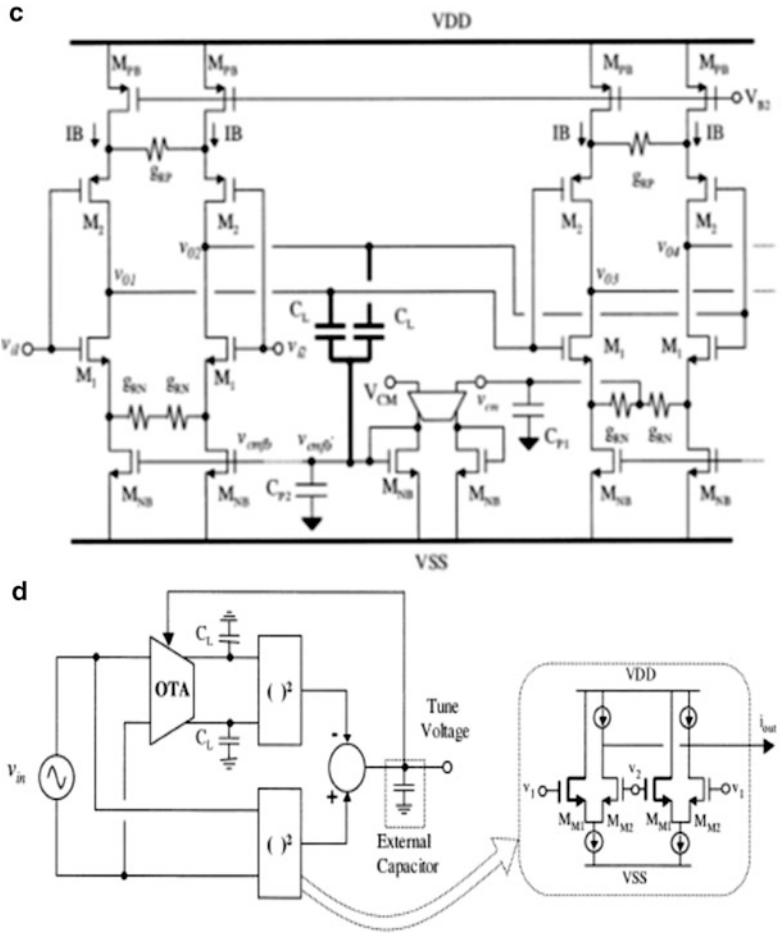


Fig. 5.61 (continued)

The authors have fabricated a fifth-order low-pass elliptic filter for a 135 KHz cutoff frequency using the leap-frog technique. An on-chip PLL-based automatic frequency tuning loop is also incorporated (see Fig. 5.64c) which uses a three-phase RC oscillator shown in Fig. 5.64b with a nominal frequency of $f_o = \frac{\sqrt{3}}{2\pi R_a C_a}$. The XOR detector compares the reference frequency with the VCO frequency and controls the body voltage of the capacitors in the VCO. The VCO control voltage V_{tune} is fed to all the capacitors in the filter.

Andreani and Matison [5.55] have considered the use of the Nauta transconductor [5.29] for low-frequency applications. They have derived the effect of NQS (nonquasi-static) behavior of resonators and conclude that there is a possibility of instability of LC resonators (see Fig. 5.65b). They also point out that in the case of band-pass filters, tank transconductors need a low dc gain to achieve high-Q whereas transmission transconductors need a high gain. They have

described two band-pass filters: one for a low IF receiver and another for a real band-pass filter. The complex band-pass filter is based on the fifth-order Butterworth filter prototype of Fig. 5.65c. Note that this is followed by a notch stage to increase the out-of-band attenuation close to pass-band. The real filter is a fourth- plus fourteenth-order doubly terminated band-pass ladder filter as shown in Fig. 5.65d. The reader is referred to their work for an exhaustive discussion on Nauta's transconductor.

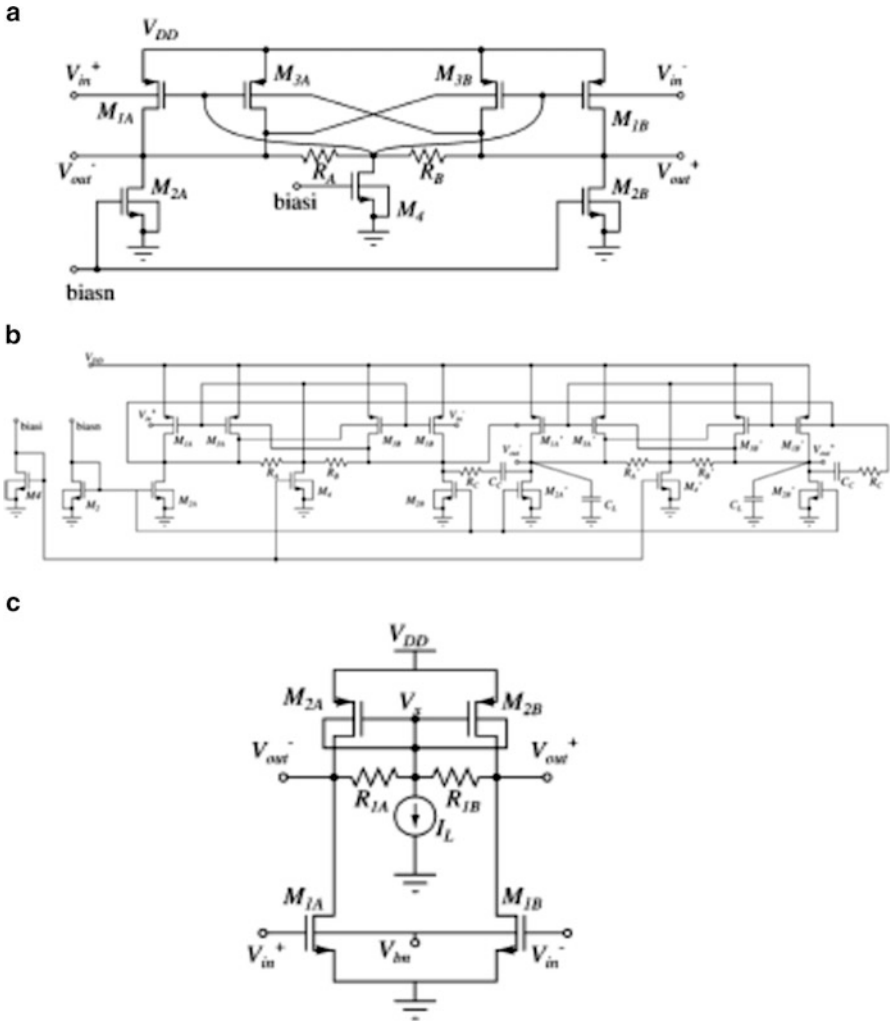


Fig. 5.62 (**a**) Fully differential body-input gain stage with CMFB, (**b**) two-stage version of (**a**) with Miller compensation, (**c**) conceptual circuit of a gate-input OTA, (**d**) more detailed version of (**c**), and (**e**) two-stage fully differential OTA using (**d**) (Adapted from [5.54] ©IEEE 2005)

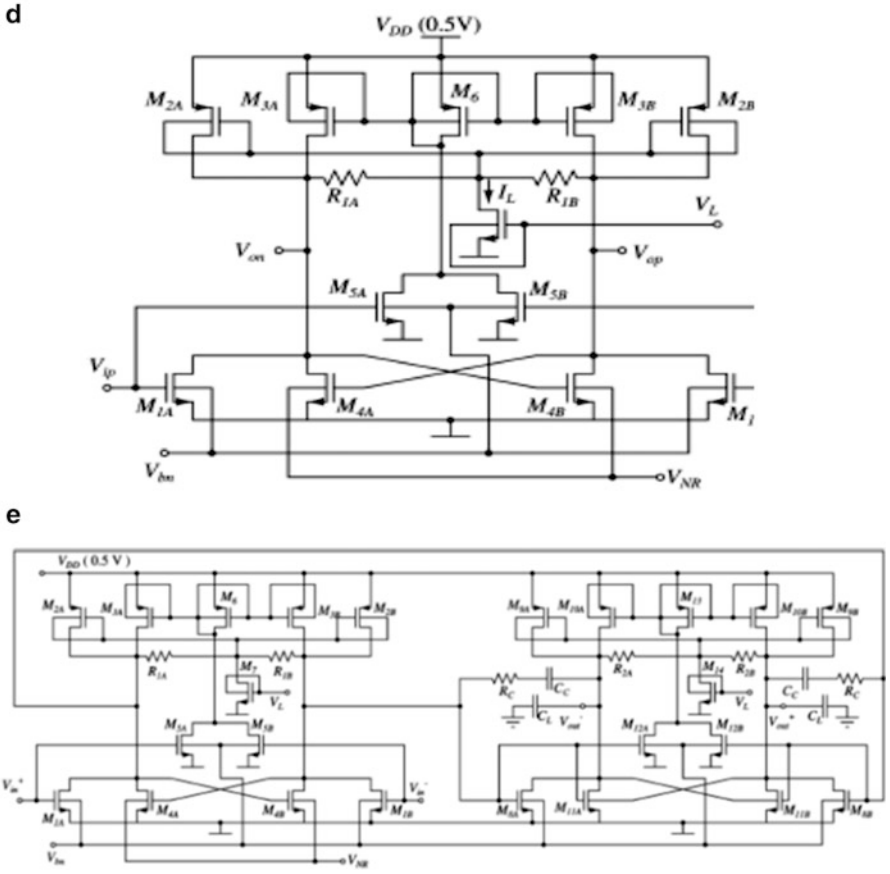


Fig. 5.62 (continued)

Nauta's transconductor shown in Fig. 5.65a has the advantage that there are no internal nodes and hence the parasitic capacitances can be merged with the filter capacitances. Note that V_{DD} is not power supply but a voltage generated by a frequency tuning loop. The common mode and differential mode gains are, respectively,

$$A_{cm} = \frac{g_m}{3g_m + 2g_d},\ A_o = \frac{g_m}{3g_d} \tag{5.38}$$

Since A_{cm} is less than unity, there is no concern about common mode stability. For very high frequency applications, short channel devices must be used leading to low gain A_o. However, in such cases, supply voltage can be tuned to obtain $G_{m5} \approx g_{m6} - (g_{d1} + g_{d5} - g_{d6})$ to obtain high A_o.

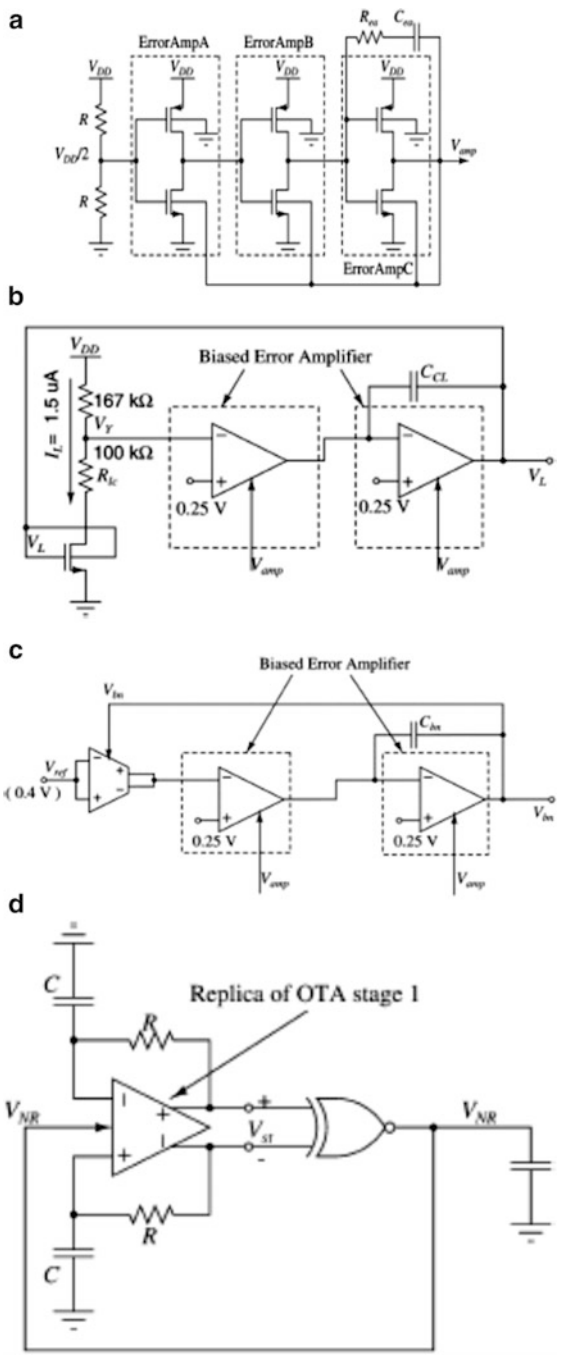


Fig. 5.63 (**a**) Error amplifier for fixing the switching threshold voltage to $V_{DD}/2$, (**b**) circuit for biasing the level shifting current source, (**c**) circuit for generating body bias of input NMOS devices to set the common mode voltage, and (**d**) Schmitt trigger-based oscillator and biasing technique to improve the gain of the OTA (Adapted from [5.54] ©IEEE 2005)

5.13 G_m-C Filter Tuning Techniques

Durham et al. [5.1] and Durham et al. [5.2] have suggested a tuning scheme using a dual-slope calibrator shown in Fig. 5.66a. The basic principle is to match the time constant in the filter with a reference clock. As shown in the timing diagram in Fig. 5.66b, capacitor C_o is reset and during φ_B, R_1 and C_o and the opamp work as an integrator thus generating the negative voltage ramp waveform. At the end of φ_B (2^N clock cycles), the SC branch C_1 pumps charge into capacitor C_o. When the voltage V_o reaches ground and the comparator changes state, the counter value is

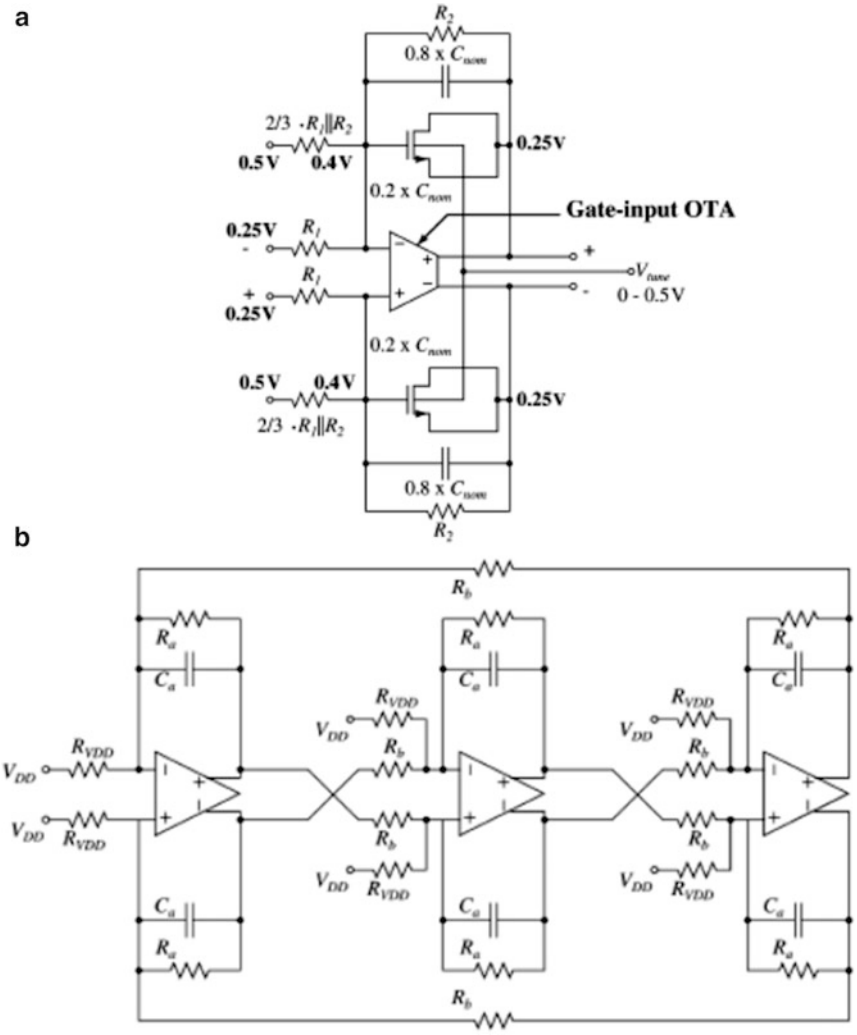


Fig. 5.64 (**a**) 0.5 V tunable damped integrator, (**b**) three-stage low-voltage oscillator, and (**c**) block diagram of the full chip (Adapted from [5.54] ©IEEE 2005)

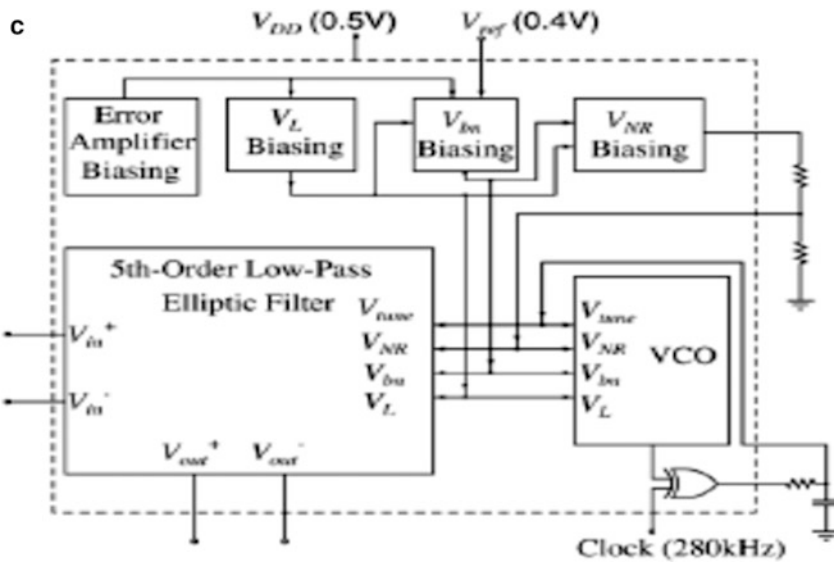


Fig. 5.64 (continued)

read indicating the number of clock pulses used to reach zero voltage. This value is fed to all the resistors in the filter. Evidently, $\delta V_o = V_{REF}\,\frac{C_1}{C_o}$ and $\frac{V_{REF}\,2^N\,T_{ck}}{C_o\,R_1} = \frac{V_{REF}\,C_1\,n_s}{C_o}$ .Thus, the tuning code is $n = \frac{2^N\,T_{ck}}{C_1\,R_1}$.

Vemulapalli et al. [5.56] suggested a technique for tuning continuous-time filters using time constant matched master–slave tuning combined with power-up mismatch calibration. The system-level block diagram is shown in Fig. 5.67a which combines the advantages of direct and indirect tuning methods. In the indirect tuning method (e.g., master–slave technique), tuning is performed in the background without affecting normal filter operation. The PVT variations in the slave filter are annulled by the PVT invariant master filter only in the ideal case. However, mismatch between the master and slave filters limits the accuracy to about 5%. Moreover, in low voltage designs, the room for tuning range is limited by the threshold voltage of the M_{Master} (M_{slave}) transistor (see Fig. 5.67b showing a SC frequency control loop).

In the digitally programmable master–slave tuning circuit of Fig. 5.67c, the master reference tunes the slave filter continuously to the required frequency. On the other hand, the power-up direct tuning cancels the master–slave mismatch thus resulting in a very accurately tuned filter. On power-up, a sine wave typically of the 3-dB frequency of the filter is applied to the slave filter. The master–slave mismatch is measured by the output amplitude of the filter and correction is applied to the slave filter. After this step, the filter is switched back to normal operation.

In Fig. 5.67c, a resistor R is used in series with a MOSFET in order to reduce the contribution of the nonlinearity of the MOSFET. The tuning loop makes the sum of

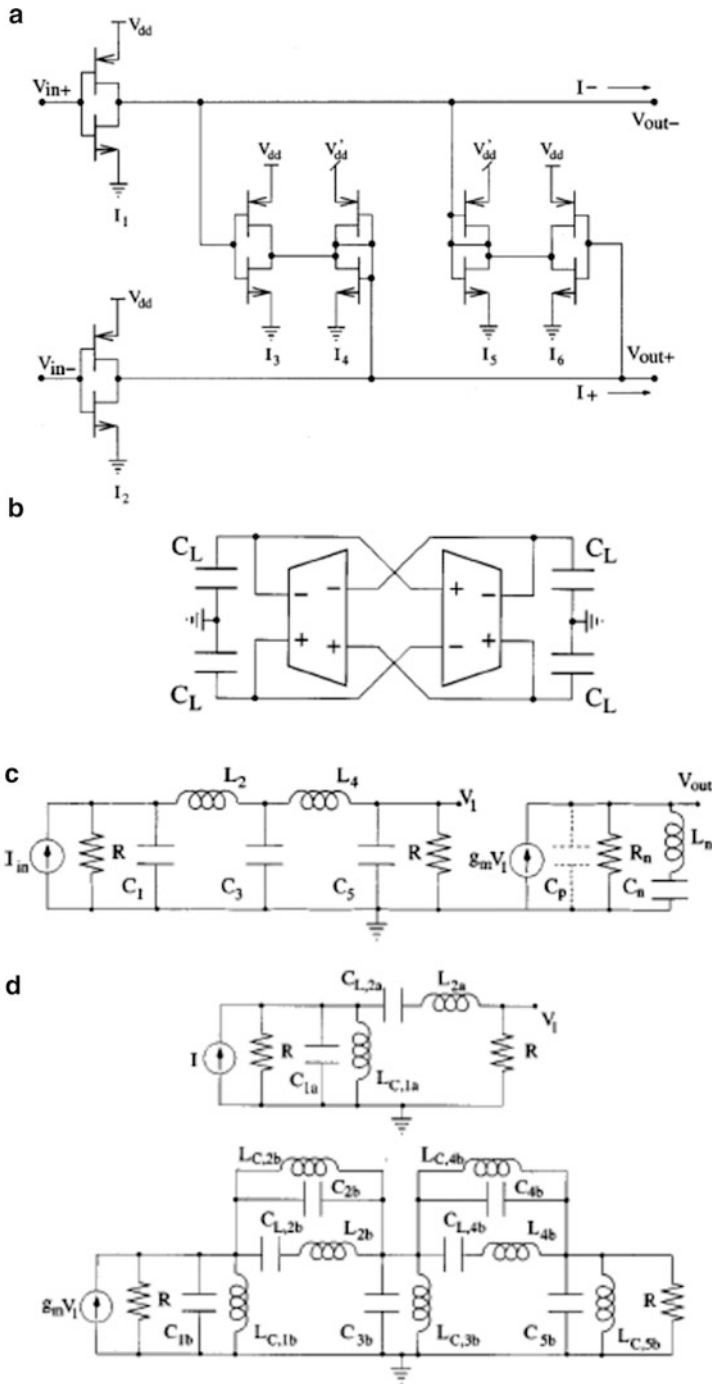


Fig. 5.65 (**a**) Nauta's symmetric transconductor, (**b**) active LC resonator, (**c**) passive low-pass filter prototype for the complex filter, and (**d**) passive prototype of the real band-pass filter (Adapted from [5.55] ©IEEE 2002)

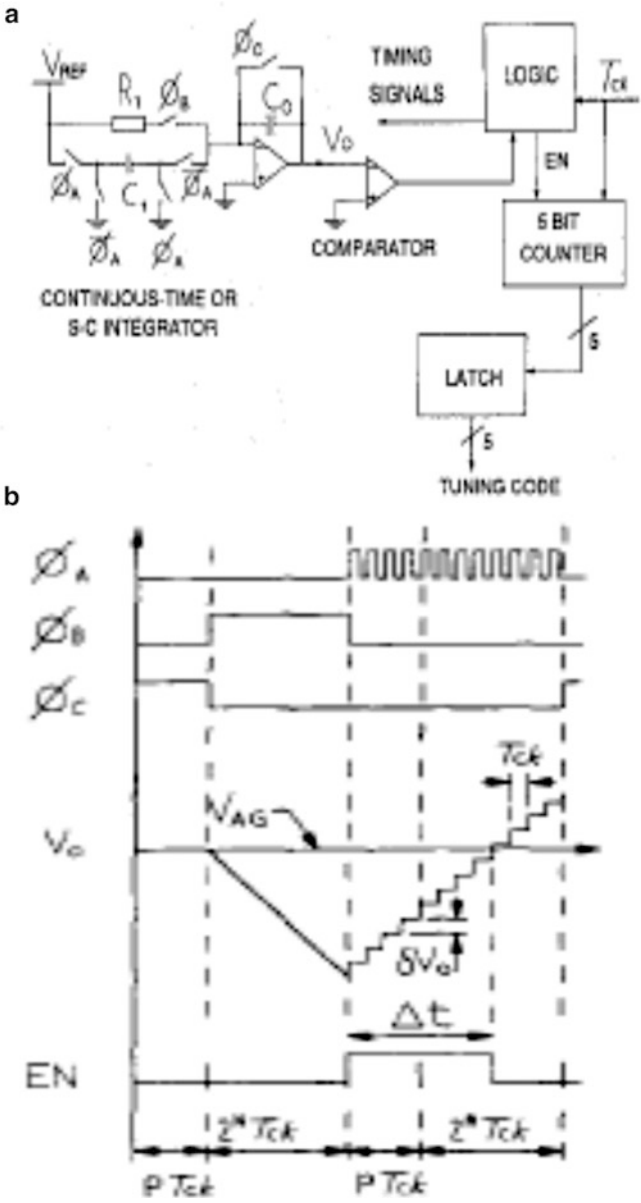


Fig. 5.66 (**a**) Dual slope calibrator, and (**b**) timing diagram of the calibrator (Adapted from [5.2] ©IEEE 1992)

R and MOSFET resistance equal to the resistance of the SC. Note that capacitor C_1 is replaced by a 5-bit PCA. The calibration can take into care of a $\pm 10\%$ mismatch between the master and the slave.

The sine wave source is synthesized using a digital state machine and a nonlinear current-mode D/A converter (see Fig. 5.67d). There are only four current sources used. The current-to-phase mapping is as shown in table in the inset of Fig. 5.67d.

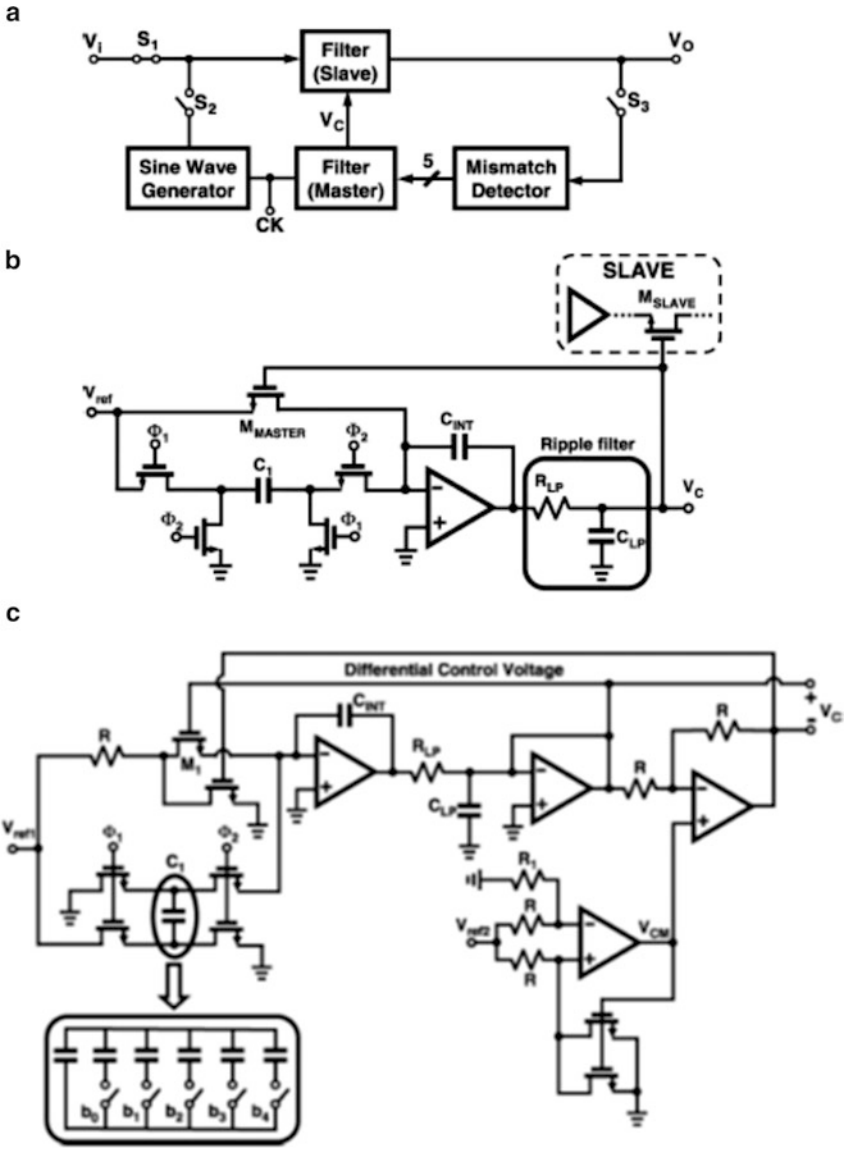


Fig. 5.67 (**a**) Combined master–slave and power-up direct frequency tuning, (**b**) master–slave tuning circuitry, (**c**) digital programmable version of (**c**), (**d**) digital synthesis of a sine wave using array of current sources, (**e**) mismatch detection and correction scheme, (**f**) peak detector schematic, and (**g**) differential difference comparator (Adapted from [5.56] ©IEEE 2005)

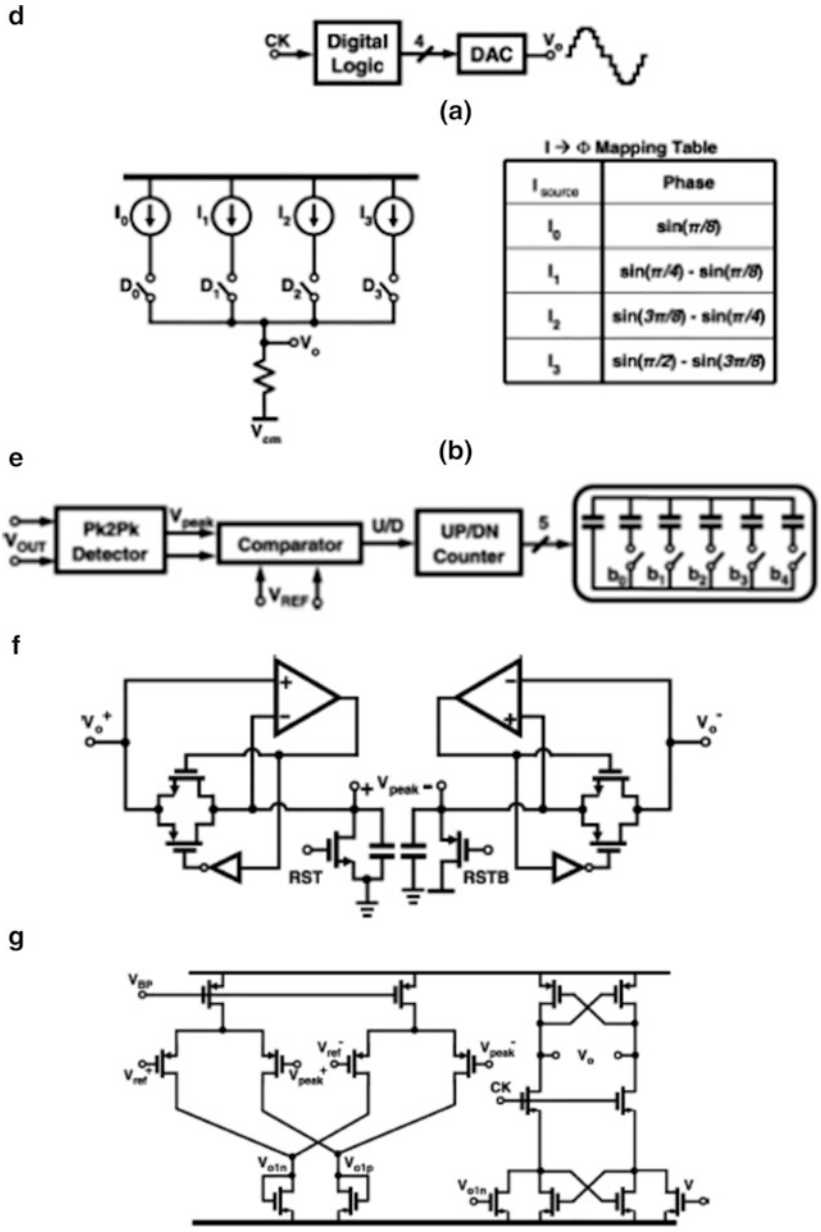


Fig. 5.67 (continued)

The mismatch detection circuit is presented in Fig. 5.67e. The peak filter output is detected by a peak detector and is compared with the reference peak voltage. The error signal of the comparator is integrated by a counter and then used to drive the capacitor

bank C_1. The peak detector is shown in Fig. 5.67f. The output capacitors are charged to V_o when the comparator determines $V_o > V_{peak}$. As long as the input remains less than V_{peak}, the comparator output is low thus switching off the transmission gate (TG). Once the input goes above V_{peak}, TG turns on and the new peak voltage is updated on the capacitor. A differential difference comparator shown in Fig. 5.67g compares $(V_{peak+} - V_{peak-})$ with $(V_{ref+} - V_{ref-})$ and provides a 1-bit error signal.

Sumesaglam and Karsilayan [5.57] have described a digital approach for tuning CT high Q filters. The authors use the phase response of a second-order block rather than magnitude for tuning so that the Q-tuning and center frequency tuning are independent of gain. This technique is based on the observation that at ω_a and ω_b, the phase of the band-pass output is $-45°$ and $-135°$. For digital implementation, the measurement frequencies ω_a and ω_b are discretized as $(N - 1)\omega_i$ and $(N + 1)\omega_i$ where N is an integer and the center frequency is $N\omega_i$. The frequency ω_i can be obtained from a reference frequency ω_R such that $\omega_i = \omega_R/M$. The parasitic poles exist, however, in second-order filters due to various parasitic capacitances, output resistances of transconductors, and the excess phase of the g_ms. Denoting the nonideal transfer function as $H'(s)_{LP}$, we have

$$|H'(j\omega)|_{LP} = \alpha(R(\omega) + jI(\omega)) \tag{5.39}$$

Hence, $|\phi'((N-1)\,\omega_i)| = -45°$ and $|\phi'((N+1)\,\omega_i)| = -135°$ need to be solved where $\phi = \tan^{-1}\left(\frac{I(\omega)}{R(\omega)}\right)$. It is also possible to choose the tuning frequencies taking into account the estimated value of the parasitic pole position for high-frequency filters. The tuning frequencies will then be $N_1\omega_i$ and $N_2\omega_i$.

The complete tuning system based on the above principles is shown in Fig. 5.68a. If Q_{od} and ω_{od} are the desired pole-Q and pole-frequency, then we have

$$N = 2\,Q_d\,,\ M = 2\,Q_d\,\frac{\omega_R}{\omega_{od}} \tag{5.40}$$

Note that the input frequency of the filter is switched between $(N - 1)\omega_R/M$ and $(N + 1)\omega_R/M$ using the MUX control. The signals V_{45} and V_{135} are delayed clocks whereas V_o is a clock signal without delay. V_F and V_Q are the control voltages for changing the frequency and Q, respectively.

The filter is calibrated when the "Tune" signal is high. Normal operation is resumed when the "Tune" signal is low. The two reference frequencies ω_1 and ω_2 are changed periodically. When ω_1 is applied, the phase of the low-pass output is compared with $-45°$. The phase detection is carried out using a D flip-flop (see Fig. 5.68b). The low-pass output is given to clock input and reference is applied to the D input. If the delay is more than 45°, the flip-flop stores high. The output of the flip-flop updates the U/D counter when the Tune signal is high. Note that V_F and V_Q do not change simultaneously. The DAC is needed only in the case of analog tuning being used for tuning the filter.

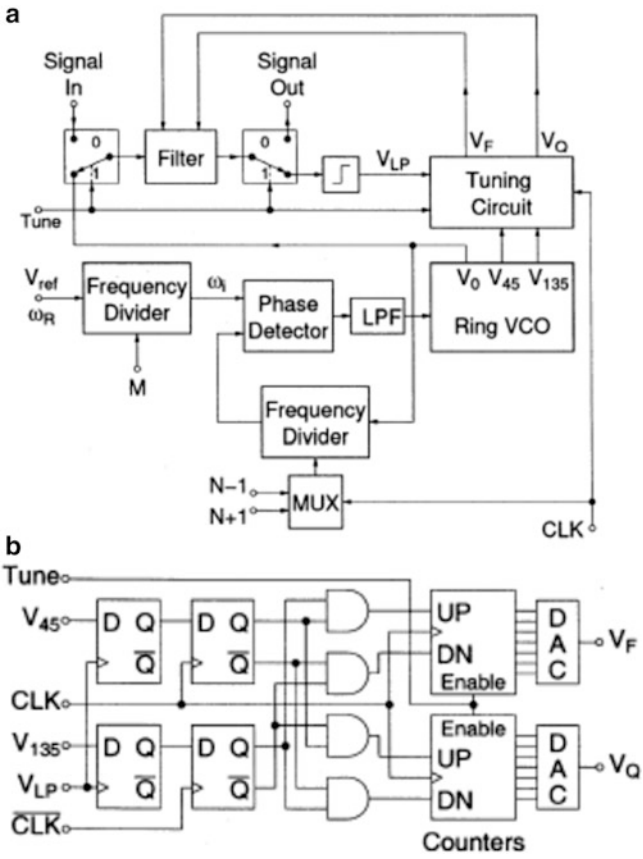


Fig. 5.68 (**a**) Complete tuning system, and (**b**) timing circuit (Adapted from [5.57] ©IEEE 2003)

5.14 SC Filters Using Comparators

Comparator-based SC (CBSC) circuits have been proposed for scaled CMOS technologies [5.58]. In these, a comparator and current source replace the opamp. The circuits using opamps can thus be easily adapted to realize CBSC circuits. In an opamp circuit, the opamp forces a virtual ground whereas in CBSC circuits, a comparator detects the virtual ground during the charge transfer process and triggers sampling. The operation of a CSBC amplifier is considered next to illustrate these ideas. The operation of this circuit is in three phases. In a small duration preset phase I, as shown in Fig. 5.69a, by connecting the capacitor C_1 to ground using switch P, the voltage V_x goes to V_{xo}, a voltage below V_{cm}. In the coarse charge transfer phase E_1, the circuit is as shown in Fig. 5.69b. This phase is used to get a rough estimate of the output voltage. Due to the finite delay of the comparator and high output ramp rate, the output will overshoot the final value V_o. The comparator output switches the

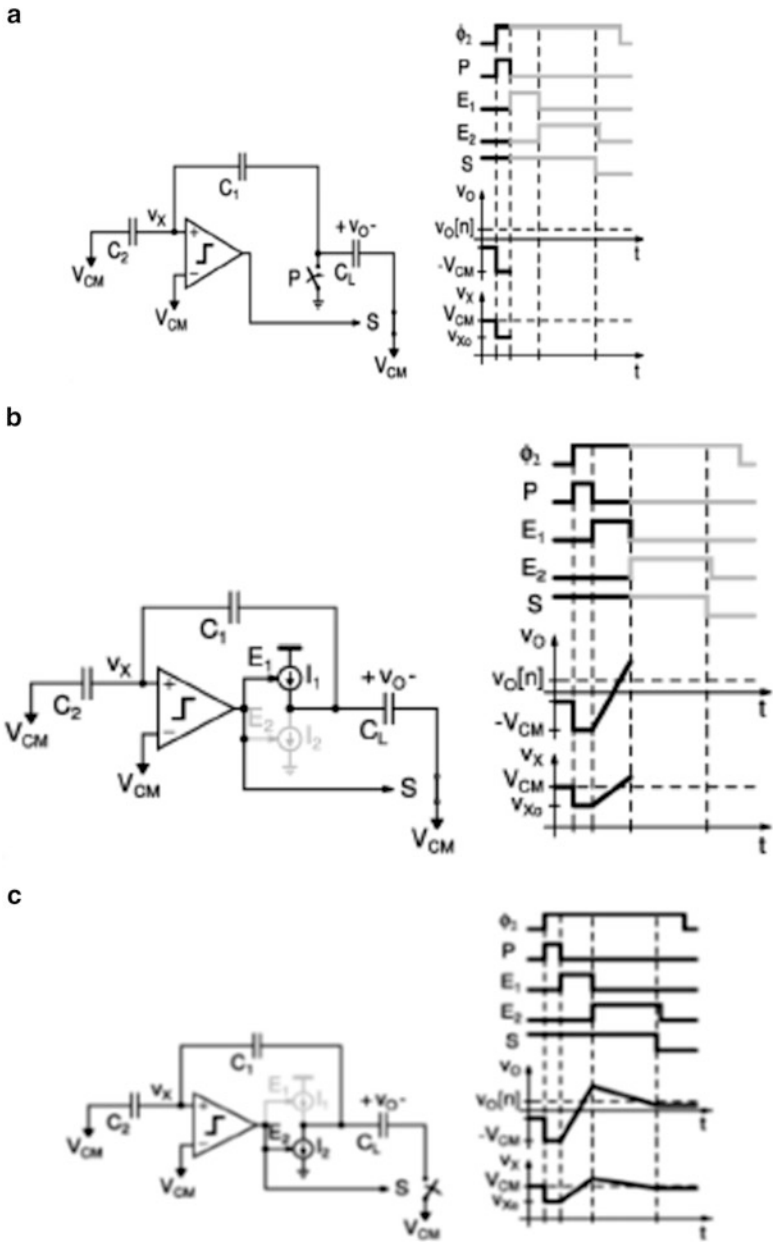


Fig. 5.69 CBSC amplifier: (**a**) preset phase configuration, (**b**) coarse charge transfer phase configuration (E1), (**c**) fine transfer phase configuration (E2), (**d**) overshoot cancellation technique with waveforms, (**e**) a two-stage 1.5-bit/stage CBSC pipe-lined ADC, and (**f**) threshold detection comparator preceded by band-limiting preamplifier (Adapted from [5.58] 2006)

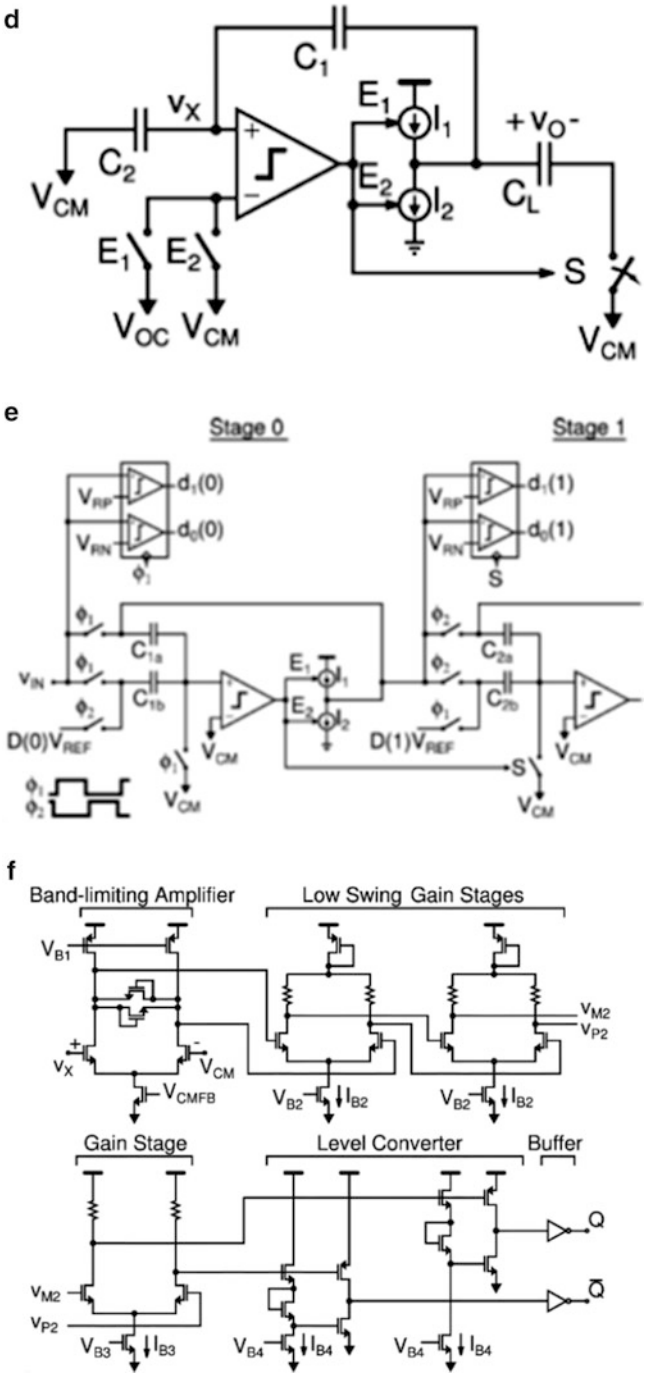


Fig. 5.69 (continued)

current source I_1 in this phase. In the fine transfer phase, E_2 (see Fig. 5.69c), the current sink I_2 is switched on. Note that $I_2 < I_1$. When the output of the comparator reaches the threshold crossing, I_2 is switched off after the sampling switch S opens. The output V_o will be the desired value. Note that the fine transfer time is large. The coarse transfer phase uses a large current to charge the output capacitance. The overshoot value can be reduced by having a modified circuit as shown in Fig. 5.69d. Note that the voltage V_{oc} is a reference voltage that is lower than V_{cm}. The overshoot and voltage drop across the switches cause nonlinearity and can create offset. It can be shown that the noise of the CBSC circuit is dominated by the threshold detection comparator. The input referred noise can be reduced by using a band-limited preamplifier.

Florenza et al. [5.58] have described a 1.5-bit/stage CBSC pipeline ADC comprising two stages as shown in Fig. 5.69e. The threshold detection amplifier is

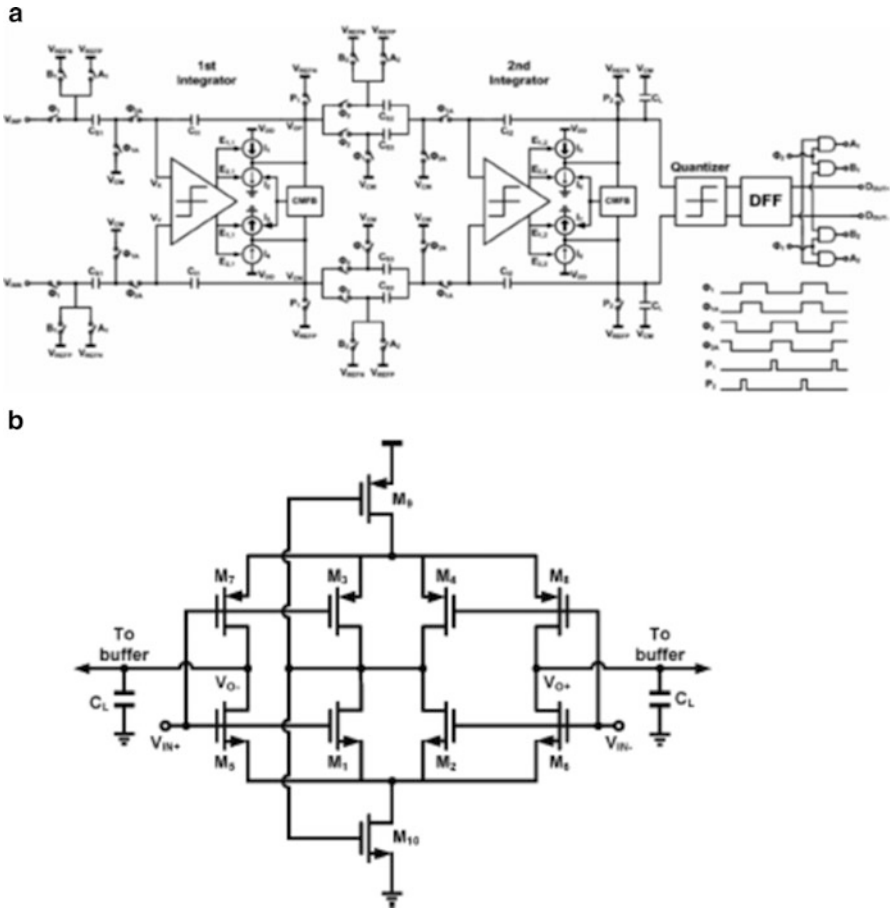


Fig. 5.70 (**a**) Fully differential second-order Σ-Δ modulator, (**b**) preamplifier of the threshold detection comparator, and (**c**) ramp generator with a CMFB circuit (Adapted from [5.59] ©IEEE 2009)

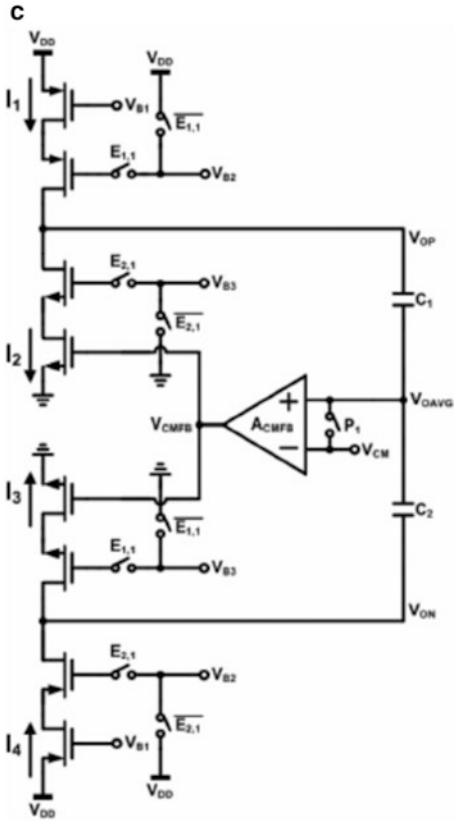


Fig. 5.70 (continued)

shown in Fig. 5.69f where several low swing gain stages are employed following a bandlimiting preamplifier. The bandlimiting amplifier output is limited by two diode-connected transistors for faster recovery. The last gain stage drives two level converters whose output is buffered using CMOS inverters.

Huang and Liu [5.59] realized the preamplifier as shown in Fig. 5.70b using a self-biased differential amplifier [5.60]. It consists of a replica input stage M_1–M_4 to serve as the self-biased CMFB circuit. The ramp generator is shown in Fig. 5.70c. Note that I_1 and I_3 are coarse current sources and I_2 and I_4 are fine current sources. The pull-up current sources are fixed whereas the pull-down current sources are controlled by the CMFB circuit. The CMFB circuit adjusts the pull-down current sources to match the pull-up ones. In Phase P_1, the charges on capacitors C_1 and C_2 are reset. These capacitors sense the differential outputs V_{OP} and V_{ON}. If the two fine or coarse current sources have different magnitudes, the difference between V_{OAVG} and V_{CM} is amplified by A_{CMFB} to adjust the current sources. The effective open loop gain of the CMFB circuit is $C_T R_o/(\beta t_d)$ where β is the feedback factor where C_T is the total capacitance at the output of the stage, R_o is the output resistance

of *the current source*, t_D is the delay of the threshold detection comparator. The large R_o is obtained by using cascode devices.

White et al. [5.61] studied the errors in CBSC-based biquads. They note that the average overshoot voltage produces offset voltage. The comparator delay varies with the ramp rate. The total variation in overshoot voltage is dominated by the finite output resistance of the charging current sources. For high sampling frequencies, the magnitude and phase errors are approximately t_D/RC, where t_D is comparator delay. The CBSC errors are equivalent to those of SC integrators when $A = (RC/t_D)\ (1/f)$. The reader is referred to [5.61] for a detailed analysis of the CBSC-based integrators and biquads.

5.15 Sigma-Delta Modulators

A pseudo differential version of the inverter-based SC integrator [5.62] is shown in Fig. 5.71 which circumvents the need for a CMFB circuit. This does not limit the output swing of the integrator. Note that CMFB capacitors CM are discharged to ground during φ_1 and form a CM detector in φ_2. The difference between the CMFB detector output and signal ground is fed to the integrator. The CMFB loop gain is C_M/C_I. The capacitor C_M does not load the Δ-Σ modulator. The circuit is immune to offset mismatch as well.

When $V_{DD} = V_{Tn} + V_{Tp}$, the *power settling time product* (product of average power consumption per switching event and setting time) is optimal. During φ_1 and φ_2, the devices M_1 and M_2 go through weak and strong inversion regions. The operation in class C is preferred over class AB since the slew rate, power efficiency, and the common mode input range are superior and the circuit needs low

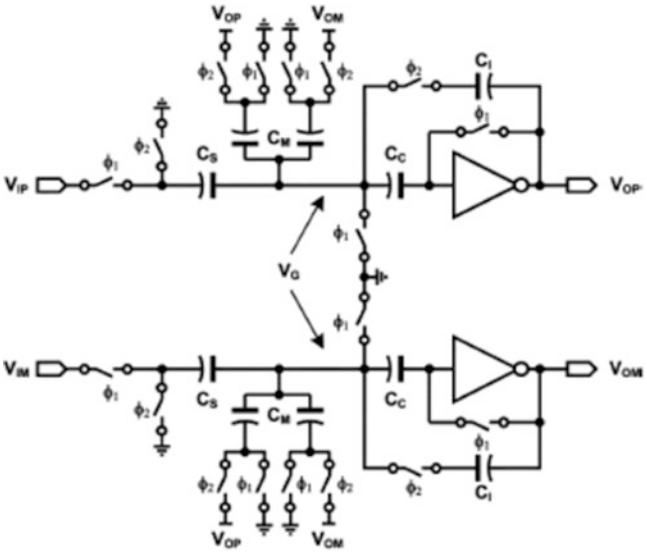


Fig. 5.71 Psudo-differential inveter based SC integrator (Adapted from [5.62] ©IEEE 2009)

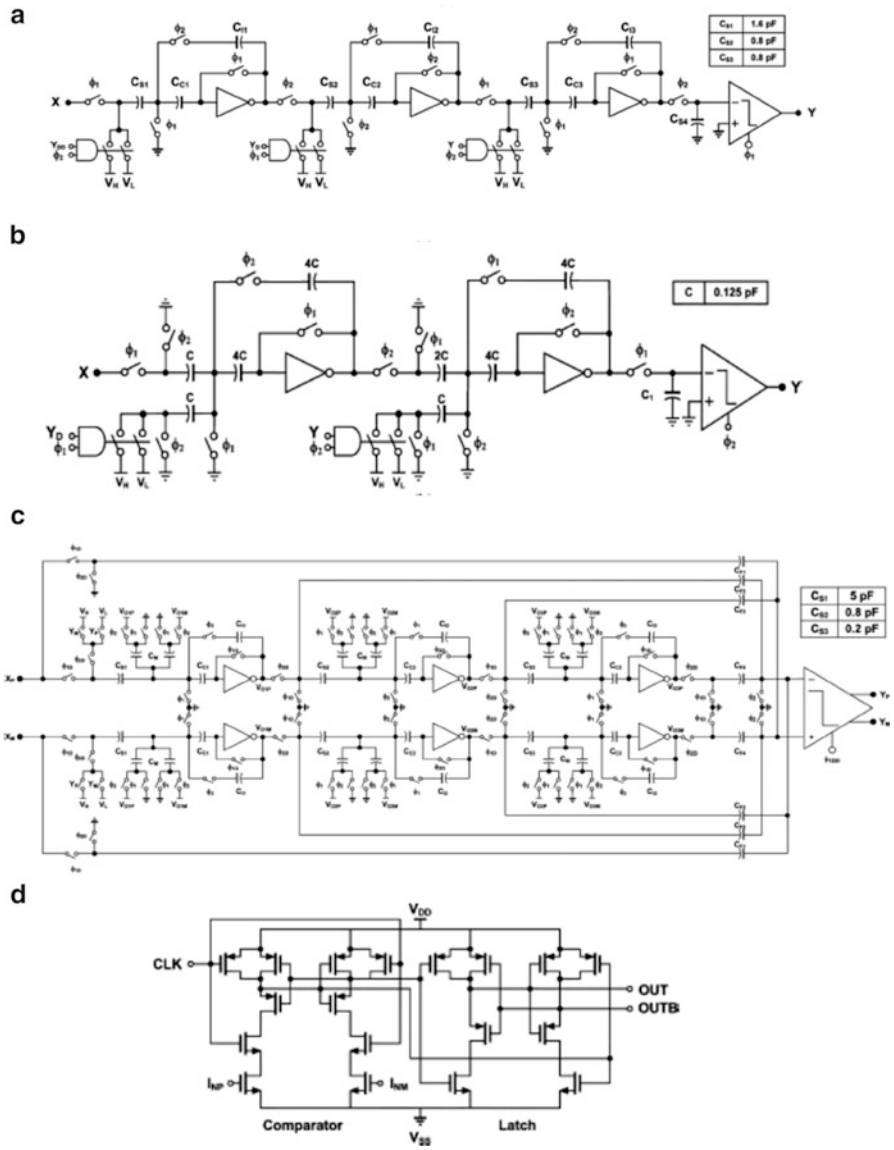


Fig. 5.72 Sigma-delta modulators using inverters: (**a**) modulator I (**b**) modulator II, (**c**) modulator III, and (d) schematic of the quantizer (Adapted from [5.62] ©IEEE 2009)

supply voltages. The thermal noise of such integrators is lower than SC integrators using OTA.

Chae and Han [5.62] described three sigma-delta modulators shown in Fig. 5.72a–c using inverter-based integrators. The quantizer is shown in Fig. 5.72d. The first Σ-Δ modulator (see Fig. 5.72a) is 1-bit second-order and uses single loop. The second Σ-Δ modulator (see Fig. 5.72b) is third-order single loop and uses class AB

operation for the inverters ($V_{Tn} + V_{Tp} < V_{DD}$). The third using feedforward topology is a third-order sigma-delta modulator and uses pseudo differential configuration. The reader is referred to [5.62] for more design information.

Pavan and Sankar [5.63] described a third-order CT Σ-Δ modulator using the architecture of Fig. 5.73a. The objective was to achieve low distortion and low power consumption. The Σ-Δ modulator uses an active filter using CIFF (cascade of integrators with feedforward). It has a direct path to the input of the comparator via R_D. A 1-bit A/D converter is employed. The DAC is realized using the SCR technique as shown in Fig. 5.73c. The first integrator with the DAC output summation is shown in Fig. 5.73b. Note that in the φ_2 phase, the capacitor is charged to the input and in the φ_1 phase, an exponentially decaying pulse is produced as shown in Fig. 5.73d with a time constant defined by C_D and R_D. The R_D used was 18 KΩ and the switches have resistance of 4.5 KΩ and $C_D = 1.1$ pF. The first integrator uses the assisted-opamp technique in order to have adequate linearity and reduced power dissipation. As explained before, the virtual ground is created by the feedback of the assistant current as described earlier in Sect. 5.5 (see Fig. 5.17). The noise introduced by the DAC due to clock jitter is proportional to the discharging current $I_1 = \left(\frac{V_{ref}}{R_D}\right) e^{-\frac{T}{2\tau}}$ where $\tau = C_D R_D$ and can be reduced by choosing a small τ but it increases the peak current thereby imposing more stringent conditions on the linearity of the integrator. The large value of resistor R_x is needed to realize the notch frequency and is realized by the T network (using R_x, R_{x1}, and R_{x2}; see Fig. 5.73a). The opamp shown in Fig. 5.73e is feedforward compensated with p channel input devices to reduce noise. M_5 and M_6 provide CM feedback for the first stage. M_1–M_4 have a long channel to reduce the input referred noise. The CMFB is realized using transistors to detect the common mode voltage. This is better than using resistors which will degrade the gain of the amplifier and furthermore, it saves area. The second stage of the opamp is formed by transistors M_7–M_{10} which uses a local CMFB using a resistor-based CM detector.

The comparator used together with the waveforms is shown in Fig. 5.73f. When LC is high, the inverters formed by M_1, M_2, M_3, and M_4 are disabled and the differential input is sampled on nodes X and Y. After LC falls, the regeneration begins when L goes high. The decision of the latch is sampled by two clocked CMOS inverters. The assistant transconductor is a class AB design consisting of complimentary common gate stages M_2 and M_6 (see Fig. 5.37g).

The exponentially decaying pulse generator [5.64] needed for the assistant DAC is shown in Fig. 5.73h. During Φ_1, the capacitor is charged to V_{high}. In Φ_2, it is discharged to $V_{low} = V_{Tn}$ through a resistor R. The gate voltage of M_1 is an exponentially decaying pulse with a time constant $\tau = RC$.

Chae et al. [5.65] described a Σ-Δ architecture for a 2.1-M pixel, 120-frames/s CMOS image sensor. The architecture is presented in Fig. 5.74a. The image sensor consists of a pixel array, column-parallel Σ-Δ ADCs, buffer memory, scanning circuits, and bias circuits. The pixel output is fed to a Σ-Δ ADC for conversion with correlated double sampling for offset cancellation. The Σ-Δ ADC is followed by a digital decimation filter. The 14-bit output of the decimation filter is transferred to a buffer memory.

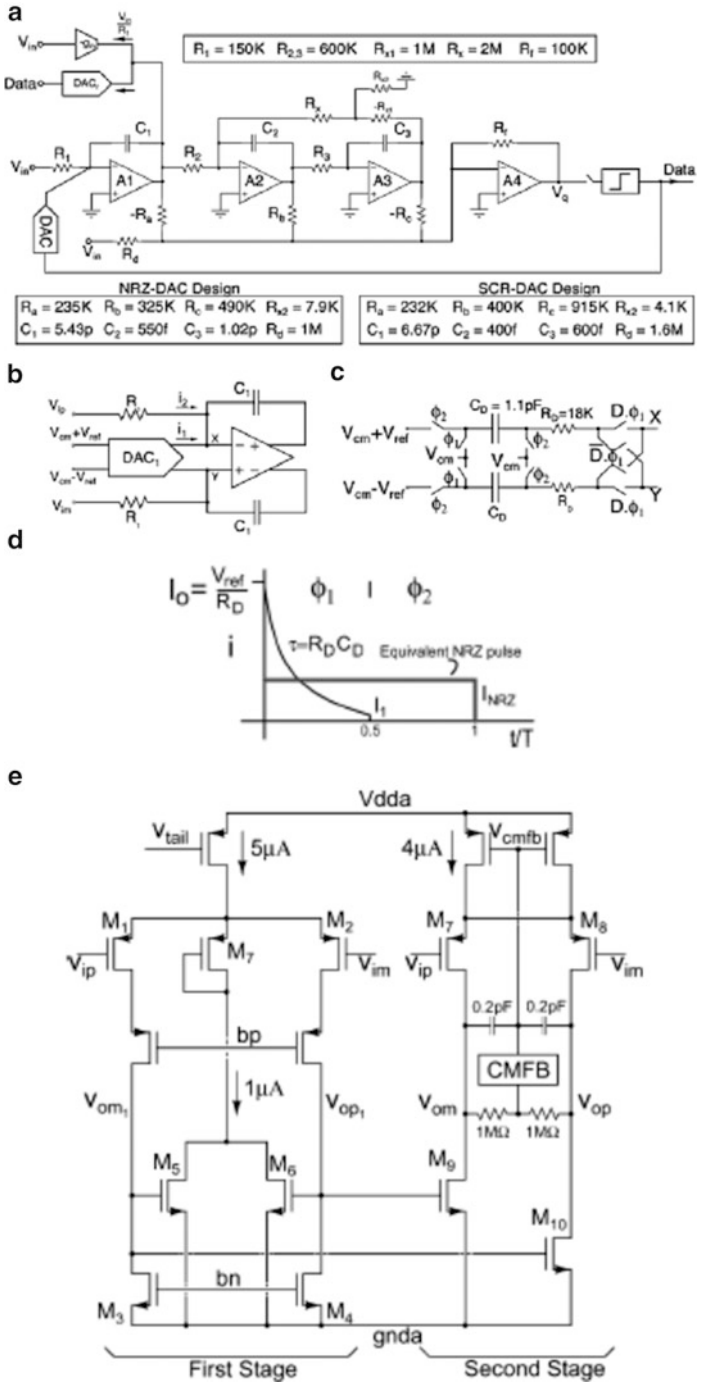


Fig. 5.73 (**a**) Σ-Δ modulator architecture, (**b**) schematic of first integrator, (**c**) schematic of differential SCR DAC, (**d**) exponentially decaying pulse produced by the DAC, (**e**) operational amplifier used in the first integrator, (**f**) schematic of comparator together with switching waveforms, (**g**) transconductor used in the assistant, and (**h**) exponentially decaying pulse generator (Adapted from [5.63] ©IEEE 2010)

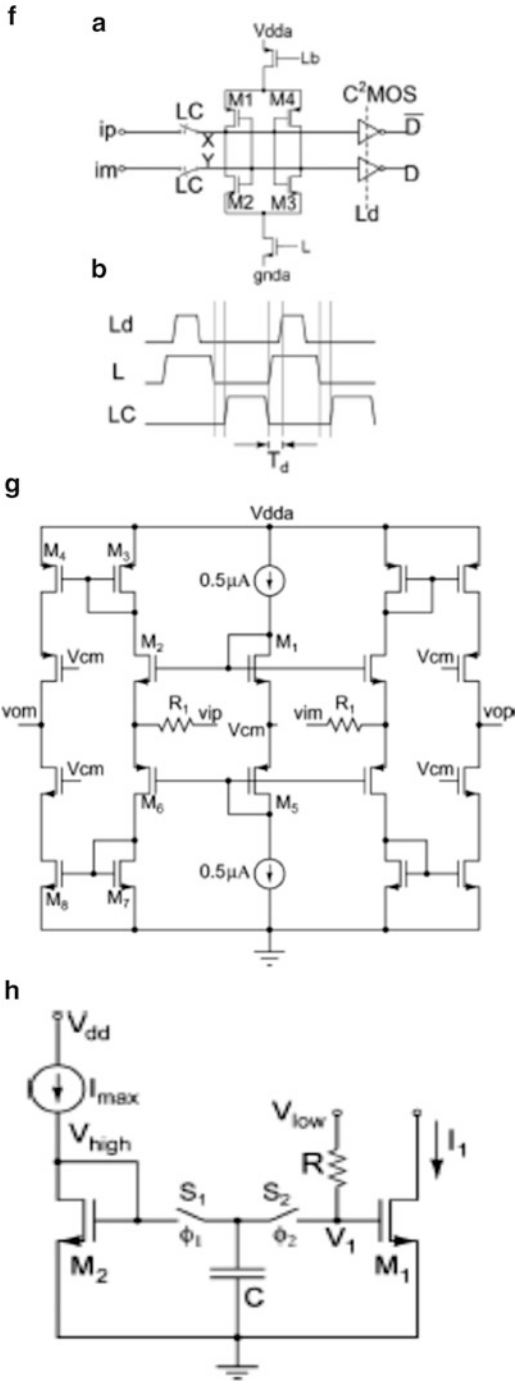


Fig. 5.73 (continued)

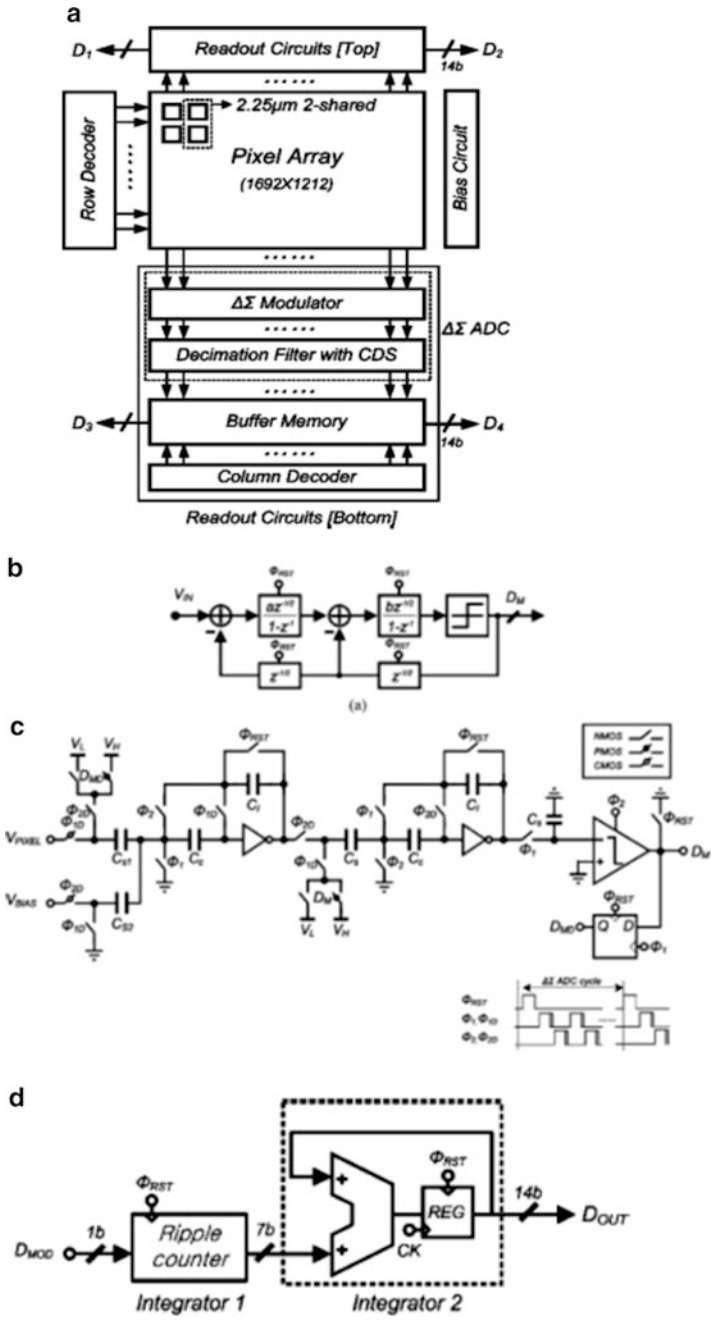


Fig. 5.74 (**a**) Block diagram of CMOS image sensor, (**b**) block diagram of second-order sigma-delta modulator, (**c**) SC implementation of (**b**), (**d**) cascaded integrator, and (**e**) decimation filter (Adapted from [5.65] ©IEEE 2011)

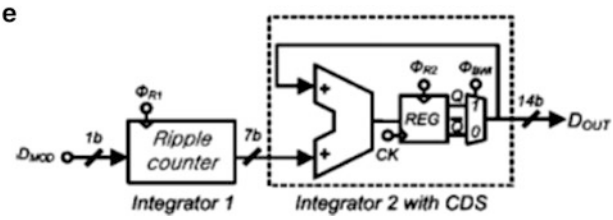


Fig. 5.74 (continued)

The two-loop sigma-delta modulator uses a scheme of Fig. 5.74b and its SC implementation is shown in Fig. 5.74c using inverters in place of opamps to conserve power and area as described earlier. This uses the well-known offset compensation techniques described in Chap. 4. The offset is sampled on C_C and C_S with input connected in Phase Φ_1, and in Φ_2 the charge on C_S is transferred to C_I and the offset is cancelled by subtraction of the offset stored on C_C in Φ_1. This technique reduces the noise of the inverter as well. The input capacitor of the first integrator in the Σ-Δ modulator is split in two: one for connecting the input and another to provide a dc offset to compensate the dc offset of the pixel which is 2 V. Before every conversion cycle, the Σ-Δ modulator capacitors are reset (discharged) and then the conversion starts.

The decimation filter is made up of a second-order cascaded integrator (see Fig. 5.74d). The input V_{Pixel} is constant. Thus that fact can be taken into account in simplifying the design of the decimator. It can be shown that the output of the decimator can be expressed as

$$D_o(z) = \frac{Y(z)}{(1-z^{-1})^2} = \frac{z^{-1}}{(1-z^{-1})^2}X(z) + E(z) \tag{5.41a}$$

Since x is constant, it follows that

$$D(out(n))) = \frac{n(n+1)}{2} + E(n) \tag{5.41b}$$

After n clock cycles, in order for the quantization error to be less than half LSB, the required number of cycles of the incremental Σ-Δ converter can be computed. For a 12-bit resolution, 95 clock cycles are required. Due to the possible inaccuracy of integrator coefficients, the authors use 110 clock cycles. Note that in the cascaded integrator shown in Fig. 5.74d, the first block is a simple counter since the input is 1 bit. The second stage, however, is an accumulator. The offset cancellation is achieved by a simple modification of the circuit of Fig. 5.74d as shown in Fig. 5.74e wherein two steps are needed. In the first step, with zero input, after resetting the register, D_{out} is computed by operating the Σ-Δ converter for 110 clock cycles. This value is saved in the register and in the second actual conversion takes place with input D_{SIG} present for another 110 cycles.

The IC fabricated in a 0.13 μm process caters for a pixel array of 12.1 M pixels with each pixel size of 2.25 μm × 2.25 μm. The rows and columns are 1,696 × 1,212. The FOM used for such devices which represents energy efficiency of an image sensor is

$$FOM = \frac{Power.noise}{\#of\ pixels.Framerate}\ 10^9\ (e^-\ nj) \tag{5.42}$$

For the proposed converter, it is 1.70.

A fifth-order CT sigma-delta modulator using single-opamp resonators has been presented by Matsukawa et al. [5.66]. The architecture of this chip is shown in Fig. 5.75a. It uses a 3-bit quantizer (flash ADC). Two second-order filters and one first-order filter are used. The use of SAB for the resonator reduces the power consumption and area. The single opamp resonator is derived from a twin-T based active RC filter systematically so that the numerator can be of universal type with each coefficient controllable independently. The Σ-Δ converter also uses a feedforward path. In order to increase the speed, the current summation is done at the virtual ground of the first-order filter.

The ringing relaxation filter shown in Fig. 5.75b suppresses the ringing of the integrator due to the phase compensation resistor. Note that the ringing relaxation filter is basically an integrator with compensation using series resistor R_z. The addition of current steering DAC causes ringing, which is suppressed by splitting the integrator capacitor into two C_b and C_{int} to bypass the high-frequency components.

The opamp used in this design is presented in Fig. 5.75c which is a single-stage telescopic configuration and includes CMFB. The excess loop delay of the Σ-Δ modulator is compensated using a second feedback path using DAC2. The opamp-less adder is elaborated in Fig. 5.75d which sums three signals with attenuation. The adder also is passive-type in order to avoid problems of finite opamp bandwidth in the case of an active adder.

5.16 LC Filters

Vallese et al. [5.67] described the design of an integrated notch filter for rejection of interference in UWB systems. The ultra wide-band communication is used for short range communication at data rates up to 480 Mb/s using multi-band OFDM format. The frequency band 3.1–10.6 GHz is divided into fourteen 528-MHz wide bands. These are grouped into four groups. Three groups contain three bands each whereas the last group contains two bands. There are several other systems such as wireless LANs in the 5–6-GHz band. In this case, the second band group is dropped. On the other hand, Bluetooth and IEEE 802.11b/g systems operate in the 2.4–2.5 GHz band. WiMAX operates in the 2.5–2.9 GHz, 3.4–3.6 GHz, and 5.2–5.9 GHz bands.

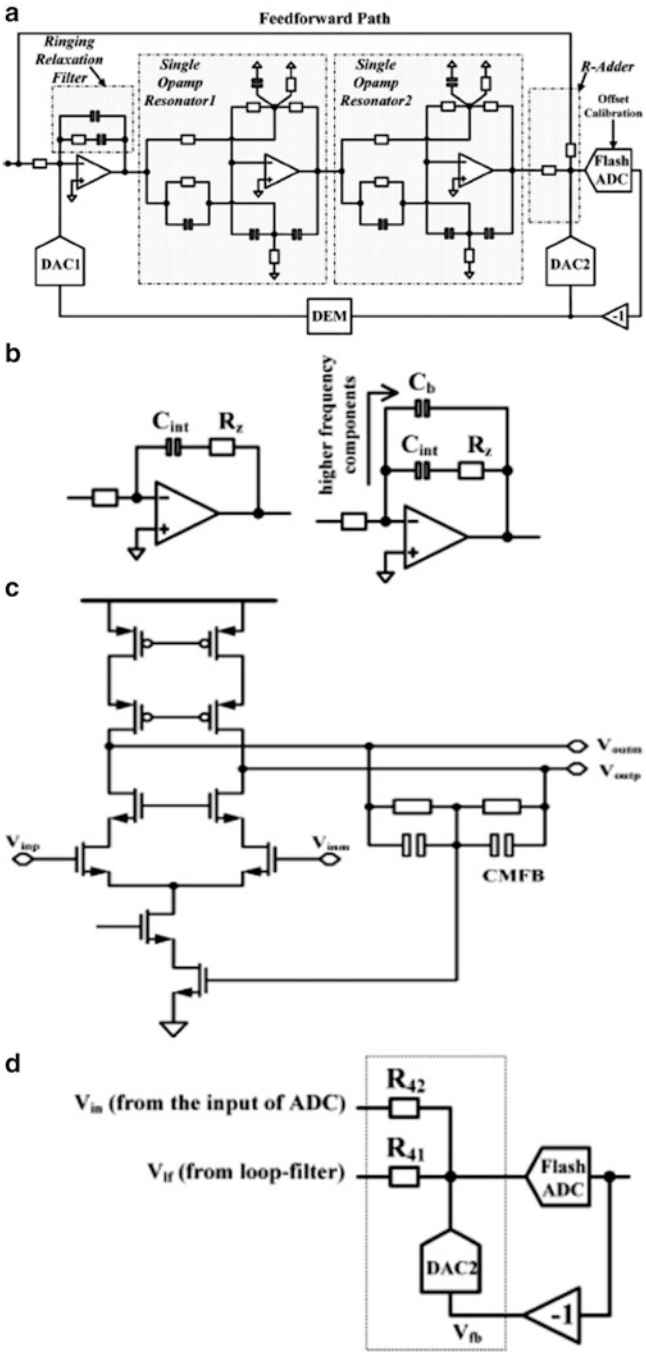


Fig. 5.75 (**a**) Schematic of fifth-order CT Σ-Δ ADC, (**b**) integrators with compensation resistor, (**c**) single-stage telescopic opamp with continuous-time CMFB, and (**d**) opamp-less resistor adder (Adapted from [5.66] ©IEEE 2010)

Cell phones utilize the 0.9–1.9 GHz frequency band. Thus, all these other systems are "blockers" for UWB systems. Interference from other bands can cause suppression of receiver gain and also intermodulation products due to other systems may fall in the UWB band. The hardest blockers are from WiMAX in the 3.6–3.9 GHz and those in the 5–6 GHz band. Vallese et al. [5.67] consider operation in the 3.1–4.8-GHz band (also denoted as Mode1). They have implemented the architecture of Fig. 5.76a shown comprising LNA, a notch filter, and a buffer in the first version. The second version comprises a double-balanced mixer and additional buffers. The basic circuit of the LC notch filter is shown in Fig. 5.76b and the equivalent circuit is shown in Fig. 5.76c. The basic notch filter configuration is based on series resonance of a reactive network working in the current mode. At the notch frequency, the drain current of the transistor is diverted away from the signal path so that a notch appears in the current transfer function. The capacitance C_p is due to parasitics. The circuit exhibits parallel resonance at a frequency higher than the notch frequency (see Fig. 5.76d). Thus the rolloff of the notch is steeper at the high-frequency side. An alternative topology shown in Fig. 5.76e has two series resonances and thus introduces an additional notch at a higher frequency and makes it possible to realize a flatter pass-band (see Fig. 5.76f). In the presence of parasitic resistances of the inductors (see Fig. 5.76g), the response deteriorates to that shown in Fig. 5.76h. The parasitic resistances can be compensated by using a negative resistance R_N (see Fig. 5.76g). The value of R_N is chosen to compensate the loss at the higher notch frequency. The authors describe a detailed optimization procedure for choosing the values of inductors, capacitors, and negative resistance so as to minimize the power dissipation and area as well.

Since the blocker frequency may not be at a fixed frequency, a tuning procedure will be required for which varactors can be used as shown in the complete circuit in Fig. 5.76i in which case continuous tuning can be done. Alternatively, programmable capacitor arrays can be used. In the latter case, discrete tuning steps are required. The tuning for the desired frequency band can be carried out by measuring the V_x/I_D through the received signal strength indicator (RSSI) since V_x/I_D is a band-pass transfer function and can be set to maximum by tuning the capacitor array. This guarantees that notch is realized at the blocker frequency. Note that changing C_2 also necessitates changing R_N. In order to facilitate this, the authors suggest a calibration procedure wherein the circuit can be configured as an oscillator as shown in Fig. 5.76j. The complete notch filter circuit in both cases is presented in Fig. 5.76i, j wherein a fully differential structure is used. Note that tightly coupled coils are used to realize the inductance L_1 whereas a symmetric coil is used to realize the inductance L_2. Note that the cross-coupled transistors M_5 and M_6 realize a negative resistance. The switches A are used to ground the input when the filter is turned off to avoid spurious resonances. In the second configuration shown in Fig. 5.76j, the switches are connected to V_{DD}. The switches S_R and capacitors C_R (which are a replica of C_1) are used for calibration by connecting the circuit as an oscillator. The resulting binary words controlling the capacitor array are stored for later use when configured as a notch filter for the chosen blocker frequency.

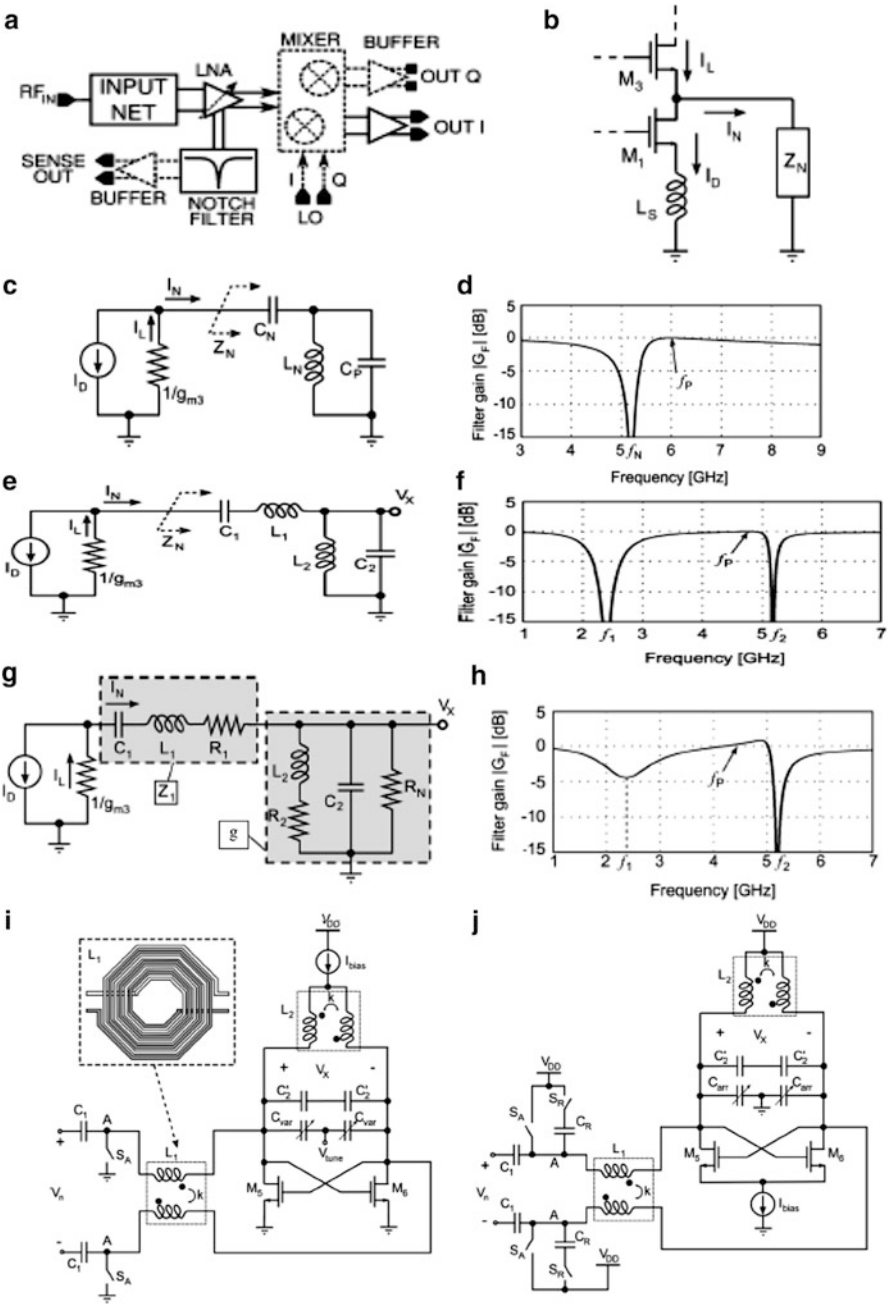


Fig. 5.76 (**a**) Block diagram of a UWB receiver, (**b**) schematic of a notch filter, (**c**) equivalent of (**b**), (**d**) frequency response of (**c**), (**e**) double-inductor notch filter, (**f**) frequency response of (**e**), (**g**) nonidealities in (**e**), (**h**) frequency response of circuit in (**e**), (**i**) schematic of notch filter version 1, and (**j**) version 2 (Adapted from [5.67] ©IEEE 2009)

Pirola et al. [5.68] extended the in-band noise shaping approach of Tekin et al. [5.15] discussed earlier to realize a WCDMA channel filter for current mode applications. They denote such filters as PIPE filters which pass signal in the pass-band and noise in the stop band. In the pass-band, the output current equals the input current whereas in the stop-band both noise and distortion components enter the pipe and reach the output. A first-order pipe filter is conceptually illustrated in Fig. 5.77a. It can be noted that the input current I_{in} leaves through the drain of the transistor whereas the noise of the MOS transistor is high-pass filtered at the I_{out} terminal as shown in the frequency response of signal and noise in Fig. 5.77a. At low frequencies, when the capacitor is an open circuit, the noise current of the transistor is forced to recirculate whereas at high frequencies, it reaches the output. The noise output can be expressed as

$$Noise_{out}(\omega) = 4kT\gamma G_m \frac{\left(\frac{\omega}{\omega_p}\right)^2}{1+\left(\frac{\omega}{\omega_p}\right)^2} + \frac{4kT\gamma}{G_m R_s^2} \frac{1}{1+\left(\frac{\omega}{\omega_p}\right)^2} \tag{5.43}$$

Note that the second term is due to the source resistance and is not high-pass filtered.

The circuit can be extended to realize a second-order filter by using the configuration of Fig. 5.77b. The realized second-order transfer function is given by

$$\frac{I_{out}}{I_{in}} = \frac{\frac{g_m^2}{C_1 C_2}}{s^2 + s\frac{g_m}{C_1} + \frac{g_m^2}{C_1 C_2}} \tag{5.44}$$

where g_m is the transconductance of M_1 and M_2. Note that the Q depends on the ratio of capacitors. The transistor M_1, inverter of gain -1 and C_2 realize an active inductor. The total noise due to the bias current sources and due to transistor M_1 and M_2 is shown in Fig. 5.77c. Note that the flicker noise is present at low frequencies. The noise of the bias generator also is important. Beyond the filter cut-off frequency, the noise of M_2 and upper current bias generator remain unfiltered. A fourth-order fully differential filter for WCDMA applications is shown in Fig. 5.77d. The cutoff frequency chosen was 2.8 MHz which is 1.45 times the channel bandwidth of 1.92 MHz. The blockers occur at 10 MHz and 20 MHz.

Dhanasekharan et al. [5.69] have described a fifth-order active-LC-Butterworth-type equalizing filter. The concept of the series resonator-based prototype is illustrated in Fig. 5.78a whose transistor implementation is as shown in Fig. 5.78b. The resistance R_s in Fig. 5.78a can be realized by the transistor M_1. Note that M_1 also helps to tap out the band-pass current output. The equalizer based on the Fig. 5.78b is presented in Fig. 5.78c whose transfer function can be derived as

$$I_o(s) = -\frac{V_{in}(sC + G_{m2})}{s^2 LC + s\frac{C}{G_{m1}} + 1} \tag{5.45}$$

Note that the additional transistor M_2 realizes the second term creating a real zero thus causing an increase in gain at the rate of 6 dB/octave at high frequencies. The equalizing zero needs to be placed two octaves ahead of the resonant frequency to achieve a 12-dB equalization gain. This means that $G_{m2}/C = \omega_o/4$ where $\omega_o = \frac{1}{\sqrt{LC}}$. The equalization gain can be programmed by scaling the band-pass current. R_L and C_L represent the *I*/*V* converter and load capacitor. These introduce a parasitic pole.

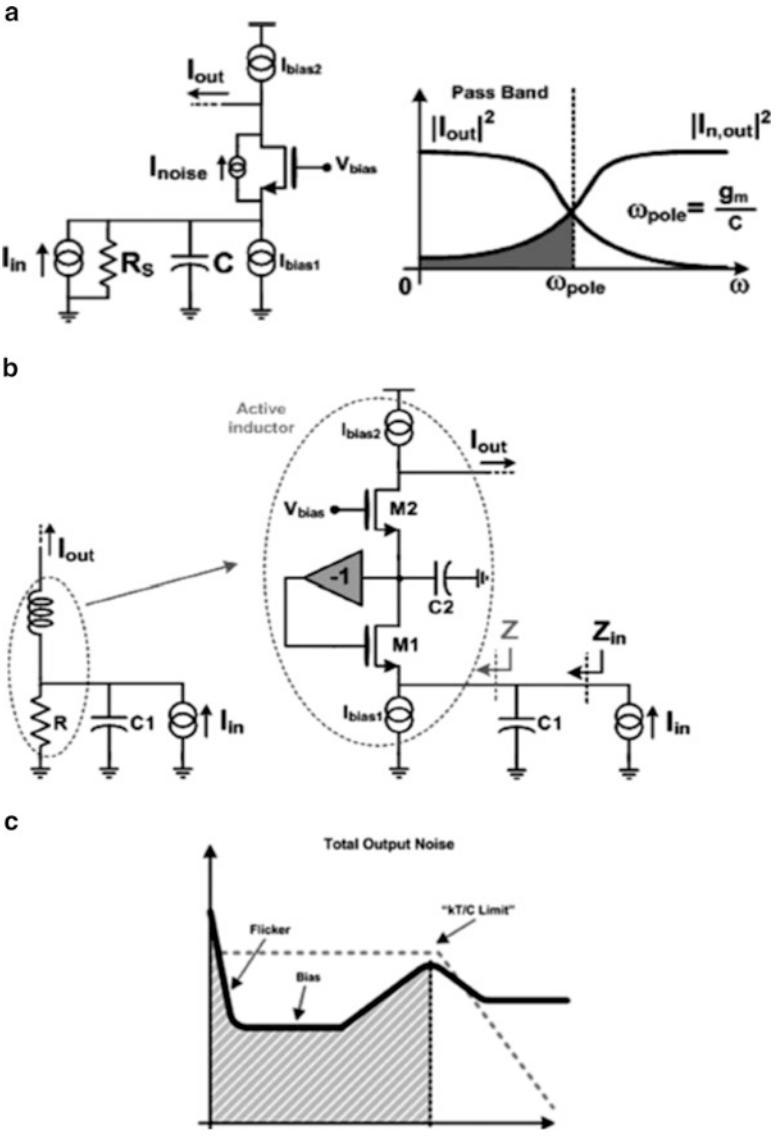


Fig. 5.77 (**a**) First-order LP pipe filter, (**b**) current biquad cell, (**c**) output noise of the biquad of (**b**), and (**d**) schematic of fourth-order filter (Adapted from [5.68] ©IEEE 2010)

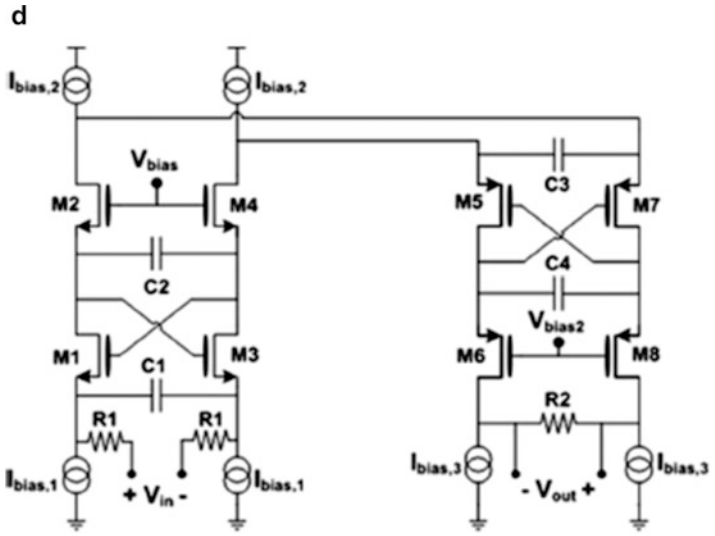


Fig. 5.77 (continued)

A fifth-order fully differential Butterworth filter realized using the biquad of Fig. 5.78c is presented in Fig. 5.78e which shows a single-ended version. For programmability of equalization gain, the current attenuators A_1 and A_2 are used which are controlled using V_B. The equalizer section is elaborated in Fig. 5.78d. The real pole of the first section is pushed to high frequency using the negative capacitor $-C_n$. The realized fifth-order filter transfer function is given as

$$H(s) = -\frac{(sC_1 + G_{m2})(sC_2 + G_{m4})}{\left(s^2\, L_1C_1 + s\frac{C_1}{G_{m1}} + 1\right)\left(s^2\, C_2L_2 + s\frac{C_2}{G_{m2}} + 1\right)(1 + s(C_3 - C_n)\,R_1)(1 + sC_4\,R_2)} \tag{5.46}$$

Note that for balanced implementation, the capacitor C is shared by both arms.

Frequency tuning can be performed by varactors using the voltage V_{tune}. The attenuators A_1 and A_2 are realized using a Gilbert cell formed by transistors M_g (see Fig. 5.78d). The current sources I_B are controlled by a CMFB loop shown in Fig. 5.78g. A CMFB bandwidth of 2.2 GHz is realized. The common mode voltage is sensed by R_2 and C_4. Note that additional common mode load resistance is also used to realize a low-frequency pole-zero pair. The error amplifier shown in Fig. 5.78h features high gain and the resistors R_5 and capacitor C_5 introduce a zero to cancel the pole of the split frequency current source formed by M_{15} and M'_{15}. Note that the dc transconductance of the current source is decided by M_{15} and M'_{15} whereas high-frequency behavior is decided by M_{15} alone. Combination of two paths through M_{15} and M'_{15} results in a pole zero pair in the transconductance of I_{B2}.

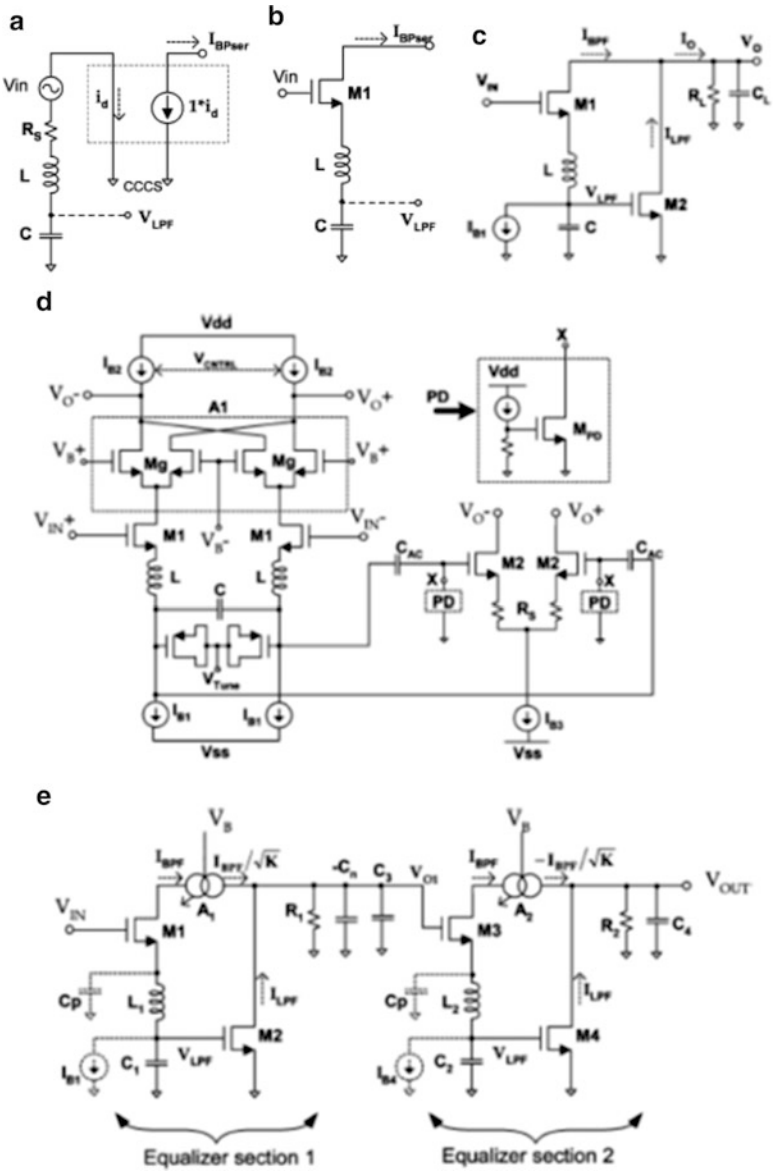


Fig. 5.78 (**a**) Series resonator prototype, (**b**) transistor implementation of (**a**), (**c**) series resonator LC-based equalizer section, (**d**) schematic of single-ended fifth-order Butterworth filter based on (**c**), (**e**) fully differential implementation of (**c**), (**f**) negative capacitance emulation circuit, (**g**) CMFB loop, and (**h**) error amplifier and split frequency current source (Adapted from [5.69] ©IEEE 2007)

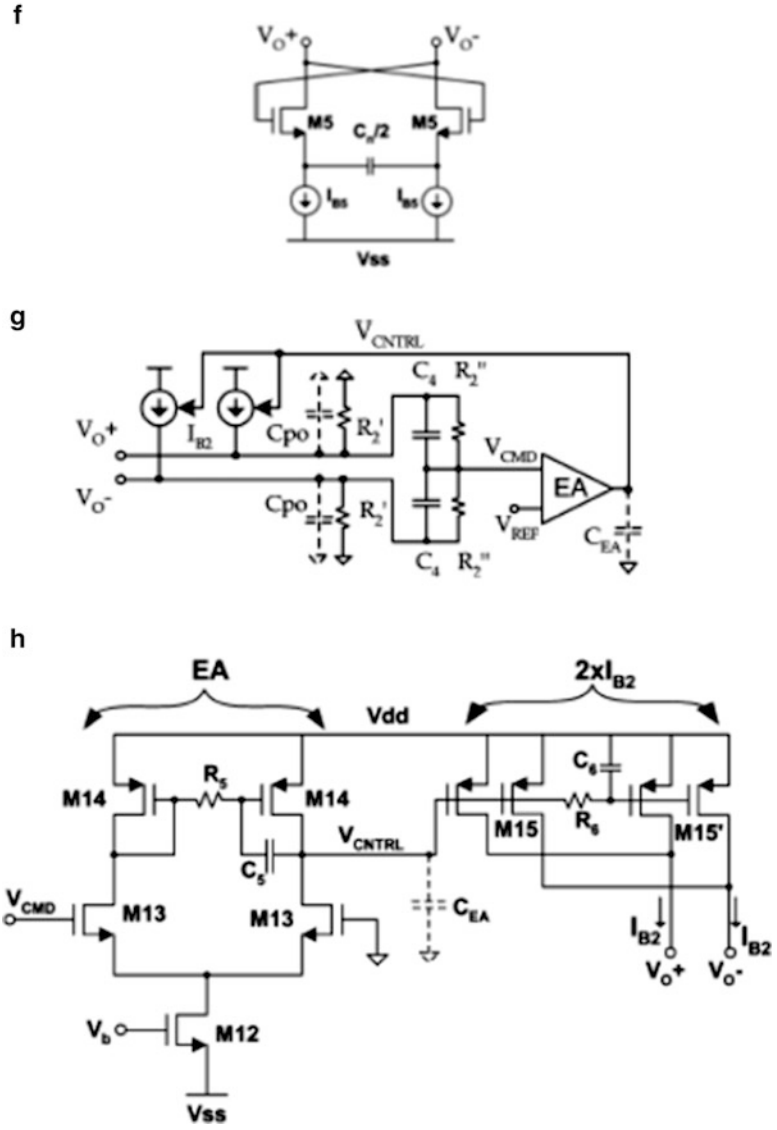


Fig. 5.78 (continued)

The differential pair M_2 realizes the low-pass path that is ac coupled to the resonator (see Fig. 5.78d). The ac coupling network is formed by C_{AC} and PD (pull-down resistor circuit; see inset of Fig. 5.78d) to realize a cutoff frequency of <100 KHz. The negative capacitance circuit is presented in Fig. 5.78f. The input admittance of this circuit can be found approximately as $-\frac{s C_n G_{m5}}{C_n + G_{m5}}$ which will behave like a negative capacitance for frequencies less than $\omega_{cn} = \frac{G_{m5}}{C_n}$.

5.17 Evaluation of CT Filters

CT filters can be compared using a figure of merit (FOM) [5.21, 5.70] defined as

$$FOM = \frac{P_C / N}{f_c \left(SFDR.N^{4/3}\right)} \tag{5.47}$$

where P_c is the power consumption of the filter, N is the number of poles and zeroes, f_c is the cutoff frequency, and SFDR.$N^{4/3}$ is the normalized spurious-free dynamic range with SFDR defined as

$$SFDR = \left(\frac{IIP_3}{P_N}\right)^{2/3} \tag{5.48a}$$

where P_N is the input referred noise power. In the case of SFDR in decibels, which is not given by the respective authors, it can be derived from I_{IP3} and noise data using the formula

$$SFDR_{dB} = \frac{2}{3}\left(IIP_{3,dbV} - P_{Noise,dbV}\right) \tag{5.48b}$$

where P_{noise} is RMS noise. The two-tone SFDR is the ratio of the input power to the power of the intermodulation products when the latter is equal to the noise power of the filter.

Note that some authors [5.7] have included area as well in the numerator of FOM expression in (5.47).

In Table 5.7 a comparison of several continuous-time filters [5.7, 5.9, 5.19, 5.21, 5.22, 5.25, 5.70, 5.71] and [5.72] is presented together with the intended application and various other aspects including FOM.

5.18 Problems

P.5.1. Derive the transfer function of the biquadratic cell of Fig. 5.23b taking into account g_{ds} of all the transistors and evaluate the sensitivity of pole-Q, gain, and pole-frequency to these nonidealities [5.22].

P.5.2. Derive the small signal equivalent circuit of the biquad of Fig. 5.22b considering the half circuit. Derive expressions for pole-frequency, pole-Q, and gain [5.21].

P.5.3. Compare using SPICE the two G_m-C filter configurations to show that the input voltage of the circuit of Fig. 5.51b is smaller than that of Fig. 5.51a [5.45].

Table 5.7 Characteristics of filter and comparison (Adapted from [5.21] @IEEE2011)

Parameters	[5.21]	[5.70] ESSCIRC 2003	[5.71] ESSCIRC 2004	[5.22] JSSC 2006	[5.7] JSSC 2006	[5.72] CICC 2007	[5.9] JSSC 2007	[5.19] JSSC 2009	[5.25] JSSC 2009
Technology (μm)	0.09	0.18	0.18	0.18	0.12	0.18	0.13	0.18	0.13
Topology	G_m-C	G_m-C	G_m-C	Source follower	Active-RC	G_m-C	Active-RC	G_m-C	Active G_m-RC
Supply voltage (V)	1.0	1.8	1.8	1.8	1.0	1.0	1.5	1.2	0.55
Order	6	6	4	4	3.5	3	5	3	4
Type	Butterworth	Elliptic	Butterworth	–	Chebyshev elliptic	Butterworth	Chebyshev	Butterworth	Butterworth
Application	WLAN WiMAX	WLAN WCDMA	WLAN WCDMA Bluetooth	WLAN	–	GSM Bluetooth CDMA	802.11n	Bluetooth CDMA WLAN	Baseband
f_{-3dB} (MHz)	8.1–13.5	1.5–12	0.5–12	6–14	5,10	0.135–2.2	8.9,19.7	0.5–20	11.3
Continuous tuning	Yes	Yes	Yes	No	No	Yes	No	No	No
Power (mW)	4.35	10[a]–15	1.1–4.5[a]	4.1	4.6	1.57–1.92	11.25	4.1–11.1	3.5
Power/pole (mW/pole)	0.725	1.66[a]–2.5	0.275–1.125[a]	1.025	0.92	0.52–0.62	2.25	1.36–3.7	0.875
P1-dB (dBm)	7.6	(−0.9[a])–(−2)	1[a]–8.5	5	(−3)–3.6	–	6	–	0.5
IIP3 (dBm)	21.7–22.1	7.2–9.3[a]	9.4[a]–12.5	17.5	18.8–21.3	16.3–20.1	18.3	19–22.3	10
Out-of-band IIP3 (dBm)	17.5–18.9	–	–	–	–	–	–	13–17.5	13
Out-of-band IIP2 (dBm)	51.9–53.4	–	–	–	–	–	–	30.8–40	–
IRN (nV/√Hz)	75	170[a]	255[a]	7.5	85,143[a]	65	30	12–425	33
Area (mm^2)	0.239	0.83	0.125	0.26	0.17	0.5	0.2	0.23	0.43
FoM (fJ)	0.0246	0.35[a]	2.3[a]	0.0055	0.12[a]	0.207–0.179	0.04	0.0345–3.055	0.103

[a]For IEEE802.11a application (f_c = 10 MHz)

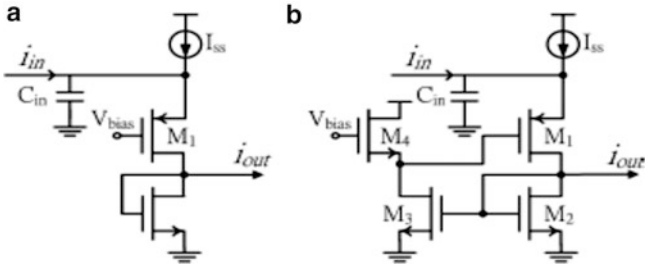


Fig. P.5.12

P.5.4. Derive the transfer function of the seventh-order filter of Fig. 5.37c. Demonstrate ways of removing the floating capacitance. Analyze the effect of parasitic capacitances of the floating and grounded capacitors and output resistances of the OTAs [5.36].

P.5.5. Discuss the stability of the fourth-order G_m-C filters of Fig. 5.50a, b [5.44].

P.5.6. Derive the transfer function of the lossy ladder filter of Fig. 5.21b, c. Analyze the effect of parasitic capacitances. Find the effective Q-factors of each stage [5.20].

P.5.7. Derive the transfer function of the current-mode biquad cell of Fig. 5.77b. Evaluate the noise at the output due to noise sources of M_1, M_2 and bias current sources [5.68].

P.5.8. Derive the transfer functions of the single- and double-inductor notch filters of Fig. 5.76c, e. Discuss techniques for optimization to reduce power consumption in the presence of losses, using the negative resistance R_N [5.67].

P.5.9. Derive expressions for the noise of LPF and BPF outputs for the circuit of Fig. P.6.9 in terms of the input referred noise V_{gm2}. Derive similar expressions for the G_m-C biquad equalizer of Fig. 5.78c. Derive expressions for power dissipation for both cases [5.69].

P.5.10. Consider the opamp-based lossy integrator. Taking into account the finite bandwidth of the amplifier, realize an equivalent circuit using an ideal opamp and discuss techniques for compensation of the effect of finite bandwidth [5.9].

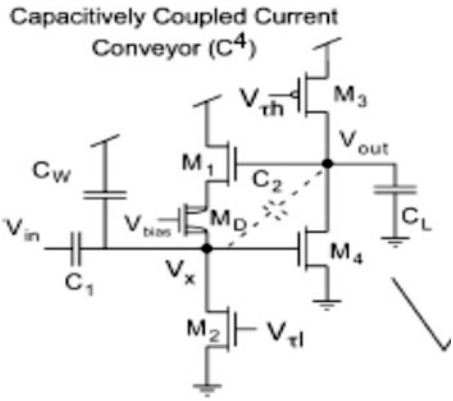
P.5.11. Evaluate the dominant pole-frequency for various PRAs of Fig. 5.7a, b considering the effect of distributed capacitance and its variation with the code word used [5.9].

P.5.12. Evaluate the input resistances of the current amplifiers of Fig. P.5.12a, b in terms of various G_{mi} values [5.5].

P.5.13. Derive the transfer function of the current mode Sallen–Key filter of Fig. 5.4c taking into account the nonzero input resistance of the current amplifier [5.5].

P.5.14. Study the effect of mismatch between the two halves in the complex bandpass filter of Fig. 5.3c [5.4].

Fig. P.5.24



P.5.15. Analyze the Sallen–Key filter noise using a unity gain amplifier and noise of the FDNR-based filter of Fig. 5.14b. Evaluate the results [5.15].

P.5.16. Evaluate the integrated inband noise of the third-order Sallen–Key Butterworth filter, third-order leap-frog ladder filter, third-order multiple feedback filter first-order RC passive filter followed by Tow-Thomas biquad in terms of the capacitance. Consider only the noise contribution of resistors [5.15].

P.5.17. Derive the transfer function of the instrumentation topology of the ADFNR circuit shown in Fig. 5.14c. Derive the noise shaping property and compare that with the FDNR-based circuit of Fig. 5.14b [5.15].

P.5.18. Analyze the effect of parasitic resistance across the capacitor in the active-G_m-RC filter of Fig. 5.25a. Analyze the effect of the second pole of the amplifier [5.24].

P.5.19. Derive expressions for quantization errors in the four types of arrays shown in Fig. 5.1. Consider the fixed component as $C_{\min}$ or $R_{\min}$ and consider δR or δC as the step size. The variation desired is 50% of the nominal value. Consider an n-bit programmable array [5.1].

P.5.20. Derive the various transfer functions of the three HPF structures of Fig. 5.11c and obtain the design equations for various resistors. Evaluate the noise performance of the three structures [5.12].

P.5.21. Evaluate the error of the resistor array of Fig. 5.5d [5.7].

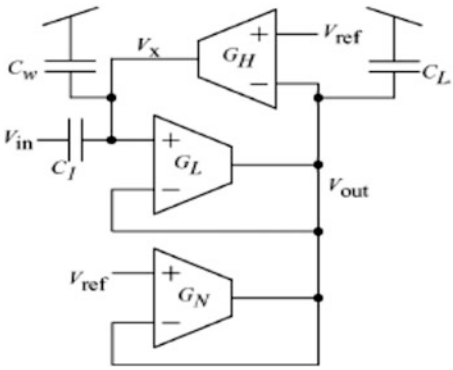
P.5.22. Evaluate the input impedance of the negative capacitance block of Fig. 5.78f [5.69].

P.5.23. Analyze the effect of input capacitance of the OTA on the OTA-C filter of Fig. 5.52a [5.46].

P.5.24. Derive the transfer function of a second-order band-pass filter realized using floating gate MOS device M_D. This technique (shown in Fig. P.5.24) is known as C^4 (capacitively coupled current conveyor) since the input signal is capacitively coupled [5.73].

P.5.25. Derive the transfer function of the OTA-C filter using a nonlinear transconductance G_L shown in Fig. P.5.25. This will be useful for realizing an

Fig. P.5.25



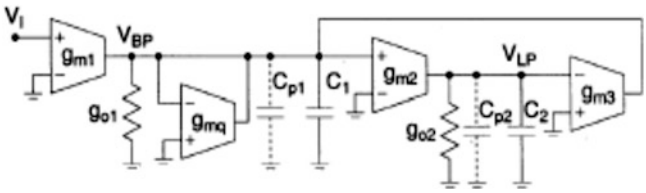


Fig. P.5.28

adaptive Q in hearing aids. Note that the Q reduces with increasing input amplitude [5.74].

P.5.26. Evaluate the effective Q of the integrator realized using Nauta's OTA (see Fig. 5.65a) considering NQS (nonquasi-static) phenomena in the transistors. Under this condition, the G_m, g_{ds}, and C_{gs} are affected by the time constants τ_1 and τ_2 as follows:

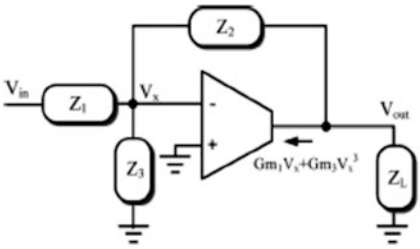
$$g_m \rightarrow \frac{g_m}{1+s\tau_1}, g_{ds} \rightarrow \frac{g_{ds}}{1+s\tau_2}, C_{gs} \rightarrow \frac{C_{gs}\,(1+s\,\tau_2)}{1+s\,\tau_1}$$

P.5.27. Analyze the error amplifier of Fig. 5.41d in the CMFB loop. Evaluate its zeroes and poles and determine the bandwidth of the CMFB loop [5.41].

P.5.28. Analyze the effect of frequency-dependent G_m on the OTA-C filter of Fig. P.5.28. Determine the phase of the low-pass response and frequency at which phase is $-45°$ and $-135°$. Discuss the choice of N to enable precise tuning of pole frequency and pole Q in the presence of nonideal G_m [5.57].

P.5.29. Determine the improvement in the third-order intermodulation distortion in the differential amplifier with linearity enhancement shown in Fig. 5.59a. Consider that v_{res} is a odd function of v_{in} given as $v_{res} = C_1\, v_{in} + C_2\, v_{in}^3$ [5.51].

Fig. P.5.31



P.5.30. Derive the transfer function of the single opamp resonator of Fig. 5.75a. Discuss its utility as a general biquad [5.66].

P.5.31. Derive an expression for IM3 for the first-order nonlinear circuit of Fig. P.5.31 assuming that the closed-loop output voltage can be expressed as

$$v_o = b_1\ v_{in} + b_3\ v_{in}^3$$

P.5.32. Considering a two-pole model for the opamp, determine the condition for stability of Tow-Thomas active RC biquad in terms of $\frac{\omega_o}{B}$ and $\frac{\omega_o}{\omega_2}$. This can be estimated using "minimum acceptable phase margin" for the opamp defined as

$$PM = 90^\circ - \tan^{-1}\frac{B}{\omega_2}$$

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Appendix A

The peak magnitude of a second-order transfer function is of importance in the scaling of the internal node voltage in a biquad realized using several active devices such as opamps or operational transconductance amplifiers. Closed-form solutions in terms of the coefficients of the numerator and denominator of the second-order transfer function will be beneficial in computer-aided design programs. Table A.1 gives these in the case of both analog and digital transfer functions.

The second-order digital transfer function considered is

$$H(z) = \frac{p\,z^2 - qz + r}{z^2 - uz + v} \tag{A.1}$$

Using bilinear transformation and considering without loss of generality T = 2 s, we have

$$H(s) = \frac{\left(\frac{p+q+r}{1+u+v}\right) s^2 + s\frac{2(p-r)}{1+u+v} + \frac{p-q+r}{1+u+v}}{s^2 + s\frac{2(1-v)}{1+u+v} + \frac{1-u+v}{1+u+v}} \tag{A.2}$$

or

$$H(s) = \frac{a\,s^2 + bs + c}{s^2 + ds + e} \tag{A.3}$$

The peak or valley of (A.3) can be found by equating the squared magnitude $|H(j\omega)|^2$ with K^2. The resulting quadratic equation in ω^2 will have equal roots in the case where the solution corresponds to a peak or valley. This yields the relationship:

$$K^4\,(d^4 - 4e\,d^2) + K^2\,(4\,b^2\,e - 8ace - 2\,b^2\,d^2 + 4ac\,d^2 + 4\,c^2 + 4\,a^2\,e^2) + (b^4 - 4\,b^2\,ac) = 0 \tag{A.4}$$

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Table A.1 (Adapted from [A.1] © IEEE 1983)

	Type of transfer function	Magnitude of the peak
1	Band-pass (bilinear) a = c = 0	$\frac{p-r}{1-v}$
2	Low-pass (bilinear) a = b = 0	$\frac{(p-q+r)(1+u+v)}{2(1-v)\sqrt{4v-u^2}}$
3	High-pass (bilinear) b = c = 0	$\frac{(p+q+r)(1-u+v)}{2(1-v)\sqrt{4v-u^2}}$
4	Notch b = 0	$\frac{2\sqrt{ac\,d^2+c^2+a^2\,e^2-2ace}}{d\sqrt{4e-d^2}}$
5	All-pass $u=\frac{q}{r}$ and $v=\frac{p}{r}$	r
6	General biquadratic function	$\frac{-y+\sqrt{y^2-4xz}}{2x}$

The quadratic equation in K^2 can be solved to obtain the peak and/or valley values of K. For special cases such as a band-pass transfer function, for example, $a = c = 0$, simple cases, the expression will be much simpler. Since the design of digital filters based on a bilinear s → z transformation starts with an analog prototype transfer function, (A.4) can be used directly to obtain K in terms of a, b, c, d, and e. In other cases, formulae in Table A.1 will be useful. Note that we have defined

$$x = d^4 - 4e\,d^2, y = 4\,b^2\,e - 8ace - 2\,b^2\,d^2 + 4ac\,d^2 + 4\,c^2 + 4\,a^2\,e^2, z = b^4 - 4\,b^2\,ac$$

in entry 6 in Table A.1.

Note also that from (A.1) directly, the peak or valley value can be found without using bilinear transformation. In this approach, $z = e^{j\omega T}$ is substituted to obtain first the relationship

$$K^2 = \frac{a_o\,\cos^2\omega T - b_o\,\cos\omega T + c_o}{\cos^2\omega T - d_o\,\cos\omega T + e_o} \tag{A.5}$$

where $a_o = \frac{pr}{v}, b_o = \frac{(p+r)q}{2v}, c_o = \frac{(p-r)^2+q^2}{4v}, d_o = \frac{(1+v)u}{2v}, e_o = \frac{(1-v)^2+u^2}{4v}$.

From (A.5), the peak or valley can be found by following a similar approach as described in the case of (A.3), from the equation

$$K^4\,(d_o^2 - 4\,e_o) + K^2\,(4\,c_o + 4\,a_o\,e_o - 2\,b_o\,d_o) + (b_o^2 - 4\,a_o\,c_o) = 0 \tag{A.6}$$

Laakso has pointed out that in both approaches described above, K is real. In the case where K is not real, the value of the transfer function at dc and infinite frequencies needs to be found and the higher among them is the maximum

magnitude. These are from (A.5) (at $\cos(\omega T) = 1$ and $\cos(\omega T) = -1$), respectively,

$$K^2 = \frac{a_o - b_o + c_o}{1 - d_o + e_o} \quad \text{and} \quad K^2 = \frac{a_o + b_o + c_o}{1 + d_o + e_o}$$

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Appendix B

The realized transfer function is affected by the nonideal passive and active components. The variation in the transfer function due to variations in pole-frequency and pole-Q can first be evaluated. These yield topology-independent expressions or curves. The variation in pole-frequency and pole-Q due to the active and passive components in the chosen topology is topology-dependent and can be estimated easily. Substituting the latter in the former expressions gives the total variation in the transfer function. Considering $H(s)$ as the desired biquadratic transfer function

$$H(s) = \frac{1}{D(s)} = \frac{1}{s^2 + s\frac{\omega_p}{Q_p} + \omega_p^2} \tag{B.1}$$

we can obtain

$$S_{\omega_p}^{|H(jw)|} = -\left(\frac{2(1-\gamma^2) + \frac{\gamma^2}{Q_p^2}}{(1-\gamma^2)^2 + \frac{\gamma^2}{Q_p^2}}\right) \tag{B.2}$$

and

$$S_{Q_p}^{|H(jw)|} = \left(\frac{\frac{\gamma^2}{Q_p^2}}{(1-\gamma^2)^2 + \frac{\gamma^2}{Q_p^2}}\right) \tag{B.3}$$

where $\gamma = \frac{\omega}{\omega_p}$. It can be seen from (B.2) and (B.3) that both sensitivities are functions of γ and hence universal curves as functions of γ are of interest. These are presented in Fig. B.1a, b [B.1]. It may be noted that $S_{\omega_p}^{|H(jw)|}$ reaches a maximum of about Q_p at the 3-dB frequencies $\gamma = 1 \pm \frac{1}{2Q_p}$ whereas the maximum value of $S_{Q_p}^{|H(jw)|}$ is unity. The ratio of $S_{\omega_p}^{|H(jw)|}$ to $S_{Q_p}^{|H(jw)|}$ is

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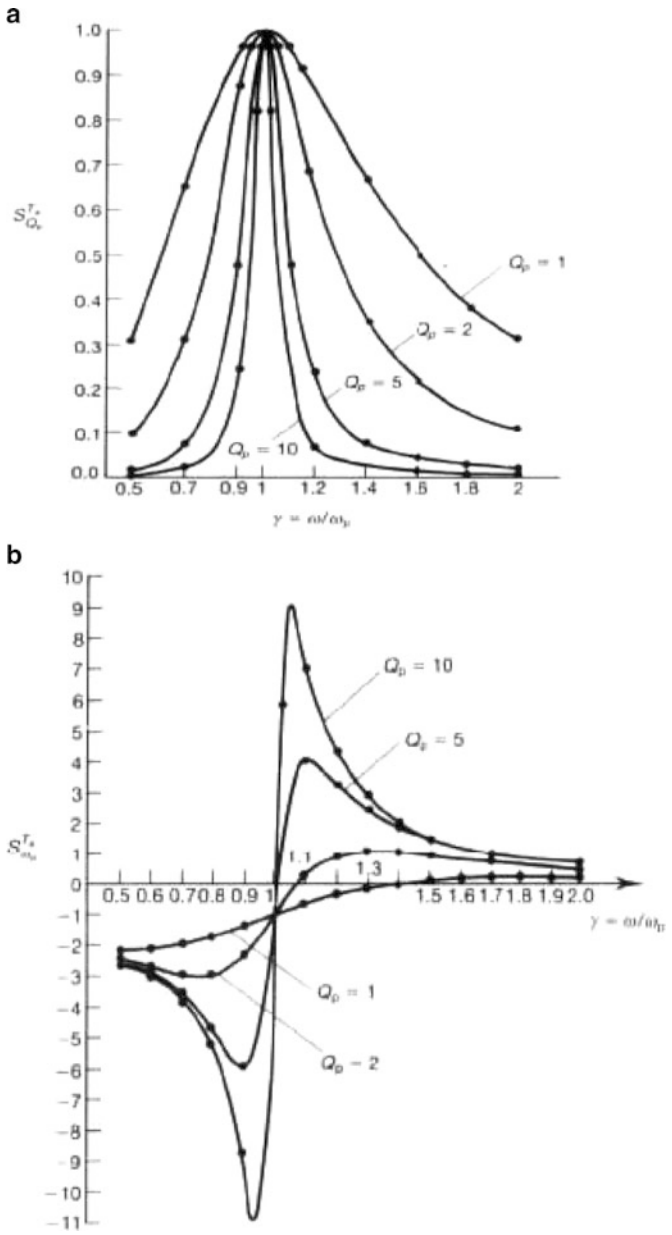

Fig. B.1 Universal *curves* showing sensitivity of transfer function to pole-frequency (**a**) and pole-Q (**b**) with pole-Q as a parameter (Adapted from [B.1] © IEEE 1973)

$$\frac{S_{\omega_p}^{|H(jw)|}}{S_{Q_p}^{|H(jw)|}} = -\left(1 + 2\,Q_p^2\left(\frac{1}{\gamma^2} - 1\right)\right) \tag{B.4}$$

At the 3-dB frequencies, this ratio is $2Q_p$. This is an important result showing that the magnitude of sensitivities to pole-frequency must be kept less than $2Q_p$ times the magnitude of sensitivities to pole-Q.

It can next be observed that the percentage variation in the transfer function can be expressed as

$$\frac{\Delta|H|}{|H|} = S_{\omega_p}^{|H|} \cdot \frac{\Delta\,\omega_p}{\omega_p} + S_{Q_p}^{|H|} \cdot \frac{\Delta\,Q_p}{Q_p} \tag{B.5}$$

We next note that

$$\frac{\Delta\,\omega_p}{\omega_p} = \sum_{i=1}^{k} S_{C_i}^{\omega_p} \cdot \frac{\Delta\,C_i}{C_i} + \sum_{i=1}^{l} S_{R_i}^{\omega_p} \cdot \frac{\Delta\,R_i}{R_i} \tag{B.6}$$

considering that the filter needs k capacitors and l resistors. Note that the active devices also need to be included in the above expressions since we have earlier described the evaluation of pole-Q and pole-frequency sensitivities to opamp finite gain and finite bandwidth.

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