An Improved CMOS Error Amplifier Design for LDO Regulators in Communication Applications

XINQUAN LAI
Institute of Electronic CAD
Xidian University
Xi'an, 710071
P. R. CHINA

DONGLAI XU
School of Science and Technology
University of Teesside
Middlesbrough, TS1 3BA
UNITED KINGDOM

Abstract: - A new CMOS error amplifier, which is primarily used in LDO regulators for communication applications, is presented in this paper. Using the structure of symmetrical OTA, dynamic frequency compensation and nested Miller compensation, the characteristics and performance of the designed amplifier have been significantly improved. The simulation results based on Hynix *0.5μm* CMOS models show that across a wide frequency range, the gain of the amplifier is greater than *60dB*, and the PSRR and CMRR reach *65dB* and *70dB*, respectively.

Key-Word: - Error amplifier, LDO, Regulators, CMOS, VLSI, OTA

1 Introduction

With the development of modern portable communication products and equipment, power management ICs, such as LDO regulator, have been becoming increasingly important for systems integration, particularly in wireless and hand-held applications. As one of the most basic components in analogue VLSI, error amplifier has been widely used in LDO regulator, ADC, DAC, and RF circuits that require highly accurate voltage reference, low noise, high power-supply rejection ratio (PSRR) and high common-mode rejection ratio (CMRR). In this paper, a new error amplifier used in LDO regulator circuits is presented. Compared with conventional designs, the key features of the redesigned CMOS error amplifier lies in: firstly, the power-supply bias of the input-stage of the error amplifier is connected to the stable output of the LDO, rather than the power supply of the whole chip; secondly, a dynamic frequency compensation circuit is introduced to enhance frequency characteristic and to reduce the high cost incurred from the classical frequency compensation method of using the output capacitor ESR (equivalent series resistance); thirdly, while nested Miller capacitor works for further frequency compensation, it also improves PSRR; finally, a few additional circuits, such as start-up, load current sampling and over-current protection, are incorporated into the design to improve accuracy.

The rest of the paper is organized as follows. Section 2 presents and explains the circuit of the proposed error amplifier in detail. In section 3, simulation results of the design are given in terms of amplifier gain, PSRR and CMRR. Finally, conclusions are drawn in section 4.

2 Circuit Design

The overall schematic of the error amplifier with pass element and feedback network is shown in Fig.1. For the ease of the discussions below, the functional blocks of the circuit are separated by the dash-lined boxes.

2.1 Error Amplifier Circuit Design

The core of the design is a symmetrical operational trans-conductance amplifier (OTA) [1] with high gain and PSRR, as illustrated in Fig.1. It is composed of the first-stage amplifier *Gm1*, the second-stage amplifier *Gm2* and frequency compensation circuit.

Gm1 is a basic symmetrical OTA with differential input, which amplifies the differential-mode signal of the output feedback voltage of LDO (*INP* terminal) and the reference voltage (*INN* terminal). The bias circuit consists of *M7, M8, M11, M12, M13, M14, M15* and *R3*. The bias current *I0* is twice *I3*, and it is determined by reference voltage, threshold of NMOS transistor *M15* and resistor *R3*. The common source of *M7* and *M8* is connected to the LDO's output (*OUT*), so the error amplifier will not function until the voltage of *OUT* (V_{OUT}) reaches a certain value (2V or so). The signal *SU* generated by this part of the circuit provides bias and start-up for the over-current protection circuit followed. The output stage of *Gm1* is a structure of current

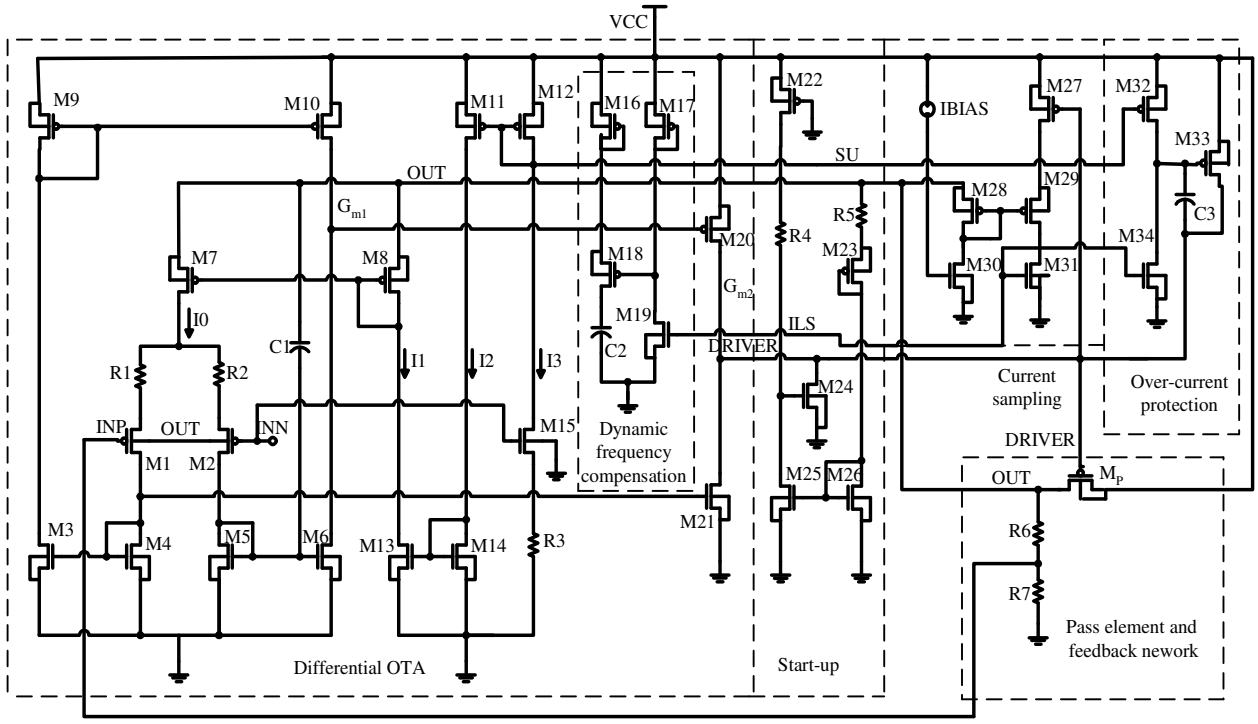

Fig.1 Error amplifier schematic with pass element and feedback network

amplification, which is made up of *M3, M6, M9* and *M10* with a amplification ratio of 3:1, i.e., *(W/L)6:(W/L)5=(W/L)4:(W/L)3=3:1*, where *W* and *L* are the width and length of a transistor, respectively. This ratio value is calculated as a result of the tradeoffs between the design parameters gain-bandwidth, phase margin and output noise.

The second-stage amplifier *Gm2* is designed to increase open-loop gain and to reduce the output resistance of the error amplifier, therefore increasing bandwidth. It's an inverse amplifier composed of *M20* and *M21*, both having relatively large width-length ratio. The *W/L* ratios of the *M16* (in frequency compensation circuit) and *M20* predominately determine open-loop low-frequency gain. Moreover, *M20* and *M21* can realize the rail-to-rail output to control the gate of the pass element *Mp*.

In order to improve the frequency characteristic of the traditional LDOs [2, 3, 4], two types of compensation circuits are introduced in this design. One is the dynamic frequency compensation circuit, in which an RC network composed of the switch resistance and parasitical capacitance of MOS transistor is used to sample load current, thus changing the operation point of the MOS transistor. That is, as a result of changing the values of the switch resistance and parasitical capacitance, dynamic frequency compensation is realized. The zero and pole frequencies increase (decrease) while load current increases (decreases). This means that the zero *Zc* and the pole *Po* change simultaneously with the change of load current. Therefore, the unit gain frequency (UGF) of LDO remains almost unchanged when load changes. This makes operation stable in the whole range of load. Fig.2 shows the principle of this compensation method [2].

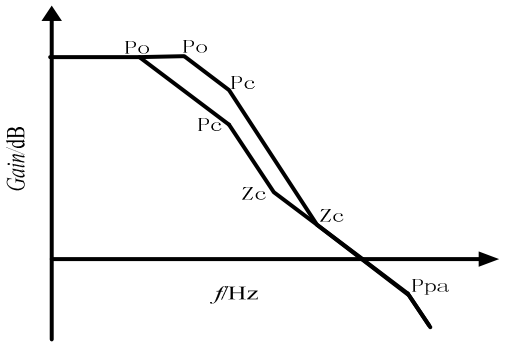

Fig.2 Dynamic frequency compensation

As shown in Fig.1, the dynamic frequency compensation circuit consists of the components *M16, M17, M18, M19* and *C2*. Of them, *M16, M18* and *C2* are not only the load of the amplifier *Gm1*, they also perform the function of frequency compensation. Here the area of *M18* is designed to be very large in order to generate a large parasitical

capacitance. The *M31* (of current sampling circuit) and *M19* form a mirror current source with a design *W/L* ratio of 1:5. Based on the principle of transistors [5], V_{GM18} (the voltage at the gate of *M18*) can be expressed as

$$\begin{aligned} V_{GM18} &= VCC - V_{SGM17} \\ &= VCC - \sqrt{\frac{2I_{DM19}}{\mu_p C_{OX}(\frac{W}{L})_{M17}}} - |V_{THP}| \\ &\approx VCC - \sqrt{\frac{2I_S}{5\mu_p C_{OX}(\frac{W}{L})_{M17}}} - |V_{THP}| \end{aligned} \quad (1)$$

From the above equation, the relationship between V_{GM18} and *Is* (sampling current, here *Is*≈*IL/3000*) is apparent, i.e., V_{GM18} varies with *IL* (load current). Thus, the function that the RC dynamic compensation network changes with the change of load is achieved.

Another frequency compensation used in the circuit is the nested Miller compensation for the loop consisting of the error amplifier and pass element *Mp*. It uses a capacitor *C1* between the first and second stage amplifiers, and in this case the feedback introduced is from *OUT*. This method increases PSRR.

2.2 Other Functional Blocks

Fig.1 also gives the other functional blocks of the design, which include start-up circuit, load current sampling circuit, and over-current protection circuit and so on.

Different from conventional methods, in this design the power supply bias of the differential input of *Gm1* is connected to *OUT*, rather than the power supply itself (*VCC*) of the chip. This makes the power supply bias (reference output) very stable, i.e., very small ripple and significantly reduced noise at the terminal *OUT*. However, a problem arises with the above design. Since V_{OUT} (i.e., power supply bias) is zero immediately after the power supply of the system is turned on, the error amplifier cannot operate and the output *DRIVER* cannot drive the pass element *Mp*. Thus, a start-up circuit is needed in order that as soon as power supply is switched on, the start-up circuit controls the gate of *Mp* (*DRIVER*) and makes it conductive. Then, when V_{OUT} reaches a threshold that triggers the operation of the error amplifier, the feedback from *OUT* shuts down the start-up circuit. After the starting-up, V_{DRIVER} is controlled by the output of the error amplifier. As shown in Fig.1, *M22, R4* and *M24* turn on the start-up circuit, and *M23, M25, M26* and *R5* shut it down.

The load current sampling circuit is to obtain a small current *Is* that is proportional to the load current *IL* by means of sampling the voltages of the source, gate and drain of *Mp*. It consists of *M27, M28, M29* and *M30*. The sources and gates of *M27* and *Mp* are connected together, respectively. Therefore, if the drain voltages (V_{DRAIN}) of *M27* and *Mp* are equal, then

$$\frac{I_S}{I_L} = \frac{W_{27}L_P}{L_{27}W_p} \approx \frac{1}{3000} \quad (2)$$

In this circuit, the equality of V_{DRAIN} of *M27* and *Mp* is ensured by the structures of *M28, M29* and *M30*. The principle is as follows: reference circuit provides a very small bias current (about *1μA*) so that V_{GS} of *M28* is almost its threshold voltage. The *W/L* ratio of *M29* is designed to be large, so according to the equation (2), the sampling current *Is* is very small. Hence the V_{GS} of *M29* is very small, which can be calculated using the current and voltage expression of MOS transistor [1]. For a maximum operation current *150μA*,

$$V_{SG} \approx |V_{THP}| + 0.13 \quad (3)$$

So, V_{DRAIN} of *M27* and *Mp* are just about equal and the equation (2) is relatively accurate.

The over-current protection circuit controls the V_{GATE} of *Mp* through the sampling current *Is*, therefore limiting the maximum *IL*. The signal *SU* functions as starting-up and bias to ensue that this circuit does not control *Mp* when LDO operates normally. The over-current protection circuit is composed of *M32, M33* and *M34*. Here, the *M31* of load current sampling circuit and *M34* are mirrored one another. When *IL* is within normal range, *Is* is small, *M32* and *M34* together drive V_{GATE} of *M33* high, and the over-current protection circuit does not function. As *IL* increases, the V_{DRAIN} of *M34* (i.e. V_{GATE} of *M33*) will decrease gradually. When *IL* reaches a certain value, *M33* conducts entirely and V_{DRIVER} is kept to a limit by feedback loop. Thus, the output *IL* can be restricted to a limited value. It is obvious that in order to meet the requirement of current limitation, the sizes of *M32*, *M33* and *M34* have to be matched carefully in the circuit design. While operating at the state of limiting current, a feedback loop is formed in the circuit and then *C3* acts as a miller compensation capacitor to keep the restricted current value stable.

3 Simulation Results

To evaluate the performance of the designed circuit, the simulations based on Hynix *0.5μm* CMOS process have been carried out. Fig. 3 gives the HSPICE simulation results of the gain versus frequency with different power supply values. The results demonstrate that within a broad bandwidth,

the gain of the circuit is over *60dB*.

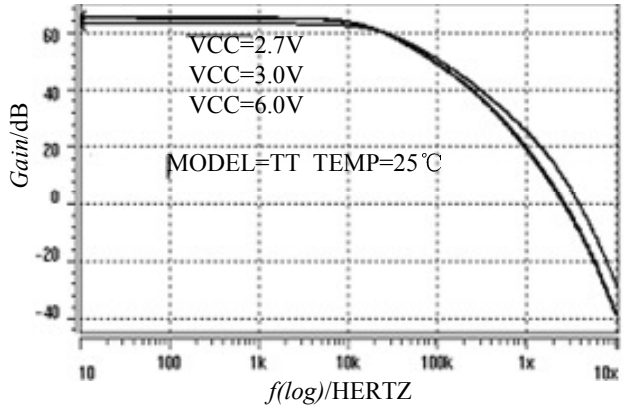

Fig.3 Gains with different *VCC*

The HSPICE simulation results of the PSRR versus frequency with different power supply values and the CMRR versus frequency with different load currents values are presented in Fig. 4 and Fig. 5, respectively. The results show that the PSRR and CMRR of the circuit reach *65dB* and *70dB*, respectively.

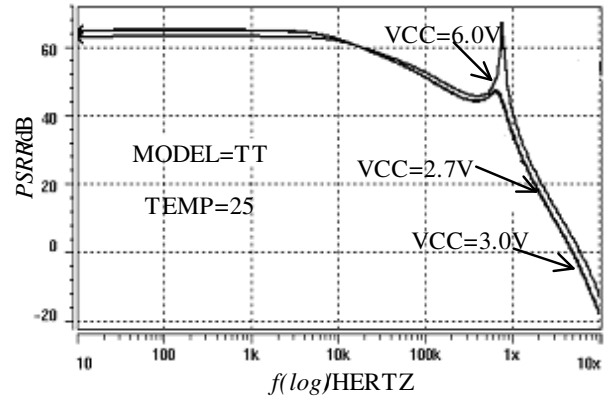

Fig.4 PSRR with different *VCC*

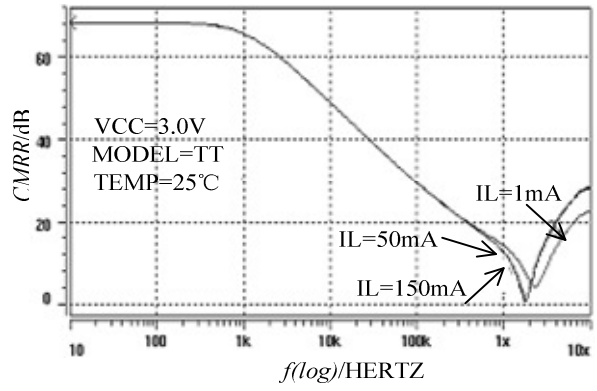

Fig.5 CMRR with different load currents

To further test the suitability of this design for the intended applications, a layout of the LDO regulator using the proposed error amplifier has also been designed, as illustrated in Fig.6. The further work on the LDO is going to be carried out.

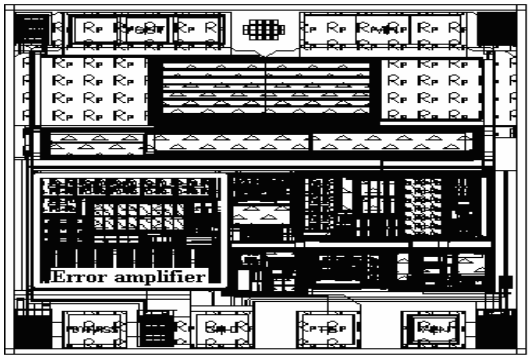

Fig.6 Layout of the LDO

4 Conclusions

Based on symmetrical OTA structure, a new CMOS error amplifier used in LDO regulators has been designed by incorporating dynamic frequency compensation and nested Miller compensation into the traditional structure. The new circuit not only reduces output ripple and noise, but also improves stability. The circuit analysis and simulation results show that using Hynix *0.5μm* CMOS process, within the frequency range from *100Hz* to *10MHz*, the design achieves an improved performance of over *60dB* gain, *65dB* PSRR and *70dB* CMRR.

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