Patrice DELPY - 38 years old.
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ELECTRONICS ENGINEER
Analog IC layout Designer full custom: 8+ years of experience

Professional experience

Layout leader for several projects, technical responsibilities, resource management.
Top cell assembly, blocks layout: Floorplanning, place and route, DRC/LVS.
Realization of mixed analog blocks and IPs : ADC / LDO / SMPS / Bias / VBG / CAN / Oscillator.
Ensuring quality of the physical - aware of the robustness and reliability problems
Understanding of DFM layout techniques: matching, technological, mechanical, heat constraints
Insertion of ESD protection strategies, isolation, shielding, parasitic extraction. power routing.
Development of circuits with submicronic dimensions (high degree integration).
Methodologies definitions, team planning function, interface with the design team.
Good knowledge of microelectronic process, physics of Semiconductor and analog design.
Qualification to work on BiCMOS technologies, HDTMOS, low and high current (1.5V to 65V).

Sept 2008 to today (11 months) — **Backend Subcontractor :** ON SEMICONDUCTOR
Execution of Headset amplifier (Audio IC) and power management blocks (CP/ LDO / Buck /Boost).
Creation of complex skill based Pcell for ESD. Writing macros for custom applications

Jan 2007/Aug 2008 / Jan 2000/Oct 2004 (7 years and 5 months) — **Backend Subcontractor** : FREESCALE / MOTOROLA (work on a multi-site team)
Contributions to complex automotive ASIC's (20 to 55 mm²) in Smartpower: ESP, ABS, Airbag.
Using Cadence's language. Writing and debugging ability in SKILL.
Making of blocks for Power Management circuits for wireless and power over Ethernet systems.
Setting up of a Metrix frame measuring a project advancement as well as the re-use impact.

Nov 2005/Dec 2006 (14 months) — **Test Engineer:** Automotive Group - FREESCALE
Implementation of a Zero Defects plan. Action aiming at reducing costs: redundancy, optimization.
Development of tests algorithms on ATE, debugging hardware, measurement and characterization,
Analysis: Cp/Cpk, R&R, Gage, defective tracking. Use of dedicated statistical tools to it.
Improving of tests packages (stability, test coverage) in final test and probe area.

1999 (1 year) — **Supervisor :** TV and radios - TDF (France Telecom)
Remote monitoring, failure diagnosis, intervention handling.
Planning of technical means, of maintenance operations/actions (curative and preventive)
Restoration of functioning and incidents follow-up with customers

1998 (1 year) — **Technician R&D:** PCB – STUDELEC
Design of cards for Airbus, Pluton project by Siemens: linear supply, DCDC switching converter, bench test for Alcatel.

Education

2005: Master's Degree of Engineering in Electronic (INPT / CNAM Toulouse).
1993: BTEC Higher National Diploma in Electronic Engineering.

Specific Knowledge/Skills

EDA tools:	Cadence Design Systems, Calibre, Assura , Diva, Chip Floorplanner, VCR, Spectre, Pspice.
Programming experience:	SKILL language, VHDL, C/C++, Visual Basic, Perl, Tcl, , Matlab, shell scripting on linux.
ATE equipments:	Teradyne IntegraFlex, LTX, MiST, Prober Electroglas, Handler Delta Design.
FPGA/microcontrollers:	Xilinx ISE suite, Intel/Motorola, IDE Metrowerks, ImageCraft, Axiom Emulator.

Achievement and interests

Foreign languages:	English: everyday and technical (read, written and spoken)
Pastimes:	Astronomy, computer programming, home automation, rifle shooting.