Coordonnées

55 Chemin du Chapitre
Appt 2B
31100 Toulouse
0635291573 (Mobile)
patrice.delpy@outlook.fr

www.linkedin.com/in/patrice-delpy-35a763272 (LinkedIn)

Patrice Delpy

Ingénieur Layout Analogique & mixte chez onsemi
Toulouse, Occitanie, France

Résumé

I'm Layout leader on power management products dedicated to automotive and wireless (up to 65V).
· I have worked on BICMOS processes (ON, TSMC, Tower) and know chip packaging flow: bonding, FC, CSP, CuPillar.
· Good understanding semiconductor technology, device physics, layout practices and analog functionality.
· Driving floorplanning activities on block or top level : ESD strategy, PDN, signal integrity, assembly, route, checks.
· Conduct feasibility study to know technical effort and cost viability of project: size, process options, packaging…
· I manage and commit to a schedule: identifying, prioritizing tasks / risks: workload evaluation, tracking progress.
· I co-work with team to design high quality layout, with reuse to achieve best choice in term of performance/cost/area.
· Demonstrates analytical skills and leadership to resolve problems, purpose solutions and drive execution.
· Good communication skills, I organizes reviews, provide reporting documents and defines methodologies.
· Motivated to mentoring and learn, I introduces ideas for improve your efficiency and automation of layout tasks.

Specific knowledge/Skills

EDA tools : Cadence , Calibre Suite, EAD, Floorplanner, Magwel, R3D, Simvision, Spectre, Explorer, Innovus. Programming and other : SKILL, JAVA, Python, C, Verilog, linux, Microsift Office

Expérience

onsemi
Ingénieur Layout Analogique & mixte
septembre 2008 - Present (14 ans 8 mois)
Toulouse, Occitanie, France

Physical design Engineer: ON SEMICONDUCTOR

Leader and contributor on circuits: Amoled Driver, SBC, IC audio, PMIC, LED driver, DCDC.
Interface between all teams: design, application, test, package to ensure successful tapeout.
Experienced to run post layout extraction tools to prevent EMIR effects and increase robustness.
Using advanced EDA tools: foorplanner, constraint manager to be more productive.
Support Digital Team: Perform Verilog RTL code and validation, execute synthesis, P&R.

PSI Electronics

Physical design contractor: FREESCALE
janvier 2007 - septembre 2008 (1 an 9 mois)

Layout lead of a multi-system companion chip MSC2 (21mm2) – more 10 layouters.
Working on E-switch (double die IC), realize large part of control and design power device in HDTMOS.
IP leader on new single wire bus architecture.

PSE Electronic

Final internship in Electronic Engineering (1 year): Test GROUP : FREESCALE
novembre 2005 - novembre 2006 (1 an 1 mois)

Master's thesis on the optimization of the test of integrated circuits dedicated to automotive. Action aiming at reduce test time: ATE resources sharing in multi-site configuration.

PSI Electronics

Physical design contractor: MOTOROLA / FREESCALE
avril 2000 - octobre 2005 (5 ans 7 mois)

Contributions to complex automotive ASIC's (35 to 55 mm²): ESD, ABS, Airbag
Ability to analyze schematic, taking in account design constraints, place, route, DRC/LVS.
Practices to design critical layout of blocks or IP's : ADC, LDO, CAN, PLL, BG, OSC. VREF.
Solid understanding of layout constraints: Matching, symmetry, ERC, Isolation, DFM …

Familiar with analog reliability requirements: parasitic, ESD, LUP, noise, antenna, delay …

Formation

CNAM Toulouse

Diplôme d’ingénieur en Electronique (option microélectronique) · (2006)

BTS Électronique

· (1993)