Patrice DELPY - 52 ans.
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ELECTRONICS ENGINEER
Senior analog IC layout Designer - full custom: 22+ years of

Professional expertise

- Layout leader on power management products dedicated to automotive and wireless (up to 65V).
- Design of blocks, IP's and topcell assembly according these main keys points: min area, quality, re-use concept.
- Good understanding semiconductor technology, device physics, layout practices and analog functionality.
- Can conduct feasibility that include constraints to estimate size, validate manufacturability, elaborate schedule.
- I manage and commit to a planning: identifying, prioritizing tasks / risks: workload evaluation, tracking progress.
- With burndown chart I make actions in case of timescales because I responsible for the on time delivery of project.
- Co-work with designers on block, top level floorplan to achieve best choice in term of performance/cost/area.
- Demonstrates analytical skills and leadership to resolve problems, purpose solutions and drive execution.
- Good communication skills, organize reviews, meeting, writes documents and define methodologies.
- Self-motivated to mentoring, introduce ideas for improve your efficiency and automation of layout tasks.

Professional career

09/2008 present — **Physical design Engineer**: ON SEMICONDUCTOR

Leader and contributor on circuits: Amoled Driver, SBC, IC audio, PMIC, LED driver, DCDC.
Manage activities such as floor planning: PDN, IC partition, assembly, route, package integration.
Interface between all teams: design, application, test, package to ensure successful tapeout.
Experienced to run post layout extraction tools to prevent EMIR effects and increase robustness.
Utilizing advanced EDA tools: foorplanner, constraint manager to be more productive.
Support Digital Team: Perform Verilog RTL code and validation, execute synthesis, P&R.

01/2007 – 09/2008 — **Physical design contractor**: FREESCALE

Layout lead of a multi-system companion chip MSC2 (21mm2) – more 10 layouters.
Working on E-switch (double die IC), realize large part of control and design power device in HDTMOS. IP leader on new single wire bus architecture.

11/2005 – 11/2006 — **Final internship in Electronic Engineering : Test GROUP :** FREESCALE

Master's thesis on the optimization of the test of integrated circuits dedicated to automotive.
Action aiming at reduce test time: ATE resources sharing in multi-site configuration.

04/2000 - 11/2005 — **Physical design contractor**: FREESCALE / MOTOROLA

Contributions to complex automotive ASIC's (35 to 55 mm²): ESD, ABS, Airbag
Ability to analyze schematic, taking in account constraints, place and route, DRC & LVS.
Design of mixed analog blocks and IP's : ADC, LDO, CAN, SMPS, PLL, BG, BIAS, OSC. VREF.
Solid understanding of layout practices: Matching, symmetry, ERC, Isolation, DFM …
Familiar to apply techniques to avoid issues such as parasitics, ESD, LUP, delay, crosstalk …

Education

2006 : Diplôme d'ingénieur en Electronique (option microélectronique) – CNAM Toulouse.
1993 : BTS Électronique (Albi).

Specific knowledge/Skills

EDA tools : Cadence , Calibre Suite, EAD, Floorplanner, Magwel, R3D, Simvision, Spectre, Explorer, Innovus.
Programming and other : SKILL, JAVA, Python, C, Verilog, linux, Suite Office.

Achievement and interests

Foreign languages : English : everyday and technical (read, written and spoken).
Pastimes : Computer programming focused to « Electronic », home automation (ARM & Raspberry).