SOLUTION MANUAL

FOR

"FUNDAMENTALS OF

POWER SEMICONDUCTOR DEVICES"

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SPRINGER-SCIENTIFIC

Chapter 1
Introduction

Problem 1.1:

Define the current and voltage ratings of power devices for typical automotive applications.

Solution:

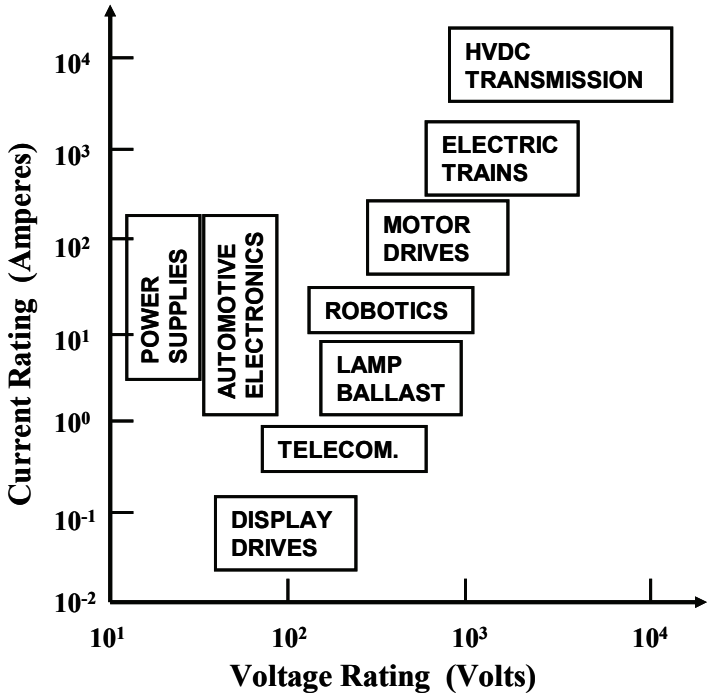


Fig. 1.2 System Ratings for Power Devices.

The current ratings for power devices range from 1 to 120 amperes and the voltage ratings for power devices range from 30 to 100 volts for typical automotive applications based upon using Fig. 1.2 (shown above).

Problem 1.2:

Define the current and voltage ratings of power devices for typical computer power supply applications.

Solution:

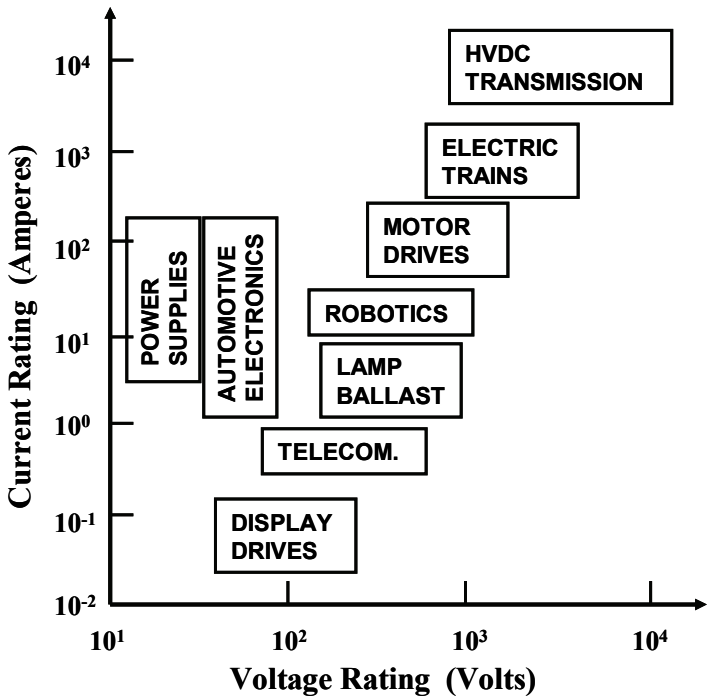


Fig. 1.2 System Ratings for Power Devices.

The current ratings for power devices range from 5 to 120 amperes and the voltage ratings for power devices range from 15 to 30 volts for typical power supply applications based upon using Fig. 1.2 (shown above).

Problem 1.3:

Define the current and voltage ratings of power devices for typical motor control applications.

Solution:

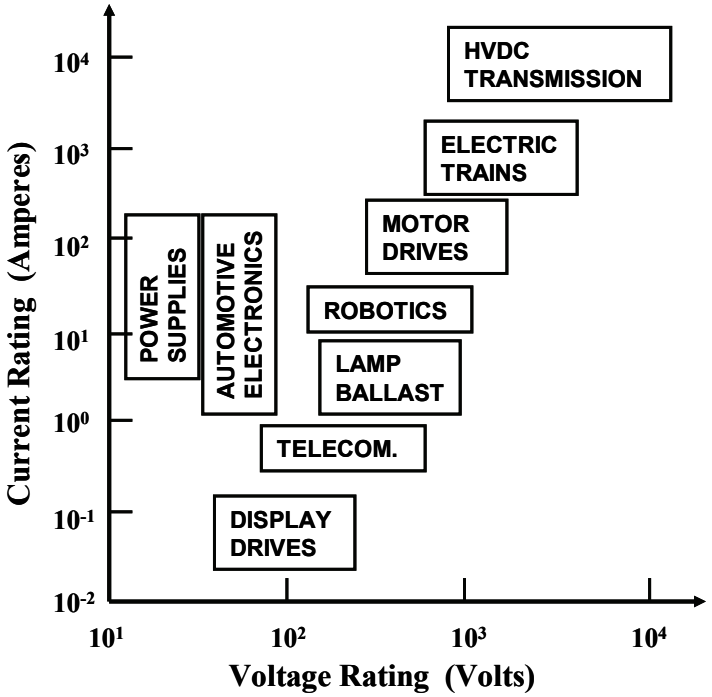


Fig. 1.2 System Ratings for Power Devices.

The current ratings for power devices range from 50 to 200 amperes and the voltage ratings for power devices range from 300 to 1500 volts for typical motor control applications based upon using Fig. 1.2 (shown above).

Problem 1.4:

Define the current and voltage ratings of power devices for typical electric locomotive applications.

Solution:

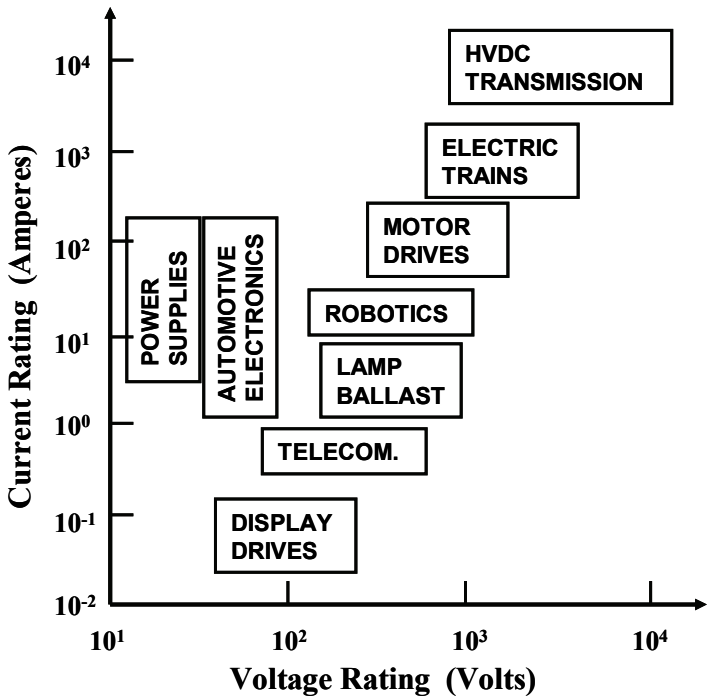


Fig. 1.2 System Ratings for Power Devices.

The current ratings for power devices range from 300 to 2000 amperes and the voltage ratings for power devices range from 500 to 3000 volts for typical electric locomotive applications based upon using Fig. 1.2 (shown above).

Problem 1.5:

What are the characteristics for an ideal power device?

Solution:

An ideal power device is capable of controlling power flow through it with zero power dissipations. It has zero voltage drop on the on-state, zero leakage current in the off-state, and zero switching time.

Problem 1.6:

Describe the characteristics for an ideal power rectifier?

Solution:

An ideal power rectifier is capable of carrying any amount of current in the first quadrant with zero on-state voltage drop. It is capable of supporting any amount of voltage in the third quadrant with zero leakage current. In addition, an ideal rectifier can make the transition between the on and off states instantaneously with zero switching losses.

Problem 1.7:

How do the characteristics of actual power rectifiers defer from those for the ideal device?

Solution:

Actual power rectifiers exhibit a finite on-state voltage drop that increases with increasing current flow in the first quadrant. They exhibit a finite leakage current that increases with increasing reverse bias voltage in the third quadrant. Actual power rectifiers exhibit finite transition times when switching between the on and off-states resulting in switching power losses.

Problem 1.8:

Describe the characteristics for an ideal power transistor?

Solution:

An ideal power transistor is capable of supporting a large voltage in the off-state with zero leakage current and a large current in the on-state with zero voltage drop. It is capable of switching between these states in response to a gate bias voltage. The ideal power transistor also exhibits current saturation with the current determined by the applied gate bias voltage.

Problem 1.9:

How do the characteristics of actual power transistors defer from those for the ideal device?

Solution:

Actual power transistors exhibit a finite voltage drop in the on-state and a finite leakage current in the off-state. The switching time for the transition between these states is finite leading to significant power dissipation or switching losses. The saturation current for actual power transistors increases with increasing applied voltage and may not extend to its breakdown voltage.

Problem 1.10:

Why are unipolar power device structures more attractive for applications than bipolar power devices?

Solution:

Unipolar power devices are preferred over bipolar power devices because they operate in the on-state without the injection of minority carriers leading to no stored charge in the drift region. This allows unipolar devices to switch faster than bipolar devices because of the long time interval required to remove the stored charge in the bipolar devices. Power systems that utilize unipolar power devices can operate at higher frequencies with low switching power losses.

Problem 1.11:

Calculate Baliga's figure-of-merit for a semiconductor with an electron mobility of 2000 cm^2/V-s and critical breakdown electric field strength of 5 x 10^5 V/cm.

Solution:

The Baliga's figure-of-merit for semiconductors is given by:

$$Baliga's\ FOM = \varepsilon_S \mu_n E_C^3 \qquad \textbf{[P1.11a]}$$

For silicon, a typical value for the electron mobility is 1350 cm^2/V-s and the critical breakdown electric field strength is 2 x 10^5 V/cm. Assuming that the dielectric constant for the semiconductors is the same as that for silicon, the Baliga's figure-of-merit is given by:

$$Baliga's\ FOM = \frac{\mu_n E_C^3}{\mu_n(Si) E_C^3(Si)} = \left(\frac{2000}{1350}\right)\left(\frac{5x10^5}{2x10^5}\right)^3 = 23.15 \qquad \textbf{[P1.11b]}$$

The Baliga's figure-of-merit is a measure of the reduction in the resistance of the drift region that can be achieved by replacing silicon with another semiconductor.

Problem 1.12:

Determine Baliga's figure-of-merit for Gallium Nitride assuming it has an electron mobility of 900 cm^2/V-s and critical breakdown electric field strength of 3.3 x 10^6 V/cm.

Solution:

The Baliga's figure-of-merit for semiconductors is given by:

$$Baliga's\ FOM = \varepsilon_S \mu_n E_C^3 \qquad \textbf{[P1.12a]}$$

For silicon, a typical value for the electron mobility is 1350 cm^2/V-s and the critical breakdown electric field strength is 2 x 10^5 V/cm. Assuming that the dielectric constant for GaN is the same as that for silicon, the Baliga's figure-of-merit is given by:

$$Baliga's\ FOM = \frac{\mu_n (GaN) E_C^3 (GaN)}{\mu_n (Si) E_C^3 (Si)} = \left(\frac{900}{1350}\right)\left(\frac{3.3x10^6}{2x10^5}\right)^3 = 2990 \qquad \textbf{[P1.12b]}$$

The Baliga's figure-of-merit is a measure of the reduction in the resistance of the drift region that can be achieved by replacing silicon with GaN.

Chapter 2
Material Properties and Transport Physics

Problem 2.1:

Determine the intrinsic carrier concentration for silicon at 300, 400 and 500 ^{o}K.

Solution:

For silicon, the intrinsic carrier concentration is given by:

$$n_i = 3.87x10^{16} T^{3/2} e^{-(7.02x10^3)/T} \qquad \textbf{[P2.1a]}$$

Using this equation, the values for the intrinsic carrier concentration are:

Temperature (^{o}K)	**Intrinsic Concentration (cm^{-3})**
300	1.38×10^{10}
400	7.39×10^{12}
500	3.46×10^{14}

Problem 2.2:

Determine the intrinsic carrier concentration for 4H-SiC at 300, 400 and 500 ^{o}K.

Solution:

For 4H-SiC, the intrinsic carrier concentration is given by:

$$n_i = 1.70x10^{16} T^{3/2} e^{-(2.08x10^4)/T} \qquad \textbf{[P2.2a]}$$

Using this equation, the values for the intrinsic carrier concentration are:

Temperature (^{o}K)	**Intrinsic Concentration (cm^{-3})**
300	6.74 x 10^{-11}
400	3.51 x 10^{-3}
500	1.62 x 10^{2}

Problem 2.3:

Calculate the band-gap narrowing in silicon at a doping concentration of 1 x 10^{19} cm^{-3}.

Solution:

The band-gap narrowing in silicon is given by:

$$\Delta E_G = 22.5x10^{-3}\sqrt{\frac{N_I}{10^{18}}} \qquad \textbf{[P2.3a]}$$

where N_I is the impurity (donor or acceptor) concentration responsible for the reduction in the band gap. A band-gap narrowing of 0.0712 eV at room temperature is obtained by using a doping concentration (N_I) of 1 x 10^{19} cm^{-3} in the above equation.

Problem 2.4:

Calculate the intrinsic carrier concentration in silicon at 300 ^{o}K for a region with doping concentration of 1 x 10^{19} cm^{-3}.

Solution:

The effective intrinsic carrier concentration in silicon at room temperature in the presence of high doping concentration is given by:

$$n_{ie} = 1.4x10^{10} \exp\left(0.433\sqrt{\frac{N_I}{10^{18}}} \right) \qquad \textbf{[P2.4a]}$$

where N_I is the doping concentration in cm^{-3}. The effective intrinsic carrier concentration obtained by using a doping concentration of 1 x 10^{19} cm^{-3} in the above equation is 5.51 x 10^{10} cm^{-3}. This value is a factor of 4-times larger than the intrinsic carrier concentration in lightly doped silicon at room temperature.

Problem 2.5:

Calculate the built-in potential for silicon at 300, 400 and 500 ^{o}K using a doping concentration of 1 x 10^{19} cm^{-3} on the P-side and 1 x 10^{16} cm^{-3} on the N-side of the junction.

Solution:

The built-in voltage is given by:

$$V_{bi} = \frac{kT}{q} \ln\left(\frac{N_A^- . N_D^+}{n_i^2}\right) \qquad \textbf{[P2.5a]}$$

where N_A^- and N_D^+ are the ionized impurity concentrations on the two sides of an abrupt P-N junction. For silicon, their values are equal to the doping concentration because of the small dopant ionization energy levels. The built-in voltage obtained by using a doping concentration of 1 x 10^{19} cm^{-3} on the P-side and 1 x 10^{16} cm^{-3} on the N-side of the junction is given in the table below when the intrinsic carrier concentration in the table for Problem 2.1 is used:

Temperature (^{o}K)	**Built-in Voltage (Volts)**
300	0.877
400	0.736
500	0.588

The built-in voltage decreases with increasing temperature.

Problem 2.6:

Calculate the built-in potential for 4H-SiC at 300, 400 and 500 ^{o}K using a doping concentration of 1 x 10^{19} cm^{-3} on the P-side and 1 x 10^{16} cm^{-3} on the N-side of the junction.

Solution:

The built-in voltage is given by:

$$V_{bi} = \frac{kT}{q} \ln\left(\frac{N_A^- . N_D^+}{n_i^2} \right) \qquad \textbf{[P2.6a]}$$

where N_A^- and N_D^+ are the ionized impurity concentrations on the two sides of an abrupt P-N junction. For silicon, their values are equal to the doping concentration because of the small dopant ionization energy levels. The built-in voltage obtained by using a doping concentration of 1 x 10^{19} cm^{-3} on the P-side and 1 x 10^{16} cm^{-3} on the N-side of the junction is given in the table below when the intrinsic carrier concentration in the table for Problem 2.2 is used:

Temperature (^{o}K)	**Built-in Voltage (Volts)**
300	3.297
400	3.170
500	3.037

The built-in voltage decreases with increasing temperature.

Problem 2.7:

Determine the impact ionization coefficients for electrons and holes in silicon at an electric field of 2 x 10^5 V/cm. What is the ratio of the values?

Solution:

The impact ionization coefficients for semiconductors are dictated by Chynoweth's Law:

$$\alpha = a.e^{-b/E} \qquad \textbf{[P2.7a]}$$

where E is the electric field component in the direction of current flow. The parameters for silicon have been found to be a_n = 7 x 10^5 per cm and b_n = 1.23 x 10^6 V/cm for electrons; a_p = 1.6 x 10^6 per cm and b_p = 2 x 10^6 V/cm for holes for electric fields ranging between 1.75 x 10^5 to 6 x 10^5 V/cm.

At an electric field of 2 x 10^5 V/cm, the impact ionization coefficients for electrons and holes in silicon are found to be 1.49 x 10^3 cm^{-1} and 7.26 x 10^1 cm^{-1}, respectively.

The ratio of the impact ionization coefficient for electrons to that for holes in silicon at an electric field of 2 x 10^5 V/cm is 20.5.

Problem 2.8:

Determine the impact ionization coefficients for holes in 4H-SiC at an electric field of 2 x 10^6 V/cm.

Solution:

The impact ionization coefficients for semiconductors are dictated by Chynoweth's Law:

$$\alpha = a.e^{-b/E} \qquad \textbf{[P2.8a]}$$

where E is the electric field component in the direction of current flow. For defect free material, the extracted values for the impact ionization coefficient parameters for holes in 4H-SiC are:

$$a(4H-SiC) = 6.46x10^6 - 1.07x10^4 T \qquad \textbf{[P2.8b]}$$

with

$$b(4H-SiC) = 1.75x10^7 \qquad \textbf{[P2.8c]}$$

At an electric field of 2 x 10^6 V/cm, the impact ionization coefficient for holes in 4H-SiC is found to be 5.15 x 10^2 cm^{-1}.

Problem 2.9:

Determine the mobility for electrons and holes in silicon at 300, 400 and 500 ^{o}K for a doping concentration of 1 x 10^{14} cm^{-3}. What is the ratio of the values at each temperature?

Solution:

The mobility for electrons in silicon is given by:

$$\mu_n = 1360\left(\frac{T}{300}\right)^{-2.42} \qquad \textbf{[P2.9a]}$$

and the mobility for holes in silicon is given by:

$$\mu_p = 495\left(\frac{T}{300}\right)^{-2.20} \qquad \textbf{[P2.9b]}$$

The mobility computed using these expressions is provided in the table together with the ratio:

Temperature (^{o}K)	**Electron Mobility (cm^2/V-s)**	**Hole Mobility (cm^2/V-s)**	**Ratio**
300	1360	495	2.75
400	678	263	2.58
500	395	161	2.46

The electron and hole mobility in silicon decreases significantly with increasing temperature but the ratio of the mobility remains approximately the same.

Problem 2.10:

Determine the mobility for electrons in 4H-SiC at 300, 400 and 500 ^{o}K for a doping concentration of 1 x 10^{14} cm^{-3}.

Solution:

For 4H-SiC, the temperature dependence of the mobility at low doping concentrations can be modeled by:

$$\mu_n(4H-SiC) = 1140\left(\frac{T}{300}\right)^{-2.70} \qquad \textbf{[P2.10a]}$$

The mobility computed using this expression is provided in the table:

Temperature (^{o}K)	**Electron Mobility (cm^2/V-s)**
300	1140
400	524
500	287

The electron mobility in 4H-SiC decreases by a factor of 3.97-times when compared with a reduction by a factor of 3.44-times for silicon when the temperature increases from 300 to 500 ^{o}K.

Problem 2.11:

Determine the mobility for electrons and holes in silicon at 300 ^{o}K for doping concentrations of 1 x 10^{15} cm^{-3}, 1 x 10^{16} cm^{-3}, 1 x 10^{17} cm^{-3}, 1 x 10^{18} cm^{-3}, and 1 x 10^{19} cm^{-3}.

Solution:

The mobility of electrons in silicon at room temperature as a function of the doping concentration can be modeled by:

$$\mu_n(Si) = \frac{5.10x10^{18} + 92N_D^{0.91}}{3.75x10^{15} + N_D^{0.91}} \qquad \textbf{[P2.11a]}$$

where N_D is the donor concentration per cm^3. The mobility of holes in silicon at room temperature as a function of the doping concentration can be modeled by:

$$\mu_p(Si) = \frac{2.90x10^{15} + 47.7N_A^{0.76}}{5.86x10^{12} + N_A^{0.76}} \qquad \textbf{[P2.11b]}$$

where N_A is the acceptor concentration per cm^3.

The mobility computed using these expressions is provided in the table:

Doping Concentration (cm^{-3})	**Electron Mobility (cm^2/V-s)**	**Hole Mobility (cm^2/V-s)**
1 x 10^{15}	1345	477
1 x 10^{16}	1248	406
1 x 10^{17}	802	233
1 x 10^{18}	263	97
1 x 10^{19}	116	57

Problem 2.12:

Determine the mobility for electrons in 4H-SiC at 300 ^{o}K for doping concentrations of 1 x 10^{15} cm^{-3}, 1 x 10^{16} cm^{-3}, 1 x 10^{17} cm^{-3}, 1 x 10^{18} cm^{-3}, and 1 x 10^{19} cm^{-3}.

Solution:

For 4H-SiC, the mobility of electrons at room temperature as a function of the doping concentration can be modeled by:

$$\mu_n(4H-SiC) = \frac{4.05x10^{13} + 20N_D^{0.61}}{3.55x10^{10} + N_D^{0.61}} \qquad \textbf{[P2.12a]}$$

where N_D is the donor concentration per cm^3.

The electron mobility computed using this expression is provided in the table:

Doping Concentration (cm^{-3})	**Electron Mobility (cm^2/V-s)**
1 x 10^{15}	1100
1 x 10^{16}	985
1 x 10^{17}	695
1 x 10^{18}	324
1 x 10^{19}	114

Problem 2.13:

Calculate the velocity and average mobility for electrons in silicon at 300 ^{o}K for electric field values of 1 x 10^2 V/cm, 1 x 10^3 V/cm, 1 x 10^4 V/cm, and 1 x 10^5 V/cm.

Solution:

At low doping concentrations in silicon, the average mobility for electrons can be related to the electric field using:

$$\mu_n^{av} = \frac{9.85x10^6}{\left(1.04x10^5 + E^{1.3}\right)^{0.77}} \qquad \textbf{[P2.13a]}$$

The velocity for electrons in silicon at 300 ^{o}K can be obtained by multiplying the average velocity with the electric field:

$$v_n = \frac{9.85x10^6\ E}{\left(1.04x10^5 + E^{1.3}\right)^{0.77}} \qquad \textbf{[P2.13b]}$$

The values computed using these expressions are provided in the table:

Electric Field (V/cm)	**Average Electron Mobility (cm^2/V-s)**	**Electron Velocity (cm/s)**
1 x 10^2	1350	1.35 x 10^5
1 x 10^3	1280	1.28 x 10^6
1 x 10^4	662	6.62 x 10^6
1 x 10^5	95	9.5 x 10^5

The velocity for electrons in silicon saturates at a value of 1 x 10^7 cm/s.

Problem 2.14:

Calculate the velocity and average mobility for electrons in 4H-SiC at 300 ^{o}K for electric field values of 1 x 10^2 V/cm, 1 x 10^3 V/cm, 1 x 10^4 V/cm, 1 x 10^5 V/cm, and 1 x 10^6 V/cm.

Solution:

At low doping concentrations in 4H-SiC, the average mobility for electrons can be related to the electric field using:

$$\mu_n^{av} = \frac{\mu_0}{\left[1 + (\mu_0 E / v_{sat,n})^2\right]^{0.5}} \qquad \textbf{[P2.14a]}$$

where μ_0 is the mobility for electrons in 4H-SiC at low electric fields (1140 cm^2/V-s) and $v_{sat,n}$ is the saturated drift velocity for electrons in 4H-SiC, which has a value of 2 x10^7 cm/s.

The velocity for electrons in 4H-SiC at 300 ^{o}K can be obtained by multiplying the average velocity with the electric field:

$$v_n = \frac{\mu_0 \, E}{\left[1 + (\mu_0 E / v_{sat,n})^2\right]^{0.5}} \qquad \textbf{[P2.14b]}$$

The values computed using these expressions are provided in the table:

Electric Field (V/cm)	**Average Electron Mobility (cm^2/V-s)**	**Electron Velocity (cm/s)**
1 x 10^2	1140	1.14 x 10^5
1 x 10^3	1140	1.14 x 10^6
1 x 10^4	990	9.90 x 10^6
1 x 10^5	197	1.97 x 10^7
1 x 10^6	20	2.00 x 10^7

The velocity for electrons in 4H-SiC saturates at a value of 2 x 10^7 cm/s.

Problem 2.15:

Determine the mobility for electrons and holes in silicon at 300 ^{o}K for injected concentrations of 1 x 10^{15} cm^{-3}, 1 x 10^{16} cm^{-3}, 1 x 10^{17} cm^{-3}, 1 x 10^{18} cm^{-3}, and 1 x 10^{19} cm^{-3}. Assume that high-level injection conditions prevail in the material.

Solution:

At high injection levels, the mobility becomes reduced by the carrier-carrier scattering phenomenon. The mobility is then given by:

$$\frac{1}{\mu} = \frac{1}{\mu_0} + \frac{n.\ln\left(1 + 4.54x10^{11} n^{-0.667}\right)}{1.428x10^{20}} \qquad \textbf{[P2.15a]}$$

where μ is the mobility at a carrier density of 'n' per cm^3, and μ_0 is the majority carrier mobility (i.e. either μ_n or μ_p). In deriving this expression, it has been assumed that high level injection conditions prevail so that the concentration of electrons (n) is equal to the concentration of holes (p).

The mobility computed using this expression is provided in the table:

Carrier Concentration (cm^{-3})	**Electron Mobility (cm^2/V-s)**	**Hole Mobility (cm^2/V-s)**
1 x 10^{15}	1310	489
1 x 10^{16}	1110	457
1 x 10^{17}	657	356
1 x 10^{18}	301	217
1 x 10^{19}	139	118

Note that the mobility for electrons and holes becomes nearly equal at very high injection levels.

Problem 2.16:

Determine the intrinsic resistivity for silicon and 4H-SiC at 300 ^{o}K.

Solution:

The intrinsic resistivity (ρ_i) of a semiconductor region is governed by the transport of both carriers as given by:

$$\rho_i = \frac{1}{qn_i\left(\mu_n + \mu_p\right)} \qquad \textbf{[P2.16a]}$$

where μ_n and μ_p are the mobility for electrons and holes, and n_i is the intrinsic carrier concentration.

For the case of silicon at 300 ^{o}K, the intrinsic concentration is 1.38 x 10^{10} cm^{-3}, the mobility for electrons is 1360 cm^2/V-s, and the mobility for holes is 495 cm^2/V-s. Using these values, the intrinsic resistivity for silicon at 300 ^{o}K is found to be 2.44 x 10^5 Ohm-cm.

For the case of 4H-SiC at 300 ^{o}K, the intrinsic concentration is 6.74 x 10^{-11} cm^{-3}, and the mobility for electrons is 1140 cm^2/V-s. The mobility for holes is much smaller than for electrons in 4H-Sic and can be neglected. Using these values, the intrinsic resistivity for 4H-SiC at 300 ^{o}K is found to be 8.13 x 10^{25} Ohm-cm.

The much larger intrinsic resistivity for 4H-SiC when compared with silicon is due to its much greater band-gap.

Problem 2.17:

Determine the resistivity for n- and p-type silicon at 300 ^{o}K for doping concentrations of 1 x 10^{13} cm^{-3}, 1 x 10^{14} cm^{-3}, 1 x 10^{15} cm^{-3}, 1 x 10^{16} cm^{-3}, 1 x 10^{17} cm^{-3}, 1 x 10^{18} cm^{-3}, and 1 x 10^{19} cm^{-3}.

Solution:

The resistivity for n-type silicon is related to the doping concentration by:

$$\rho_n(Si) = \frac{3.75x10^{15} + N_D^{0.91}}{1.47x10^{-17} N_D^{1.91} + 8.15x10^{-1} N_D} \qquad \textbf{[P2.17a]}$$

where N_D is the donor concentration per cm^3. The resistivity for p-type silicon is related to the doping concentration:

$$\rho_p(Si) = \frac{5.86x10^{12} + N_A^{0.76}}{7.63x10^{-18} N_A^{1.76} + 4.64x10^{-4} N_A} \qquad \textbf{[P2.17b]}$$

where N_A is the acceptor concentration per cm^3.

The resistivity computed using these expressions is provided in the table:

Doping Concentration (cm^{-3})	**n-Type Resistivity (Ohm-cm)**	**p-Type Resistivity (Ohm-cm)**
1 x 10^{13}	4.60 x 10^{2}	1.26 x 10^{3}
1 x 10^{14}	4.60 x 10^{1}	1.27 x 10^{2}
1 x 10^{15}	4.65 x 10^{0}	1.31 x 10^{1}
1 x 10^{16}	5.01 x 10^{-1}	1.54 x 10^{0}
1 x 10^{17}	7.80 x 10^{-2}	2.69 x 10^{-1}
1 x 10^{18}	2.37 x 10^{-2}	6.48 x 10^{-2}
1 x 10^{19}	5.39 x 10^{-3}	1.10 x 10^{-2}

Problem 2.18:

Determine the resistivity for n-type 4H-SiC at 300 ^{o}K for doping concentrations of 1 x 10^{13} cm^{-3}, 1 x 10^{14} cm^{-3}, 1 x 10^{15} cm^{-3}, 1 x 10^{16} cm^{-3}, 1 x 10^{17} cm^{-3}, 1 x 10^{18} cm^{-3}, and 1 x 10^{19} cm^{-3}.

Solution:

The resistivity for n-type 4H-SiC can be related to the doping concentration by using the dependence of the mobility on the doping concentration:

$$\rho_n(4H-SiC) = \frac{3.55x10^{10} + N_D^{0.61}}{3.20x10^{-18} N_D^{1.61} + 6.48x10^{-6} N_D} \qquad \textbf{[P2.18a]}$$

where N_D is the donor concentration per cm^3.

The resistivity computed using this expression is provided in the table:

Doping Concentration (cm^{-3})	**n-Type Resistivity (Ohm-cm)**
1 x 10^{13}	5.53 x 10^{2}
1 x 10^{14}	5.53 x 10^{1}
1 x 10^{15}	5.69 x 10^{0}
1 x 10^{16}	6.35 x 10^{-1}
1 x 10^{17}	8.99 x 10^{-2}
1 x 10^{18}	1.93 x 10^{-2}
1 x 10^{19}	5.50 x 10^{-3}

Problem 2.19:

Determine the low-level lifetime at 300 ^{o}K in n-type silicon with doping concentration of 1 x 10^{14} cm^{-3} for the cases of recombination centers located at an energy of 0.3, 0.5, 0.7, and 0.9 eV from the valence band. Assume a value of 1 microsecond for τ_{p0} and 10 for the ζ parameter.

Solution:

The normalized low-level lifetime is given by:

$$\frac{\tau_{LL}}{\tau_{p0}} = \left[1 + e^{(E_r - E_F)/kT}\right] + \zeta\left[e^{(2E_i - E_r - E_F)/kT}\right] \qquad \textbf{[P2.19a]}$$

The Fermi level position can be determined from the doping concentration by using:

$$E_F = E_i + \frac{kT}{q}\ln\frac{N_D}{n_i} \qquad \textbf{[P2.19b]}$$

Using a doping concentration of 1 x 10^{14} cm^{-3}, the Fermi level position is found to be at 0.785 eV above the valence band. Using this value and a ζ parameter of 10 in Eq. [P2.19a] yields the following values for the low-level lifetime:

Recombination Level Position (eV)	**Low-Level Lifetime (μs)**
0.3	27.4
0.5	1.01
0.7	1.04
0.9	86.3

The smallest value for the low-level lifetime is observed when the recombination center is located near the mid-gap position.

Problem 2.20:

Determine the space-charge-generation lifetime at 300 ^{o}K in n-type silicon with doping concentration of 1 x 10^{14} cm^{-3} for the cases of recombination centers located at an energy of 0.3, 0.5, 07, and 0.9 eV from the valence band. Assume a value of 1 microsecond for τ_{p0} and 10 for the ζ parameter.

Solution:

The space-charge-generation lifetime is given by:

$$\tau_{SC} = \tau_{p0}\left[e^{(E_r - E_i)/kT} + \zeta . e^{(E_i - E_r)/kT}\right] \qquad \textbf{[P2.20a]}$$

Using a τ_{p0} value of 1 microsecond and a ζ parameter of 10 in Eq. [P2.20a] yields the following values for the space-charge-generation lifetime:

Recombination Level Position (eV)	**Space-Charge Generation Lifetime (s)**
0.3	1.90 x 10^{-1}
0.5	8.37 x 10^{-5}
0.7	2.70 x 10^{-4}
0.9	6.10 x 10^{-1}

The smallest value for the space-charge-generation lifetime is observed when the recombination center is located near the mid-gap position.

Problem 2.21:

Determine the high-level lifetime at 300 ^{o}K in n-type silicon with doping concentration of 1 x 10^{14} cm^{-3} for the cases of recombination centers located at an energy of 0.3, 0.5, 07, and 0.9 eV from the valence band. Assume a value of 1 microsecond for τ_{p0} and 10 for the ζ parameter.

Solution:

The normalized high level lifetime is given by:

$$\frac{\tau_{HL}}{\tau_{p0}} = 1 + \zeta \qquad \textbf{[P2.21a]}$$

From this expression, it can be seen that the high level lifetime is not dependent on the position of the recombination center and the Fermi level. A high level lifetime of 11 microseconds is obtained by using a τ_{p0} value of 1 microsecond and a ζ parameter of 10 in Eq. [P2.21a].

Problem 2.22:

Determine the Auger recombination lifetime at 300 ^{o}K in n- and p-type silicon with doping concentration of 1 x 10^{19} cm^{-3}.

Solution:

In the case of heavily doped n-type silicon, since the Auger process transfers the energy and momentum due to recombination to an electron in the conduction band, Auger recombination lifetime is given by:

$$\tau_A^N = \frac{1}{C_{AN}.n^2} = \frac{1}{2.8x10^{-31}.n^2} \qquad \textbf{[P2.22a]}$$

where n is the concentration of electrons. The Auger recombination lifetime obtained for the case of an n-type doping concentration of 1 x 10^{19} cm^{-3} by using this equation is 35.7 nanoseconds.

In the case of heavily doped p-type silicon, since the Auger process transfers the energy and momentum due to recombination to a hole in the valence band, Auger recombination lifetime is given by:

$$\tau_A^P = \frac{1}{C_{AP}.p^2} = \frac{1}{1.0x10^{-31}.p^2} \qquad \textbf{[2.90]}$$

where p is the concentration of holes. The Auger recombination lifetime obtained for the case of a p-type doping concentration of 1 x 10^{19} cm^{-3} by using this equation is 100 nanoseconds.

Chapter 3:
Breakdown Voltage

Problem 3.1:

Compare the impact ionization coefficient obtained using Fulop's approximation to that for electrons and holes in silicon at an electric field of 2 x 10^5 V/cm.

Solution:

The Fulop's approximation for the impact ionization coefficient in silicon is given by:

$$\alpha_F(Si) = 1.8x10^{-35} E^7 \qquad \textbf{[P3.1a]}$$

The impact ionization coefficient obtained by using this formula at an electric field of 2 x 10^5 V/cm is 2.30 x 10^2 cm^{-1}.

At an electric field of 2 x 10^5 V/cm, the impact ionization coefficients for electrons and holes in silicon are found to be 1.49 x 10^3 cm^{-1} and 7.26 x 10^1 cm^{-1}, respectively. (See Problem 2.7).

The Fulop's approximation underestimates the impact ionization when compared with that for electrons by 6.48-times and over-estimates its value when compared with the value for holes by 3.17-times.

Problem 3.2:

Compare the impact ionization coefficient obtained using Baliga's approximation to that for holes in 4H-SiC at an electric field of 2 x 10^6 V/cm.

Solution:

The Baliga's power law approximation for the impact ionization coefficients for 4H-SiC is:

$$\alpha_B(4H-SiC) = 3.9x10^{-42}E^7 \qquad \textbf{[P3.2a]}$$

The impact ionization coefficient obtained by using this formula at an electric field of 2 x 10^6 V/cm is 4.99 x 10^2 cm^{-1}.

At an electric field of 2 x 10^6 V/cm, the impact ionization coefficient for holes in 4H-SiC is found to be 5.15 x 10^2 cm^{-1}. (See Problem 2.8).

The Baliga's approximation for the impact ionization is within 5 percent of that for holes in 4H-SiC.

Problem 3.3:

Calculate the parallel-plane breakdown voltage for silicon abrupt P-N junctions at drift region doping concentrations of 1 x 10^{13} cm^{-3}, 1 x 10^{14} cm^{-3}, 1 x 10^{15} cm^{-3}, and 1 x 10^{16} cm^{-3}.

Solution:

The parallel-plane breakdown voltage for an abrupt junction in silicon can be obtained by using:

$$BV_{PP}(Si) = 5.34x10^{13} N_D^{-3/4} \qquad \textbf{[P3.3a]}$$

The breakdown voltages obtained by using this equation are provided in the table below:

Doping Concentration (cm^{-3})	**Breakdown Voltage (Volts)**
1 x 10^{13}	9.50 x 10^{3}
1 x 10^{14}	1.69 x 10^{3}
1 x 10^{15}	3.00 x 10^{2}
1 x 10^{16}	5.34 x 10^{1}

Problem 3.4:

Calculate the parallel-plane breakdown voltage for 4H-SiC abrupt P-N junctions at drift region doping concentrations of 1 x 10^{14} cm^{-3}, 1 x 10^{15} cm^{-3}, 1 x 10^{16} cm^{-3}, and 1 x 10^{17} cm^{-3}.

Solution:

The parallel-plane breakdown voltage for an abrupt junction in silicon can be obtained by using:

$$BV_{PP}(4H-SiC) = 3.0x10^{15} N_D^{-3/4} \qquad \textbf{[P3.4a]}$$

The breakdown voltages obtained by using this equation are provided in the table below:

Doping Concentration (cm^{-3})	**Breakdown Voltage (Volts)**
1 x 10^{14}	9.46 x 10^{4}
1 x 10^{15}	1.68 x 10^{4}
1 x 10^{16}	2.99 x 10^{3}
1 x 10^{17}	5.32 x 10^{2}

Problem 3.5:

Calculate the maximum depletion layer width at breakdown for silicon abrupt P-N junctions at drift region doping concentrations of 1 x 10^{13} cm^{-3}, 1 x 10^{14} cm^{-3}, 1 x 10^{15} cm^{-3}, and 1 x 10^{16} cm^{-3}.

Solution:

The maximum depletion layer width at breakdown for an abrupt junction in silicon can be obtained by using:

$$W_{PP}(Si) = 2.67x10^{10} N_D^{-7/8} \qquad \textbf{[P3.5a]}$$

The maximum depletion layer widths at breakdown obtained by using this equation are provided in the table below:

Doping Concentration (cm^{-3})	**Maximum Depletion Width (microns)**
1 x 10^{13}	1.13 x 10^{3}
1 x 10^{14}	1.50 x 10^{2}
1 x 10^{15}	2.00 x 10^{1}
1 x 10^{16}	2.67 x 10^{0}

Problem 3.6:

Calculate the maximum depletion layer width at breakdown for 4H-SiC abrupt P-N junctions at drift region doping concentrations of 1 x 10^{14} cm^{-3}, 1 x 10^{15} cm^{-3}, 1 x 10^{16} cm^{-3}, and 1 x 10^{17} cm^{-3}.

Solution:

The maximum depletion layer width at breakdown for an abrupt junction in 4H-SiC can be obtained by using:

$$W_{PP}(4H-SiC) = 1.82x10^{11} N_D^{-7/8} \qquad \textbf{[P3.6a]}$$

The maximum depletion layer widths at breakdown obtained by using this equation are provided in the table below:

Doping Concentration (cm^{-3})	**Maximum Depletion Width (microns)**
1 x 10^{14}	1.02 x 10^{3}
1 x 10^{15}	1.37 x 10^{2}
1 x 10^{16}	1.82 x 10^{1}
1 x 10^{17}	2.43 x 10^{0}

Problem 3.7:

Compare the critical electric field at breakdown for silicon and 4H-SiC abrupt P-N junctions with the same breakdown voltage of 1000 volts.

Solution:

The critical electric field for breakdown in silicon is given by:

$$E_C(Si) = 4010.N_D^{1/8} \qquad \textbf{[P3.7a]}$$

while that for 4H-SiC is given by:

$$E_C(4H-SiC) = 3.3x10^4 N_D^{1/8} \qquad \textbf{[P3.7b]}$$

The doping concentration required in the drift region to obtain a breakdown voltage of 1000 volts is 2.00 x 10^{14} cm^{-3} for silicon and 4.32 x 10^{16} cm^{-3} for 4H-SiC. Using these values in the above equations, the critical electric field at breakdown for silicon and 4H-SiC abrupt P-N junctions with the same breakdown voltage of 1000 volts are found to be 2.46 x 10^5 V/cm and 3.96 x 10^6 V/cm, respectively. It is more meaningful from a design viewpoint to compare these values rather than the critical electric field at the same doping concentration for the two semiconductors.

Problem 3.8:

Compare the ideal specific on-resistance for the drift region in silicon and 4H-SiC devices with the same breakdown voltage of 1000 volts.

Solution:

The specific on-resistance is given by:

$$R_{on,sp} = \frac{W_{PP}}{q\mu_n N_D} \qquad \textbf{[P3.8a]}$$

The doping concentration required in the drift region to obtain a breakdown voltage of 1000 volts is 2.00 x 10^{14} cm^{-3} for silicon and 4.32 x 10^{16} cm^{-3} for 4H-SiC. The mobility values for electrons at these doping concentrations are 1357 and 823 cm^2/V-s for silicon and 4H-SiC, respectively. The depletion layer widths for an abrupt parallel-plane junction at breakdown in silicon and 4H-SiC are 81.9 and 5.06 microns, respectively. Using these values in the above equation, the ideal specific on-resistance for the drift region in silicon and 4H-SiC devices with the same breakdown voltage of 1000 volts is found to be 189 and 0.089 millOhm-cm^2, respectively. The ratio of the ideal specific on-resistance for the drift region in silicon and 4H-SiC devices with the same breakdown voltage of 1000 volts is found to be 2120.

Problem 3.9:

Calculate the width of the drift region for a silicon punch-through diode to achieve a breakdown voltage of 1000 volts if the drift region doping concentration is 2 x 10^{13} cm^{-3}.

Solution:

The breakdown voltage for the punch-through diode is given by:

$$BV_{PT} = E_c W_P - \frac{qN_{AP}W_P^2}{2\varepsilon_S} \qquad \textbf{[P3.9a]}$$

The second term in this equation can be neglected because the doping concentration in the drift region is very low. Consequently:

$$BV_{PT} = E_c W_P \qquad \textbf{[P3.9b]}$$

The critical electric field for breakdown for a doping concentration of 2 x 10^{13} cm^{-3} is 1.84 x 10^5 V/cm for silicon. Using this value in the above equation with a breakdown voltage of 1000 volts yields a width of the drift region for a silicon punch-through diode of 54.3 microns.

Problem 3.10:

Calculate the width of the drift region for a 4H-SiC punch-through diode to achieve a breakdown voltage of 1000 volts if the drift region doping concentration is 1 x 10^{15} cm^{-3}.

Solution:

The breakdown voltage for the punch-through diode is given by:

$$BV_{PT} = E_c W_P - \frac{qN_{AP}W_P^2}{2\varepsilon_S} \qquad \textbf{[P3.10a]}$$

The critical electric field for breakdown for a doping concentration of 2 x 10^{13} cm^{-3} is 2.47 x 10^6 V/cm for 4H-SiC. Using this value in the above equation with a breakdown voltage of 1000 volts yields a width of the drift region for a 4H-SiC punch-through diode of 4.09 microns.

If the second term in the above equation is neglected:

$$BV_{PT} = E_c W_P \qquad \textbf{[P3.10b]}$$

The width of the drift region for a 4H-SiC punch-through diode is found to be 4.05 microns by suing this equation.

Problem 3.11:

Calculate the breakdown voltage for a cylindrical junction termination with a depth of 3 microns for a silicon drift region with doping concentration of 1 x 10^{14} cm^{-3}.

Solution:

The maximum depletion layer width at breakdown in silicon is given by:

$$W_{PP}(Si) = 2.67x10^{10} N_D^{-7/8} \qquad \textbf{[P3.11a]}$$

For a doping concentration of 1 x 10^{14} cm^{-3}, the maximum depletion layer width at breakdown is found to be 150 microns. Using this value, the normalized radius of curvature (r_J/W_{PP}) is found to be 0.020.

The normalized breakdown voltage for a cylindrical junction is given by:

$$\frac{BV_{CYL}}{BV_{PP}} = \frac{1}{2}\left[\left(\frac{r_J}{W_{PP}}\right)^2 + 2\left(\frac{r_J}{W_{PP}}\right)^{6/7}\right].\ln\left[1 + 2\left(\frac{W_{PP}}{r_J}\right)^{8/7}\right] - \left(\frac{r_J}{W_{PP}}\right)^{6/7} \qquad \textbf{[P3.11b]}$$

Using a normalized radius of curvature (r_J/W_{PP}) of 0.020 yields a normalized breakdown voltage for the cylindrical junction termination of 0.147. The parallel-plane breakdown voltage is 1690 at a doping concentration of 1 x 10^{14} cm^{-3}. Consequently, the breakdown voltage for the cylindrical junction termination is 248 volts.

Problem 3.12:

Calculate the breakdown voltage for a spherical junction termination with a depth of 3 microns for a silicon drift region with doping concentration of 1 x 10^{14} cm^{-3}.

Solution:

The maximum depletion layer width at breakdown in silicon is given by:

$$W_{PP}(Si) = 2.67x10^{10} N_D^{-7/8} \qquad \textbf{[P3.12a]}$$

For a doping concentration of 1 x 10^{14} cm^{-3}, the maximum depletion layer width at breakdown is found to be 150 microns. Using this value, the normalized radius of curvature (r_J/W_{PP}) is found to be 0.020.

The normalized breakdown voltage for the spherical junction is given by:

$$\frac{BV_{SP}}{BV_{PP}} = \left(\frac{r_J}{W_{PP}}\right)^2 + 2.14\left(\frac{r_J}{W_{PP}}\right)^{6/7} - \left[\left(\frac{r_J}{W_{PP}}\right)^3 + 3\left(\frac{r_J}{W_{PP}}\right)^{13/7}\right]^{2/3} \qquad \textbf{[P3.12b]}$$

Using a normalized radius of curvature (r_J/W_{PP}) of 0.020 yields a normalized breakdown voltage for the spherical junction termination of 0.059. The parallel-plane breakdown voltage is 1690 at a doping concentration of 1 x 10^{14} cm^{-3}. Consequently, the breakdown voltage for the cylindrical junction termination is 99.7 volts. This value is 2.5-times smaller than that obtained for the cylindrical edge termination.

Problem 3.13:

Calculate the breakdown voltage for a junction termination using the single optimally located floating field ring with a depth of 3 microns for a silicon drift region with doping concentration of 1 x 10^{14} cm^{-3}.

Solution:

The maximum depletion layer width at breakdown in silicon is given by:

$$W_{PP}(Si) = 2.67x10^{10} N_D^{-7/8} \qquad \textbf{[P3.13a]}$$

For a doping concentration of 1 x 10^{14} cm^{-3}, the maximum depletion layer width at breakdown is found to be 150 microns. Using this value, the normalized radius of curvature (r_J/W_{PP}) is found to be 0.020.

The breakdown voltage for a junction termination using the single optimally located floating field ring is given by:

$$\left(\frac{BV_{FFR} - BV_{CYL}}{BV_{PP}}\right) = \frac{1}{2}\left(\frac{r_J}{W_{PP}}\right)^2 - 0.96\left(\frac{r_J}{W_{PP}}\right)^{6/7}$$

$$+1.92\left(\frac{r_J}{W_{PP}}\right)^{6/7} \ln\left[1.386\left(\frac{W_{PP}}{r_J}\right)^{4/7}\right] \qquad \textbf{[P3.13b]}$$

Using a normalized radius of curvature (r_J/W_{PP}) of 0.020 yields a normalized breakdown voltage for the spherical junction termination of 0.286. The parallel-plane breakdown voltage is 1690 at a doping concentration of 1 x 10^{14} cm^{-3}. Consequently, the breakdown voltage for the cylindrical junction termination is 483 volts. This value is 2.0-times larger than that obtained for the cylindrical edge termination.

Problem 3.14:

Determine the spacing for the single optimally located floating field ring in the previous problem. What is the mask dimension required for this design?

Solution:

The optimum field ring spacing in terms of the breakdown voltage of the cylindrical and floating field ring cases, when the spacing is normalized to the depletion width of the parallel-plane junction at breakdown, is given by:

$$\frac{W_S}{W_{PP}} = \sqrt{\frac{BV_{FFR}}{BV_{PP}}} - \sqrt{\left(\frac{BV_{FFR}}{BV_{PP}}\right) - \left(\frac{BV_{CYL}}{BV_{PP}}\right)} \qquad \textbf{[P3.14a]}$$

Using a normalized breakdown voltage of 0.286 and 0.147 for the floating field ring and cylindrical junction terminations yield a normalized optimum spacing of 0.162. For a doping concentration of 1 x 10^{14} cm^{-3}, the maximum depletion layer width at breakdown is 150 microns. Thus, the optimum field ring spacing is 24.3 microns.

Once the optimum spacing of W_S is obtained, the spacing on the mask is given by:

$$W_M = W_S + 2x_J \qquad \textbf{[P3.14b]}$$

Using a junction depth (xJ) of 3 microns, the optimum spacing on the mask is found to be 30.3 microns.

Problem 3.15:

Determine the normalized surface electric field for a positive bevel termination with an angle of 45 degrees.

Solution:

The normalized maximum electric field at the surface of a positive bevel (E_{mPB}/E_{mB}) is given by:

$$\frac{E_{mPB}}{E_{mB}} = \left(\frac{\sin(\theta)}{1+\cos(\theta)} \right) \qquad \textbf{[3.77]}$$

For a positive bevel termination with an angle of 45 degrees, the normalized surface electric field is found to be 0.414. This reduction of the surface electric field with a positive bevel enables obtaining parallel-plane breakdown voltage with stable operation using typical surface passivation techniques.

Problem 3.16:

Determine the normalized surface electric field for a negative bevel termination with an angle of 3 degrees if the ratio of the depletion layer widths on the lightly doped side to the heavily doped side of the junction is 10.

Solution:

The maximum normalized electric field at the surface of a negative bevel (E_{mNB}/E_{mB}) is given by:

$$\frac{E_{mNB}}{E_{mB}} = \frac{W_N}{W_P}\sin(\theta) \qquad \textbf{[P3.16a]}$$

For a negative bevel termination with an angle of 3 degrees, the normalized surface electric field is found to be 0.523 if the ratio of the depletion layer widths (W_N/W_P) on the lightly doped side to the heavily doped side of the junction is 10. This reduction of the surface electric field with a shallow negative bevel enables obtaining stable operation using typical surface passivation techniques.

Problem 3.17:

Determine the optimum charge for the junction termination extension in a silicon device.

Solution:

The optimum charge for the junction termination extension is:

$$Q_{OPT} = \varepsilon_S E_C \qquad \textbf{[P3.17a]}$$

Using a critical electric field of 2 x 10^5 V/cm for silicon and a relative dielectric constant of 11.7 in the above equation yields an optimum charge of 2.09 x 10^{-7} C/cm^2. This corresponds to a dose for the JTE region of 1.3 x 10^{12} cm^{-2}.

Problem 3.18:

Determine the optimum charge for the junction termination extension in a 4H-SiC device.

Solution:

The optimum charge for the junction termination extension is:

$$Q_{OPT} = \varepsilon_S E_C \qquad \textbf{[P3.18a]}$$

Using a critical electric field of 2.5 x 10^6 V/cm for 4H-SiC and a relative dielectric constant of 9.7 in the above equation yields an optimum charge of 2.15 x 10^{-6} C/cm^2. This corresponds to a dose for the JTE region of 1.34 x 10^{13} cm^{-2}.

Problem 3.19:

Calculate the breakdown voltage for an open-base silicon transistor with a drift region doping concentration of 5 x 10^{13} cm^{-3} and thickness of 300 microns if the low-level lifetime is 10 microseconds. Compare this value to the avalanche breakdown voltage and the reach-through breakdown voltage.

Solution:

The criterion for breakdown for the open-base transistor can therefore be written as:

$$\alpha_{PNP} = \gamma_E \alpha_T M = 1 \qquad \textbf{[P3.19a]}$$

where M is the multiplication coefficient. Due to the low doping concentration in the N-base region, the injection efficiency can be assumed to be equal to unity. The base transport factor is less than unity as determined by the un-depleted base width ($W_N - W_D$) and the minority carrier diffusion length (L_p):

$$\alpha_T = \cosh^{-1}\left[\frac{W_N - W_D}{L_p}\right] \qquad \textbf{[P3.19b]}$$

where W_D is the width of the depletion layer. The thickness of the depletion region (W_D) is related to the applied reverse bias (V_a):

$$W_D = \sqrt{\frac{2\varepsilon_S V_a}{qN_D}} \qquad \textbf{[P3.19c]}$$

The multiplication coefficient for a high voltage P^+/N diode is given by:

$$M_p = \frac{1}{1-(V/BV)^6} \qquad \textbf{[P3.19d]}$$

where V is the applied reverse bias voltage and BV is the breakdown voltage.

Using a drift region doping concentration of 5 x 10^{13} cm^{-3}, thickness of 300 microns, and a low-level lifetime of 10 microseconds in the above equations, the current gain (α_{PNP}) is found to become equal to unity at an applied bias of 2085 volts. This value is the open-base transistor breakdown voltage. In comparison, the avalanche breakdown voltage is 2840 volts and the reach-through breakdown voltage is 3473 volts.

Problem 3.20:

Determine the impact of changing the drift region doping concentration to 2 x 10^{13} cm^{-3} in the previous problem.

Solution:

The open-base transistor breakdown voltage is reduced to 1380 volts when the doping concentration in the drift region is reduced to 2 x 10^{13} cm^{-3}. This corresponds to a reach-through breakdown voltage of 1389 volts.

Chapter 4
Schottky Rectifiers

Problem 4.1:

Calculate the barrier height for a Schottky contact to silicon made using a metal with a work function of 4.6 eV.

Solution:

The Schottky barrier height is given by:

$$\Phi_{BN} = \Phi_M - \chi_S \qquad \textbf{[P4.1a]}$$

Using the work function of 4.6 eV for the metal and an electron affinity of 4.05 eV for silicon, the barrier height is found to be 0.55 eV.

Problem 4.2:

Calculate the specific resistance for the ideal drift region for a silicon Schottky barrier rectifier designed to block 100-V.

Solution:

The specific on-resistance of the drift region for silicon is given by:

$$R_{D,SP} = R_{on-ideal}(Si) = 5.93x10^{-9} BV^{2.5} \qquad \textbf{[P4.2a]}$$

For the case of a breakdown voltage of 100 volts, the specific on-resistance of the drift region for silicon is found to be 5.93 x 10^{-4} Ohm-cm^2.

Problem 4.3:

Calculate the on-state voltage drop for a Silicon Schottky barrier rectifier designed to block 100-V under the following assumptions: (a) parallel-plane breakdown voltage; (b) On-state current density of 100 A/cm^2; (c) Barrier height of 0.8 eV; (d) Operation at room temperature (300^{o}K); (e) Zero substrate and ohmic contact resistance. Provide the voltage drop across the Schottky barrier and the drift region.

Solution:

The on-state voltage drop (V_F) for the power Schottky rectifier, including the resistive voltage drop, is given by:

$$V_F = \frac{kT}{q}\ln\left(\frac{J_F}{J_S}\right) + R_{S,SP}J_F \qquad \textbf{[P4.3a]}$$

where J_F is the forward (on-state) current density, J_S is the saturation current density, and $R_{S,SP}$ is the total series specific resistance. In this expression, the saturation current is given by:

$$J_S = AT^2 e^{-(q\Phi_{BN}/kT)} \qquad \textbf{[P4.3b]}$$

and the total series specific resistance is given by:

$$R_{S,SP} = R_{D,SP} + R_{SUB} + R_{CONT} \qquad \textbf{[P4.3c]}$$

Using a barrier height of 0.8 eV, the saturation current density is found to be 3.81 x 10^{-7} A/cm^2 at 300 ^{o}K. The specific series resistance for the drift region is found to be 5.93 x 10^{-4} Ohm-cm^2 (see Problem 4.2). This is also the total series specific resistance in this problem. Substituting these values in Eq. [P4.3a], the on-state voltage drop (V_F) for the power Schottky rectifier is found to be 0.561 volts. The voltage drops across the Schottky barrier and the drift region are 0.502 and 0.059 volts, respectively. The voltage drop across the Schottky barrier is dominant in this case.

Problem 4.4:

Calculate the specific resistance for the ideal drift region for a silicon Schottky barrier rectifier designed to block 1000-V.

Solution:

The specific on-resistance of the drift region for silicon is given by:

$$R_{D,SP} = R_{on-ideal}(Si) = 5.93x10^{-9} BV^{2.5} \qquad \textbf{[P4.4a]}$$

For the case of a breakdown voltage of 1000 volts, the specific on-resistance of the drift region for silicon is found to be 1.87 x 10^{-1} Ohm-cm^2.

Problem 4.5:

Calculate the on-state voltage drop for a Silicon Schottky barrier rectifier designed to block 1000-V under the following assumptions: (a) parallel-plane breakdown voltage; (b) On-state current density of 100 A/cm^2; (c) Barrier height of 0.8 eV; (d) Operation at room temperature (300^{o}K); (e) Zero substrate and ohmic contact resistance. Provide the voltage drop across the Schottky barrier and the drift region.

Solution:

The on-state voltage drop (V_F) for the power Schottky rectifier, including the resistive voltage drop, is given by:

$$V_F = \frac{kT}{q}\ln\left(\frac{J_F}{J_S}\right) + R_{S,SP}J_F \qquad \textbf{[P4.5a]}$$

where J_F is the forward (on-state) current density, J_S is the saturation current density, and $R_{S,SP}$ is the total series specific resistance. In this expression, the saturation current is given by:

$$J_S = AT^2 e^{-(q\Phi_{BN}/kT)} \qquad \textbf{[P4.5b]}$$

and the total series specific resistance is given by:

$$R_{S,SP} = R_{D,SP} + R_{SUB} + R_{CONT} \qquad \textbf{[P4.5c]}$$

Using a barrier height of 0.8 eV, the saturation current density is found to be 3.81 x 10^{-7} A/cm^2 at 300 ^{o}K. The specific series resistance for the drift region is found to be 1.87 x 10^{-1} Ohm-cm^2 (see Problem 4.4). This is also the total series specific resistance in this problem. Substituting these values in Eq. [P4.5a], the on-state voltage drop (V_F) for the power Schottky rectifier is found to be 19.25 volts. The voltage drops across the Schottky barrier and the drift region are 0.502 and 18.75 volts, respectively. The voltage drop across the drift region is dominant in this case.

Problem 4.6:

Calculate the specific resistance for the ideal drift region for a 4H-SiC Schottky barrier rectifier designed to block 1000-V.

Solution:

The specific on-resistance of the drift region for 4H-SiC is given by:

$$R_{D,SP} = R_{on-ideal}(4H-SiC) = 2.97x10^{-12} BV^{2.5} \qquad \textbf{[P4.6a]}$$

For the case of a breakdown voltage of 1000 volts, the specific on-resistance of the drift region for 4H-SiC is found to be 9.39 x 10^{-5} Ohm-cm^2.

Problem 4.7:

Calculate the on-state voltage drop for a 4H-SiC Schottky barrier rectifier designed to block 1000-V under the following assumptions: (a) parallel-plane breakdown voltage; (b) On-state current density of 100 A/cm^2; (c) Barrier height of 1.1 eV; (d) Operation at room temperature (300^{o}K); (e) Zero substrate and ohmic contact resistance. Provide the voltage drop across the Schottky barrier and the drift region.

Solution:

The on-state voltage drop (V_F) for the power Schottky rectifier, including the resistive voltage drop, is given by:

$$V_F = \frac{kT}{q}\ln\left(\frac{J_F}{J_S}\right) + R_{S,SP}J_F \qquad \textbf{[P4.7a]}$$

where J_F is the forward (on-state) current density, J_S is the saturation current density, and $R_{S,SP}$ is the total series specific resistance. In this expression, the saturation current is given by:

$$J_S = AT^2 e^{-(q\Phi_{BN}/kT)} \qquad \textbf{[P4.7b]}$$

and the total series specific resistance is given by:

$$R_{S,SP} = R_{D,SP} + R_{SUB} + R_{CONT} \qquad \textbf{[P4.7c]}$$

Using a barrier height of 1.1 eV, the saturation current density is found to be 4.52 x 10^{-12} A/cm^2 at 300 ^{o}K. The specific series resistance for the drift region is found to be 9.39 x 10^{-5} Ohm-cm^2 (see Problem 4.6). This is also the total series specific resistance in this problem. Substituting these values in Eq. [P4.7a], the on-state voltage drop (V_F) for the power Schottky rectifier is found to be 0.805 volts. The voltage drops across the Schottky barrier and the drift region are 0.796 and 0.009 volts, respectively. The voltage drop across the Schottky barrier is dominant in this case.

Problem 4.8:

A Silicon Schottky barrier rectifier is designed to block 100-V.
(a) Calculate the leakage current density without Schottky barrier lowering.
(b) Calculate the leakage current density with Schottky barrier lowering.
(c) What is the barrier reduction in eV due to the image force?
Use the following assumptions: (a) parallel-plane breakdown voltage; (b) Reverse bias voltage of 80V; (c) Barrier height of 0.8 eV; (d) No impact ionization (e) No generation or diffusion current.

Solution:

(a) Without Schottky barrier lowering, the leakage current is determined by the saturation current:

$$J_L = -AT^2 e^{-(q\Phi_{BN}/kT)} = -J_S \qquad \textbf{[P4.8a]}$$

For a barrier height of 0.8 eV, the leakage current density is found to be 3.81 x 10^{-7} A/cm^2 at 300 ^{o}K.

(b) Assuming parallel-plane breakdown voltage, the doping concentration in the drift region required to obtain a breakdown voltage of 100 volts in silicon is 4.33 x 10^{15} cm^{-3} (using Eq. [3.18]). With Schottky barrier lowering, the leakage current density is found to be 4.43 x 10^{-6} A/cm^2 at 300 ^{o}K at a reverse bias of 80 volts. This is a factor of 11.6-times larger than without the Schottky barrier lowering.

(c) The barrier reduction due to the image force lowering is 0.064 eV at a reverse bias of 80 volts.

Comment: A further increase in the leakage current by a factor of 3.89-times occurs due to the pre-breakdown multiplication effect (see Eq. [4.28].

Problem 4.9:

A 4H-SiC Schottky barrier rectifier is designed to block 1000-V.
(a) Calculate the leakage current density without Schottky barrier lowering and tunneling.
(b) Calculate the leakage current density with Schottky barrier lowering but without tunneling.
(c) Calculate the leakage current density with Schottky barrier lowering and tunneling.
(d) What is the barrier reduction in eV due to the image force?
Use the following assumptions: (a) parallel-plane breakdown voltage; (b) Reverse bias voltage of 800V; (c) Barrier height of 1.1 eV; (d) No impact ionization (e) No generation or diffusion current.

Solution:

(a) Without Schottky barrier lowering and tunneling, the leakage current is determined by the saturation current:

$$J_L = -AT^2 e^{-(q\Phi_{BN}/kT)} = -J_S \qquad \textbf{[P4.9a]}$$

For a barrier height of 1.1 eV, the leakage current density in 4H-SiC is found to be 4.52 x 10^{-12} A/cm^2 at 300 ^{o}K.
(b) Assuming parallel-plane breakdown voltage, the doping concentration in the drift region required to obtain a breakdown voltage of 1000 volts in 4H-SiC is 4.31 x 10^{16} cm^{-3} (using Eq. [3.20]). With Schottky barrier lowering, the leakage current density is found to be 3.48 x 10^{-8} A/cm^2 at 300 ^{o}K at a reverse bias of 800 volts. This is a factor of 7700-times larger than without the Schottky barrier lowering.
(c) The thermionic field emission model for the tunneling current leads to a barrier lowering effect proportional to the square of the electric field at the metal-semiconductor interface. When combined with the thermionic emission model, the leakage current density can be written as:

$$J_S = AT^2 \exp\left(-\frac{q\phi_{BN}}{kT}\right).\exp\left(\frac{q\Delta\phi_{BN}}{kT}\right).\exp\left(C_T E_M^2\right) \qquad \textbf{[P4.9b]}$$

where C_T is a tunneling coefficient (8 x 10^{-13} cm^2/V^2). At a reverse bias of 800 volts for this rectifier structure, the maximum electric field is found to be 3.59 x 10^6 V/cm. Using this value and the barrier reduction [provided in part (d) below], the leakage current density is found to be 1.05 x 10^{-3} A/cm^2 at 300 ^{o}K at a reverse bias of 800 volts. This is a factor of 30,000-times larger than without the tunneling effect.
(d) The barrier reduction due to the image force lowering is 0.231 eV at a reverse bias of 800 volts.

Problem 4.10:

Calculate the specific capacitance for a silicon Schottky barrier rectifier designed to block 100-V at reverse bias voltages of 10, 20, 40, and 80 volts.

Solution:

The specific capacitance (capacitance per unit area) associated with the depletion region of a reverse biased Schottky rectifier is given by:

$$C_{SBD,SP} = \frac{\varepsilon_S}{W_D} \qquad \textbf{[P4.10a]}$$

where ε_S is the dielectric constant of the semiconductor. Assuming parallel-plane breakdown voltage, the doping concentration in the drift region required to obtain a breakdown voltage of 100 volts in silicon is 4.33×10^{15} cm^{-3} (using Eq. [3.18]).

The thickness of the depletion region (W_D) is related to the applied reverse bias voltage (V_R) by:

$$W_D = \sqrt{\frac{2\varepsilon_S}{qN_D}\left(V_R + V_{bi}\right)} \qquad \textbf{[P4.10b]}$$

where V_{bi} is the built-in voltage. The width of the depletion region for the silicon Schottky rectifier at the various reverse bias voltages calculated by using this expression with a built-in voltage of 0.5 volts are given in the table below. The specific capacitance for a silicon Schottky barrier rectifier at the various reverse bias voltages calculated using this depletion width is also provided in the table.

Reverse Bias Voltage (Volts)	**Depletion Width (microns)**	**Specific Capacitance (F/cm^2)**
10	1.79	5.79×10^{-9}
20	2.49	4.16×10^{-9}
40	3.49	2.97×10^{-9}
80	4.91	2.11×10^{-9}

Problem 4.11:

Calculate the specific capacitance for a 4H-SiC Schottky barrier rectifier designed to block 1000-V at reverse bias voltages of 100, 200, 400, and 800 volts.

Solution:

The specific capacitance (capacitance per unit area) associated with the depletion region of a reverse biased Schottky rectifier is given by:

$$C_{SBD,SP} = \frac{\varepsilon_S}{W_D} \qquad \textbf{[P4.11a]}$$

where ε_S is the dielectric constant of the semiconductor. Assuming parallel-plane breakdown voltage, the doping concentration in the drift region required to obtain a breakdown voltage of 1000 volts in 4H-SiC is 4.31 x 10^{16} cm^{-3} (using Eq. [3.20]).

The thickness of the depletion region (W_D) is related to the applied reverse bias voltage (V_R) by:

$$W_D = \sqrt{\frac{2\varepsilon_S}{qN_D}\left(V_R + V_{bi}\right)} \qquad \textbf{[P4.11b]}$$

where V_{bi} is the built-in voltage. The width of the depletion region for the 4H-SiC Schottky rectifier at the various reverse bias voltages calculated by using this expression with a built-in voltage of 1.0 volt are given in the table below. The specific capacitance for a 4H-SiC Schottky barrier rectifier at the various reverse bias voltages calculated using this depletion width is also provided in the table.

Reverse Bias Voltage (Volts)	**Depletion Width (microns)**	**Specific Capacitance (F/cm^2)**
100	1.59	5.42 x 10^{-9}
200	2.24	3.84 x 10^{-9}
400	3.16	2.72 x 10^{-9}
800	4.47	1.92 x 10^{-9}

Problem 4.12:

Calculate the power dissipation for a silicon Schottky barrier rectifier designed to block 100-V at 300, 350, 400, 450, and 500 ^{o}K. Use the following assumptions: (a) parallel-plane breakdown voltage; (b) Reverse bias voltage of 80V; (c) Barrier height of 0.8 eV; (d) Duty cycle of 50 percent; (e) On-state current density of 100 A/cm^2. Estimate the temperature at which minimum power dissipation is observed.

Solution:

The total power dissipation incurred in the Schottky rectifier can be obtained by using:

$$P_L(total) = P_L(on) + P_L(off) \qquad \textbf{[P4.12a]}$$

The on-state power dissipation can be obtained by using:

$$P_L(on) = J_F.V_F = J_F.\left[\frac{kT}{q}\ln\left(\frac{J_F}{J_S}\right) + R_{S,SP}J_F\right] \qquad \textbf{[P4.12b]}$$

where J_F is the forward (on-state) current density, J_S is the saturation current density, and $R_{S,SP}$ is the total series specific resistance. For the case of a silicon Schottky rectifier with blocking voltage of 100 volts, the specific series resistance for the drift region is found to be 5.93 x 10^{-4} Ohm-cm^2 (see Problem 4.2) at 300 ^{o}K. The specific series resistance for the drift region increases with temperature due to a reduction in the mobility (see Eq. [2.25]).

The off-state power dissipation can be obtained by using:

$$P_L(off) = J_L.V_R \qquad \textbf{[P4.13b]}$$

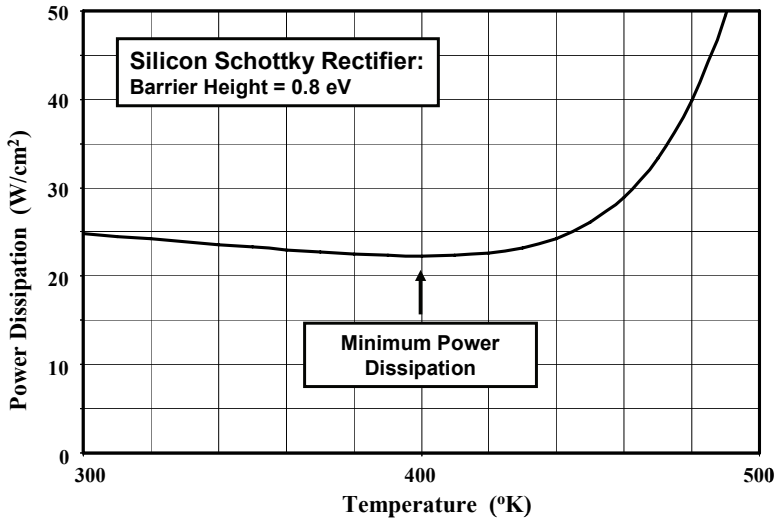
where J_L is the reverse (off-state) leakage current density. The leakage current density is given by:

$$J_L = -AT^2 e^{-(q\Phi_{BN}/kT)} e^{(q\Delta\Phi_{BN}/kT)} \qquad \textbf{[P4.13c]}$$

where the Schottky barrier lowering has been taken into account. The barrier reduction due to the image force lowering is 0.064 eV at a reverse bias of 80 volts.

The values for the on-state voltage drop, leakage current density, and power dissipation obtained by using the above expressions are provided in the table:

Temperature (^oK)	P_L(on) (W/cm^2)	P_L(off) (W/cm^2)	P_L(total) (W/cm^2)
300	24.87	0.00	24.87
350	23.26	0.02	23.28
400	21.89	0.39	22.28
450	20.79	5.28	26.07
500	19.97	43.31	63.28



The minimum power dissipation occurs at about 400 ^oK.

Chapter 5
P-i-N Rectifiers

Problem 5.1:

Determine the on-state current density for a silicon P-i-N rectifier at which the average injected carrier concentration becomes 5-times the doping concentration of 5 x 10^{13} cm^{-3} in a drift region with a width of 200 microns. The high-level lifetime in the drift region is 1 microsecond. Neglect end-region recombination.

Solution:

The average carrier density in the drift region is then given by:

$$n_a = \frac{J_T \tau_{HL}}{2qd} \qquad \textbf{[5.1a]}$$

From the given width of the drift region, d =100 microns. The average injected carrier concentration (n_a) is 2.5 x 10^{14} cm^{-3} based upon the doping concentration of 5 x 10^{13} cm^{-3} in a drift region. The on-state current density can then be determined using:

$$J_{ON} = \frac{2qdn_a}{\tau_{HL}} \qquad \textbf{[5.1b]}$$

For a high-level lifetime in the drift region is 1 microsecond, on-state current density is found to be 0.8 A/cm^2.

Problem 5.2:

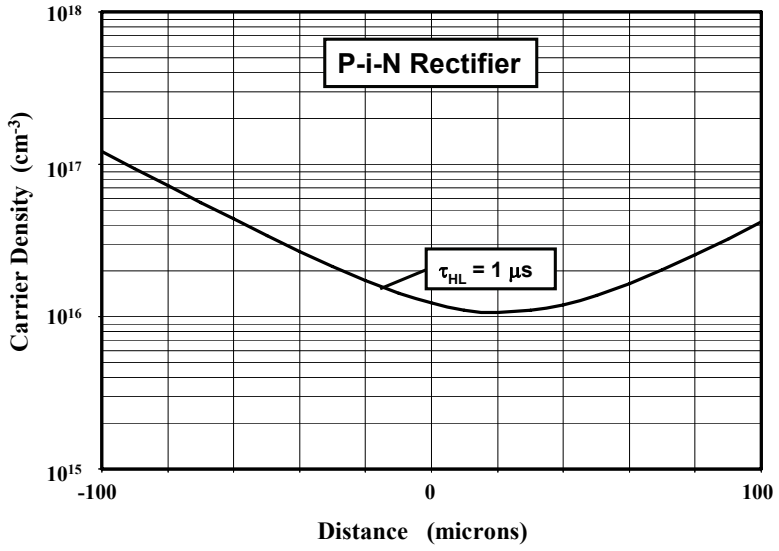
Plot the distribution of the injected carrier concentration as a function of distance within the drift region for the above P-i-N rectifier at an on-state current density of 100 A/cm^2.

Solution:

The injected carrier concentration is given by:

$$n(x) = p(x) = \frac{\tau_{HL} J_T}{2qL_a}\left[\frac{\cosh(x/L_a)}{\sinh(d/L_a)} - \frac{\sinh(x/L_a)}{2\cosh(d/L_a)}\right] \qquad \textbf{[5.2a]}$$

The ambipolar diffusion length (L_a) is 38.7 microns for a high-level lifetime of 1 microsecond if an ambipolar diffusion coefficient of 15 cm^2/s is used. The distribution of the injected carriers at an on-state current density of 100 A/cm^2 obtained by using the above expression is shown below.



Problem 5.3:

Obtain the on-state voltage drop for the above P-i-N rectifier at an on-state current density of 100 A/cm^2.

Solution:

The on-state voltage drop for a P-i-N rectifier is given by:

$$V_{ON} = \frac{2kT}{q} \ln\left[\frac{J_T d}{2qD_a n_i F(d/L_a)}\right] \qquad \textbf{[5.3a]}$$

The function F(d/La) is 8.69 x 10^{-4} at a (d/L_a) value of 2.58 for this structure. The calculated on-state voltage drop for this silicon P-i-N rectifier with a drift region width of 200 microns is found to be 1.22 volts at an on-state current density of 100 A/cm^2.

Problem 5.4:

Obtain the on-state voltage drop for the above P-i-N rectifier at an on-state current density of 100 A/cm^2 if the high-level lifetime is increased by a factor of 2-times.

Solution:

The on-state voltage drop for a P-i-N rectifier is given by:

$$V_{ON} = \frac{2kT}{q} \ln\left[\frac{J_T d}{2qD_a n_i F(d/L_a)}\right] \qquad \textbf{[5.4a]}$$

When the lifetime is increased by a factor of 2-times, the function F(d/La) becomes 7.82 x 10^{-2} at a (d/L_a) value of 1.83 for this structure. The calculated on-state voltage drop for this silicon P-i-N rectifier with a drift region width of 200 microns is found to be 0.988 volts at an on-state current density of 100 A/cm^2.

Problem 5.5:

Obtain the on-state voltage drop for the above P-i-N rectifier at an on-state current density of 100 A/cm^2 if the high-level lifetime is decreased by a factor of 2-times.

Solution:

The on-state voltage drop for a P-i-N rectifier is given by:

$$V_{ON} = \frac{2kT}{q} \ln\left[\frac{J_T d}{2qD_a n_i F(d/L_a)}\right] \qquad \textbf{[5.5a]}$$

When the lifetime is decreased by a factor of 2-times, the function F(d/La) becomes 2.77 x 10^{-11} at a (d/L_a) value of 3.65 for this structure. The calculated on-state voltage drop for this silicon P-i-N rectifier with a drift region width of 200 microns is found to be 2.11 volts at an on-state current density of 100 A/cm^2.

Problem 5.6:

Determine the reverse breakdown voltage of the P-i-N rectifier in problem 5.1.

Solution:

The breakdown voltage for the punch-through diode is given by:

$$BV_{PT} = E_c W_P - \frac{qN_{AP}W_P^2}{2\varepsilon_S} \qquad \textbf{[P5.6a]}$$

The critical electric field for breakdown for a doping concentration of 5 x 10^{13} cm^{-3} is 2.07 x 10^5 V/cm for silicon. Using this value in the above equation with a width of the drift region of 200 microns yields a breakdown voltage of 2590 volts. In comparison, the non-punch-through breakdown voltage is 2840 volts.

Problem 5.7:

What is the drift region thickness to achieve the same reverse breakdown voltage for a 4H-SiC P-i-N rectifier?

Solution:

The breakdown voltage for the punch-through diode is given by:

$$BV_{PT} = E_c W_P - \frac{qN_{AP}W_P^2}{2\varepsilon_S} \qquad \textbf{[P5.7a]}$$

The critical electric field for breakdown for a doping concentration of 5 x 10^{13} cm^{-3} is 1.7 x 10^6 V/cm for 4H-SiC. Using this value in the above equation with a breakdown voltage of 2590 volts yields a width of 15.27 microns. In comparison, the non-punch-through breakdown voltage is 160,000 volts. A much smaller width of the drift region is required to support the punch-through breakdown voltage in 4H-SiC when compared with silicon.

Problem 5.8:

Obtain the on-state voltage drop for the 4H-SiC P-i-N rectifier in Problem 5.7 at an on-state current density of 100 A/cm^2 if the high-level lifetime in the drift region is 0.1 microseconds.

Solution:

The on-state voltage drop for a P-i-N rectifier is given by:

$$V_{ON} = \frac{2kT}{q} \ln\left[\frac{J_T d}{2qD_a n_i F(d/L_a)}\right] \qquad \textbf{[5.8a]}$$

When the lifetime is decreased by a factor of 2-times, the function F(d/La) becomes 3.02 x 10^{-1} at a (d/L_a) value of 1.25 for this structure. The calculated on-state voltage drop for this 4H-SiC P-i-N rectifier with a drift region width of 15.27 microns is found to be 3.24 volts at an on-state current density of 100 A/cm^2.

Problem 5.9:

Determine the leakage currents for the silicon P-i-N rectifier in problem 5.1 at 300, 400, and 500 ^{o}K if the space-charge-generation and the low-level lifetimes are equal to the high-level lifetime. Assume that the entire drift region is depleted.

Solution:

When the entire drift region is depleted, space charge generation current is given by:

$$J_{SC} = \frac{qW_D n_i}{\tau_{SC}} \qquad \textbf{[5.9a]}$$

where W_D is the width of the drift region. For the case of drift region width of 200 microns and a space-charge-generation lifetime of 1 microsecond, the leakage current density computed by using the above equation is provided in the table. The diffusion currents can be neglected.

Temperature (^{o}K)	**Leakage Current Density (A/cm^2)**
300	4.43×10^{-5}
400	2.37×10^{-2}
500	1.11×10^{0}

Problem 5.10:

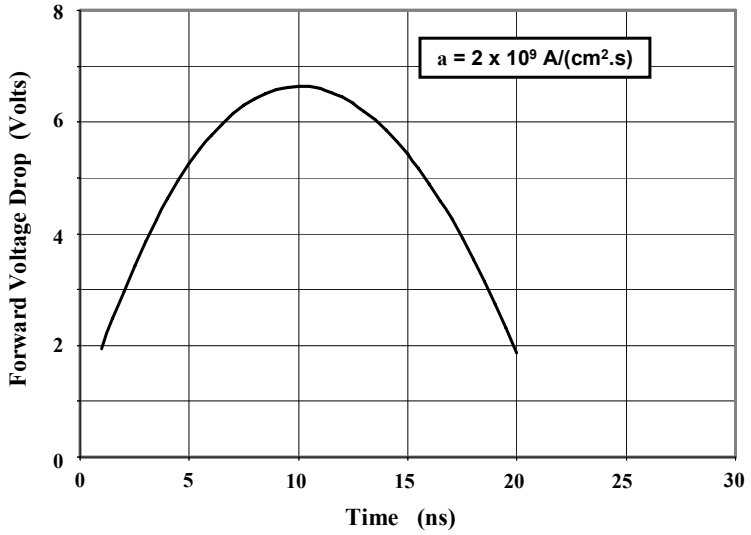
A silicon P-i-N rectifier has a drift region with doping concentration of 5 x 10^{13} cm^{-3} and thickness of 60 microns. The diode is turned on using a current ramp rate of 2 x 10^9 A/cm^2s. Determine the time at which the peak occurs in the voltage overshoot. Determine the values for the conductivity modulation distance and the specific resistance of the drift region at this time. What is the maximum overshoot voltage?

Solution:

The voltage drop across the drift region [$v_D(t)$] can be obtained by multiplying the specific resistance of the un-modulated region and the current density pertaining to each time instant:

$$v_D(t) = R_D(t).J_F(t) \qquad \textbf{[5.99]}$$

The resistance of the drift region can be obtained by determination of the width of the un-modulated portion of the drift region. The resulting voltage overshoot waveform is shown below. The maximum overshoot voltage is 6.64 volts at 10 nanoseconds. The conductivity modulation distance (x_M) at this time is 28.2 microns and the specific resistance of the drift region is 0.292 Ohm-cm^2.



Problem 5.11:

The P-i-N rectifier in problem 5.10 undergoes reverse recovery with a current ramp rate of 2 x 10^9 A/cm^{2}s from an initial on-state current density of 100 A/cm^2. Determine the time taken for the current to cross zero. What is the time taken for the reverse voltage to reach a supply voltage of 300 volts? Use a high-level lifetime of 0.5 microseconds in the drift region.

Solution:

The time t_0 at which the current crosses zero is given by:

$$t_0 = \frac{J_F}{a} \qquad \textbf{[5.11a]}$$

In the case of an initial on-state current density of 100 A/cm^2 and ramp rate of 2 x 10^9 A/cm^{2}s, the time t_0 is found to be 50 nanoseconds.

The time t_1 taken for the P-i-N rectifier to begin supporting the reverse voltage is given by:

$$t_1 = \frac{J_F}{a}\sqrt{\frac{L_a}{(Kd - L_a)} + 1} \qquad \textbf{[5.11b]}$$

where

$$K = \left[\frac{\cosh(-d/L_a)}{\sinh(d/L_a)} - \frac{\sinh(-d/L_a)}{2\cosh(d/L_a)}\right] \qquad \textbf{[5.11c]}$$

Using d = 30 microns and La= 31.6 microns in this expression, K = 1.72. Using this in Eq. [5.11b] yields a time t_1 of 80.3 nanoseconds.

The voltage supported by the space-charge region is given by:

$$V_R(t) = \frac{q\left[N_D + p(t)\right]}{2\varepsilon_S} W_{SC}(t)^2 \qquad \textbf{[5.11d]}$$

with the space-charge layer width given by:

$$W_{SC}(t) = \frac{a}{2qn_a}\left(t^2 - t_1^2\right) - \frac{J_F}{qn_a}(t - t_1) \qquad \textbf{[5.11e]}$$

The time required to complete the third phase of the reverse recovery process can be obtained using these equations to be 150 nanoseconds. The time taken to reach the reverse voltage of 300 volts is 230 nanoseconds.

Problem 5.12:

For the P-i-N rectifier in problem 5.11, determine the peak reverse recovery current density. What is the space-charge layer width at this time?

Solution:

The peak reverse recovery current is given by:

$$J_{PR} = J_F - at_2 \qquad \textbf{[5.12a]}$$

Using a time t_2 of 230 nanoseconds (See Problem 5.12) with an initial current of 100 A/cm^2 and a ramp rate of 2 x 10^9 A/cm^{2}s yields a peak reverse of 360 A/cm^2.

The space-charge layer width given by:

$$W_{SC}(t) = \frac{a}{2qn_a}\left(t^2 - t_1^2\right) - \frac{J_F}{qn_a}\left(t - t_1\right) \qquad \textbf{[5.12b]}$$

Using a time interval t_2 = 230 nanoseconds in this expression yields a space-charge layer width of 38 microns.

Problem 5.13:

For the P-i-N rectifier in problem 5.11, determine the time t_B for the reverse current to decay to zero. What is the reverse [dJ/dt] for this rectifier?

Solution:

The time interval (t_B) for the reduction of the reverse current is given by:

$$t_B = (t_3 - t_2) = \frac{2qn_a}{J_{PR}}\left[2d - W_{SC}(t_2) - h\right] \qquad \textbf{[5.13a]}$$

where $W_{SC}(t_2)$ is the width of the space-charge-layer at the time when the peak reverse recovery current occurs during the transient. The parameter h is given by:

$$h = \frac{2qD_a n_a}{J_{PR}} \qquad \textbf{[5.13b]}$$

For this example, the value for parameter h is found to be 9.3 microns. Using these values in Eq. [5.13a], the time interval (t_B) for the reduction of the reverse current is found to be 60 nanoseconds.

The reverse [dJ/dt] for this rectifier can be obtained by taking the ratio of the peak reverse recovery current density and the time interval (t_B). Using the previously calculated values, the reverse [dJ/dt] is found to be 6 x 10^9 A/cm^2-s. This is three times greater than the turn-off ramp rate of 2 x 10^9 A/cm^2-s.

Problem 5.14:

What are the advantages of replacing the punch-through P-i-N rectifier design in problem 5.10 with a non-punch-through design? Define the drift region doping concentration and thickness for the non-punch-through design in order to achieve the same reverse blocking voltage as the punch-through structure.

Solution:

The main advantage of replacing the punch-through P-i-N rectifier design in problem 5.10 with a non-punch-through design is that the space-charge-layer does not extend through the entire drift region during the turn-off transient. The presence of stored charge in the drift region produces a softer turn-off transient.

The breakdown voltage for the punch-through diode is given by:

$$BV_{PT} = E_c W_P - \frac{qN_{AP}W_P^2}{2\varepsilon_S} \qquad \textbf{[P5.14a]}$$

The critical electric field for breakdown for a doping concentration of 5 x 10^{13} cm^{-3} is 2.07 x 10^5 V/cm for silicon. Using this value in the above equation with a width of the drift region of 60 microns yields a breakdown voltage of 1100 volts.

A non-punch-through design with a breakdown voltage of 1100 volts can be achieved by using a drift region doping concentration of 1.8 x 10^{14} cm^{-3} and a drift region thickness of 100 microns.

Chapter 6
Power MOSFETs

Problem 6.1:

Determine the ideal specific on-resistances for n-channel silicon power MOSFET structures with breakdown voltages of 30, 60, 100, 500, and 1000 volts. Take into account the variation of the critical electric field and mobility with doping concentration. Compare these values with those obtained by using Eq. [6.2].

Solution:

The ideal specific on-resistance can be computed by using:

$$R_{on-sp,ideal} = \rho_D W_{C,PP} = \frac{W_{C,PP}}{q\mu_n N_D} \qquad \textbf{[P6.1a]}$$

The appropriate values for the parameters in this equation for each breakdown voltage are given in the table below. The values obtained by using Eq. [6.2] are also provided in the table.

Breakdown Voltage (Volts)	Doping Concentration (cm^{-3})	Mobility (cm^2/V-s)	Depletion Width (cm)	Specific On-Resistance (Ohm-cm^2)	Specific On-Resistance (Ohm-cm^2)
30	2.16×10^{16}	1153	1.36×10^{-4}	3.42×10^{-5}	2.92×10^{-5}
60	8.56×10^{15}	1262	3.06×10^{-4}	1.77×10^{-4}	1.65×10^{-4}
100	4.33×10^{15}	1305	5.55×10^{-4}	6.14×10^{-4}	5.93×10^{-4}
500	5.07×10^{14}	1352	3.63×10^{-3}	3.31×10^{-2}	3.31×10^{-2}
1000	2.01×10^{14}	1357	8.15×10^{-3}	1.87×10^{-1}	1.88×10^{-1}

Problem 6.2:

Calculate the P-base doping concentration (assuming it is uniformly doped) of an n-channel silicon power MOSFET structure to obtain a threshold voltage of 2 volts. The gate oxide thickness is 500 angstroms. The fixed charge in the gate oxide is 2 x 10^{11} cm^{-2}. Assume N^+ polysilicon with a doping concentration of 1 x 10^{20} cm^{-3} is used as the gate electrode.

Solution:

The threshold voltage is given by:

$$V_{TH} = \frac{\sqrt{4\varepsilon_S kTN_A \ln(N_A / n_i)}}{C_{OX}} + \frac{2kT}{q}\ln\left(\frac{N_A}{n_i}\right) - \frac{Q_{OX}}{C_{OX}} \qquad \textbf{[6.2a]}$$

where the total *effective charge* in the oxide (Q_{OX}). In addition, the work-function difference between heavily doped N^+ polysilicon and P-silicon must be taken into account. A threshold voltage of 2.0 volts is achieved at a doping concentration of 1.16 x 10^{17} cm^{-3}. The contribution from the fixed oxide charge is -0.469 volts. The shift due to the N^+ polysilicon gate electrode is -0.968. These contributions require increasing the P-base doping concentration which is beneficial for suppressing reach-through in the base region.

Problem 6.3:

Determine the drift region doping concentration and thickness for an n-channel silicon power MOSFET structure when the structure is designed to support 100 volts assuming all the blocking voltage is supported by the drift region. Assume one-dimensional (parallel-plane) breakdown voltage is achievable in this case.

Solution:

The drift region doping concentration and thickness are determined by the parallel-plane breakdown voltage analysis. The doping concentration required to achieve a desired parallel-plane breakdown voltage for an abrupt junction in silicon can be obtained by using:

$$BV_{PP}(Si) = 5.34x10^{13} N_D^{-3/4} \qquad \textbf{[P6.3a]}$$

For a breakdown voltage of 100 volts, the doping concentration is 4.33 x 10^{15} cm^{-3} (also see Problem 6.1). The maximum depletion layer width at breakdown for an abrupt junction in silicon can then be obtained from the doping concentration by using:

$$W_{PP}(Si) = 2.67x10^{10} N_D^{-7/8} \qquad \textbf{[P6.3b]}$$

For a breakdown voltage of 100 volts, the depletion layer width at breakdown is 5.55 microns (also see Problem 6.1). This is the thickness required for the drift region for one-dimensional (parallel-plane) breakdown conditions.

Problem 6.4:

Determine the drift region doping concentration and thickness for an n-channel silicon power MOSFET structure when the structure is designed to support 100 volts assuming all the blocking voltage is supported by the drift region. In this case, assume that the breakdown voltage is limited by the edge termination to 80 percent of the parallel-plane value.

Solution:

The parallel-plane breakdown voltage for the case of an edge termination that limits the breakdown to 80 percent of the parallel-plane value is:

$$BV_{PP} = \frac{100}{0.8} = 125\,V \qquad \textbf{[P6.4a]}$$

The doping concentration required to achieve this parallel-plane breakdown voltage for an abrupt junction in silicon can be obtained by using:

$$BV_{PP}(Si) = 5.34x10^{13}\,N_D^{-3/4} \qquad \textbf{[P6.4b]}$$

For a breakdown voltage of 125 volts, the doping concentration is 3.22 x 10^{15} cm^{-3}.

The depletion layer width at breakdown (100 V) can then be obtained by using:

$$W_D = \sqrt{\frac{2\varepsilon_S V}{qN_D}} \qquad \textbf{[P6.4c]}$$

For a breakdown voltage of 100 volts, the depletion layer width at breakdown is 6.35 microns. This is the thickness required for the drift region for one-dimensional (parallel-plane) breakdown conditions. Note that this value is less than the depletion width (7.2 microns) at the parallel-plane breakdown voltage of 125 V but greater than the value for the parallel-plane breakdown voltage of 100 volts.

Problem 6.5:

Calculate the depletion width within the P-base region of the n-channel silicon power MOSFET structure defined in Problem 6.4 when the structure is supporting 100 volts.

Solution:

The depletion width within the P-base region is given by:

$$W_P = \sqrt{\frac{2\varepsilon_S BV}{q}\left[\frac{N_D}{N_A\left(N_A + N_D\right)}\right]} \qquad \textbf{[P6.5a]}$$

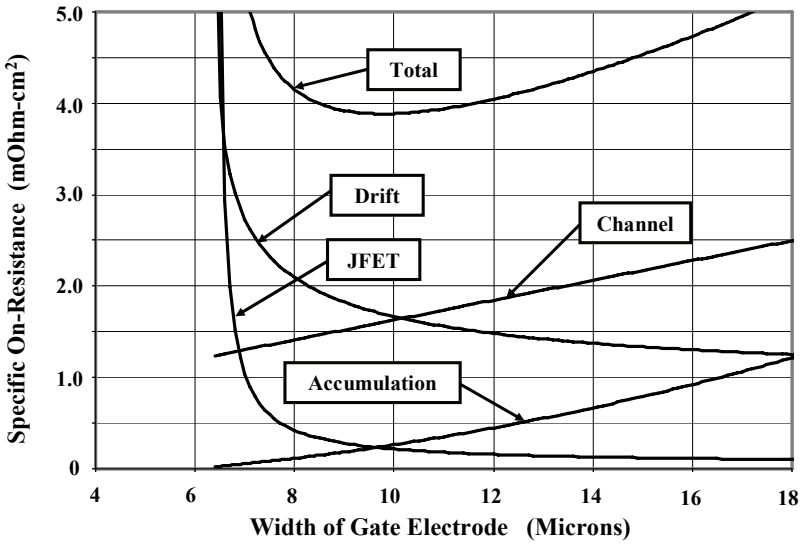
Using a doping concentration (N_D) of 3.22 x 10^{15} cm^{-3} in the N-drift region and a doping concentration (N_A) of 1.16 x 10^{17} cm^{-3} in the P-base region with a breakdown voltage of 100 volts in this equation yields a depletion width within the P-base region of 0.17 microns. The small depletion of the P-base region prevents reach-through breakdown problems even for short channel length devices.

Problem 6.6:

Determine the optimum width for the gate electrode for a linear cell topology for the n-channel silicon power MOSFET structure defined in Problem 6.4 using the following parameters: (a) inversion mobility of 450 cm^2/Vs; (b) accumulation mobility of 1000 cm^2/Vs; (c) JFET region doping concentration of 3 x 10^{16} cm^{-3}; (d) cell polysilicon window width of 5 microns; (e) N^+ source length of 2.5 microns and sheet resistance of 10 Ohms/sq; (f) contact resistance of 1 x 10^{-6} Ohm-cm^2 for both the N^+ source and the drain; (g) N^+ source contact width of 1 micron; (h) N^+ substrate resistivity of 0.002 Ohm-cm and thickness of 500 microns; (i) gate bias of 5 volts; (j) K factor for accumulation spreading of 0.6; (k) N^+ source depth of 1.0 microns; (l) P-base depth of 3 microns. What are the absolute and percentage contributions from each of the on-resistance components for the optimum design?

Solution:

The optimum gate width can be obtained by computing each of the components for the on-resistance of the planar MOSFET structure given in section 6.6. A graph of the variation in the specific on-resistance as a function of gate width is provided below:



The minimum specific on-resistance of 3.88 milliOhm-cm^2 is obtained at an optimum gate width of 9.8 microns.

The absolute and percentage contributions from each of the on-resistance components for the optimum design are provided in the table.

Resistance	**Value ($m\Omega$-cm^2)**	**Percentage Contribution**
Source Contact	0.007	0.18
Source	0.002	0.05
Channel	1.61	41.49
Accumulation	0.25	6.44
JFET	0.23	5.93
Drift	1.69	43.56
Substrate	0.10	2.58
Drain Contact	0.001	0.03
Total	3.88	100

Problem 6.7:

Calculate the specific on-resistance (in mOhm-cm^2) for the ideal drift region for blocking 100 volts. Compare the optimum design in Problem 6.6 to the ideal case by taking the ratio of specific on-resistances.

Solution:

The specific on-resistance (in mOhm-cm^2) for the ideal drift region is given by:

$$R_{on-sp,ideal}\left(n-channel\right) = 5.93x10^{-9}.BV_{PP}^{2.5} \qquad \textbf{[6.7a]}$$

The value for a blocking voltage of 100 volts is 0.593 milli-Ohm-cm^2.

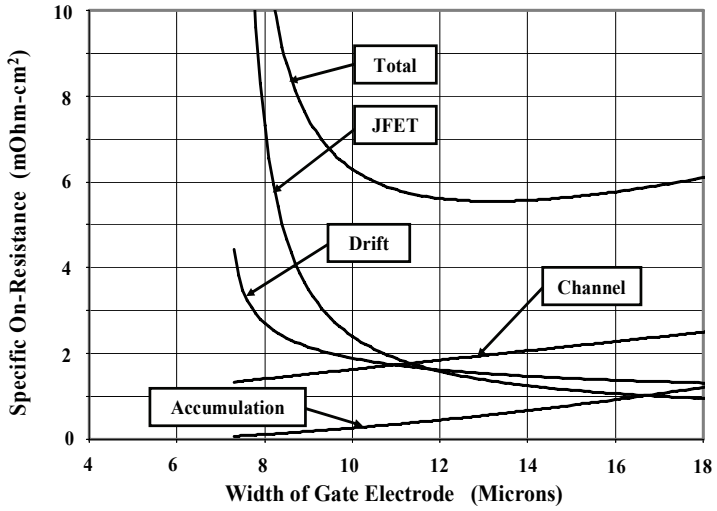
The ratio of the specific on-resistance for the optimum design to that for the ideal case is 6.54-times.

Problem 6.8:

Repeat Problem 6.6 without the enhanced doping in the JFET region.

Solution:

The optimum gate width can be obtained by computing each of the components for the on-resistance of the planar MOSFET structure given in section 6.6. A graph of the variation in the specific on-resistance as a function of gate width is provided below:



The minimum specific on-resistance of 5.55 milliOhm-cm^2 is obtained at an optimum gate width of 13.2 microns.
The absolute and percentage contributions from each of the on-resistance components for the optimum design are provided in the table.

Resistance	Value (mΩ-cm^2)	Percentage Contribution
Source Contact	0.009	0.16
Source	0.002	0.04
Channel	1.98	35.68
Accumulation	0.58	10.45
JFET	1.36	24.50
Drift	1.52	27.39
Substrate	0.10	1.80
Drain Contact	0.001	0.02
Total	5.55	100

Problem 6.9:

Calculate the specific input capacitance ($C_{IN,SP}$) for the optimum cell design (in nF/cm^2) in Problem 6.6.

Solution:

The specific input (or gate) capacitance for the power VD-MOSFET structure can be obtained by using:

$$C_{IN,SP} = C_{N+} + C_P + C_{SM} = \frac{2x_{PL}}{W_{Cell}}\left(\frac{\varepsilon_{OX}}{t_{OX}}\right) + \frac{W_G}{W_{Cell}}\left(\frac{\varepsilon_{OX}}{t_{IEOX}}\right) \qquad \textbf{[6.9a]}$$

where t_{OX} and t_{IEOX} are the thicknesses of the gate and inter-electrode oxides, respectively. The inter-electrode capacitance can be neglected. The cell pitch for the optimum gate width of 9.8 microns for the planar MOSFET structure is 14.8 microns due to a polysilicon window of 5 microns. The P-base junction depth is 3 microns and the gate oxide thickness is 500 angstroms. Using these values in the above equation yields a specific input capacitance of 27.7 nF/cm^2.

Problem 6.10:

Calculate the specific drain overlap capacitance ($C_{GD,SP}$) for the optimum cell design (in nF/cm^2) in Problem 6.6 at a drain bias of 10 volts.

Solution:

The gate-drain (or reverse transfer) capacitance for the power VD-MOSFET structure is given by:

$$C_{GD,SP} = \frac{(W_G - 2x_{PL})}{W_{Cell}} \left(\frac{C_{OX} C_{S,M}}{C_{OX} + C_{S,M}} \right) \qquad \textbf{[6.10a]}$$

where $C_{S,M}$ is the semiconductor capacitance under the gate oxide, which decreases with increasing drain bias voltage. The specific capacitance of the semiconductor depletion region can be obtained by computation of the depletion layer width. The depletion layer width in the semiconductor under the gate oxide is given by:

$$W_{D,MOS} = \frac{\varepsilon_S}{C_{OX}} \left\{ \sqrt{1 + \frac{2V_D C_{OX}^2}{q\varepsilon_S N_D}} - 1 \right\} \qquad \textbf{[6.10b]}$$

At a drain bias of 10 volts, the depletion layer width in the semiconductor under the gate oxide is found to be 1.86 microns.

The specific capacitance for the semiconductor is then obtained using:

$$C_{S,M} = \frac{\varepsilon_S}{W_{D,MOS}} \qquad \textbf{[6.10c]}$$

The specific capacitance for the semiconductor at a drain bias of 10 volts is found to be 5.57 nF/cm^2.

The specific oxide capacitance is 68.2 nF/cm^2 for a gate oxide thickness of 500 angstroms.

The gate-drain (or reverse transfer) capacitance computed by using Eq. [6.10a] with the above values is 1.32 nF/cm^2.

Problem 6.11:

Determine the Figures of Merit [$R_{DSon,SP}$*$C_{IN,SP}$] and [$R_{DSon,SP}$*$C_{GD,SP}$] in mΩ*nF for the optimum cell design in Problem 6.6.

Solution:

The specific on-resistance for this optimized planar power MOSFET structure with optimum gate width of 9.8 microns is 3.88 mΩ-cm^2 (see Problem 6.6). The specific input capacitance for this structure is 27.7 nF/cm^2 (see Problem 6.9).

Using these values, the Figure of Merit [$R_{DSon,SP}$*$C_{IN,SP}$] calculated for this optimized planar power MOSFET structure is found to be 107.5 mΩ*nF.

The specific gate-drain capacitance for this structure is 1.32 nF/cm^2 (see Problem 6.10). Using this value, the Figure of Merit [$R_{DSon,SP}$*$C_{GD,SP}$] calculated for this optimized planar power MOSFET structure is found to be 5.12 mΩ*nF.

Problem 6.12:

Calculate the specific input capacitance ($C_{IN,SP}$) for the optimum cell design (in nF/cm^2) in Problem 6.8.

Solution:

The specific input (or gate) capacitance for the power VD-MOSFET structure can be obtained by using:

$$C_{IN,SP} = C_{N+} + C_P + C_{SM} = \frac{2x_{PL}}{W_{Cell}}\left(\frac{\varepsilon_{OX}}{t_{OX}}\right) + \frac{W_G}{W_{Cell}}\left(\frac{\varepsilon_{OX}}{t_{IEOX}}\right) \qquad \textbf{[6.12a]}$$

where t_{OX} and t_{IEOX} are the thicknesses of the gate and inter-electrode oxides, respectively. The inter-electrode capacitance can be neglected. The cell pitch for the optimum gate width of 13.2 microns for the planar MOSFET structure is 18.2 microns due to a polysilicon window of 5 microns. The P-base junction depth is 3 microns and the gate oxide thickness is 500 angstroms. Using these values in the above equation yields a specific input capacitance of 22.5 nF/cm^2.

Problem 6.13:

Calculate the specific drain overlap capacitance ($C_{GD,SP}$) for the optimum cell design (in nF/cm^2) in Problem 6.8 at a drain bias of 10 volts.

Solution:

The gate-drain (or reverse transfer) capacitance for the power VD-MOSFET structure is given by:

$$C_{GD,SP} = \frac{(W_G - 2x_{PL})}{W_{Cell}} \left(\frac{C_{OX} C_{S,M}}{C_{OX} + C_{S,M}} \right) \qquad \textbf{[6.13a]}$$

where $C_{S,M}$ is the semiconductor capacitance under the gate oxide, which decreases with increasing drain bias voltage. The specific capacitance of the semiconductor depletion region can be obtained by computation of the depletion layer width. The depletion layer width in the semiconductor under the gate oxide is given by:

$$W_{D,MOS} = \frac{\varepsilon_S}{C_{OX}} \left\{ \sqrt{1 + \frac{2V_D C_{OX}^2}{q\varepsilon_S N_D}} - 1 \right\} \qquad \textbf{[6.13b]}$$

At a drain bias of 10 volts, the depletion layer width in the semiconductor under the gate oxide is found to be 1.86 microns.

The specific capacitance for the semiconductor is then obtained using:

$$C_{S,M} = \frac{\varepsilon_S}{W_{D,MOS}} \qquad \textbf{[6.13c]}$$

The specific capacitance for the semiconductor at a drain bias of 10 volts is found to be 5.57 nF/cm^2.

The specific oxide capacitance is 68.2 nF/cm^2 for a gate oxide thickness of 500 angstroms.

The gate-drain (or reverse transfer) capacitance computed by using Eq. [6.13a] with the above values is 2.04 nF/cm^2.

Problem 6.14:

Determine the Figures of Merit [$R_{DSon,SP}$*$C_{IN,SP}$] and [$R_{DSon,SP}$*$C_{GD,SP}$] in mΩ*nF for the optimum cell design in Problem 6.8.

Solution:

The specific on-resistance for this optimized planar power MOSFET structure with optimum gate width of 13.2 microns is 5.55 mΩ-cm^2 (see Problem 6.8). The specific input capacitance for this structure is 22.5 nF/cm^2 (see Problem 6.12).

Using these values, the Figure of Merit [$R_{DSon,SP}$*$C_{IN,SP}$] calculated for this optimized planar power MOSFET structure is found to be 124.9 mΩ*nF.

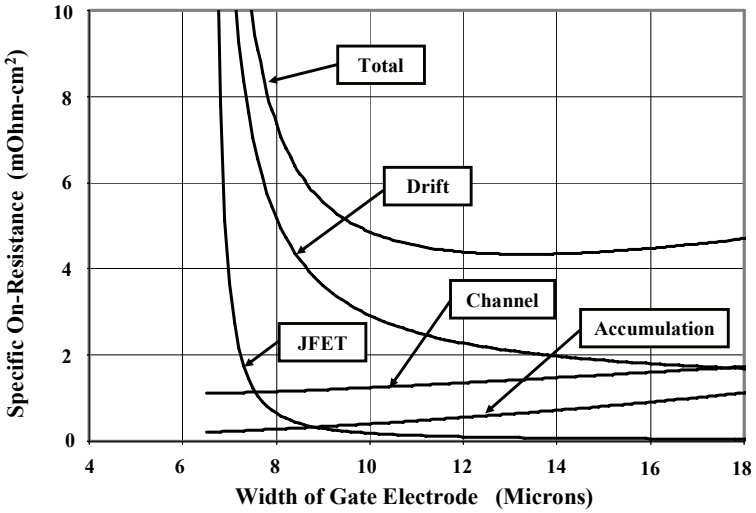
The specific gate-drain capacitance for this structure is 2.04 nF/cm^2 (see Problem 6.13). Using this value, the Figure of Merit [$R_{DSon,SP}$*$C_{GD,SP}$] calculated for this optimized planar power MOSFET structure is found to be 11.3 mΩ*nF.

Problem 6.15:

Repeat Problem 6.6 with the A-L-L cell topology using a bar width of 5 microns.

Solution:

The optimum gate width can be obtained by computing each of the components for the on-resistance of the planar MOSFET structure with A-L-L cell topology given in section 6.7.4. A graph of the variation in the specific on-resistance as a function of gate width is provided below:



The minimum specific on-resistance of 4.34 mΩ-cm^2 (nearly the same as for linear cell) is obtained at an optimum gate width of 13.3 microns.
The absolute and percentage contributions from each of the on-resistance components for the optimum design are provided in the table.

Resistance	Value (mΩ-cm^2)	Percentage Contribution
Source Contact	0.008	0.18
Source	0.002	0.05
Channel	1.43	32.95
Accumulation	0.65	14.98
JFET	0.08	1.84
Drift	2.06	47.47
Substrate	0.10	2.30
Drain Contact	0.001	0.02
Total	4.34	100

Problem 6.16:

Calculate the specific input capacitance ($C_{IN,SP}$) for the optimum cell design (in nF/cm^2) in Problem 6.15.

Solution:

The specific input (or gate) capacitance for the power VD-MOSFET structure with A-L-L cell topology can be obtained by using:

$$C_{IN,SP} = C_{N+} + C_P + C_{SM} = \frac{\pi W_G x_{PL}}{W_{Cell}^2}\left(\frac{\varepsilon_{OX}}{t_{OX}}\right) \qquad \textbf{[6.16a]}$$

if the inter-electrode capacitance is neglected. The cell pitch for the optimum gate width of 13.3 microns for the planar MOSFET structure with A-L-L topology is 15.3 microns due to a polysilicon bar of 2 microns. The P-base junction depth is 3 microns and the gate oxide thickness is 500 angstroms. Using these values in the above equation yields a specific input capacitance of 36.5 nF/cm^2.

Problem 6.17:

Calculate the specific drain overlap capacitance ($C_{GD,SP}$) for the optimum cell design (in nF/cm^2) in Problem 6.15 at a drain bias of 10 volts.

Solution:

The gate-drain (or reverse transfer) capacitance for the power VD-MOSFET structure with A-L-L cell topology is given by:

$$C_{GD,SP} = \frac{\pi \left(W_G - 2x_{PL}\right)^2}{W_{Cell}^2} \left(\frac{C_{OX} C_{S,M}}{C_{OX} + C_{S,M}} \right) \qquad \textbf{[6.17a]}$$

where $C_{S,M}$ is the semiconductor capacitance under the gate oxide, which decreases with increasing drain bias voltage. The specific capacitance of the semiconductor depletion region can be obtained by computation of the depletion layer width. The depletion layer width in the semiconductor under the gate oxide is given by:

$$W_{D,MOS} = \frac{\varepsilon_S}{C_{OX}} \left\{ \sqrt{1 + \frac{2V_D C_{OX}^2}{q\varepsilon_S N_D}} - 1 \right\} \qquad \textbf{[6.17b]}$$

At a drain bias of 10 volts, the depletion layer width in the semiconductor under the gate oxide is found to be 1.86 microns.

The specific capacitance for the semiconductor is then obtained using:

$$C_{S,M} = \frac{\varepsilon_S}{W_{D,MOS}} \qquad \textbf{[6.13c]}$$

The specific capacitance for the semiconductor at a drain bias of 10 volts is found to be 5.57 nF/cm^2.

The specific oxide capacitance is 68.2 nF/cm^2 for a gate oxide thickness of 500 angstroms.

The gate-drain (or reverse transfer) capacitance computed by using Eq. [6.17a] with the above values is 0.92 nF/cm^2.

Problem 6.18:

Determine the Figures of Merit [$R_{DSon,SP}$*$C_{IN,SP}$] and [$R_{DSon,SP}$*$C_{GD,SP}$] in mΩ*nF for the optimum cell design in Problem 6.15.

Solution:

The specific on-resistance for the optimized A-L-L planar power MOSFET structure with optimum gate width of 13.3 microns is 4.34 mΩ-cm^2 (see Problem 6.15). The specific input capacitance for this structure is 36.5 nF/cm^2 (see Problem 6.16).

Using these values, the Figure of Merit [$R_{DSon,SP}$*$C_{IN,SP}$] calculated for this optimized planar power MOSFET structure with A-L-L cell topology is found to be 158.4 mΩ*nF. This is larger than the value for the linear cell topology.

The specific gate-drain capacitance for this structure is 0.92 nF/cm^2 (see Problem 6.17). Using this value, the Figure of Merit [$R_{DSon,SP}$*$C_{GD,SP}$] calculated for this optimized planar power MOSFET structure with A-L-L cell topology is found to be 3.99 mΩ*nF. This is much smaller than the value for the linear cell topology.

The A-L-L cell topology allows reduction of the switching losses because of the small reverse-transfer capacitance when compared with the linear cell topology.

Problem 6.19:

Determine the specific on-resistance for a linear cell n-channel silicon U-MOSFET structure with a trench width of 1 micron and mesa width of 3 microns designed to support 100 volts. Assume that the breakdown voltage is limited by the edge termination to 80 percent of the parallel-plane value. The P-base doping concentration (assuming it is uniformly doped) is chosen to obtain a threshold voltage of 2 volts. The gate oxide thickness is 500 angstroms. The fixed charge in the gate oxide is 2×10^{11} cm^{-2}. Assume N^+ polysilicon with a doping concentration of 1×10^{20} cm^{-3} is used as the gate electrode. Use the following parameters: (a) inversion mobility of 450 cm^2/Vs; (b) accumulation mobility of 1000 cm^2/Vs; (c) N^+ source length of 1 microns and sheet resistance of 10 Ohms/sq; (d) contact resistance of 1×10^{-6} Ohm-cm^2 for both the N^+ source and the drain; (e) N^+ source contact width of 0.5 microns; (f) N^+ substrate resistivity of 0.002 Ohm-cm and thickness of 500 microns; (g) gate bias of 5 volts; (h) K factor for accumulation spreading of 0.6; (i) N^+ source depth of 0.5 microns; (j) P-base depth of 1.5 microns; (k) trench depth of 2 microns; (l) mesa width is 4 microns; (m) trench width is 1 micron. What are the absolute and percentage contributions from each of the on-resistance components?

Solution:

The specific on-resistance of the U-MOSFET structure can be obtained by computing each of the components for the on-resistance given in section 6.8.

The absolute and percentage contributions from each of the on-resistance components for the given design are provided in the table.

Resistance	Value ($m\Omega$-cm^2)	Percentage Contribution
Source Contact	0.005	0.32
Source	0.000	0.00
Channel	0.271	17.15
Accumulation	0.044	2.78
JFET	0.000	0.00
Drift	1.16	73.42
Substrate	0.10	6.33
Drain Contact	0.001	0.06
Total	1.58	100

The total specific on-resistance is much smaller than for the optimized planar power MOSFET structure in problem 6.6.

Problem 6.20:

Calculate the specific input capacitance ($C_{IN,SP}$) for the U-MOSFET structure (in nF/cm^2) in Problem 6.19.

Solution:

The specific input (or gate) capacitance for the power U-MOSFET structure can be obtained by using:

$$C_{IN,SP} = C_{N+} + C_P + C_{SM} = \frac{2x_P}{W_{Cell}}\left(\frac{\varepsilon_{OX}}{t_{OX}}\right) \qquad \textbf{[6.20a]}$$

if the inter-electrode capacitance is neglected. The cell pitch for the U-MOSFET structure is 5 microns. The P-base junction depth is 1.5 microns and the gate oxide thickness is 500 angstroms. Using these values in the above equation yields a specific input capacitance of 40.9 nF/cm^2.

Problem 6.21:

Calculate the specific drain overlap capacitance ($C_{GD,SP}$) for the optimum cell design (in nF/cm^2) in Problem 6.19 at a drain bias of 10 volts.

Solution:

The gate-drain (or reverse transfer) capacitance for the power U-MOSFET structure is given by:

$$C_{GD,SP} = \frac{W_T + 2\left(t_T - x_P\right)}{W_{Cell}}\left(\frac{C_{OX}C_{S,M}}{C_{OX} + C_{S,M}}\right) \qquad \textbf{[6.21a]}$$

where $C_{S,M}$ is the semiconductor capacitance under the gate oxide, which decreases with increasing drain bias voltage. The specific capacitance of the semiconductor depletion region can be obtained by computation of the depletion layer width. The depletion layer width in the semiconductor under the gate oxide is given by:

$$W_{D,MOS} = \frac{\varepsilon_S}{C_{OX}}\left\{\sqrt{1 + \frac{2V_D C_{OX}^2}{q\varepsilon_S N_D}} - 1\right\} \qquad \textbf{[6.21b]}$$

At a drain bias of 10 volts, the depletion layer width in the semiconductor under the gate oxide is found to be 1.86 microns.

The specific capacitance for the semiconductor is then obtained using:

$$C_{S,M} = \frac{\varepsilon_S}{W_{D,MOS}} \qquad \textbf{[6.21c]}$$

The specific capacitance for the semiconductor at a drain bias of 10 volts is found to be 5.57 nF/cm^2.

The specific oxide capacitance is 68.2 nF/cm^2 for a gate oxide thickness of 500 angstroms.

The gate-drain (or reverse transfer) capacitance computed by using Eq. [6.21a] with the above values is 2.07 nF/cm^2.

Problem 6.22:

Determine the Figures of Merit [$R_{DSon,SP}$*$C_{IN,SP}$] and [$R_{DSon,SP}$*$C_{GD,SP}$] in mΩ*nF for the optimum cell design in Problem 6.19.

Solution:

The specific on-resistance for the trench-gate power U-MOSFET structure is 1.58 mΩ-cm^2 (see Problem 6.19). The specific input capacitance for this structure is 40.9 nF/cm^2 (see Problem 6.20).

Using these values, the Figure of Merit [$R_{DSon,SP}$*$C_{IN,SP}$] calculated for this trench-gate power U-MOSFET structure is found to be 66.6 mΩ*nF. This is much smaller than the value for the planar gate VD-MOSFET structure.

The specific gate-drain capacitance for this structure is 2.07 nF/cm^2 (see Problem 6.21). Using this value, the Figure of Merit [$R_{DSon,SP}$*$C_{GD,SP}$] calculated for this trench-gate power U-MOSFET structure is found to be 3.27 mΩ*nF. This is much smaller than the value for the planar gate VD-MOSFET structure.

The power U-MOSFET structure allows reduction of the on-state and switching losses because of the small specific on-resistance and reverse-transfer capacitance when compared with the planar gate VD-MOSFET structure.

Problem 6.23:

Obtain the specific gate charge for the optimum design of the VD-MOSFET structure in Problem 6.6. Use an on-state current density of 200 A/cm^2 and a drain supply voltage of 80 volts. Provide values for each of the components of the specific gate charge in nC/cm^2.

Solution:

The various components of the gate charge are given by:

$$Q_{GS1} = J_G t_1 = V_{TH}\left[C_{GS} + C_{GD}\left(V_{DS}\right)\right] \quad \textbf{[6.23a]}$$

$$Q_{GS2} = J_G\left(t_2 - t_1\right) = \left[C_{GS} + C_{GD}\left(V_{DS}\right)\right]\sqrt{\frac{J_{ON}W_{Cell}L_{CH}}{2\mu_{ni}C_{OX}}} \quad \textbf{[6.23b]}$$

$$Q_{GS} = J_G t_2 = \left[C_{GS} + C_{GD}\left(V_{DS}\right)\right]\left(V_{TH} + \sqrt{\frac{J_{ON}W_{Cell}L_{CH}}{2\mu_{ni}C_{OX}}}\right) \quad \textbf{[6.23c]}$$

$$Q_{GD} = J_G\left(t_3 - t_2\right) = \frac{2K_G q\varepsilon_S N_D}{C_{OX}}\left[\sqrt{1+\frac{2V_{DS}C_{OX}^2}{q\varepsilon_S N_D}} - \sqrt{1+\frac{2V_{ON}C_{OX}^2}{q\varepsilon_S N_D}}\right] \quad \textbf{[6.23d]}$$

$$Q_{SW} = J_G\left(t_3 - t_1\right) = \left[C_{GS} + C_{GD}\left(V_{DS}\right)\right]\sqrt{\frac{J_{ON}W_{Cell}L_{CH}}{2\mu_{ni}C_{OX}}} + \frac{2K_G q\varepsilon_S N_D}{C_{OX}}\left[\sqrt{1+\frac{2V_{DS}C_{OX}^2}{q\varepsilon_S N_D}} - \sqrt{1+\frac{2V_{ON}C_{OX}^2}{q\varepsilon_S N_D}}\right] \quad \textbf{[6.23e]}$$

$$Q_G = J_G t_4 = \left[C_{GS} + C_{GD}\left(V_{DS}\right)\right]V_{GP} + \frac{2K_G q\varepsilon_S N_D}{C_{OX}}\left[\sqrt{1+\frac{2V_{DS}C_{OX}^2}{q\varepsilon_S N_D}} - \sqrt{1+\frac{2V_{ON}C_{OX}^2}{q\varepsilon_S N_D}}\right] + \left[C_{GS} + C_{GD}\left(V_{ON}\right)\right]\left(V_G - V_{GP}\right) \quad \textbf{[6.23f]}$$

For the optimum design of the VD-MOSFET structure in Problem 6.6, the values for the specific gate-oxide (C_{OX}), input capacitance (C_{GS}=$C_{IN,SP}$) and reverse-transfer capacitance ($C_{GD,SP}$) are 68.2, 27.7 and 1.32 nF/cm^2, respectively. The gate charges can be calculated by using the rest of the device parameters given in Problem 6.6. The values are: Q_{GS1}=58 nC/cm^2; Q_{GS2}=28.5 nC/cm^2; Q_{GD}=135.6 nC/cm^2; Q_{SW}=164.1 nC/cm^2; Q_G=292.4 nC/cm^2.

Problem 6.24:

Determine the Figures of Merit [$R_{DSon,SP}$*$Q_{GD,SP}$] and [$R_{DSon,SP}$*$Q_{SW,SP}$] in mΩ*nC for the VD-MOSFET structure in Problem 6.23.

Solution:

The specific on-resistance for the planar power VD-MOSFET structure is 3.88 mΩ-cm^2 (see Problem 6.6). The specific reverse-transfer gate charge for this structure is 135.6 nC/cm^2 (see Problem 6.23).

Using these values, the Figure of Merit [$R_{DSon,SP}$*$Q_{GD,SP}$] calculated for this planar power VD-MOSFET structure is found to be 526 mΩ*nC.

The specific switching gate charge for this structure is 164.1 nC/cm^2 (see Problem 6.23). Using this value, the Figure of Merit [$R_{DSon,SP}$*$Q_{SW,SP}$] calculated for this planar power VD-MOSFET structure is found to be 637 mΩ*nC.

Problem 6.25:

Obtain the specific gate charge for the U-MOSFET structure in Problem 6.19. Use an on-state current density of 200 A/cm^2 and a drain supply voltage of 80 volts. Provide values for each of the components of the specific gate charge in nC/cm^2.

Solution:

The various components of the gate charge are given by:

$$Q_{GS1} = J_G t_1 = V_{TH}\left[C_{GS} + C_{GD}\left(V_{DS}\right)\right] \quad \textbf{[6.25a]}$$

$$Q_{GS2} = J_G\left(t_2 - t_1\right) = \left[C_{GS} + C_{GD}\left(V_{DS}\right)\right]\sqrt{\frac{J_{ON}W_{Cell}L_{CH}}{2\mu_{ni}C_{OX}}} \quad \textbf{[6.25b]}$$

$$Q_{GS} = J_G t_2 = \left[C_{GS} + C_{GD}\left(V_{DS}\right)\right]\left(V_{TH} + \sqrt{\frac{J_{ON}W_{Cell}L_{CH}}{2\mu_{ni}C_{OX}}}\right) \quad \textbf{[6.25c]}$$

$$Q_{GD} = J_G\left(t_3 - t_2\right) = \frac{2K_G q\varepsilon_S N_D}{C_{OX}}\left[\sqrt{1+\frac{2V_{DS}C_{OX}^2}{q\varepsilon_S N_D}} - \sqrt{1+\frac{2V_{ON}C_{OX}^2}{q\varepsilon_S N_D}}\right] \quad \textbf{[6.25d]}$$

$$Q_{SW} = J_G\left(t_3 - t_1\right) = \left[C_{GS} + C_{GD}\left(V_{DS}\right)\right]\sqrt{\frac{J_{ON}W_{Cell}L_{CH}}{2\mu_{ni}C_{OX}}} + \frac{2K_G q\varepsilon_S N_D}{C_{OX}}\left[\sqrt{1+\frac{2V_{DS}C_{OX}^2}{q\varepsilon_S N_D}} - \sqrt{1+\frac{2V_{ON}C_{OX}^2}{q\varepsilon_S N_D}}\right] \quad \textbf{[6.25e]}$$

$$Q_G = J_G t_4 = \left[C_{GS} + C_{GD}\left(V_{DS}\right)\right]V_{GP} + \frac{2K_G q\varepsilon_S N_D}{C_{OX}}\left[\sqrt{1+\frac{2V_{DS}C_{OX}^2}{q\varepsilon_S N_D}} - \sqrt{1+\frac{2V_{ON}C_{OX}^2}{q\varepsilon_S N_D}}\right] + \left[C_{GS} + C_{GD}\left(V_{ON}\right)\right]\left(V_G - V_{GP}\right) \quad \textbf{[6.25f]}$$

For the U-MOSFET structure in Problem 6.19, the values for the specific gate-oxide (C_{OX}), input capacitance (C_{GS}=$C_{IN,SP}$) and reverse-transfer capacitance ($C_{GD,SP}$) are 68.2, 40.9 and 2.07 nF/cm^2, respectively. The gate charges can be calculated by using the rest of the device parameters given in Problem 6.19. The values are: Q_{GS1}=85.9 nC/cm^2; Q_{GS2}=17.4 nC/cm^2; Q_{GD}=218.1 nC/cm^2; Q_{SW}=235.5 nC/cm^2; Q_G=455 nC/cm^2.

Problem 6.26:

Determine the Figures of Merit [$R_{DSon,SP}$*$Q_{GD,SP}$] and [$R_{DSon,SP}$*$Q_{SW,SP}$] in mΩ*nC for the U-MOSFET structure in Problem 6.25.

Solution:

The specific on-resistance for the trench-gate power U-MOSFET structure is 1.58 mΩ-cm^2 (see Problem 6.19). The specific reverse-transfer gate charge for this structure is 218.1 nC/cm^2 (see Problem 6.25).

Using these values, the Figure of Merit [$R_{DSon,SP}$*$Q_{GD,SP}$] calculated for this trench-gate power U-MOSFET structure is found to be 345 mΩ*nC.

The specific switching gate charge for this structure is 235.5 nC/cm^2 (see Problem 6.25). Using this value, the Figure of Merit [$R_{DSon,SP}$*$Q_{SW,SP}$] calculated for this trench-gate power U-MOSFET structure is found to be 372 mΩ*nC.

The Figures of Merit for the trench-gate U-MOSFET structure are much lower (better) than for the planar VD-MOSFET structure.

Problem 6.27:

Determine the optimum area for the VD-MOSFET structure in Problem 6.6 to minimize power losses at an operating frequency of 200 kHz. Use a gate bias of 5 volts, an on-state current of 10 A, and a duty cycle of 50 %.

Solution:

The optimum active area for the power MOSFET structure is given by:

$$A_{OPT} = \sqrt{\frac{R_{ON,sp}}{C_{IN,sp}}}\left(\frac{I_{ON}}{V_{GS}}\right)\left(\sqrt{\frac{\delta}{f}}\right) \qquad \textbf{[6.27a]}$$

For the VD-MOSFET structure in Problem 6.6, the specific on-resistance is 3.88 mΩ-cm^2 and the specific input capacitance is 27.7 nF/cm^2. Using these device parameters with the circuit parameters given in the problem, the optimum device is found to be 1.18 cm^2 to minimize the total power dissipation in the device.

Problem 6.28:

Determine the optimum area for the U-MOSFET structure in Problem 6.19 to minimize power losses at an operating frequency of 200 kHz. Use a gate bias of 5 volts, an on-state current of 10 A, and a duty cycle of 50 %.

Solution:

The optimum active area for the power MOSFET structure is given by:

$$A_{OPT} = \sqrt{\frac{R_{ON,sp}}{C_{IN,sp}}}\left(\frac{I_{ON}}{V_{GS}}\right)\left(\sqrt{\frac{\delta}{f}}\right) \qquad \textbf{[6.28a]}$$

For the U-MOSFET structure in Problem 6.19, the specific on-resistance is 1.58 mΩ-cm^2 and the specific input capacitance is 40.9 nF/cm^2. Using these device parameters with the circuit parameters given in the problem, the optimum device is found to be 0.62 cm^2 to minimize the total power dissipation in the device.

The optimum area for the trench-gate U-MOSFET structure is half that of the planar VD-MOSFET structure.

Problem 6.19:

Determine the specific on-resistance for a linear cell p-channel silicon U-MOSFET structure with a trench width of 1 micron and mesa width of 3 microns designed to support 100 volts. Assume that the breakdown voltage is limited by the edge termination to 80 percent of the parallel-plane value. The N-base doping concentration (assuming it is uniformly doped) is chosen to obtain a threshold voltage of 2 volts. The gate oxide thickness is 500 angstroms. The fixed charge in the gate oxide is 2×10^{11} cm^{-2}. Assume P^+ polysilicon with a doping concentration of 1×10^{20} cm^{-3} is used as the gate electrode. Use the following parameters: (a) inversion mobility of 150 cm^2/Vs; (b) accumulation mobility of 330 cm^2/Vs; (c) P^+ source length of 1 microns and sheet resistance of 30 Ohms/sq; (d) contact resistance of 1×10^{-6} Ohm-cm^2 for both the P^+ source and the drain; (e) P^+ source contact width of 1 micron; (f) P^+ substrate resistivity of 0.006 Ohm-cm and thickness of 500 microns; (g) gate bias of 5 volts; (h) K factor for accumulation spreading of 0.6; (i) P^+ source depth of 0.5 microns; (j) N-base depth of 1.5 microns; (k) trench depth of 2 microns; (l) mesa width is 4 microns; (m) trench width is 1 micron. What are the absolute and percentage contributions from each of the on-resistance components?

Solution:

The specific on-resistance of the U-MOSFET structure can be obtained by computing each of the components for the on-resistance given in section 6.8.

The absolute and percentage contributions from each of the on-resistance components for the given design are provided in the table.

Resistance	Value ($m\Omega$-cm^2)	Percentage Contribution
Source Contact	0.005	0.11
Source	0.000	0.00
Channel	0.814	17.51
Accumulation	0.133	2.86
JFET	0.000	0.00
Drift	3.40	73.12
Substrate	0.30	6.45
Drain Contact	0.001	0.02
Total	4.65	100

The total specific on-resistance is 2.94-times larger than for the n-channel power U-MOSFET structure in problem 6.19.

Problem 6.30:

Determine the ideal specific on-resistances for n-channel 4H-SiC power MOSFET structures with breakdown voltages of 300, 600, 1000, and 5000 volts. Take into account the variation of the critical electric field and mobility with doping concentration.

Solution:

The ideal specific on-resistance can be computed by using:

$$R_{on-sp,ideal} = \rho_D W_{C,PP} = \frac{W_{C,PP}}{q\mu_n N_D} \qquad \textbf{[P6.30a]}$$

The appropriate values for the parameters in this equation for each breakdown voltage are given in the table below.

Breakdown Voltage (Volts)	Doping Concentration (cm^{-3})	Mobility ($cm^2/V\text{-}s$)	Depletion Width (cm)	Specific On-Resistance ($Ohm\text{-}cm^2$)
300	2.15×10^{17}	566	1.24×10^{-4}	6.36×10^{-6}
600	8.55×10^{16}	720	2.78×10^{-4}	2.82×10^{-5}
1000	4.33×10^{16}	823	5.05×10^{-4}	8.87×10^{-5}
5000	5.06×10^{16}	1033	3.30×10^{-3}	3.95×10^{-3}

Problem 6.31:

Calculate the P-base doping concentration (assuming it is uniformly doped) of an n-channel 4H-SiC planar power MOSFET structure to obtain a threshold voltage of 5 volts. The gate oxide thickness is 500 angstroms. The fixed charge in the gate oxide is 2 x 10^{11} cm^{-2}. Assume N^+ polysilicon with a doping concentration of 1 x 10^{20} cm^{-3} is used as the gate electrode.

Solution:

The threshold voltage is given by:

$$V_{TH} = \frac{\sqrt{4\varepsilon_S kTN_A \ln(N_A / n_i)}}{C_{OX}} + \frac{2kT}{q}\ln\left(\frac{N_A}{n_i}\right) - \frac{Q_{OX}}{C_{OX}} \qquad \textbf{[6.31a]}$$

where the total *effective charge* in the oxide (Q_{OX}). In addition, the work-function difference between heavily doped N^+ polysilicon and P-type 4H-SiC must be taken into account. A threshold voltage of 5.0 volts is achieved at a doping concentration of 4.68 x 10^{16} cm^{-3}. The contribution from the fixed oxide charge is -0.469 volts. The shift due to the N^+ polysilicon gate electrode is -0.968. These contributions require increasing the P-base doping concentration which is beneficial for suppressing reach-through in the base region.

The P-base doping concentration in the 4H-SiC power MOSFET structure is lower than that for the silicon structure (see Problem 6.2) in spite of the larger threshold voltage. The reduced P-base doping concentration the 4H-SiC power MOSFET structure, in conjunction with the larger doping concentration in the N-drift region, makes the reach-through problem worse.

Problem 6.32:

Determine the drift region doping concentration and thickness for an n-channel 4H-SiC planar power MOSFET structure when the structure is designed to support 1000 volts assuming all the blocking voltage is supported by the drift region. Assume one-dimensional breakdown voltage is achievable in this case.

Solution:

The drift region doping concentration and thickness are determined by the parallel-plane breakdown voltage analysis. The doping concentration required to achieve a desired parallel-plane breakdown voltage for an abrupt junction in 4H-SiC can be obtained by using:

$$BV_{PP}(4H-SiC) = 3.0x10^{15} N_D^{-3/4} \qquad \textbf{[P6.32a]}$$

For a breakdown voltage of 1000 volts, the doping concentration in the drift region is 4.33 x 10^{16} cm^{-3} (also see Problem 6.30). The maximum depletion layer width at breakdown for an abrupt junction in silicon can then be obtained from the doping concentration by using:

$$W_{PP}(4H-SiC) = 1.82x10^{11} N_D^{-7/8} \qquad \textbf{[P6.32b]}$$

For a breakdown voltage of 1000 volts, the depletion layer width at breakdown is 5.05 microns (also see Problem 6.30). This is the thickness required for the drift region for one-dimensional (parallel-plane) breakdown conditions.

Problem 6.33:

Calculate the depletion width within the P-base region of the above n-channel 4H-SiC planar power MOSFET structure when the structure is supporting 1000 volts.

Solution:

The depletion width within the P-base region is given by:

$$W_P = \sqrt{\frac{2\varepsilon_S BV}{q}\left[\frac{N_D}{N_A\left(N_A + N_D\right)}\right]} \qquad \textbf{[P6.33a]}$$

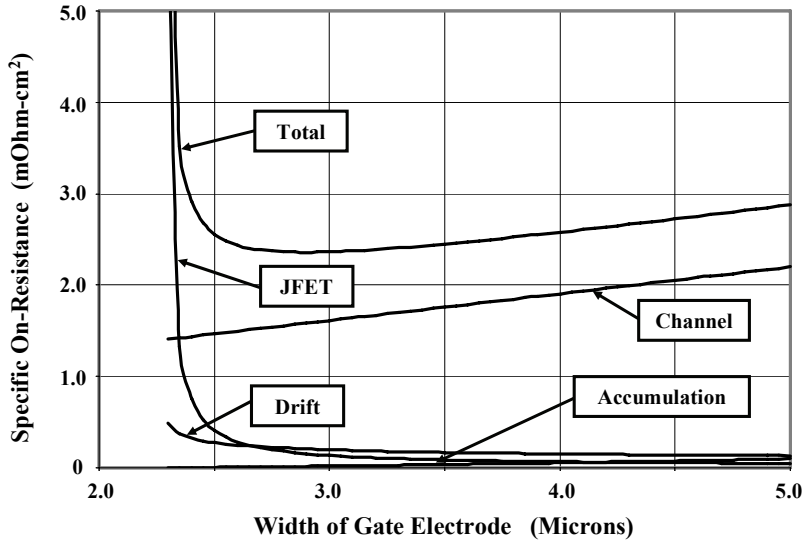
Using a doping concentration (N_D) of 4.33 x 10^{16} cm^{-3} in the N-drift region and a doping concentration (N_A) of 4.68 x 10^{16} cm^{-3} in the P-base region with a breakdown voltage of 1000 volts in this equation yields a depletion width within the P-base region of 3.59 microns. The large depletion of the P-base region requires making the channel length very large to prevent reach-through breakdown problems.

Problem 6.34:

Determine the optimum width for the gate electrode for a linear cell topology for the above n-channel 4H-SiC planar power MOSFET structure using the following parameters: (a) inversion mobility of 50 cm^2/Vs; (b) accumulation mobility of 100 cm^2/Vs; (c) cell polysilicon window width of 5 microns; (d) N^+ source length of 2.5 microns and sheet resistance of 50 Ohms/sq; (e) contact resistance of 1 x 10^{-5} Ohm-cm^2 for both the N^+ source and the drain; (f) N^+ source contact width of 1 micron; (g) N^+ substrate resistivity of 0.02 Ohm-cm and thickness of 200 microns; (h) gate bias of 15 volts; (i) K factor for accumulation spreading of 0.6; (k) P^+ region depth of 1 micron; (l) channel length of 1 micron. What are the absolute and percentage contributions from each of the on-resistance components for the optimum design?

Solution:

The optimum gate width can be obtained by computing each of the components for the on-resistance of the n-channel 4H-SiC planar power MOSFET structure given in section 6.6. A graph of the variation in the specific on-resistance as a function of gate width is provided below:



The minimum specific on-resistance of 2.36 milliOhm-cm^2 is obtained at an optimum gate width of 2.9 microns and a cell pitch of 5.4 microns for the cell structure shown in Fig. 6.113.

The absolute and percentage contributions from each of the on-resistance components for the optimum design are provided in the table.

Resistance	**Value ($m\Omega$-cm^2)**	**Percentage Contribution**
Channel	1.58	66.95
Accumulation	0.02	0.85
JFET	0.15	6.36
Drift	0.21	8.90
Substrate	0.40	16.95
Total	2.36	100

Note that the channel resistance becomes dominant for this 4H-SiC MOSFET structure due to the low channel mobility.

Problem 6.35:

Calculate the specific on-resistance (in mOhm-cm^2) for the ideal drift region in 4H-SiC for blocking 1000 volts. Compare the optimum design in Problem 6.34 to the ideal case by taking the ratio of specific on-resistances.

Solution:

The ideal specific on-resistance can be computed by using:

$$R_{on-sp,ideal} = \rho_D W_{C,PP} = \frac{W_{C,PP}}{q\mu_n N_D} \qquad \textbf{[P6.35a]}$$

The appropriate values for the parameters in this equation for a breakdown voltage of 1000 volts are a drift region thickness of 5.5 microns and a doping concentration of 4.33 x 10^{16} cm^{-3}. Using these values in the above equation yields a specific on-resistance of 0.089 mOhm-cm^2. The specific on-resistance for the optimum design in Problem 6.34 is a factor of 26.5-times larger than the ideal specific on-resistance.

Chapter 7
Bipolar Junction Transistors

Problem 7.1:

A bipolar transistor has a common emitter current gain of 50. Determine its common base current gain.

Solution:

The common-base current gain is related to the common-emitter current gain by:

$$\alpha = \frac{i_C}{\left(i_B + i_C\right)} = \frac{\beta . i_B}{\left(i_B + \beta . i_B\right)} = \frac{\beta}{\left(1 + \beta\right)} \qquad \textbf{[7.1a]}$$

The common-base current gain has a value of 0.980 at a common emitter current gain of 50.

Problem 7.2:

The open-emitter breakdown voltage of the above bipolar transistor is 1000 volts. Determine its open-base breakdown voltage.

Solution:

The open-base breakdown voltage is related to the open-emitter breakdown voltage and the common emitter current gain by:

$$\frac{BV_{CEO}}{BV_{CBO}} = \frac{1}{\left[1+\beta_{NPN}(0)\right]^{1/n}} \qquad \textbf{[7.2a]}$$

where n = 6. Substituting the values for this problem yields an open-base breakdown voltage of 519 volts.

Problem 7.3:

Consider an $N^+PN\text{-}N^+$ bipolar power transistor structure with uniformly doped emitter, base, and collector drift regions. The N^+ emitter region has a doping concentration of 2 x 10^{19} cm^{-3} and thickness of 10 microns. The P-base region has a doping concentration of 2 x 10^{17} cm^{-3} and thickness of 10 microns. The N-collector drift region has a doping concentration of 2 x 10^{14} cm^{-3} and thickness of 40 microns. The Shockley-Read-Hall (low-level, high-level, and space-charge generation) lifetimes are 10 ns in the emitter region, 1 μsec in the base region, 10 μsec in the collector drift region. Calculate the emitter injection efficiency at low injection levels in the P-base region ignoring band-gap narrowing and Auger recombination.

Solution:

The emitter injection efficiency at low injection levels in the P-base region is given by:

$$\gamma_E = \frac{D_{nB} L_{pE} n_{iB}^2 N_{DE}}{D_{nB} L_{pE} n_{iB}^2 N_{DE} + D_{pE} W_B n_{iE}^2 N_{AB}} \qquad \textbf{[7.3a]}$$

The intrinsic carrier concentrations in the emitter and base regions are equal if band gap narrowing is neglected. Based upon the doping concentrations and lifetime values in the emitter and base region, the values for the parameters in the above equation are D_{nB} = 15.6 cm^2/V-s; D_{pE} = 1.3 cm^2/V-s; L_{pE} = 1.14 microns; W_B = 10 microns; N_{DE} = 2 x 10^{19} cm^{-3}; N_{AB} = 2 x 10^{17} cm^{-3}. Using theses values in the above equation yields an emitter injection efficiency at low injection levels in the P-base region of 0.993.

Problem 7.4:

Determine the base transport factor for the power bipolar transistor described in Problem 7.3.

Solution:

The base transport factor can be obtained using:

$$\alpha_T = \frac{J_{nC}}{J_{nE}} = \frac{1}{\cosh\left(W_B / L_{nB}\right)} \qquad \textbf{[7.4a]}$$

The values for the parameters in the above equation are L_{nB} = 1.14 microns; W_B = 10 microns. Using theses values in the above equation yields a base transport factor of 0.969.

Problem 7.5:

Determine the common-emitter and common-base current gains for the power bipolar transistor described in Problem 7.3 at low injection levels in the P-base region.

Solution:

The common-base current gain is given by:

$$\alpha_{NPN} = \gamma_E . \alpha_T \qquad \textbf{[7.5a]}$$

Using the values from the previous problems, the common-base current gain is found to be 0.962.

The common-emitter current gain is given by:

$$\beta_{NPN} = \frac{\alpha_{NPN}}{1 - \alpha_{NPN}} \qquad \textbf{[7.5b]}$$

Using the values from the previous problems, the common-emitter current gain is found to be 25.3.

Problem 7.6:

Determine the open-emitter breakdown voltage (BV_{CB0}) for the power bipolar transistor described in Problem 7.3 using the critical electric field for the doping concentration in the collector drift region. Make sure to take punch-through into account for the drift region. Confirm that the depletion region has not penetrated the entire base region.

Solution:

The critical electric field for breakdown at the N-drift region doping concentration of 2×10^{14} cm^{-3} is 2.46×10^5 V/cm. The punch-through breakdown voltage for the P-base/N-drift region junction is given by:

$$BV_{CB0} = E_C W_D - \frac{qN_D W_D^2}{2\varepsilon_S} \qquad \textbf{[7.6a]}$$

Using the values for this problem yields an open-emitter breakdown voltage (BV_{CB0}) of 737 volts.

Problem 7.7:

Calculate the open-base breakdown voltage (BV_{CE0}) for the power bipolar transistor described in Problem 7.3 using n = 6 in the equation for the multiplication factor.

Solution:

The open-base breakdown voltage is related to the open-emitter breakdown voltage and the common emitter current gain by:

$$\frac{BV_{CEO}}{BV_{CBO}} = \frac{1}{\left[1+\beta_{NPN}(0)\right]^{1/n}} \qquad \textbf{[7.7a]}$$

where n = 6. Substituting the values for this problem yields an open-base breakdown voltage of 427 volts.

Problem 7.8:

Determine the leakage current density at 300°K at a collector bias of 200 volts due to space-charge-generation in the collector drift region. What is the open-base leakage current density under these conditions?

Solution:

The entire drift region is depleted at a reverse bias of 300 volts across the P-base/N-drift junction. The space-charge-generation current density in the collector drift region is then given by:

$$J_{SCG} = \frac{qn_i W_D}{\tau_{SC}} \qquad \textbf{[7.8a]}$$

Using the parameters for this problem yields a space-charge-generation current density of 0.88 microamperes/cm^2.

Under open-base operation, the space charge generation current is amplified by the gain of the transistor and is given by:

$$J_{Open-Base} = \frac{J_{SCG}}{\left(1-\alpha_{NPN}\right)} \qquad \textbf{[7.8b]}$$

Using the parameters for this problem yields a space-charge-generation current density of 23.2 microamperes/cm^2.

Problem 7.9:

Calculate the quasi-saturation specific resistance for the power bipolar transistor described in Problem 7.3.

Solution:

The quasi-saturation specific resistance is given by:

$$R_{D,sp} = \rho_D . W_D = \frac{W_D}{q\mu_n N_D} \qquad \textbf{[7.9a]}$$

Using the parameters for this problem yields a quasi-saturation specific resistance of 0.092 Ohm-cm^2.

Problem 7.10:

Determine the Webster current density for the power bipolar transistor described in Problem 7.3.

Solution:

The Webster current density is given by:

$$J_W = \frac{qD_{nB}N_{AB}}{W_B} \qquad \textbf{[7.10a]}$$

Using the parameters for this problem yields a Webster current density of 500 A/cm^2.

Problem 7.11:

What is the common-emitter current gain for the power bipolar transistor described in Problem 7.3 at a current density of 1000 A/cm^2?

Solution:

The current gain at high current density levels can be expressed as:

$$\beta_E = \frac{\beta_{LL}}{\left[1 + \left(J_C / J_W\right)\right]} \qquad \textbf{[7.11a]}$$

For this N-P-N bipolar transistor, the current gain at low current levels is 25.3 (see Problem 7.5) and the Webster current density is 500 A/cm^2 (see Problem 7.10). Using these values in the above equation yields a current gain of 8.43 at a current density of 1000 A/cm^2.

Problem 7.12:

Determine the Kirk current density for the power bipolar transistor described in Problem 7.3 at a collector bias of 300 volts.

Solution:

The Kirk current density can be expressed in terms of the device physical parameters and the applied collector bias voltage:

$$J_K = qv_{sat,n}\left(\frac{2\varepsilon_S V_C}{qW_N^2} + N_D\right) \qquad \textbf{[7.12a]}$$

Using the parameters for this problem yields a Kirk current density of 709 A/cm^2.

Problem 7.13:

What is the Early voltage for the power bipolar transistor described in Problem 7.3?

Solution:

The Early voltage is given by:

$$V_E = \frac{qW_B^2}{K_E \varepsilon_S}\left(\frac{N_{AB}}{N_D}\right)\left(N_{AB} + N_D\right) \qquad \textbf{[7.13a]}$$

Using the parameters for this problem with $K_E = 8$ yields an Early voltage of 3.1×10^7 V.

Problem 7.14:

Determine the on-state voltage drop (V_{CEsat}) for the power bipolar transistor described in Problem 7.3 in the saturation region of operation. Assume that the injected hole concentration at the B-C junction [$p_{NS}(0)$] is 2 x 10^{16} cm^{-3} and the injected hole concentration is equal to the doping concentration at the N-drift/N^+ substrate interface. What is the collector current density under these operating conditions? Calculate the stored charge in the collector drift region under these conditions.

Solution:

The on-state voltage drop (V_{CEsat}) is given by:

$$V_{CE,sat} = \frac{kT}{q} \ln\left[\frac{p_{NS}(0)}{p_{NS}(W_D)}\right] \qquad \textbf{[7.14a]}$$

Using the parameters for this problem yields an on-state voltage drop (V_{CEsat}) of 0.12 V.

The collector current density under these conditions is given by:

$$J_C = \frac{2qD_n p_{NS}(0)}{W_N} \qquad \textbf{[7.14b]}$$

Using the parameters for this problem yields a collector current density of 56.4 A/cm^2.

The stored charge under these conditions is given by:

$$Q_{Sat} = \frac{1}{2} q p_{NS}(0) W_N \qquad \textbf{[7.14c]}$$

Using the parameters for this problem yields a stored charge density of 6.40 x 10^{-6} C/cm^2.

Problem 7.15:

The power bipolar transistor described in Problem 7.3 is turned-off from an initial on-state conditions described in Problem 7.14 by using a reverse base drive current density of 5 A/cm^2. Determine the storage time during the turn-off process.

Solution:

The storage time is given by:

$$t_S = \left(\frac{J_{C,ON}}{J_{BR}} \right) \left[\frac{W_B^2}{2D_n} + \frac{W_{NM}^2}{4D_n} \frac{D_p J_{C,ON}}{\left(D_n J_{BR} + D_p J_{C,ON} \right)} \right] \qquad \textbf{[7.15a]}$$

For the operating conditions for this bipolar power transistor structure, the on-state collector current density is 56.4 A/cm^2 (see Problem 7.14) and the modulated width (W_{NM}) is equal to the width of the drift region. Using the parameters for this problem yields a storage time of 1.16 microseconds.

Problem 7.16:

What is the voltage rise-time under the turn-off conditions described in Problem 7.15 if the collector bias voltage is 300 volts? Determine the width of the emitter finger that has been turned-off at this point in time if the emitter width (W_E) is 200 microns.

Solution:

The voltage rise time (t_V) is given by:

$$t_V = \frac{\sqrt{2q\varepsilon_S N_D V_{CS}}}{J_{BR}} \qquad \textbf{[7.16a]}$$

Using the parameters for this problem with a collector bias of 300 volts and a reverse base drive current of 5 A/cm^2 yields a voltage rise time of 28 nanoseconds.

The width of the finger that has been turned-off during the voltage rise time is given by:

$$X_V = \frac{2D_n W_E J_{BR} t_V}{J_{C,ON} W_B^2} \qquad \textbf{[7.16b]}$$

For this power bipolar transistor with an emitter width of 200 microns and P-base width of 10 microns, the width (X_V) that has turned-off at the end of the voltage rise time is found to be 35.3 microns when the on-state collector current density is 56.4 A/cm^2 and reverse base current density is 5 A/cm^2. Thus, approximately one-sixth of the emitter finger is turned-off at this time while the collector current remains constant leading to a slight increase in the current density in the remaining portion of the emitter finger.

Problem 7.17:

Determine the velocity for shrinking the on-portion of the emitter finger during the turn-off process. What is the collector current fall-time for the conditions described in Problems 7.15 and 7.16?

Solution:

The velocity for the movement of the on-portion is given by:

$$v_{ON} = \frac{2D_n W_E J_{BR}}{W_B^2 J_{C,ON}} - \frac{D_n}{L_n} \qquad \textbf{[7.17a]}$$

For this power bipolar transistor with an emitter width of 200 microns and P-base width of 10 microns, the velocity for the movement of the on-portion is found to be 1.25 x 10^5 cm/s when the on-state collector current density is 56.4 A/cm^2 and reverse base current density is 5 A/cm^2.

The time taken for the collector current to decrease to zero, defined as the *current fall time*, can be obtained using:

$$t_F = \frac{W_E - X_V}{v_{ON}} \qquad \textbf{[7.17b]}$$

Using a width of 35.2 microns for the portion turned-off during the voltage transient, the collector current fall time is then found to be 134 nanoseconds.

Problem 7.18:

Calculate the energy loss incurred during the turn-off process described in Problems 7.15, 7.16, and 7.17.

Solution:

The energy loss per turn-off event is given by:

$$E_{OFF} = \int_0^{t_e} J_C(t).V_C(t)\,dt = \frac{J_{CON}V_{CS}}{3}t_v + \frac{J_{CON}V_{CS}}{2}t_F \qquad \textbf{[7.18a]}$$

In this problem, the on-state collector current density is 56.4 A/cm^2 and the collector supply voltage is 300 volts. The voltage rise-time is 28 nanoseconds (see Problem 7.16) and the current fall-time is 134 nanoseconds (see Problem 7.17). Using these values in the above equation yields an energy loss per turn-off event of 1.29 mJ/cm^2.

Problem 7.19:

A Darlington power transistor is designed with a common-emitter current gain of 10 for the input transistor and 5 for the output transistor. What is the current gain for the Darlington transistor?

Solution:

The common emitter current gain for the Darlington configuration is given by:

$$\beta_{BD} = \frac{I_{CD}}{I_{BD}} = \beta_1 + \beta_2(1+\beta_1) = \beta_1 + \beta_2 + (\beta_1\beta_2) \qquad \textbf{[7.19a]}$$

The common emitter current gain obtained with a common-emitter current gain (β_1) of 10 for the input transistor and a common-emitter current gain (β_2) of 5 for the output transistor is 65.

Problem 7.20:

What is the typical on-state voltage drop for the Darlington transistor?

Solution:

The collector potential for the Darlington configure consists of the voltage drop across the input transistor plus the base-emitter voltage drop for the output transistor:

$$V_{CE,D} = V_{CE1} + V_{BE2} \qquad \textbf{[7.20a]}$$

If the input transistor is driven into saturation to reduce its on-state voltage drop (V_{CE1}) to about 0.5 volts, the voltage drop for the Darlington configuration becomes about 1.5 volts.

Chapter 8
Thyristors

Problem 8.1:

Consider an $N^+PN\text{-}P^+$ power thyristor structure with uniformly doped N^+ cathode, P-base, N- drift and P^+ anode regions. The N^+ cathode region has a doping concentration of 2×10^{19} cm^{-3} and thickness of 10 microns. The P-base region has a doping concentration of 2×10^{17} cm^{-3} and thickness of 20 microns. The N- drift region has a doping concentration of 5×10^{13} cm^{-3} and thickness of 300 microns. The P^+ anode region has a doping concentration of 2×10^{19} cm^{-3} and thickness of 50 microns. The Shockley-Read-Hall (low-level, high-level, and space-charge generation) lifetime is 10 ns in the N^+ cathode and P^+ anode regions, 10 μsec in the P-base and N- drift regions. Ignore band-gap narrowing and Auger recombination. Use an ambipolar diffusion constant D_a of 15 cm^2/s for the on-state calculations. The structure has a linear cell geometry with an emitter width of 0.5 cm and length of 1 cm. What is the blocking voltage capability for the device?

Solution:

The blocking voltage capability for the thyristor structure is limited by open-base breakdown voltage of the P-N-P transistor. This breakdown voltage can be obtained using the procedure described in section 8.2.1. As the anode voltage is increased, the base-transport factor and multiplication co-efficient increase until the current gain becomes unity at the breakdown voltage. Using the parameters for the structure in this problem, the blocking voltage capability is found to be 2080 volts. At this anode voltage, the base transport factor is 0.844 and the multiplication co-efficient is 1.18.

Problem 8.2:

Determine the cathode short distance (D) for a square shorting array to prevent turn-on of the above thyristor structure. Use a maximum forward bias for the cathode/base junction of 0.5 volts at a leakage current density of 1 A/cm^2. Assume a cathode short size (d) of 25 microns.

Solution:

The largest forward bias produced in the P-base region by the leakage current is given by:

$$V_{B,Max} = J_L \rho_{SB} A_S \qquad \textbf{[8.2a]}$$

where the shorting geometry area factor is given by:

$$A_S = \frac{1}{16}\left\{ d^2 + D^2 \left[2\ln\left(\frac{D}{d}\right) - 1 \right] \right\} \qquad \textbf{[8.2b]}$$

Using the parameters for the P-base region, its sheet resistance is found to be 87 Ohms/square. The shorting geometry area factor is found to be 5.76 x 10^{-3} by using Eq. [8.2a]. Using this value in Eq. [8.2b] with a cathode short size (d) of 25 microns yields a cathode short distance (D) of 1173 microns.

Problem 8.3:

Determine the on-state current for the thyristor structure described in Problem 8.1 at a forward bias of 1.0 volts.

Solution:

The on-state voltage drop for a thyristor is given by:

$$V_{ON} = \frac{2kT}{q} \ln\left[\frac{J_{ON} d}{2qD_a n_i F\left(d / L_a\right)}\right] \qquad \textbf{[8.3a]}$$

The value for parameter d is $(W_P + W_N)/2 = 160$ microns. The diffusion length is 122 microns for a lifetime of 10 microseconds in the P-base and N-base regions. The function F(d/La) is 0.279 at a (d/L_a) value of 1.31 for this structure. The on-state current density for this thyristor structure is found to be 284 A/cm^2 at an on-state voltage drop of 1.0 volts by using Eq. [8.3a]. Using the device area of 0.5 cm^2, the on-state current is found to be 142 amperes.

Problem 8.4:

Calculate the gate triggering current for the thyristor structure described in Problem 8.1. Use the cathode shorting distance from Problem 8.2.

Solution:

The gate triggering current is given by:

$$I_{GT} = \frac{V_{bi} Z}{\rho_{SB} W_{KG}} \qquad \textbf{[8.4a]}$$

Using an emitter shorting distance (W_{KG}) of 0.117 cm (see Problem 8.2), an emitter length (Z) of 1 cm, a P-base sheet resistance (ρ_{SB}) of 87 Ohms/square, and a built-in potential (V_{bi}) of 0.8 volts, the gate triggering current for the thyristor structure is found to be 78.6 mA. The gate triggering current is far smaller than the on-state current for the thyristor.

Problem 8.5:

What is the holding current for the thyristor structure described in Problem 8.1? Use the cathode shorting distance from Problem 8.2 and a current gain of 0.5 for the N-P-N transistor in the on-state.

Solution:

The holding current density is given by:

$$J_H = \frac{8V_{bi}}{\left(1-\alpha_{NPN}\right)\rho_{SB}W_{KS}^2} \qquad \textbf{[8.5a]}$$

Using an emitter shorting distance (W_{KS}) of 0.117 cm, a current gain of 0.5 for the N-P-N transistor in the on-state, a P-base sheet resistance (ρ_{SB}) of 87 Ohms/square, and a built-in potential (V_{bi}) of 0.8 volts, the holding current density for the thyristor structure is found to be 10.7 A/cm^2. The holding current for this thyristor is 5.35 A based upon an area of 0.5 cm^2.

Problem 8.6:

Determine the [dV/dt] capability the thyristor structure described in Problem 8.1 when the device is blocking 100 volts. What is the maximum operating frequency for the thyristor if the sinusoidal anode voltage has a maximum value of 1000 volts?

Solution:

The [dV/dt] capability the thyristor structure is given by:

$$\left[\frac{dV}{dt}\right]_{Max} = \frac{8V_{bi}}{\rho_{SB}W_{KS}^2}\sqrt{\frac{2\left(V_A + V_{bi}\right)}{q\varepsilon_S N_D}} \qquad \textbf{[8.6a]}$$

Using an emitter shorting distance (W_{KS}) of 0.117 cm, a P-base sheet resistance (ρ_{SB}) of 87 Ohms/square, and a built-in potential (V_{bi}) of 0.8 volts, with an anode voltage of 100 volts in the above equation, the [dV/dt] capability the thyristor structure is found to be 2.65 x 10^{10} V/s.

Using a sinusoidal anode voltage waveform and recognizing that the maximum rate of change in the anode voltage occurs when the anode voltage crosses zero, the maximum operating frequency for the thyristor is given by:

$$f_{Max} = \frac{1}{\pi V_M \rho_{SB} W_{KS}^2}\sqrt{\frac{32V_{bi}^3}{q\varepsilon_S N_D}} \qquad \textbf{[8.6b]}$$

Using an emitter shorting distance (W_{KS}) of 0.117 cm, a P-base sheet resistance (ρ_{SB}) of 87 Ohms/square, and a built-in potential (V_{bi}) of 0.8 volts, with a maximum anode voltage of 1000 volts in the above equation, the maximum operating frequency for the thyristor structure is found to be 4.7 x 10^5 Hz.

However, the maximum operating frequency limited by the reverse recovery process is given by:

$$f_{Max} = \frac{1}{12\tau_{HL}} \qquad \textbf{[8.6c]}$$

Using a high-level lifetime of 10 microseconds in the N-base region, maximum operating frequency limited by the reverse recovery process is found to be 8330 Hz. The reverse recovery process limits the maximum operating frequency.

Problem 8.7:

Calculate the current rise-time when turning-on the thyristor structure described in Problem 8.1 with an anode supply voltage of 10 volts. What is the current rise-time if the anode supply voltage is increased to 100 volts? Use a gate current density of 1 A/cm^2.

Solution:

The current rise-time is defined as the time taken for the anode current density to increase to the on-state value. The rise time can be obtained using:

$$t_R = \sqrt{t_{t,NPN}.t_{t,PNP}}\ln\left(\frac{\alpha_{PNP}J_{A,SS}}{J_G}+1\right) \qquad \textbf{[8.7a]}$$

where $J_{A,SS}$ is the steady-state (on-state) anode current density. The rise-time is determined by the transit times for the internal N-P-N and P-N-P transistors within the thyristor structure. The transit time for the NPN transistor is given by:

$$t_{t,NPN} = \frac{W_P^2}{2D_n} \qquad \textbf{[8.7b]}$$

where W_P is the thickness of the P-base region. Using a value of 20 microns, the transit time for the NPN transistor is found to be 77 nanoseconds.

The transit time for the P-N-P transistor governed by the diffusion process at an anode bias of 10 volts is given by:

$$t_{t,PNP} = \frac{\left(W_N - W_{DN}\right)^2}{2D_p} \qquad \textbf{[8.7c]}$$

where W_N is the thickness of the N-base region. This value is 31 microseconds. The rise time obtaining by using these values in Eq. [8.7a] is 6.0 microseconds for a gate current density of 1 A/cm^2.

The transit time for the P-N-P transistor at an anode voltage of 100 volts is given by:

$$t_N = \frac{W_N}{v_P} = \frac{W_N^2}{\mu_P V_A} \qquad \textbf{[8.7d]}$$

The transit time determined by the drift process is 18.2 nanoseconds for a thyristor with an N-base region width of 300 microns at an anode bias of 100 volts. The rise time obtaining by using this value in Eq. [8.7a] is 0.15 microseconds for a gate current density of 1 A/cm^2.

Problem 8.8:

Using the typical current spreading velocity in a thyristor, determine the current spreading time for the thyristor structure described in Problem 8.1.

Solution:

The typical current spreading velocity in a thyristor structure is 5000 cm/s. The time taken for the anode current to spread across the 0.5 cm wide emitter finger is (0.5/5000) seconds or 100 microseconds.

Problem 8.9:

Design an amplifying gate thyristor structure using a gate electrode pad with radius of 0.25 cm to achieve a gate triggering current of 200 mA. Use the parameters given in Problem 8.1 for the semiconductor regions.

Solution:

The gate triggering current is given by:

$$I_{GT} = \frac{2\pi V_{bi}}{\rho_{S,PB} \ln\left(r_{SA} / r_{KA}\right)} \qquad \textbf{[8.9a]}$$

For the thyristor structure in Problem 8.1, the sheet resistance of the P-base region is 87 ohms/square. A gate drive current of 200 mA can be achieved for this thyristor by utilizing a ratio (r_{SA}/r_{KA}) of 1.33 based upon a built-in potential of 0.8 volts. The gate electrode pad in the center of the thyristor has a radius of 0.25 cm. An inner radius (r_{KA}) of 0.5 cm with an outer radius (r_{SA}) of 0.667 cm for the N^+ cathode region of the amplifying gate thyristor satisfies the design requirements in this case.

Problem 8.10:

Design a light-triggered thyristor using an optically generated current density of 0.1 A/cm^2 in the semiconductor. The central gate region has a radius of 0.25 cm.

Solution:

The radius of the N^+ cathode region in the optically triggered gate region for triggering the thyristor is given by:

$$r_{SG} = \sqrt{\frac{4V_{bi}}{J_0 \rho_{S,PB}}} \qquad \textbf{[8.10a]}$$

For the thyristor structure in Problem 8.1 with a sheet resistance of 87 ohms/square for the P-base region under the cathode, a design with radius (r_{SG}) of 0.606 cm will allow triggering the thyristor in the gate region if the optically induced current density is 0.1 A/cm^2.

Problem 8.11:

A gate-turn-off thyristor structure has uniformly doped N^+ cathode, P-base, N- drift and P^+ anode regions with the following parameters:. The N^+ cathode region has a doping concentration of 2 x 10^{19} cm^{-3} and thickness of 10 microns. The P-base region has a doping concentration of 2 x 10^{17} cm^{-3} and thickness of 40 microns. The N- drift region has a doping concentration of 5 x 10^{13} cm^{-3} and thickness of 300 microns. The P^+ anode region has a doping concentration of 2 x 10^{19} cm^{-3} and thickness of 50 microns. The Shockley-Read-Hall (low-level, high-level, and space-charge generation) lifetime is 10 ns in the N^+ cathode and P^+ anode regions, 10 μsec in the P-base and N- drift regions. Ignore band-gap narrowing and Auger recombination. Use an ambipolar diffusion constant D_a of 15 cm^2/s for the on-state calculations. The structure has a linear cell geometry with an emitter width of 200 microns and length of 1 cm. Determine the on-state current at an on-state voltage drop of 1.0 volts.

Solution:

The on-state voltage drop for a thyristor is given by:

$$V_{ON} = \frac{2kT}{q} \ln\left[\frac{J_{ON} d}{2qD_a n_i F\left(d / L_a\right)}\right] \qquad \textbf{[8.11a]}$$

The value for parameter d is $(W_P + W_N)/2$ = 170 microns. The diffusion length is 122 microns for a lifetime of 10 microseconds in the P-base and N-base regions. The function F(d/La) is 0.248 at a (d/L_a) value of 1.39 for this structure. The on-state current density for this thyristor structure is found to be 236 A/cm^2 at an on-state voltage drop of 1.0 volts by using Eq. [8.11a]. Using the device area of 0.02 cm^2, the on-state current is found to be 4.7 amperes.

Problem 8.12:

Determine the storage time if the gate-turn-off thyristor structure described in Problem 8.11 is turned-off at a current gain of 2 with a constant gate drive current.

Solution:

The storage time is given by:

$$t_S = \left(\frac{W_P \tau_{HL}}{W_P + W_N} \right) \left(\frac{J_{A,ON}}{J_{GR}} \right) = \left(\frac{W_P \tau_{HL}}{W_P + W_N} \right) \beta_T \qquad \textbf{[8.12a]}$$

where β_T is the turn-off gain. Using a P-base width of 40 microns, an N-drift region width of 300 microns, and a high-level lifetime of 10 microseconds in the N-drift region, the storage time is found to be 2.35 microseconds for a current gain of 2.

Problem 8.13:

The gate-turn-off thyristor structure described in Problem 8.11 is turned-off using a DC supply voltage of 1000 volts. Determine the voltage rise-time.

Solution:

The voltage rise-time t_V is given by:

$$t_V = \sqrt{\frac{2\varepsilon_S V_S}{q\left(N_D + p_{SC}\right)\left(W_P + W_N\right)^2}}\ \tau_{HL} \qquad \textbf{[8.113a]}$$

The hole concentration in the space charge region is given by:

$$p_{SC} = \frac{J_{A,ON}}{q v_{sat,p}} \qquad \textbf{[8.125]}$$

The hole concentration within the space-charge region is 1.48 x 10^{14} cm^{-3} at an anode current density of 236 A/cm^2. The voltage rise-time t_V is found to be 2.38 microseconds for an anode supply voltage of 1000 volts.

Problem 8.14:

Determine the current waveform during turn-off for the gate-turn-off thyristor structure described in Problem 8.13. Provide the magnitude of the sudden drop in the anode current. What is the time constant for the exponential decay in the anode current? Determine the current turn-off time.

Solution:

The anode current exhibits a sudden drop in magnitude followed by a current tail as illustrated in Fig. 8.44. The sudden fall in the anode current is given by:

$$I_{AT} = \beta_{PNP} I_{B,PNP} = \left(\frac{\alpha_{PNP}}{1-\alpha_{PNP}} \right) \alpha_{NPN} I_K \qquad \textbf{[8.14a]}$$

with the cathode current given by $I_K = I_{A,ON} - I_{GR}$. In this problem, $I_{A,ON}$ = 4.7 amperes and I_{GR} = 2.35 amperes resulting in I_K = 2.35 amperes. Using the parameters for this structure, the current gain (α_{NPN}) is found to be 0.924 and current gain (α_{PNP}) is found to be 0.389. Substitution of these values in Eq. [8.14a] yields a drop in anode current of 1.38 amperes.

The anode current decreases exponentially with time with a time constant of one-half of the high-level lifetime even though the free carrier density in the stored charge region is decreasing exponentially with time with a time constant equal to the high-level lifetime. The time constant for the exponential decay in the anode current is therefore 5 microseconds.

It is common practice to define a current turn-off time (t_i) as the duration for the anode current to decrease to one-tenth of its on-state value. This time is given by:

$$t_i = \frac{\tau_{HL}}{2} \ln \left[\frac{10 J_{A,D}}{J_{A,ON}} \right] = \frac{\tau_{HL}}{2} \ln \left[\frac{10 I_{A,D}}{I_{A,ON}} \right] \qquad \textbf{[8.14b]}$$

Using the value given above for the drop in anode current, the current $I_{A,D}$ = 3.32 amperes. The current turn-off time is then found to be 9.75 microseconds.

Problem 8.15:

Determine the energy loss during the turn-off of the gate-turn-off thyristor structure described in Problem 8.13 and Problem 8.14. Provide the Energy loss values associated with the voltage rise-time and the current fall time.

Solution:

The energy loss during the voltage rise-time is given by:

$$E_{OFF,V} = \frac{qJ_{A,ON}\left(N_D + p_{SC}\right)\left(W_P + W_N\right)^2}{6\varepsilon_S \tau_{HL}^2} t_V^3 \qquad \textbf{[8.15a]}$$

For the GTO structure in this problem with an anode supply voltage of 1000 volts, the energy loss during the voltage rise-time is found to be 0.187 Joules/cm^2 if the on-state current density is 236 A/cm^2.

The energy loss during the current fall-time interval is given by:

$$\begin{aligned} E_{OFF,I} &= \int_0^\infty V_S J_{A,D} e^{-2t/\tau_{HL}} dt \\ &= \frac{J_{A,D} V_S \tau_{HL}}{2} \end{aligned} \qquad \textbf{[8.15b]}$$

For the GTO structure in this problem with an anode supply voltage of 1000 volts, the energy loss during the current fall-time is found to be 0.83 Joules/cm^2 if the on-state current density is 236 A/cm^2 and the anode current density $J_{A,D}$ is 166 A/cm^2 (see Problem 8.14).

The total energy loss during the turn-off is 1.02 J/cm^2.

Problem 8.16:

What is the maximum controllable anode current for the gate-turn-off thyristor structure described in Problem 8.11. Assume one-dimensional parallel-plane breakdown voltage for the cathode/base junction.

Solution:

The maximum turn-off current density can be obtained by using:

$$J_{A,M} = \frac{4BV_{GK}}{\rho_{SB} W_{KS}^2} \left(\frac{\alpha_{NPN}}{\alpha_{NPN} + \alpha_{PNP} - 1} \right) \qquad \textbf{[8.16a]}$$

The breakdown voltage, determined by parallel-plane breakdown voltage (BV_{GK}) for a doping concentration of the P-base region of 2 x 10^{17} cm^{-3} is 5.65 volts. The current gains for the N-P-N and P-N-P transistors are 0.924 and 0.398, respectively (see Problem 8.14). Using these values with an emitter finger width of 200 microns yields a maximum controllable anode current of 3800 A/cm^2.

Chapter 9
Insulated Gate Bipolar Transistors

Problem 9.1:

Determine the doping concentration and width of the N-base region (drift region) for a planar-gate symmetric n-channel IGBT structure to obtain a blocking voltage of 600 volts. The lifetime (low-level, high-level, space-charge-generation) in the N-base region is 1 microsecond. Minimize the width of the N-base region within the nearest 5 microns. Provide the values for the depletion width, the base transport factor, and the multiplication factor for the P-N-P transistor at the breakdown condition.

Solution:

The blocking voltage for the symmetric IGBT is determined by the open-base breakdown voltage of the internal wide-base P-N-P transistor. The analysis of the blocking voltage capability can be performed using the procedure described in section 9.4.1. Using various values for the doping concentration of the N-base region, the width of the N-base region can be obtained for achieving a blocking voltage of 600 volts. From this analysis, the minimum N-base region width is found to be 75 microns for a doping concentration of 2×10^{14} cm^{-3}. For this design, the depletion width is 62 microns, the base transport factor is 0.953, and the multiplication factor is 1.05.

Problem 9.2:

What is the leakage current density for the planar-gate symmetric n-channel IGBT structure designed in Problem 9.1 at 400 ^{o}K when it is supporting 100 and 400 volts?

Solution:

In the case of the symmetric IGBT structure in the forward blocking mode, the space-charge-generation current at the reverse biased deep P^{+}/N-base junction J_2 is amplified by the gain of the internal P-N-P transistor:

$$J_L = \frac{J_{SCG}}{\left(1-\alpha_{PNP}\right)} \qquad \textbf{[9.2a]}$$

where the space-charge generation current density is given by:

$$J_{SCG} = \frac{qW_D n_i}{\tau_{SC}} = \frac{n_i}{\tau_{SC}}\sqrt{\frac{2q\varepsilon_S V_C}{N_D}} \qquad \textbf{[9.2b]}$$

The intrinsic concentration at 400 ^{o}K is 7.39 x 10^{12} cm^{-3}. Using a lifetime of 1 microsecond and a doping concentration of 2 x 10^{14} cm^{-3} in Eq. [9.2b], the space-charge-generation current density is found to be 3.01 x 10^{-3} and 6.02 x 10^{-3} A/cm^2 at 100 and 400 volts, respectively. The current gain of the PNP transistor is 0.472 and 0.810 at 100 and 400 volts, respectively. Using these values in Eq. [9.2a] yields a leakage current density of 5.70 x 10^{-3} and 3.22 x 10^{-2} A/cm^2 at 100 and 400 volts, respectively.

Problem 9.3:

Determine the width of the N-drift region for a planar-gate asymmetric n-channel IGBT structure to obtain a blocking voltage of 600 volts if its doping concentration is 1 x 10^{13} cm^{-3} assuming that punch-through breakdown voltage conditions are applicable.

Solution:

The blocking voltage for the asymmetric IGBT is determined by the open-base breakdown voltage of the internal wide-base P-N-P transistor. The analysis of the blocking voltage capability can be performed using the procedure described in section 9.4.4. In a simplified analysis, the width of the N-drift region can be obtained by dividing the blocking voltage with the critical electric field at breakdown. For a doping concentration of 1 x 10^{13} cm^{-3}, the critical electric field at breakdown 1.69 x 10^5 V/cm. The width of the N-drift region for a planar-gate asymmetric n-channel IGBT structure to obtain a blocking voltage of 600 volts is found to be 35.5 microns.

Problem 9.4:

What is the thickness of the N-buffer layer required to prevent open-base transistor breakdown in the planar-gate asymmetric IGBT structure designed in Problem 9.3 if its doping concentration is 1 x 10^{17} cm^{-3}? Assume that this width is the sum of the depletion region width in the buffer layer and one-diffusion length for minority carriers. The lifetime (low-level, high-level, space-charge-generation) in the N-drift region is 1 microsecond. Scale the lifetime for the N-buffer layer based upon its larger doping concentration. Round-up your width to the nearest 5 microns.

Solution:

The depletion region width in the buffer layer can be calculated by using the electric field of 1.69 x 10^5 V/cm in the N-drift region:

$$W_D\left(N-buffer\right)=\frac{\varepsilon_S E_C}{qN_{DB}} \qquad \textbf{[9.4a]}$$

Using a buffer layer doping concentration of 1 x 10^{17} cm^{-3}, the depletion region width in the buffer layer is found to be 0.11 microns. The diffusion length for holes in the N-buffer layer is found to be 5.36 microns. Rounding up the width, the thickness of the N-buffer layer is 10 microns.

Problem 9.5:

What is the leakage current density for the planar-gate asymmetric n-channel IGBT structure designed in Problem 9.4 at 400 ^{o}K when it is supporting 100 and 400 volts if the lifetime (low-level, high-level, space-charge-generation) in the N-drift region is 1 microsecond?

Solution:

The lightly doped portion of the N-drift region is depleted at both bias voltages. In addition, the depletion layer width in the N-buffer layer can be neglected for both bias voltages. The base-transport factor associated with the N-buffer layer can be obtained from the decay of the hole current within the N-buffer layer as given by low-level injection theory:

$$\alpha_{T,N-Buffer} = \frac{J_p\left(W_{NB}-\right)}{J_p\left(x_N\right)} = \frac{\gamma_E J_C e^{-W_{NB}/L_{p,NB}}}{\gamma_E J_C} = e^{-W_{NB}/L_{p,NB}} \qquad \textbf{[9.5a]}$$

where $J_p(x_N)$ is the hole current density at the P^+ collector/N-buffer layer junction (J_1); $J_p(W_{NB}-)$ is the hole current density at the interface between the lightly doped portion of the N-base region and the N-buffer layer; W_{NB} is the width of the N-buffer layer; and $L_{p,NB}$ is the minority carrier diffusion length in the N-buffer layer. Using a diffusion length of 5.36 microns and N-buffer region width of 10 microns, the base transport factor is found to be 0.155. The current gain of the PNP transistor is then 0.147 after accounting for an injection efficiency of 0.954. The space-charge-generation current at the reverse biased deep P^+/N-base junction J_2 is amplified by the gain of the internal P-N-P transistor:

$$J_L = \frac{J_{SCG}}{\left(1-\alpha_{PNP}\right)} \qquad \textbf{[9.5b]}$$

where the space-charge generation current density is given by:

$$J_{SCG} = \frac{qW_N n_i}{\tau_{SC}} \qquad \textbf{[9.5c]}$$

The space-charge generation current density is found to be 4.20 x 10^{-3} A/cm^2. The leakage current density is the found to be 4.92 x 10^{-3} A/cm^2.

Problem 9.6:

Determine the on-state voltage drop at an on-state current density of 100 A/cm^2 for the planar-gate symmetric n-channel IGBT design in Problem 9.1 using the one-dimensional P-i-N/MOSFET model. Use the following parameters: (a) D_a of 15 cm^2/s; (b) cell pitch of 16 microns; (c) channel length of 1.5 microns; (d) inversion mobility of 450 cm^2/V-s; (e) accumulation mobility of 1000 cm^2/V-s; (f) gate oxide thickness of 500 angstroms; (g) gate bias of 15 volts; (h) threshold voltage of 5 volts; (i) gate electrode width of 8 microns.

Solution:

In the MOSFET/P-i-N Model, the on-state voltage drop for the IGBT structure is given by the addition of the voltage drops across the P-i-N and MOSFET portions of the device:

$$V_{F,IGBT} = \frac{2kT}{q}\ln\left[\frac{J_C W_N}{4qD_a n_i F\left(W_N / 2L_a\right)}\right] + \frac{pL_{CH}J_{CH}}{\mu_{ni}C_{OX}\left(V_G - V_{TH}\right)} \qquad \textbf{[9.6a]}$$

For a width (W_N) of 75 microns and a lifetime of 1 microsecond in the N-drift region, the function F is found to be 0.351. Using the parameters provided for the symmetric IGBT structure, the on-state voltage drop at a current density of 100 A/cm^2 is found to be 0.938 volts. The contribution from the P-i-N portion is 0.860 volts and the contribution from the MOSFET portion is 0.078 volts.

Problem 9.7:

Determine the on-state voltage drop at an on-state current density of 100 A/cm^2 for the planar-gate asymmetric n-channel IGBT design in Problem 9.4 using the one-dimensional P-i-N/MOSFET model. Use the following parameters: (a) D_a of 15 cm^2/s; (b) cell pitch of 16 microns; (c) channel length of 1.5 microns; (d) inversion mobility of 450 cm^2/V-s; (e) accumulation mobility of 1000 cm^2/V-s; (f) gate oxide thickness of 500 angstroms; (g) gate bias of 15 volts; (h) threshold voltage of 5 volts; (i) gate electrode width of 8 microns.

Solution:

In the MOSFET/P-i-N Model, the on-state voltage drop for the IGBT structure is given by the addition of the voltage drops across the P-i-N and MOSFET portions of the device:

$$V_{F,IGBT} = \frac{2kT}{q}\ln\left[\frac{J_C W_N}{4qD_a n_i F\left(W_N / 2L_a\right)}\right] + \frac{pL_{CH}J_{CH}}{\mu_{ni}C_{OX}\left(V_G - V_{TH}\right)} \qquad \textbf{[9.7a]}$$

For a width (W_N) of (35.5 + 10) microns and a lifetime of 1 microsecond in the N-drift region, the function F is found to be 0.238. Using the parameters provided for the asymmetric IGBT structure, the on-state voltage drop at a current density of 100 A/cm^2 is found to be 0.932 volts. The contribution from the P-i-N portion is 0.854 volts and the contribution from the MOSFET portion is 0.078 volts.

Problem 9.8:

Compare the on-state voltage drops for the above IGBT designs to that for a planar-gate power MOSFET structure designed to support 600 volts using the same cell parameters.

Solution:

The specific on-resistance for a planar-gate power VD-MOSFET structure capable of supporting 600 volts is 0.1 ohm-cm^2 (see Fig. 6.50). The on-state voltage drop for the planar-gate power VD-MOSFET structure is 10 volts at an on-state current density of 100 A/cm^2. This value is approximately 10-times larger than the on-state voltage drop of the IGBT structures.

Problem 9.9:

Calculate the injected hole concentration at the P^+ collector/N-base junction for the planar-gate symmetric IGBT structure under the operating conditions defined in Problem 9.6. Assume an effective doping concentration of 1 x 10^{18} cm^{-3} for the P^+ collector region with a diffusion length for electrons of 0.5 microns. What is the injection efficiency at the P^+ collector/N-base junction under these operating conditions?

Solution:

The value of the hole concentration (p_0) at the P^+ collector/N-base junction can be computed using:

$$p_0 = -\frac{b}{2a}\left[1+\sqrt{1-\left(\frac{4ac}{b^2}\right)}\right] \qquad \textbf{[9.9a]}$$

with coefficients:

$$a = \frac{qD_{nE}}{L_{nE}N_{AE}J_C}\left(1-\frac{\mu_n}{\mu_p}\right) \qquad \textbf{[9.9b]}$$

$$b = -\frac{2qD_p}{L_a J_C \tanh\left(W_N / L_a\right)}\left(\frac{\mu_p}{\mu_n}\right) \qquad \textbf{[9.9c]}$$

$$c = -\left(\frac{\mu_n}{\mu_p}\right) \qquad \textbf{[9.9d]}$$

Using the parameters for the symmetric IGBT structure, the values are: a=3.09 x 10^{-34}; b=-4.05 x 10^{-18}; and c=-2.727. The injected hole concentration at the P^+ collector/N-base junction is then found to be 1.01 x 10^{17} cm^{-3}.

The injection efficiency at the P^+ collector/N-base junction under these operating conditions is found to be 0.159.

Problem 9.10:

Determine the on-state voltage drop at an on-state current density of 100 A/cm^2 for the planar-gate symmetric n-channel IGBT design in Problem 9.1 using the two-dimensional model. Use the following parameters: (a) D_a of 15 cm^2/s; (b) cell width of 32 microns; (c) channel length of 1.5 microns; (d) inversion mobility of 450 cm^2/V-s; (e) accumulation mobility of 1000 cm^2/V-s; (f) gate oxide thickness of 500 angstroms; (g) gate bias of 15 volts; (h) threshold voltage of 5 volts; (i) gate electrode width of 16 microns; (j) junction depth of P^+ region is 5 microns; (k) JFET region doping concentration of 5 x 10^{15} cm^{-3}. Provide the values for the voltage drop across the P^+/N junction, the N-base region, the JFET region, the accumulation region, and the channel region.

Solution:

The voltage drops in the symmetric IGBT structure for the two dimensional model can be calculated by using the equations in section 9.5.3. The on-state voltage drop for the IGBT structure can be obtained by using:

$$V_{ON} = V_{P+N} + V_{NB} + V_{MOSFET} \qquad \textbf{[9.10a]}$$

where V_{P+N} is the voltage drop across the P^+ collector/N-base junction (J_1), V_{NB} is the voltage drop across the N-base region after accounting for conductivity modulation due to high-level injection conditions, and V_{MOSFET} is the voltage drop across the MOSFET portion.

The voltage drop across the P^+ collector/N-base junction (J_1) can be obtained from the increase in the minority carrier concentration at the junction boundary:

$$V_{P+N} = \frac{kT}{q}\ln\left(\frac{p_0}{p_{0N}}\right) = \frac{kT}{q}\ln\left(\frac{p_0 N_D}{n_i^2}\right) \qquad \textbf{[9.10b]}$$

where the minority carrier density in equilibrium (p_{0N}) has been related to the doping concentration in the N-base region. The increase in the hole concentration at the junction (p_0) was obtained from the analysis in Problem 9.9. The voltage drop across the P^+ collector/N-base junction (J_1) is found to be 0.657 volts.

The voltage drop across the N-base region can be obtained by adding the voltage drop associated with the first part of the above electric field expression is:

$$V_{NB1} = \frac{2L_a J_C \sinh\left(W_N / L_a\right)}{qp_0\left(\mu_n + \mu_p\right)}\left\{\tanh^{-1}\left[e^{-(W_{ON}/L_a)}\right] - \tanh^{-1}\left[e^{-(W_N/L_a)}\right]\right\} \qquad \textbf{[9.10c]}$$

to the voltage drop associated with the second part of the above electric field expression is:

$$V_{NB2} = \frac{kT}{q}\left(\frac{\mu_n - \mu_p}{\mu_n + \mu_p}\right)\ln\left[\frac{\tanh\left(W_{ON}/L_a\right)\cosh\left(W_{ON}/L_a\right)}{\tanh\left(W_N/L_a\right)\cosh\left(W_N/L_a\right)}\right] \qquad \textbf{[9.10d]}$$

Using the parameters for the symmetric IGBT structure, the contribution from the drift region is found to be 0.178 volts.

Based upon the analysis for the power MOSFET structure:

$$V_{JFET} = J_C.R_{JFET,SP} = \frac{J_C\rho_{JFET}\left(x_{JP} + W_0\right)W_{CELL}}{\left(W_G - 2x_{JP} - 2W_0\right)} \qquad \textbf{[9.10e]}$$

where x_{JP} is the junction depth of the deep P^+ region. The voltage drop across the accumulation layer in the IGBT structure can also be derived based upon the analysis for the power MOSFET structure (see Eq. [6.66]):

$$V_{ACC} = J_C.R_{A,SP} = \frac{J_C K_A\left(W_G - 2x_{JP}\right)W_{CELL}}{4\mu_{nA}C_{OX}\left(V_G - V_{TH}\right)} \qquad \textbf{[9.10f]}$$

The accumulation layer coefficient (K_A) for the IGBT structure can be assumed to have the same value (0.6) as for power MOSFET structures. The voltage drop across the channel of the MOSFET portion can also be obtained by using the analysis for the power MOSFET structure (see Eq. [6.63]:

$$V_{CH} = J_C.R_{CH,SP} = \frac{J_C L_{CH} W_{CELL}}{2\mu_{ni}C_{OX}\left(V_G - V_{TH}\right)} \qquad \textbf{[9.10g]}$$

Using the parameters for this structure, the JFET, accumulation, and channel contributions are found to be 0.354, 0.035, and 0.078 volts, respectively. The total voltage drop associated with the MOSFET portion is 0.467 volts.

The total on-state voltage drop for the symmetric IGBT structure is then found to be 1.30 volts.

Problem 9.11:

Calculate the injected hole concentration at the P^+ collector/N-base junction for the planar-gate asymmetric IGBT structure under the operating conditions defined in Problem 9.7 with the assumption of low-level injection conditions in the N-buffer layer. Assume an effective doping concentration of 1 x 10^{19} cm^{-3} for the P^+ collector region with a diffusion length for electrons of 0.5 microns. What is the injection efficiency at the P^+ collector/N-base junction under these operating conditions? What is the hole concentration in the N-buffer layer at the interface between the N-drift and N-buffer regions? What is the hole concentration in the N-drift region at the interface between the N-drift and N-buffer regions?

Solution:

Low-level injection conditions prevail in the N-buffer layer due to its high doping concentration of 1 x 10^{17} cm^{-3}. The injected hole concentration at the P^+ collector/N-base junction is given by:

$$p\left(x_N\right)=\frac{p_{0,NB}L_{p,NB}L_{n,P+}}{\left(qD_{p,NB}p_{0,NB}L_{n,P+}+qD_{n,P+}n_{0,P+}L_{p,NB}\right)}J_C+p_{0,NB} \qquad \textbf{[9.11a]}$$

Using the parameters for the asymmetric IGBT structure, the injected hole concentration at the P^+ collector/N-base junction is found to be 5.31 x 10^{16} cm^{-3}.

The minority carrier density decreases to:

$$p\left(W_{NB}-\right)=\frac{p_{0,NB}L_{p,NB}L_{n,P+}}{\left(qD_{p,NB}p_{0,NB}L_{n,P+}+qD_{n,P+}n_{0,P+}L_{p,NB}\right)}J_C e^{-\left(W_{NB}/L_{p,NB}\right)} \qquad \textbf{[9.11b]}$$

at the interface between the N-drift and N-buffer regions. Using the parameters for the asymmetric IGBT structure, the injected hole concentration at the P^+ collector/N-base junction is found to be 8.21 x 10^{15} cm^{-3}.

The hole concentration in the N-drift region at the interface between the N-drift and N-buffer regions is given by:

$$p\left(W_{NB}+\right)=\frac{L_a\tanh\left[\left(W_N+W_{NB}\right)/L_a\right]}{2qD_p}J_p\left(W_{NB}-\right) \qquad \textbf{[9.11c]}$$

Using the parameters for the asymmetric IGBT structure, the hole concentration in the N-drift region at the interface between the N-drift and N-buffer regions is found to be 1.15 x 10^{16} cm^{-3}.

Problem 9.12:

Determine the on-state voltage drop at an on-state current density of 100 A/cm^2 for the planar-gate asymmetric n-channel IGBT design in Problem 9.4 using the two-dimensional model. Use the following parameters: (a) D_a of 15 cm^2/s; (b) cell width of 32 microns; (c) channel length of 1.5 microns; (d) inversion mobility of 450 cm^2/V-s; (e) accumulation mobility of 1000 cm^2/V-s; (f) gate oxide thickness of 500 angstroms; (g) gate bias of 15 volts; (h) threshold voltage of 5 volts; (i) gate electrode width of 16 microns. Provide the values for the voltage drop across the P^+/N junction, the N-base region, the JFET region, the accumulation region, and the channel region.

Solution:

The voltage drops in the asymmetric IGBT structure for the two dimensional model can be calculated by using the equations in section 9.5.3 and 9.5.5. The on-state voltage drop for the IGBT structure can be obtained by using:

$$V_{ON} = V_{P+N} + V_{NB} + V_{MOSFET} \qquad \textbf{[9.12a]}$$

where V_{P+N} is the voltage drop across the P^+ collector/N-buffer layer junction (J_1), V_{NB} is the voltage drop across the N-base region after accounting for conductivity modulation due to high-level injection conditions, and V_{MOSFET} is the voltage drop across the MOSFET portion.

The voltage drop across the P^+ collector/N-buffer layer junction (J_1) can be obtained from the increase in the minority carrier concentration at the junction boundary:

$$V_{P+N} = \frac{kT}{q}\ln\left(\frac{p(x_N)}{p_{0,NB}}\right) = \frac{kT}{q}\ln\left(\frac{p(x_N)N_{D,NB}}{n_i^2}\right) \qquad \textbf{[9.12b]}$$

where $p(x_N)$ is the injected hole concentration at the junction in the N-buffer layer (see Fig. 9.36) and $N_{D,NB}$ is the doping concentration in the N-buffer layer. The increase in the hole concentration at the junction [$p(x_N)$] was obtained from the analysis in Problem 9.11. The voltage drop across the P^+ collector/N-buffer layer junction (J_1) is found to be 0.802 volts.

The voltage drop across the N-base region can be obtained by adding the voltage drop associated with the first part of the above electric field expression is:

$$V_{NB1} = \frac{2L_aJ_C\sinh(W_N/L_a)}{qp(W_{NB}+)(\mu_n+\mu_p)}\left\{\tanh^{-1}\left[e^{-(W_{ON}/L_a)}\right] - \tanh^{-1}\left[e^{-(W_N/L_a)}\right]\right\} \qquad \textbf{[9.12c]}$$

to the voltage drop associated with the second part of the above electric field expression is:

$$V_{NB2} = \frac{kT}{q}\left(\frac{\mu_n - \mu_p}{\mu_n + \mu_p}\right)\ln\left[\frac{\tanh\left(W_{ON}/L_a\right)\cosh\left(W_{ON}/L_a\right)}{\tanh\left(W_N/L_a\right)\cosh\left(W_N/L_a\right)}\right] \qquad \textbf{[9.12d]}$$

Using the parameters for the asymmetric IGBT structure, the contribution from the drift region is found to be 0.122 volts.

Based upon the analysis for the power MOSFET structure:

$$V_{JFET} = J_C.R_{JFET,SP} = \frac{J_C\rho_{JFET}\left(x_{JP}+W_0\right)W_{CELL}}{\left(W_G - 2x_{JP} - 2W_0\right)} \qquad \textbf{[9.12e]}$$

where x_{JP} is the junction depth of the deep P^+ region. The voltage drop across the accumulation layer in the IGBT structure can also be derived based upon the analysis for the power MOSFET structure (see Eq. [6.66]):

$$V_{ACC} = J_C.R_{A,SP} = \frac{J_C K_A\left(W_G - 2x_{JP}\right)W_{CELL}}{4\mu_{nA}C_{OX}\left(V_G - V_{TH}\right)} \qquad \textbf{[9.12f]}$$

The accumulation layer coefficient (K_A) for the IGBT structure can be assumed to have the same value (0.6) as for power MOSFET structures. The voltage drop across the channel of the MOSFET portion can also be obtained by using the analysis for the power MOSFET structure (see Eq. [6.63]:

$$V_{CH} = J_C.R_{CH,SP} = \frac{J_C L_{CH} W_{CELL}}{2\mu_{ni}C_{OX}\left(V_G - V_{TH}\right)} \qquad \textbf{[9.12g]}$$

Using the parameters for this structure, the JFET, accumulation, and channel contributions are found to be 0.354, 0.035, and 0.078 volts, respectively. The total voltage drop associated with the MOSFET portion is 0.467 volts.

The total on-state voltage drop for the symmetric IGBT structure is then found to be 1.39 volts.

Problem 9.13:

Consider a transparent-emitter n-channel IGBT structure having a N-base region with a thickness of 300 microns and doping concentration of 5 x 10^{13} cm^{-3}. The lifetime (low-level, high-level, space-charge-generation) in the N-base region is 10 microseconds. The P^+ collector region has a surface concentration of 1 x 10^{18} cm^{-3} and depth of 1 micron. Determine the on-state voltage drop at an on-state current density of 100 A/cm^2 using the two-dimensional model. Use the following parameters: (a) D_a of 15 cm^2/s; (b) cell width of 32 microns; (c) channel length of 1.5 microns; (d) inversion mobility of 450 cm^2/V-s; (e) accumulation mobility of 1000 cm^2/V-s; (f) gate oxide thickness of 500 angstroms; (g) gate bias of 15 volts; (h) threshold voltage of 5 volts; (i) gate electrode width of 16 microns. Provide the values for the voltage drop across the P^+/N junction, the N-base region, the JFET region, the accumulation region, and the channel region.

Solution:

The voltage drops in the transparent emitter IGBT structure for the two dimensional model can be calculated by using the equations in section 9.5.7. The on-state voltage drop for the IGBT structure can be obtained by using:

$$V_{ON} = V_{P+N} + V_{NB} + V_{MOSFET} \qquad \textbf{[9.13a]}$$

where V_{P+N} is the voltage drop across the P^+ collector/N-base junction (J_1), V_{NB} is the voltage drop across the N-base region after accounting for conductivity modulation due to high-level injection conditions, and V_{MOSFET} is the voltage drop across the MOSFET portion.

The voltage drop across the P^+ collector/N-base junction (J_1) can be obtained from the increase in the minority carrier concentration at the junction boundary:

$$V_{P+N} = \frac{kT}{q}\ln\left(\frac{p_0}{p_{0N}}\right) = \frac{kT}{q}\ln\left(\frac{p_0 N_D}{n_i^2}\right) \qquad \textbf{[9.13b]}$$

where the minority carrier density in equilibrium (p_{0N}) has been related to the doping concentration in the N-base region. The increase in the hole concentration at the junction (p_0) is found to be 1.86 x 10^{16} cm^{-3}. The voltage drop across the P^+ collector/N-base junction (J_1) is found to be 0.578 volts.

The voltage drop in the N-base region is given by:

$$V_{NB} = \left[\frac{J_C W_N}{q\left(\mu_n + \mu_p\right)p_0} + \frac{kT}{q}\left(\frac{\mu_n - \mu_p}{\mu_n + \mu_p}\right)\right]\ln\left(\frac{W_N}{W_{ON}}\right) \qquad \textbf{[9.13c]}$$

Using the parameters for the symmetric IGBT structure, the contribution from the drift region is found to be 1.97 volts.

Based upon the analysis for the power MOSFET structure:

$$V_{JFET} = J_C.R_{JFET,SP} = \frac{J_C \rho_{JFET} \left(x_{JP} + W_0\right) W_{CELL}}{\left(W_G - 2x_{JP} - 2W_0\right)} \quad \textbf{[9.13d]}$$

where x_{JP} is the junction depth of the deep P^+ region. The voltage drop across the accumulation layer in the IGBT structure can also be derived based upon the analysis for the power MOSFET structure (see Eq. [6.66]):

$$V_{ACC} = J_C.R_{A,SP} = \frac{J_C K_A \left(W_G - 2x_{JP}\right) W_{CELL}}{4\mu_{nA} C_{OX} \left(V_G - V_{TH}\right)} \quad \textbf{[9.13e]}$$

The accumulation layer coefficient (K_A) for the IGBT structure can be assumed to have the same value (0.6) as for power MOSFET structures. The voltage drop across the channel of the MOSFET portion can also be obtained by using the analysis for the power MOSFET structure (see Eq. [6.63]:

$$V_{CH} = J_C.R_{CH,SP} = \frac{J_C L_{CH} W_{CELL}}{2\mu_{ni} C_{OX} \left(V_G - V_{TH}\right)} \quad \textbf{[9.13f]}$$

Using the parameters for this structure, the JFET, accumulation, and channel contributions are found to be 0.354, 0.035, and 0.078 volts, respectively. The total voltage drop associated with the MOSFET portion is 0.467 volts.

The total on-state voltage drop for the symmetric IGBT structure is then found to be 3.01 volts.

Problem 9.14:

Determine the injected hole concentration at the P^+ collector/N-base junction for the planar-gate transparent-emitter n-channel IGBT structure under the operating conditions defined in Problem 9.13. What is the injection efficiency at the P^+ collector/N-base junction under these operating conditions?

Solution:

The value of the hole concentration (p_0) at the P^+ collector/N-base junction can be computed using:

$$p_0 = -\frac{b}{2a}\left[1+\sqrt{1-\left(\frac{4ac}{b^2}\right)}\right] \qquad \textbf{[9.14a]}$$

with coefficients:

$$a = \frac{qD_{nE}}{W_{P+}N_{AE}} \qquad \textbf{[9.14b]}$$

$$b = -\left(\frac{2\mu_n\mu_p}{\mu_n+\mu_p}\right)\frac{kT}{W_N} \qquad \textbf{[9.14c]}$$

$$c = -\left(\frac{\mu_n}{\mu_n+\mu_p}\right)J_C \qquad \textbf{[9.14d]}$$

Using the parameters for the transparent-emitter IGBT structure, the values are: a=2.06 x 10^{-31}; b=-1.00 x 10^{-16}; and c=-73.17. The injected hole concentration at the P^+ collector/N-base junction is then found to be 1.86 x 10^{16} cm^{-3}.

The injection efficiency at the P^+ collector/N-base junction under these operating conditions is found to be 0.287.

Problem 9.15:

Obtain the saturated collector current density for the planar-gate symmetric n-channel IGBT design in Problem 9.1 using the P-N-P transistor/MOSFET model at a gate bias of 7 volts. Use the parameters defined in Problem 9.6.

Solution:

The saturated collector current density for the planar-gate symmetric n-channel IGBT structure is given by:

$$J_{C,SAT} = \frac{I_{C,SAT}}{p.Z} = \frac{\mu_{ni} C_{OX}}{2pL_{CH}\left(1-\alpha_{PNP}\right)}\left(V_G - V_{TH}\right)^2 \qquad \textbf{[9.15a]}$$

Using the parameters for this structure, the current gain (base transport factor) for the P-N-P transistor is found to be 0.283. The emitter injection efficiency at this gate bias is found to be 0.426. The current gain of the P-N-P transistor is then 0.120. Using this value, the saturated collector current density at a gate bias of 7 volts is then found to be 291 A/cm^2.

Problem 9.16:

Obtain the saturated collector current density for the planar-gate asymmetric n-channel IGBT design in Problem 9.4 using the P-N-P transistor/MOSFET model at a gate bias of 7 volts. Use the parameters defined in Problem 9.7 and Problem 9.11.

Solution:

The saturated collector current density J_{C0} at low collector bias voltages can be obtained from the base-drive current which is function of the gate bias voltage:

$$J_{C0} = \frac{J_{B,PNP}}{\left[1-\alpha_{PNP,0}\right]} \qquad \textbf{[9.16a]}$$

The base-drive current density provided via the channel of the MOSFET portion is given by:

$$J_{B,PNP} = \frac{\mu_{ni} C_{OX}}{2pL_{CH}}\left(V_G - V_{TH}\right)^2 \qquad \textbf{[9.16b]}$$

The base-drive current density is found to be 256 A/cm^2 using the parameters for this structure at a gate bias of 7 volts.

The current gain of the P-N-P transistor at low collector bias voltages is given by:

$$\alpha_{PNP,0} = \gamma_E \alpha_{T,0} = \gamma_E \alpha_{T,N-Buffer} \alpha_{T,N-Base,0} \qquad \textbf{[9.16c]}$$

The injection efficiency can be obtained by using:

$$\gamma_E = \frac{D_{p,NB} p_{0,NB} L_{n,P+}}{\left(D_{p,NB} p_{0,NB} L_{n,P+} + D_{n,P+} n_{0,P+} L_{p,NB}\right)} \qquad \textbf{[9.16d]}$$

Using the parameters for this structure, the injection efficiency is found to be 0.956. The base transport factor for the P-N-P transistor can be obtained by using:

$$\alpha_{T,N-Buffer} = \frac{J_p\left(W_{NB}-\right)}{J_p\left(x_N\right)} = \frac{\gamma_E J_C e^{-W_{NB}/L_{p,NB}}}{\gamma_E J_C} = e^{-W_{NB}/L_{p,NB}} \qquad \textbf{[9.16e]}$$

Using the parameters for this structure, the base transport factor is found to be 0.143. The current gain of the P-N-P transistor is found to be 0.136.

The saturated collector current density at a gate bias of 7 volts is then found to be 296 A/cm^2.

Problem 9.17:

Obtain the saturated collector current density for the planar-gate transparent-emitter n-channel IGBT design in Problem 9.13 using the P-N-P transistor/MOSFET model at a gate bias of 7 volts.

Solution:

The saturated collector current density J_{C0} at low collector bias voltages can be obtained from the base-drive current which is function of the gate bias voltage:

$$J_{C0} = \frac{J_{B,PNP}}{\left[1-\alpha_{PNP,0}\right]} \qquad \textbf{[9.17a]}$$

The base-drive current density provided via the channel of the MOSFET portion is given by:

$$J_{B,PNP} = \frac{\mu_{ni} C_{OX}}{2pL_{CH}}\left(V_G - V_{TH}\right)^2 \qquad \textbf{[9.17b]}$$

The base-drive current density is found to be 256 A/cm^2 using the parameters for this structure at a gate bias of 7 volts.

The current gain of the P-N-P transistor at low collector bias voltages is given by:

$$\alpha_{PNP,0} = \gamma_E \alpha_T \qquad \textbf{[9.17c]}$$

The injection efficiency can be obtained by using:

$$\gamma_{E,S} = 1 - \frac{qD_{nE}}{J_{C0}W_{P+}}\frac{p_0^2}{N_{AE}} \qquad \textbf{[9.17d]}$$

Using the parameters for this structure, the injection efficiency is found to be 0.283. The base transport factor for the P-N-P transistor can be assumed to be unity for the transparent-emitter structure. The current gain of the P-N-P transistor is then also 0.283.

Using the above values in Eq. [9.17a] yields a saturated collector current density at a gate bias of 7 volts of 357 A/cm^2.

Problem 9.18:

Calculate the specific output resistance for the planar-gate symmetric n-channel IGBT design in Problem 9.1 at a collector bias of 400 volts and a gate bias of 7 volts. What is the hole concentration in the space-charge-region?

Solution:

The specific output resistance for the symmetric IGBT structure is given by:

$$R_{O,sp} = \frac{\left[\left(1-\gamma_{E,S}\right)\left(BV_{SC}\right)^{n} - \left(V_C\right)^{n}\right]^2}{n\gamma_{E,S}J_{B,PNP}\left(BV_{SC}\right)^{n}\left(V_C\right)^{n-1}} \qquad \textbf{[9.18a]}$$

The emitter injection efficiency at the gate bias of 7 volts is 0.426. The value for BV_{SC} is found to be 1140 volts. The base-drive current density is 256 A/cm^2 at the gate bias of 7 volts.

Using these values in Eq. [9.18a] with a collector bias of 400 volts yields a specific output resistance of 9.31 ohm-cm^2.

The hole concentration in the space charge region is given by:

$$p_{SC} = \frac{J_{C0}}{qv_{sat,p}} \qquad \textbf{[9.18b]}$$

Using a saturated collector current density at a gate bias of 7 volts of 357 A/cm^2 (see Problem 9.15), the hole concentration in the space charge region is found to be 2.23 x 10^{14} cm^{-3}.

Problem 9.19:

Calculate the specific output resistance for the planar-gate asymmetric n-channel IGBT design in Problem 9.4 at a collector bias of 400 volts and a gate bias of 7 volts. What is the hole concentration in the space-charge-region?

Solution:

The specific output resistance for the asymmetric IGBT structure is given by:

$$R_{O,sp} = \frac{\left[\left(1-\gamma_E \alpha_{T,N-Buffer}\right)\left(BV_{SC}\right)^n - \left(V_{NPT}\right)^n\right]^2}{n\gamma_E \alpha_{T,N-Buffer} J_{B,PNP} \left(BV_{SC}\right)^n \left(V_{NPT}\right)^{n-1}} \qquad \textbf{[9.19a]}$$

The emitter injection efficiency at the gate bias of 7 volts is 0.72. The base transport factor for the N-buffer layer is found to be 0.155. The value for BV_{SC} is found to be 4450 volts. The base-drive current density is 256 A/cm^2 at the gate bias of 7 volts.

Using these values in Eq. [9.19a] with a collector bias of 400 volts yields a specific output resistance of 1490 ohm-cm^2.

The hole concentration in the space charge region is given by:

$$p_{SC} = \frac{J_{C0}}{q v_{sat,p}} \qquad \textbf{[9.19b]}$$

Using a saturated collector current density at a gate bias of 7 volts of 284 A/cm^2 (see Problem 9.15), the hole concentration in the space charge region is found to be 1.77 x 10^{14} cm^{-3}.

Problem 9.20:

Calculate the specific output resistance for the planar-gate transparent-emitter n-channel IGBT design in Problem 9.13 at a collector bias of 400 volts and a gate bias of 7 volts. What is the hole concentration in the space-charge-region?

Solution:

The specific output resistance for the transparent-emitter IGBT structure is given by:

$$R_{O,sp} = \frac{\left[\left(1-\gamma_{E,S}\right)\left(BV_{SC}\right)^n - \left(V_C\right)^n\right]^2}{n\gamma_{E,S}J_{B,PNP}\left(BV_{SC}\right)^n\left(V_C\right)^{n-1}} \qquad \textbf{[9.20a]}$$

The emitter injection efficiency at the gate bias of 7 volts is 0.278. The value for BV_{SC} is found to be 1530 volts. The base-drive current density is 256 A/cm^2 at the gate bias of 7 volts.

Using these values in Eq. [9.19a] with a collector bias of 400 volts yields a specific output resistance of 450 ohm-cm^2.

The hole concentration in the space charge region is given by:

$$p_{SC} = \frac{J_{C0}}{qv_{sat,p}} \qquad \textbf{[9.20b]}$$

Using a saturated collector current density at a gate bias of 7 volts of 284 A/cm^2 (see Problem 9.15), the hole concentration in the space charge region is found to be 2.24 x 10^{14} cm^{-3}.

Problem 9.21:

The planar-gate symmetric n-channel IGBT design in Problem 9.1 is switched off under inductive load conditions from the on-state operating conditions defined in Problem 9.6. Calculate the voltage rise-time to reach a collector DC supply voltage of 400 volts. What is the current fall-time? Obtain the energy loss per cycle.

Solution:

The analytical model for turn-off of the symmetric IGBT structure under inductive load conditions predicts a linear increase in the collector voltage with time. The end of the first phase of the turn-off process, where the collector voltage increases while the collector current remains constant, occurs when the collector voltages reaches the collector supply voltage (V_{CS}). This time interval ($t_{V,OFF}$) is given by:

$$t_{V,OFF} = \frac{\varepsilon_S p_0 V_{CS}}{W_N \left(N_D + p_{SC}\right) J_{C,ON}} \qquad \textbf{[9.21a]}$$

Under the operating conditions for this problem, the concentration $p_0 = 1.10 \times 10^{17}$ cm^{-3} (see Problem 9.9). Using this value with the other device parameters, the voltage rise-time interval is found to be 0.213 microseconds.

The collector current turn-off time is given by:

$$\tau_{I,OFF} = \frac{\tau_{HL}}{2} \ln\left(10\right) = 1.15 \tau_{HL} \qquad \textbf{[9.21b]}$$

Using a lifetime of 1 microsecond in the N-drift region, the collector current turn-off time is found to be 1.15 microseconds.

The energy loss during the first phase (voltage rise-time) of the turn-off process can be calculated using:

$$E_{V,OFF} = \frac{1}{2} J_{C,ON} V_{CS} t_{V,OFF} \qquad \textbf{[9.21c]}$$

Using the voltage rise-time interval of 0.213 microseconds, the energy loss during the first phase (voltage rise-time) is found to be 4.26 mJ/cm^2.

The energy loss during the second phase (current fall-time) of the turn-off process can be calculated using:

$$E_{I,OFF} = J_{C,ON} V_{CS} \left(\frac{\tau_{HL,N-Base}}{2} \right) \qquad \textbf{[9.21d]}$$

Using a high-level lifetime of 1 microsecond in the drift region, the energy loss during the second phase (current fall-time) is found to be 20.0 mJ/cm^2.

The total energy loss during turn-off is then found to be 24.26 mJ/cm^2.

Problem 9.22:

The planar-gate asymmetric n-channel IGBT design in Problem 9.4 is switched off under inductive load conditions from the on-state operating conditions defined in Problem 9.7. Calculate the voltage rise-time to reach a collector DC supply voltage of 400 volts. What is the current fall-time? Obtain the energy loss per cycle.

Solution:

The analytical model for turn-off of the asymmetric IGBT structure under inductive load conditions predicts a linear increase in the collector voltage with time. The end of the first phase of the turn-off process, where the collector voltage increases while the collector current remains constant, occurs when the collector voltages reaches the collector supply voltage (V_{CS}). This time interval ($t_{V,OFF}$) is given by:

$$t_{V,OFF} = \frac{\varepsilon_S p_{WNB+} V_{CS}}{W_N \left(N_D + p_{SC}\right) J_{C,ON}} \qquad \textbf{[9.22a]}$$

Under the operating conditions for this problem, the concentration p_{WNB+} = 1.15 x 10^{16} cm^{-3} (see Problem 9.11). Using this value with the other device parameters, the voltage rise-time interval is found to be 0.185 microseconds.

The collector current turn-off time is given by:

$$\tau_{I,OFF} = \tau_{p0,NB} \ln\left(10\right) = 2.3\tau_{p0,NB} \qquad \textbf{[9.22b]}$$

Using a scaled lifetime of 0.048 microseconds in the N-buffer layer, the collector current turn-off time is found to be 0.11 microseconds.

The energy loss during the first phase (voltage rise-time) of the turn-off process can be calculated using:

$$E_{V,OFF} = \frac{1}{2} J_{C,ON} V_{CS} t_{V,OFF} \qquad \textbf{[9.22c]}$$

Using the voltage rise-time interval of 0.185 microseconds, the energy loss during the first phase (voltage rise-time) is found to be 3.71 mJ/cm^2.

The energy loss during the second phase (current fall-time) of the turn-off process can be calculated using:

$$E_{I,OFF} = J_{C,ON} V_{CS} \tau_{p0,N-Buffer} \qquad \textbf{[9.22c]}$$

Using a lifetime of 0.048 microseconds in the N-buffer layer, the energy loss during the second phase (current fall-time) is found to be 1.9 mJ/cm^2.

The total energy loss during turn-off is then found to be 5.61 mJ/cm^2.

Problem 9.23:

The planar-gate transparent-emitter n-channel IGBT design in Problem 9.13 is switched off under inductive load conditions from the on-state operating conditions. Calculate the voltage rise-time to reach a collector DC supply voltage of 2000 volts. What is the current fall-time? Obtain the energy loss per cycle.

Solution:

The analytical model for turn-off of the transparent-emitter IGBT structure under inductive load conditions predicts a nearly-linear increase in the collector voltage with time. The end of the first phase of the turn-off process, where the collector voltage increases while the collector current remains constant, occurs when the collector voltages reaches the collector supply voltage (V_{CS}). This time interval ($t_{V,OFF}$) is given by:

$$t_{V,OFF} = \frac{\varepsilon_S V_{CS}\left(p_0 + p_{SC}\right)}{J_{C,ON} W_N \left(N_D + p_{SC}\right)} + \frac{p_{WN}}{J_{C,ON}} \sqrt{\frac{2q\varepsilon_S V_{CS}}{\left(N_D + p_{SC}\right)}} \qquad \textbf{[9.23a]}$$

Under the operating conditions for this problem, the concentration $p_0 = 1.86 \times 10^{16}$ cm^{-3} (see Problem 9.14). Using this value with the other device parameters, the voltage rise-time interval is found to be 0.115 microseconds.

The collector current turn-off time is given by:

$$\tau_{I,OFF} = K_{TE2}\sqrt{N_{AE}}\,\ln^2\left(10\right) = 5.3K_{TE2}\sqrt{N_{AE}} \qquad \textbf{[9.23b]}$$

Using a parameter K_{TE2} of 2.2×10^{-16} sec-$cm^{3/2}$, the collector current turn-off time is found to be 0.786 microseconds.

The energy loss during the first phase (voltage rise-time) of the turn-off process can be calculated using:

$$E_{V,OFF} = \frac{1}{2} J_{C,ON} V_{CS} t_{V,OFF} \qquad \textbf{[9.23d]}$$

Using the voltage rise-time interval of 0.115 microseconds, the energy loss during the first phase (voltage rise-time) is found to be 11.5 mJ/cm^2.

The energy loss during the second phase (current fall-time) of the turn-off process can be calculated using:

$$E_{I,OFF} = J_{C,ON} V_{CS}\left(2K_{TE2}\sqrt{N_{AE}}\right) \qquad \textbf{[9.23e]}$$

Using the above device parameters, the energy loss during the second phase (current fall-time) is found to be 59.3 mJ/cm^2.

The total energy loss during turn-off is then found to be 70.8 mJ/cm^2.

The energy loss values for this transparent emitter structure should not be compared with those of the symmetric and asymmetric structures in previous problems because the transparent emitter structure is capable of operating at a much larger collector bias supply voltage in this problem.

Problem 9.24:

Determine the on-state voltage drop at an on-state current density of 100 A/cm^2 for the planar-gate symmetric p-channel IGBT structure, with the same wide base parameters as for the n-channel device in Problem 9.10, using the two-dimensional model. Use the same drift region doping concentration and thickness obtained in Problem 9.1 Use the following parameters: (a) D_a of 15 cm^2/s; (b) cell pitch of 16 microns; (c) channel length of 1.5 microns; (d) inversion mobility of 200 cm^2/V-s; (e) accumulation mobility of 400 cm^2/V-s; (f) gate oxide thickness of 500 angstroms; (g) gate bias of 15 volts; (h) threshold voltage of 5 volts; (i) gate electrode width of 8 microns; (j) junction depth of P^+ region is 5 microns; (k) JFET region doping concentration of 5 x 10^{15} cm^{-3}. Provide the values for the voltage drop across the N^+/P junction, the P-base region, the JFET region, the accumulation region, and the channel region.

Solution:

The voltage drops in the symmetric IGBT structure for the two dimensional model can be calculated by using the equations in section 9.5.3. The on-state voltage drop for the IGBT structure can be obtained by using:

$$V_{ON} = V_{N+P} + V_{PB} + V_{MOSFET} \qquad \textbf{[9.24a]}$$

where V_{N+P} is the voltage drop across the N^+ collector/P-base junction (J_1), V_{PB} is the voltage drop across the P-base region after accounted for conductivity modulation due to high-level injection conditions, and V_{MOSFET} is the voltage drop across the MOSFET portion.

The voltage drop across the N^+ collector/P-base junction (J_1) can be obtained from the increase in the minority carrier concentration at the junction boundary:

$$V_{N+P} = \frac{kT}{q}\ln\left(\frac{n_0}{n_{0P}}\right) = \frac{kT}{q}\ln\left(\frac{n_0 N_A}{n_i^2}\right) \qquad \textbf{[9.24b]}$$

where the minority carrier density in equilibrium (n_{0P}) has been related to the doping concentration (N_A) in the P-base region. The increase in the hole concentration at the junction (n_0) is found to be 1.47 x 10^{17} cm^{-3}. The voltage drop across the N^+ collector/P-base junction (J_1) is found to be 0.667 volts.

The voltage drop across the P-base region can be obtained by adding the voltage drop associated with the first part of the above electric field expression:

$$V_{PB1} = \frac{2L_a J_C \sinh\left(W_P / L_a\right)}{q n_0 \left(\mu_n + \mu_p\right)} \left\{ \tanh^{-1}\left[e^{-(W_{ON}/L_a)}\right] - \tanh^{-1}\left[e^{-(W_P/L_a)}\right] \right\} \qquad \textbf{[9.24c]}$$

to the voltage drop associated with the second part of the above electric field expression:

$$V_{PB2} = \frac{kT}{q}\left(\frac{\mu_n - \mu_p}{\mu_n + \mu_p}\right)\ln\left[\frac{\tanh\left(W_{ON}/L_a\right)\cosh\left(W_{ON}/L_a\right)}{\tanh\left(W_P/L_a\right)\cosh\left(W_P/L_a\right)}\right] \qquad \textbf{[9.24d]}$$

Using the parameters for the symmetric IGBT structure, the contribution from the drift region is found to be 0.127 volts.

Based upon the analysis for the power MOSFET structure:

$$V_{JFET} = J_C.R_{JFET,SP} = \frac{J_C\rho_{JFET}\left(x_{JP}+W_0\right)W_{CELL}}{\left(W_G - 2x_{JP} - 2W_0\right)} \qquad \textbf{[9.24e]}$$

where x_{JP} is the junction depth of the deep P^+ region. The voltage drop across the accumulation layer in the IGBT structure can also be derived based upon the analysis for the power MOSFET structure (see Eq. [6.66]):

$$V_{ACC} = J_C.R_{A,SP} = \frac{J_C K_A\left(W_G - 2x_{JP}\right)W_{CELL}}{4\mu_{pA}C_{OX}\left(V_G - V_{TH}\right)} \qquad \textbf{[9.24f]}$$

The accumulation layer coefficient (K_A) for the IGBT structure can be assumed to have the same value (0.6) as for power MOSFET structures. The voltage drop across the channel of the MOSFET portion can also be obtained by using the analysis for the power MOSFET structure (see Eq. [6.63]:

$$V_{CH} = J_C.R_{CH,SP} = \frac{J_C L_{CH} W_{CELL}}{2\mu_{pi}C_{OX}\left(V_G - V_{TH}\right)} \qquad \textbf{[9.24g]}$$

Using the parameters for this structure, the JFET, accumulation, and channel contributions are found to be 1.01, 0.088, and 0.176 volts, respectively. The total voltage drop associated with the MOSFET portion is 1.27 volts.

The total on-state voltage drop for the symmetric IGBT structure is then found to be 2.07 volts. This value is only a factor of 1.59-times larger than that for the n-channel symmetric IGBT structure in Problem 9.10. This difference is smaller than a factor of about 3-times between n and p-channel power MOSFET structures.

Problem 9.25:

Determine the latch-up current density at 300 ^{o}K for the planar-gate symmetric n-channel IGBT structure using the following assumptions: (a) common-base current gain of 0.4; (b) average P-base doping concentration of 5 x 10^{16} cm^{-3}; (c) P-base junction depth of 3 microns; (d) N^{+} emitter junction depth of 1 micron; (e) cell width of 26 microns (pitch of 13 microns); (f) polysilicon window of 10 microns; (g) N^{+} emitter ion-implant mask of 4 microns. Assume that the P^{+} region is not included.

Solution:

The latch-up current density for the planar-gate symmetric n-channel IGBT structure without a P^{+} region is given by:

$$J_{C,L}\left(NoP^{+}\right)=\frac{V_{bi}}{\alpha_{PNP,ON}\rho_{SP}L_{N+}p} \qquad \textbf{[9.25a]}$$

For the parameters given in this problem, the pinch sheet resistance for the P-base region is found to be 2150 ohms/sq. For a 26 micron cell (W_{CELL}) with a polysilicon window of 10 microns and a diffusion of the N^{+} emitter region up to a 4 micron wide window in the middle of the polysilicon window, the length of the N^{+} region (L_{N+}) including its lateral extensions is 5 microns. Using these values, the latch-up current density obtained by using the analytical model is 1430 A/cm^{2} for a built-in potential of 0.8 volts.

Problem 9.26:

Determine the improvement in the latch-up current density for the device in Problem 9.25 obtained by the addition of a deep P^+ region with an average doping concentration of 5 x 10^{18} cm^{-3} and junction depth of 5 microns. The deep P^+ region is ion-implanted through a photoresist window of 2 microns in the middle of the cell. Use an effective lateral junction depth of 4 microns for the P^+ region.

Solution:

The latch-up current density with the addition of the deep P^+ region is given by:

$$J_{C,L}\left(WithP^{+}\right)=\frac{V_{bi}}{\alpha_{PNP,ON}\left(\rho_{SP}L_{P}+\rho_{SP+}L_{P+}\right)W_{CELL}} \qquad \textbf{[9.26a]}$$

If the lateral extension of the P^+ region is assumed to be equal to its junction depth, the length $L_P = 0$ and length $L_{P+} = 5$ microns. The sheet resistance ρ_{SP+} for the deep P^+ region for the values given in this problem is 50 ohms/square. Using these parameters, the latch-up current density is found to increase to 62,000 A/cm^2.

In practice, the doping concentration of the P^+ region reduces away from the diffusion window resulting in an increase in the sheet resistance. In this case, it is appropriate to use an effective lateral junction depth of 4 microns for the P^+ region leading to length $L_P = 1$ and length $L_{P+} = 4$ microns. Using these parameters, the latch-up current density is found to increase to 6500 A/cm^2.

Problem 9.27:

The gate oxide thickness for the planar-gate symmetric n-channel IGBT structure in Problem 9.25 is reduced from 500 to 250 angstroms while maintaining the same threshold voltage. What is the improvement in the latch-up current density?

Solution:

The threshold voltage can be computed by using:

$$V_{TH} = \frac{t_{OX}}{\varepsilon_{OX}} \sqrt{4\varepsilon_S kTN_A \ln\left(\frac{N_A}{n_i}\right)} \qquad \textbf{[9.27a]}$$

Based upon this equation, the average doping concentration in the P-base region can be increased by a factor of 4 times, from 5 x 10^{16} cm^{-3}; to 2 x 10^{17} cm^{-3}; by reducing the gate oxide thickness from 500 to 250 angstroms while maintaining the same threshold voltage. This leads to an increase in the latch-up current density to 3525 A/cm^2 after accounting for the change in the hole mobility with doping concentration.

Problem 9.28:

Compare the latch-up current densities for the planar-gate symmetric n-channel IGBT structure in Problem 9.26 if the cell topology is changed from the linear design to the square cell, circular cell and A-L-L cell designs. Use an effective lateral junction depth of 4 microns for the P^+ region.

Solution:

Square Cell Array:
The degradation of the latch-up current density with the square cell array in comparison with the linear cell in a linear array can be obtained by using:

$$\frac{J_{C,L}\left(SquareCell, SquareArray\right)}{J_{C,L}\left(LinearCell, LinearArray\right)} = f_{LP} f_A \qquad \textbf{[9.28a]}$$

In the above equation, the length factor (f_{LP}) obtained by using geometrical analysis is given by:

$$f_{LP} = \frac{L_{PE}}{L_{PC}} = \frac{\left(W_{POLY} - W_{P+}\right) - \left(x_{JP+} - x_{JN+}\right)}{\sqrt{2}\left(W_{POLY} - W_{P+}\right) - \left(x_{JP+} - x_{JN+}\right)} \qquad \textbf{[9.28b]}$$

The area factor (f_A) can be obtained by using:

$$f_A = \frac{\pi\left(x_{JP+} + x_{JN+}\right) W_{POLY}}{4W_G^2} \qquad \textbf{[9.28c]}$$

For the parameters in this problem, the length factor (f_{LP}) is found to be 0.376 and the area factor (f_A) is found to be 0.307. This degrades the latch-up current density to 750 A/cm^2, a factor of 8.66-times smaller than the linear cell topology.

Circular Cell Array:
The latch-up current density for the circular cell array is given by:

$$J_{C,L}\left(CC, CA\right) = \frac{2V_{bi}}{\alpha_{PNP,ON}\rho_{SP}W_{CELL}^2 \ln\left[\left(W_{POLY} + x_{JN+}\right)/\left(W_{P+} + x_{JP+}\right)\right]} \qquad \textbf{[9.28d]}$$

For the parameters in this problem, the latch-up current density is found to be 6040 A/cm^2. This is slightly less than that for the linear cell topology.

A-L-L Cell Array:
The latch-up current density for the A-L-L cell topology is given by:

$$J_{C,L}\left(ALL\right)=\frac{2V_{bi}}{\alpha_{PNP,ON}\rho_{SP}W_G^2\ln\left[\left(W_{P+}-x_{JP+}\right)/\left(W_{POLY}-x_{JN+}\right)\right]} \qquad \textbf{[9.28e]}$$

For the parameters in this problem, the latch-up current density is found to be 21,800 A/cm^2. This is much (3.4-times) larger than that for the linear cell topology.

Problem 9.29:

A trench-gate asymmetric n-channel IGBT structure is designed with the same parameters for the lightly-doped portion of the N-base region and the N-buffer layer as the device in Problem 9.4. Determine the on-state voltage drop at an on-state current density of 100 A/cm^2 for the device using the two-dimensional model. Use the following parameters: (a) D_a of 15 cm^2/s; (b) cell width of 4 microns; (c) channel length of 1.5 microns; (d) inversion mobility of 450 cm^2/V-s; (e) accumulation mobility of 1000 cm^2/V-s; (f) gate oxide thickness of 500 angstroms; (g) gate bias of 15 volts; (h) threshold voltage of 5 volts; (i) trench depth of 4 microns; (c) P-base junction depth of 2.5 microns; (d) N^+ emitter junction depth of 1 micron. Assume an effective doping concentration of 1 x 10^{19} cm^{-3} for the P^+ collector region with a diffusion length for electrons of 0.5 microns. Provide the values for the voltage drop across the P^+/N junction, the N-base region, the accumulation region, and the channel region.

Solution:

The voltage drops in the trench-gate asymmetric IGBT structure for the two dimensional model can be calculated by using the equations in section 9.12.3. The on-state voltage drop for the IGBT structure can be obtained by using:

$$V_{ON} = V_{P+N} + V_{NB} + V_{MOSFET} \qquad \textbf{[9.29a]}$$

where V_{P+N} is the voltage drop across the P^+ collector/N-base junction (J_1), V_{NB} is the voltage drop across the N-base region after accounting for conductivity modulation due to high-level injection conditions, and V_{MOSFET} is the voltage drop across the MOSFET portion.

The voltage drop across the P^+ collector/N-buffer layer junction (J_1) can be obtained from the increase in the minority carrier concentration at the junction boundary:

$$V_{P+N} = \frac{kT}{q}\ln\left(\frac{p(x_N)}{p_{0,NB}}\right) = \frac{kT}{q}\ln\left(\frac{p(x_N)N_{D,NB}}{n_i^2}\right) \qquad \textbf{[9.29b]}$$

where $p(x_N)$ is the injected hole concentration at the junction in the N-buffer layer (see Fig. 9.36) and $N_{D,NB}$ is the doping concentration in the N-buffer layer. The increase in the hole concentration at the junction [$p(x_N)$] is found to be 5.3 x 10^{16} cm^{-3}. The voltage drop across the P^+ collector/N-buffer layer junction (J_1) is found to be 0.961 volts.

The voltage drop across the N-base region can be obtained by adding the voltage drop associated with the first part of the above electric field expression is:

$$V_{NB1} = \frac{2L_a J_C \sinh\left(W_N / L_a\right)}{qp\left(W_{NB}+\right)\left(\mu_n + \mu_p\right)} \left\{ \tanh^{-1}\left[e^{-\left(W_{ON}/L_a\right)}\right] - \tanh^{-1}\left[e^{-\left(W_N/L_a\right)}\right] \right\} \quad \textbf{[9.29c]}$$

to the voltage drop associated with the second part of the above electric field expression is:

$$V_{NB2} = \frac{kT}{q}\left(\frac{\mu_n - \mu_p}{\mu_n + \mu_p}\right) \ln\left[\frac{\tanh\left(W_{ON}/L_a\right)\cosh\left(W_{ON}/L_a\right)}{\tanh\left(W_N/L_a\right)\cosh\left(W_N/L_a\right)}\right] \quad \textbf{[9.29d]}$$

Using the parameters for the asymmetric IGBT structure, the contribution from the drift region is found to be 0.146 volts.

Based upon the analysis for the trench-gate structure, the voltage drop across the accumulation layer in the IGBT structure is given by:

$$V_{ACC} = J_C . R_{A,SP} = \frac{J_C K_A \left[t_T - x_{JP} + \left(W_G/2\right)\right] W_{CELL}}{2\mu_{nA} C_{OX}\left(V_G - V_{TH}\right)} \quad \textbf{[9.29e]}$$

The voltage drop across the channel of the MOSFET portion is given by:

$$V_{CH} = J_C . R_{CH,SP} = \frac{J_C L_{CH} W_{CELL}}{2\mu_{ni} C_{OX}\left(V_G - V_{TH}\right)} \quad \textbf{[9.29f]}$$

Using the parameters for this structure, the accumulation and channel contributions are found to be 0.003 and 0.010 volts, respectively. The total voltage drop associated with the MOSFET portion is 0.013 volts.

The total on-state voltage drop for the asymmetric trench-gate IGBT structure is then found to be 0.961 volts.

Problem 9.30:

Calculate the latch-up current density at 300 ^{o}K for the trench-gate asymmetric n-channel IGBT structure defined in Problem 9.29 using the following assumptions: (a) common-base current gain of 0.4; (b) average P-base doping concentration of 5 x 10^{16} cm^{-3}; (c) P-base junction depth of 2.5 microns; (d) N^{+} emitter junction depth of 1 micron; (e) N^{+} emitter length of 1 micron.

Solution:

The latch-up current density for the planar-gate symmetric n-channel IGBT structure without a P^{+} region is given by:

$$J_{C,L}\left(Trench-Gate\right)=\frac{2V_{bi}}{\alpha_{PNP,ON}\rho_{SP}L_{N+}W_{CELL}} \qquad \textbf{[9.30a]}$$

For the parameters given in this problem, the pinch sheet resistance for the P-base region is found to be 2150 ohms/sq. For a 4 micron cell (W_{CELL}) and a length of the N^{+} region (L_{N+}) of 1 micron, the latch-up current density obtained by using the analytical model is 46,500 A/cm^{2} for a built-in potential of 0.8 volts.

Chapter 10
Synopsis

Problem 10.1:

Name the four basic components of power loss in transistors and rectifiers used in PWM motor control circuits.

Solution:

The four basic components of power loss in transistors and rectifiers used in PWM motor control circuits are on-state, off-state, turn-on, and turn-off losses.

Problem 10.2:

Consider motor control performed from a 20 volt DC-bus. What is the best technology for the transistor and rectifier to minimize power losses?

Solution:

In the case of a low DC-bus voltage, the best transistor technology is the silicon power MOSFET structure and the best rectifier technology is the Schottky rectifier.

Problem 10.3:

Calculate the power loss occurring at a PWM operating frequency of 10 kHz for the technology choice in Problem 10.2 if the motor current is 10 amperes. Use the on-state voltage drop and switching times provided in Fig. 10.3 and 10.4 for the analysis.

Solution:

Using the power loss equations given in Chapter 10 with the parameters for the silicon power MOSFET and Schottky rectifier in Fig. 10.3 and Fig. 10.4, the power losses are found to be:

(a) Silicon power MOSFET on-state loss = 0.25 W;
(b) Silicon power MOSFET turn-on loss = 0.02 W;
(c) Silicon power MOSFET turn-off loss = 0.02 W;
(d) Silicon power MOSFET total loss = 0.29 W;
(e) Silicon Schottky Rectifier on-state loss = 2.5 W;
(f) Silicon Schottky Rectifier turn-on loss = 0 W;
(g) Silicon Schottky Rectifier turn-off loss = 0 W;
(h) Silicon Schottky Rectifier total loss = 2.5 W;
(i) Total Power loss = 2.79 W.

Problem 10.4:

Consider motor control performed from a 400 volt DC-bus. What is the best silicon technology for the transistor and rectifier to minimize power losses?

Solution:

In the case of a medium DC-bus voltage, the best transistor technology is the silicon IGBT structure and the best rectifier technology is the P-i-N rectifier.

Problem 10.5:

Calculate the power loss occurring at a PWM operating frequency of 10 kHz for the technology choice in Problem 10.4 if the motor current is 20 amperes. Use the on-state voltage drop and switching times provided in Fig. 10.9 and 10.10 for the analysis.

Solution:

Using the power loss equations given in Chapter 10 with the parameters for the silicon IGBT structure and P-i-N rectifier in Fig. 10.9 and Fig. 10.10, the power losses are found to be:

(a) Silicon IGBT on-state loss = 18 W;
(b) Silicon IGBT turn-on loss = 22 W;
(c) Silicon IGBT turn-off loss = 12 W;
(d) Silicon IGBT total loss = 52 W;
(e) Silicon P-i-N Rectifier on-state loss = 20 W;
(f) Silicon P-i-N Rectifier turn-on loss = 4 W;
(g) Silicon P-i-N Rectifier turn-off loss = 0 W;
(h) Silicon P-i-N Rectifier total loss = 24 W;
(i) Total Power loss = 76 W.

Problem 10.6:

Consider motor control performed from a 400 volt DC-bus. What is the best silicon carbide technology for the transistor and rectifier to minimize power losses?

Solution:

In the case of a medium DC-bus voltage, the best SiC transistor technology is the power MOSFET structure and the best rectifier technology is the Schottky rectifier.

Problem 10.7:

Calculate the power loss occurring at a PWM operating frequency of 10 kHz for the technology choice in Problem 10.6 if the motor current is 20 amperes. Use the on-state voltage drop and switching times provided in Fig. 10.9 and 10.10 for the analysis.

Solution:

Using the power loss equations given in Chapter 10 with the parameters for the silicon carbide power MOSFET and Schottky rectifier in Fig. 10.9 and Fig. 10.10, the power losses are found to be:

(a) Silicon Carbide power MOSFET on-state loss = 0.8 W;
(b) Silicon Carbide power MOSFET turn-on loss = 0.8 W;
(c) Silicon Carbide power MOSFET turn-off loss = 0.8 W;
(d) Silicon Carbide power MOSFET total loss = 2.4 W;
(e) Silicon Carbide Schottky Rectifier on-state loss = 10 W;
(f) Silicon Carbide Schottky Rectifier turn-on loss = 0 W;
(g) Silicon Carbide Schottky Rectifier turn-off loss = 0 W;
(h) Silicon Carbide Schottky Rectifier total loss = 10 W;
(i) Total Power loss = 12.4 W.

Problem 10.8:

Consider motor control performed from a 3000 volt DC-bus. What is the best silicon technology for the transistor and rectifier to minimize power losses?

Solution:

In the case of a high DC-bus voltage, the best transistor technology is the silicon IGBT structure and the best rectifier technology is the P-i-N rectifier.

Problem 10.9:

Calculate the power loss occurring at a PWM operating frequency of 3 kHz for the technology choice in Problem 10.8 if the motor current is 1000 amperes. Use the on-state voltage drop and switching times provided in Fig. 10.15 and 10.16 for the analysis.

Solution:

Using the power loss equations given in Chapter 10 with the parameters for the silicon IGBT structure and P-i-N rectifier in Fig. 10.15 and Fig. 10.16, the power losses are found to be:

(a) Silicon IGBT on-state loss = 1,500 W;
(b) Silicon IGBT turn-on loss = 31,500 W;
(c) Silicon IGBT turn-off loss = 13,500 W;
(d) Silicon IGBT total loss = 46,500 W;
(e) Silicon P-i-N Rectifier on-state loss = 1,250 W;
(f) Silicon P-i-N Rectifier turn-on loss = 9,000 W;
(g) Silicon P-i-N Rectifier turn-off loss = 0 W;
(h) Silicon P-i-N Rectifier total loss = 10,300 W;
(i) Total Power loss = 56,800 W.

Problem 10.10:

Consider motor control performed from a 3000 volt DC-bus. What is the best silicon carbide technology for the transistor and rectifier to minimize power losses?

Solution:

In the case of a high DC-bus voltage, the best SiC transistor technology is the power MOSFET structure and the best rectifier technology is the Schottky rectifier.

Problem 10.11:

Calculate the power loss occurring at a PWM operating frequency of 3 kHz for the technology choice in Problem 10.10 if the motor current is 1000 amperes. Use the on-state voltage drop and switching times provided in Fig. 10.15 and 10.16 for the analysis.

Solution:

Using the power loss equations given in Chapter 10 with the parameters for the silicon carbide power MOSFET and Schottky rectifier in Fig. 10.15 and Fig. 10.16, the power losses are found to be:

(a) Silicon Carbide power MOSFET on-state loss = 190 W;
(b) Silicon Carbide power MOSFET turn-on loss = 900 W;
(c) Silicon Carbide power MOSFET turn-off loss = 900 W;
(d) Silicon Carbide power MOSFET total loss = 1990 W;
(e) Silicon Carbide Schottky Rectifier on-state loss = 500 W;
(f) Silicon Carbide Schottky Rectifier turn-on loss = 0 W;
(g) Silicon Carbide Schottky Rectifier turn-off loss = 0 W;
(h) Silicon Carbide Schottky Rectifier total loss = 500 W;
(i) Total Power loss = 2,490 W.

Problem 10.12:

Based upon the power loss analyses done in the previous problems, estimate the DC-bus voltage above which silicon carbide technology will provide an improvement in efficiency for motor control applications.

Solution:

Based upon the power loss analyses done in the previous problems, silicon carbide unipolar devices will provide an improvement in efficiency for motor control applications when the DC-bus voltage exceeds 300 volts.

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