MIXED SIGNAL IC LAYOUT

NOVATEK

Layout Engineering Department

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MIXED SIGNAL IC LAYOUT

1. **Introduction**

2. **Device layout consideration**

3. **Floor plan layout guide**

4. **Conclusion**

1. Introduction

2. Device layout consideration

    A. Device type

        a. Trans

        b. Resister

        c. Capacitor

        d. BJT

        e. OP Amplifier

        f. SCF

        g. ADC/DAC

    B. Process variation

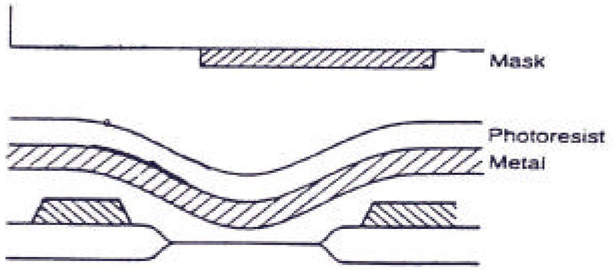


圖 (3)

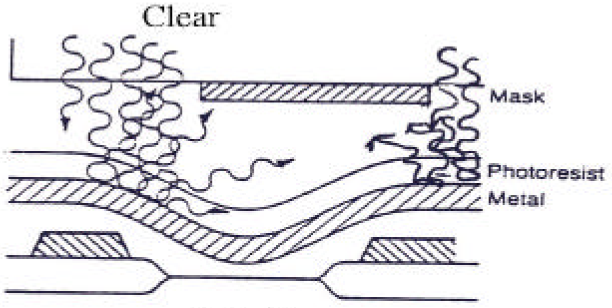


圖 (4)

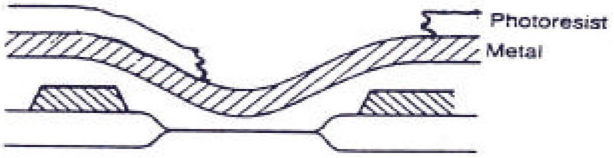


圖 (5)

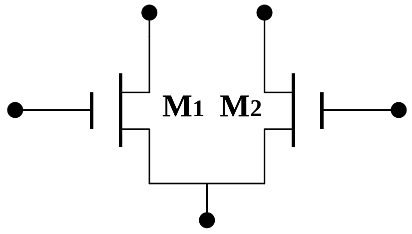
當紫外線穿過 Mask 照射至基底時，光的角度因為界質的變化 (Mask 為玻璃光罩光阻為透明物體) 及 基底凹凸不平，再加上 METAL 為金屬，其反光強度是最強等。以上種種因素，導致光折射 (如圖 4)，折射的光影響曝光時 MASK 的圖案 (如圖 5)。結果在曝光後靠近 CLEAR 的地方，因受折射的問題，其 Width、Length 皆受到影。所以同理可證其他 LAYER 亦會產生繞射的問題。

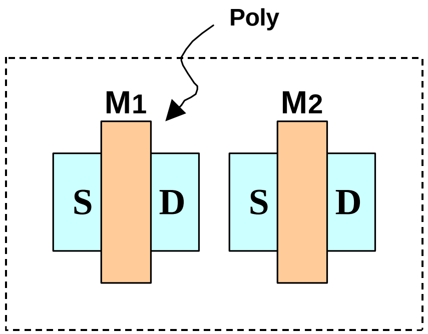
Mask 在曝光時，多多少少都會產生繞射的問題。尤其是在最外圍的 Polygon 因光折射的角度較大，所以容易改變 Width 和 Length。中間部份則因為每一個 Polygon寬度及間距都相同，所以繞射的結果都差不多。

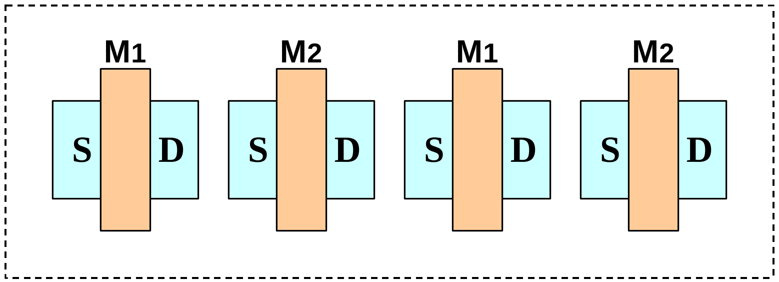
2. Device layout consideration

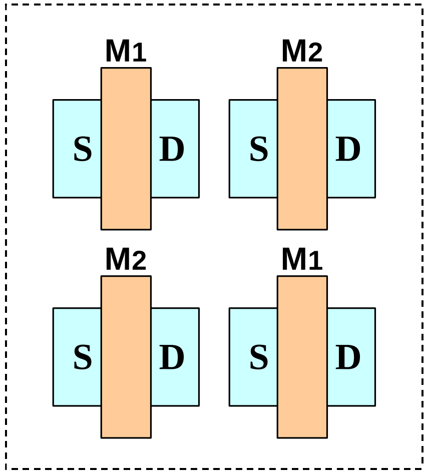
A. Device type

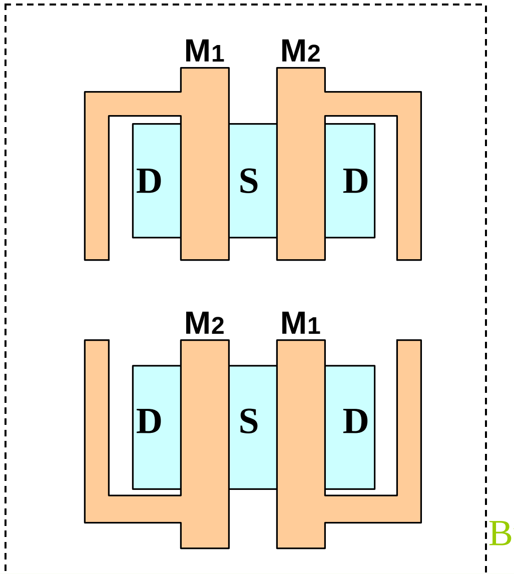
a. Trans.

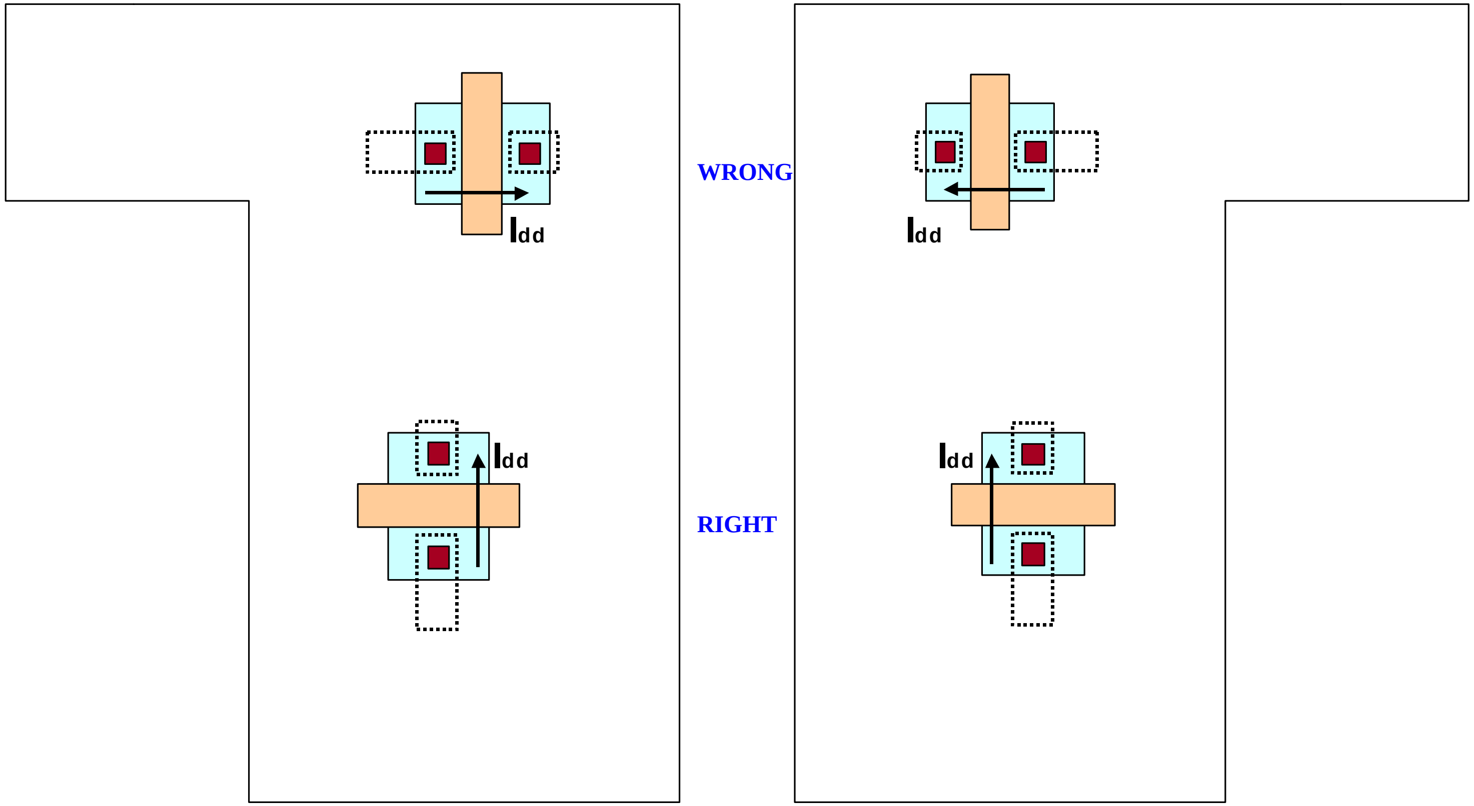











Idd
WRONG
Idd
Idd
RIGHT
Idd

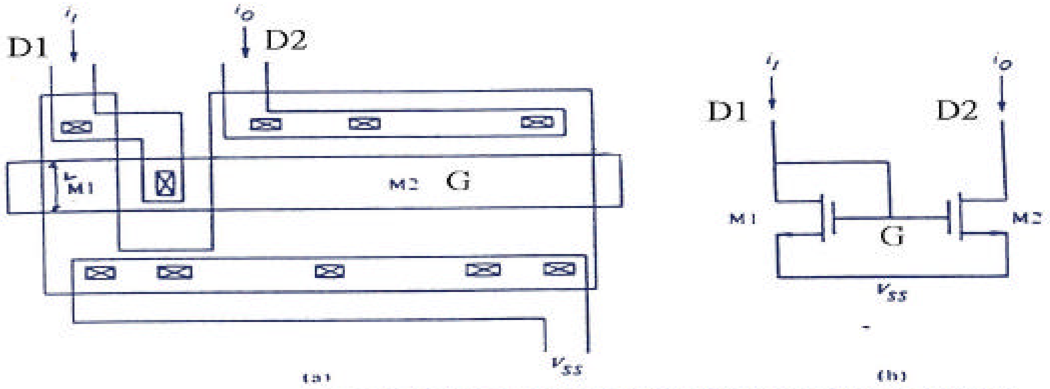
Weight current cell layout

$\frac{W - ? W}{L - ? L}$ $\frac{W - ? W}{L - ? L}$ $\frac{W - ? W}{L - ? L}$

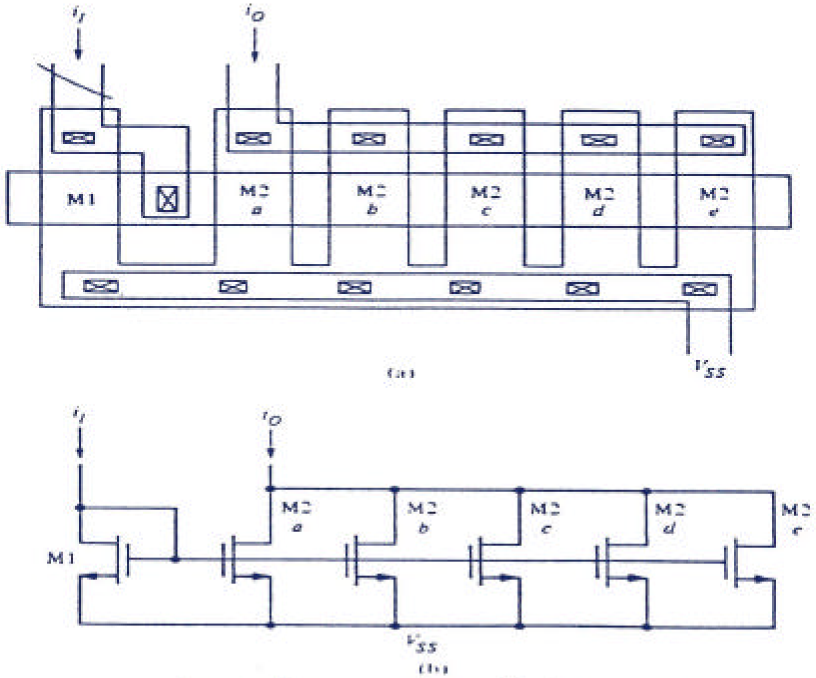
Wrong

$\left(\frac{W- ? W}{L- ? L}\right)$ $\left(\frac{W- ? W}{L- ? L}\right) \times 2$ $\left(\frac{W- ? W}{L- ? L}\right) \times 4$

Right

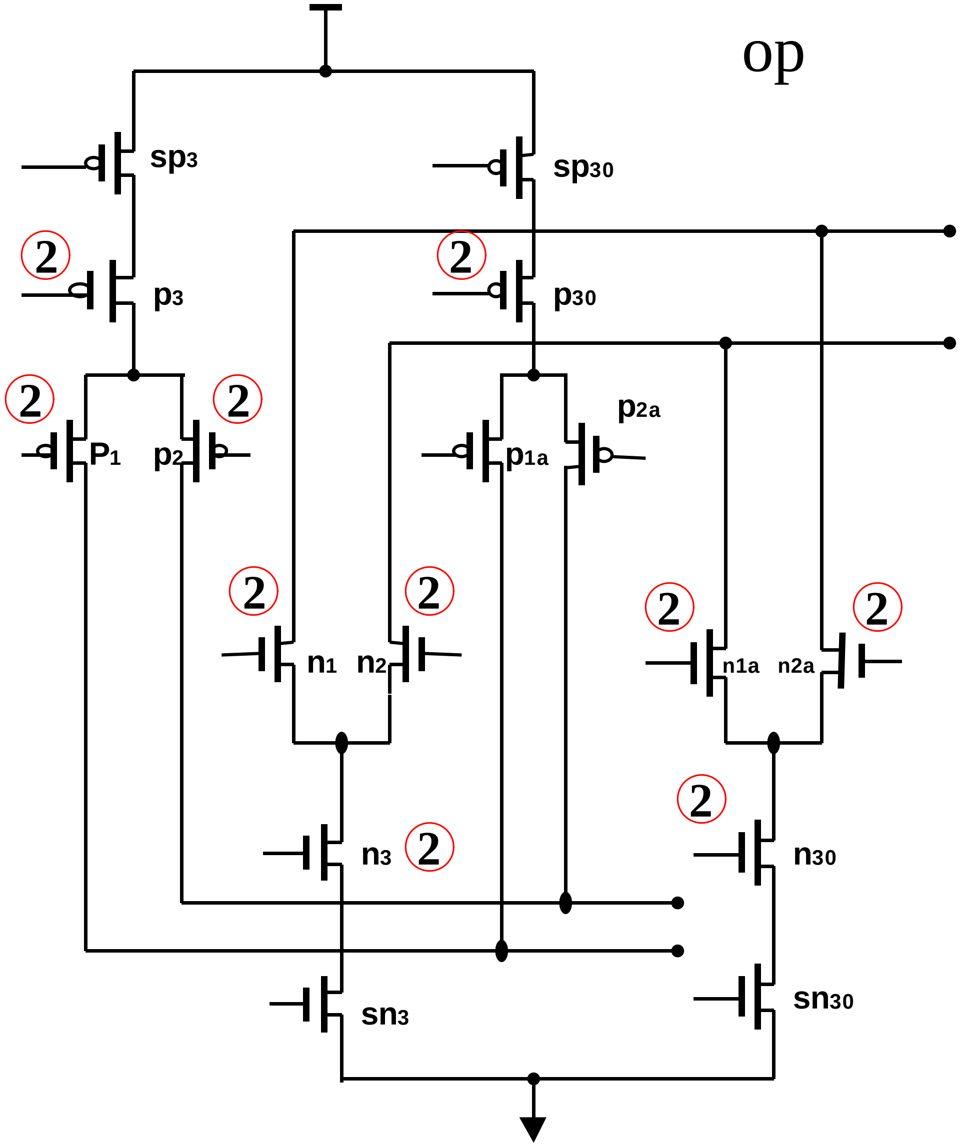


Layout of current mirror without ΔW correction techniques.

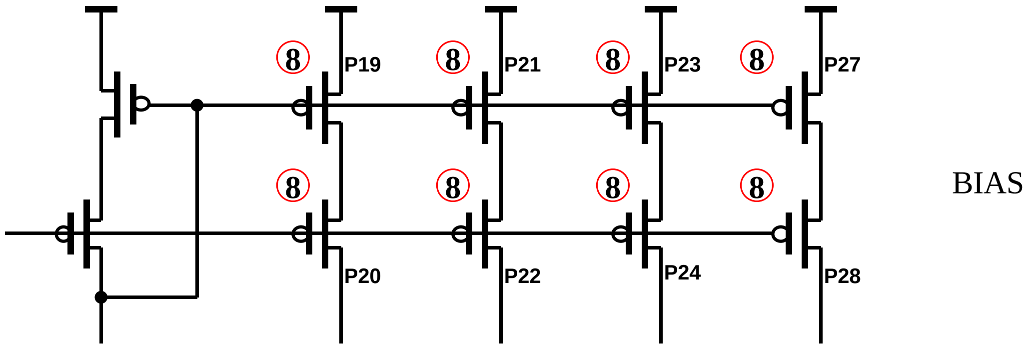


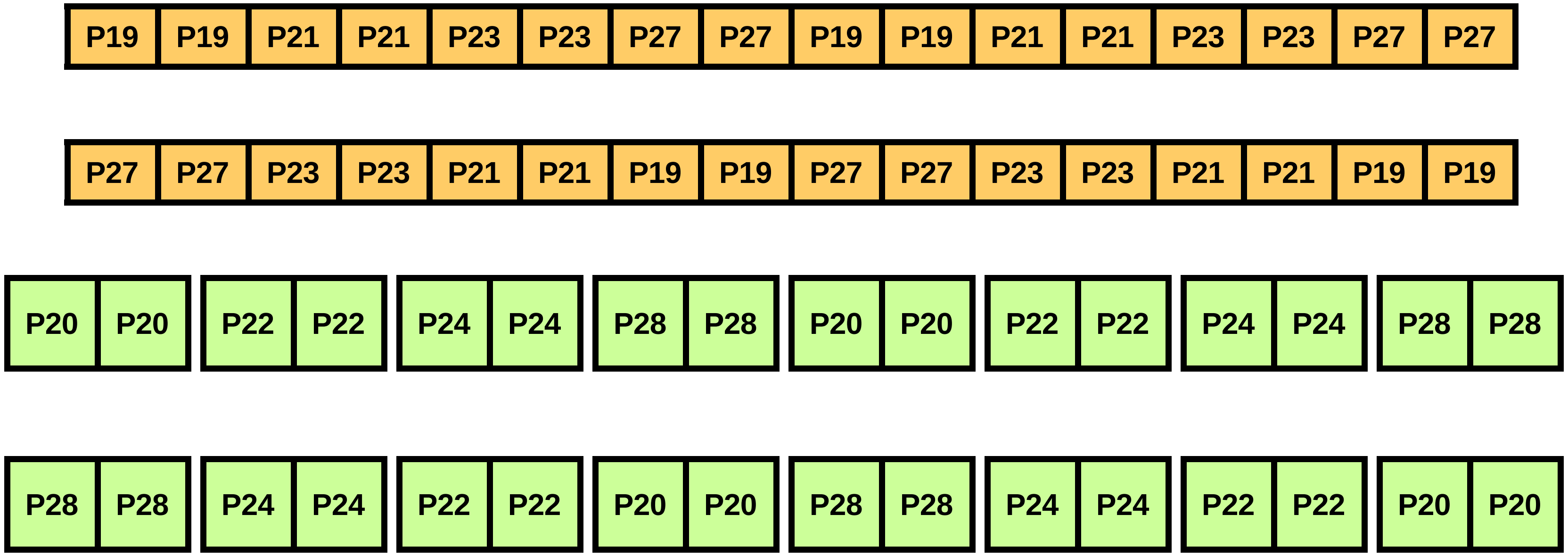
Layout of current mirror with ΔW correction techniques.

op

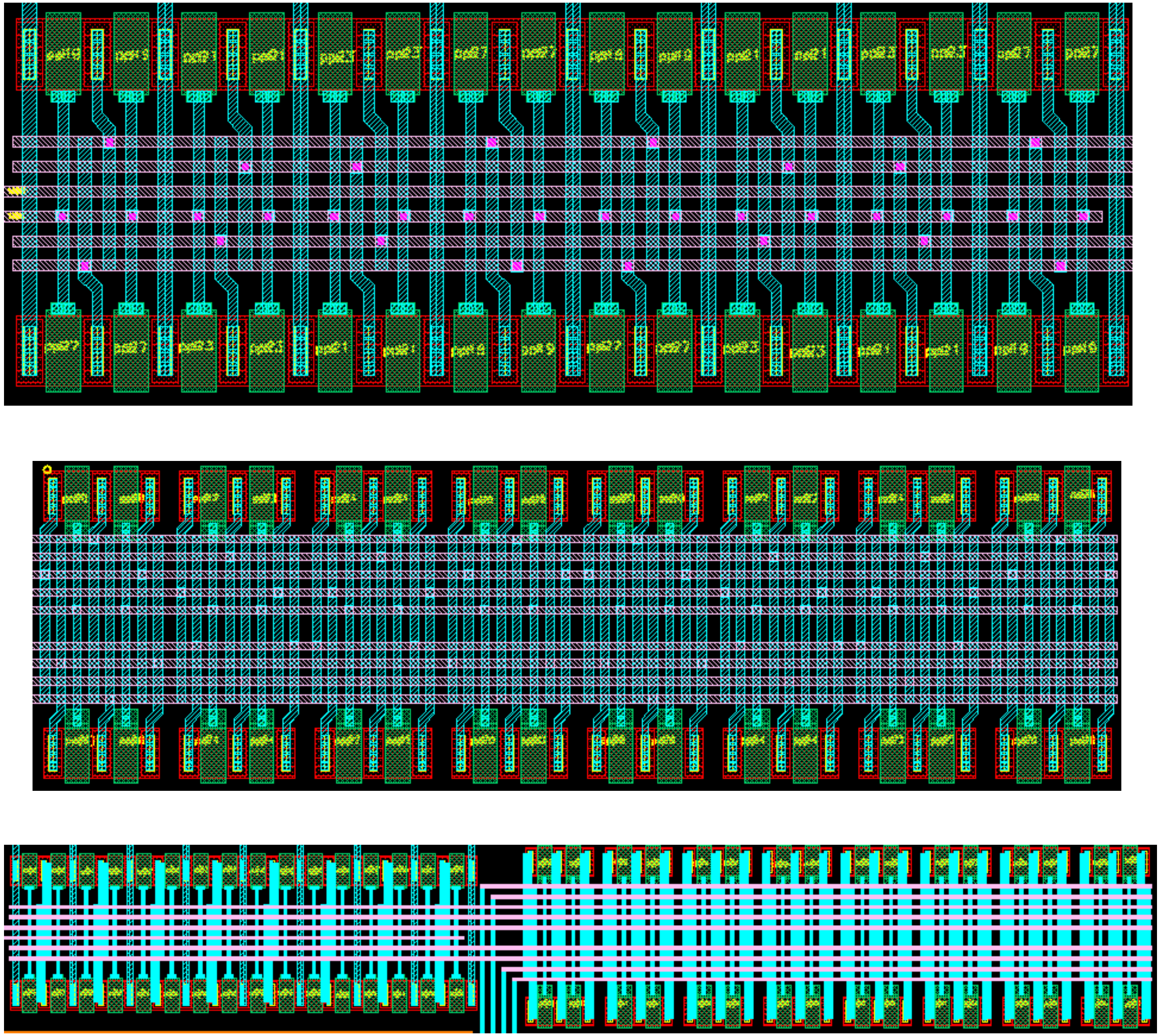


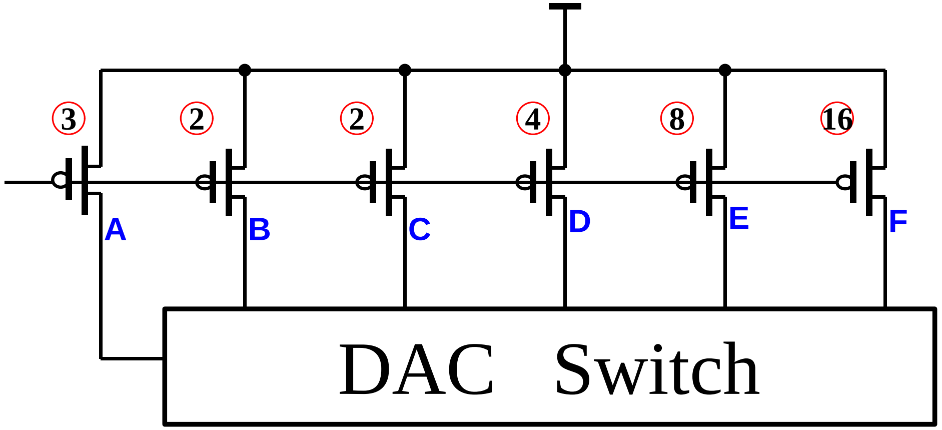
n1	n2	n1a	n2a
n2	n1	n2a	n1a
n3	n3	n30	n30
sn3		sn30	
sp3		sp30	
p3	p3	p30	p30
p2	p1	p2a	p1a
p1	p2	p1a	p2a





P19	P19	P21	P21	P23	P23	P27	P27	P19	P19	P21	P21	P23	P23	P27	P27
P27	P27	P23	P23	P21	P21	P19	P19	P27	P27	P23	P23	P21	P21	P19	P19
P20	P20	P22	P22	P24	P24	P28	P28	P20	P20	P22	P22	P24	P24	P28	P28
P28	P28	P24	P24	P22	P22	P20	P20	P28	P28	P24	P24	P22	P22	P20	P20





DAC

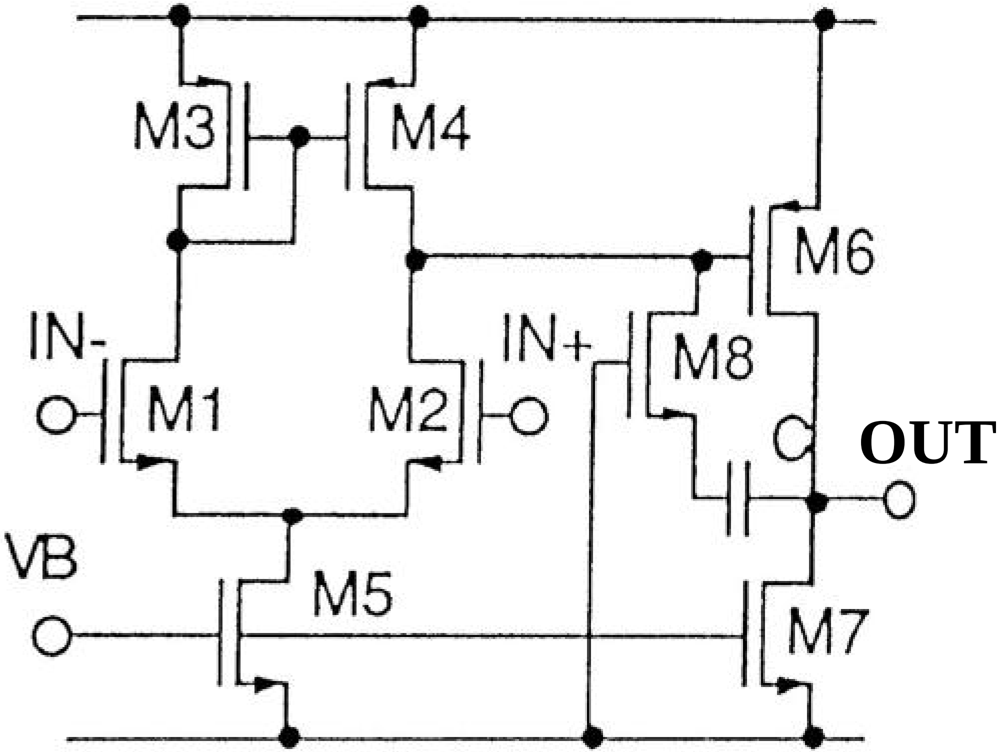
F*8	E*4	D*2	C	B	A	B	C	D*2	E*4	F*8

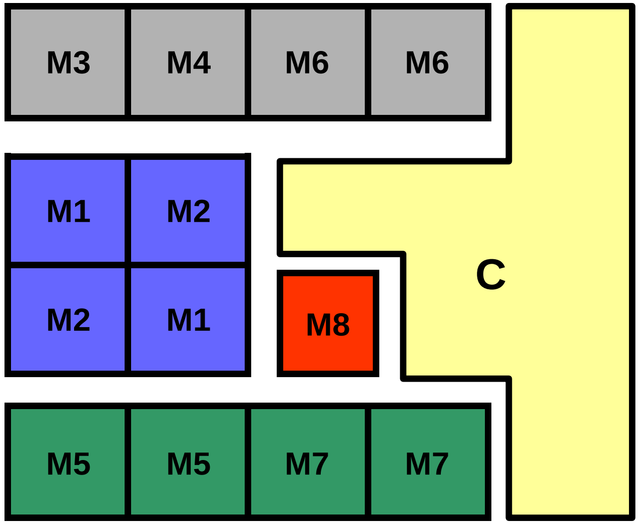
Worse

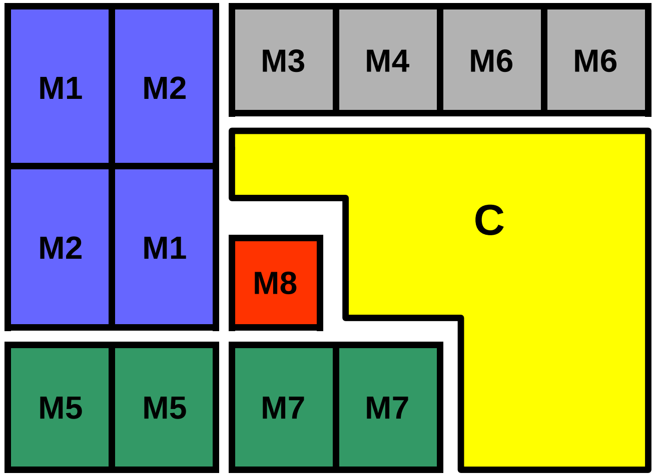
DUMMY	DUMMY	VCC	A	VCC	F	F	F	F	F	F	F	F	VCC	B	VCC	C	VCC	D	D	E	E	E	E	F	VCC	DUMMY	DUMMY
DUMMY	DUMMY	VCC	A	VCC	VCC	E	E	E	E	D	D	C	VCC	A	VCC	B	VCC	F	F	F	F	F	F	F	VCC	DUMMY	DUMMY

Better

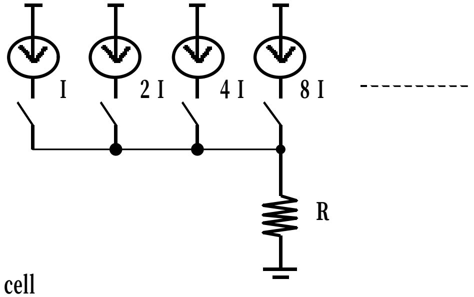
Practice



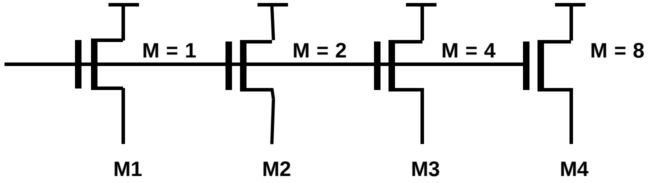

M3
M4
M6
M6
M1
M2
M2
M1
M8
C
M5
M5
M7
M7

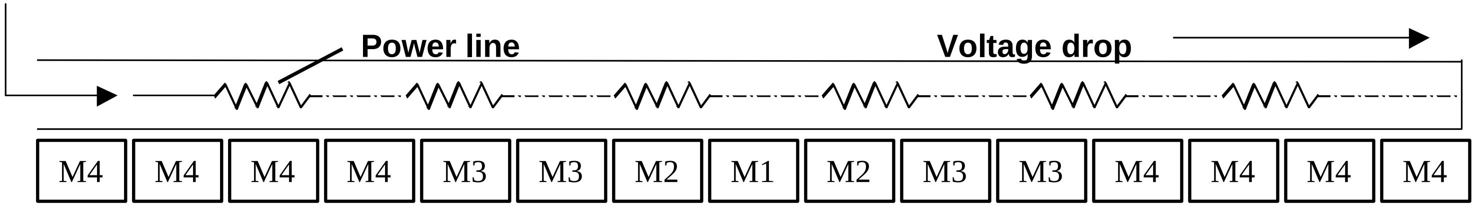

M1
M2
M2
M1
M3
M4
M6
M6
C
M8
M5
M5
M7
M7

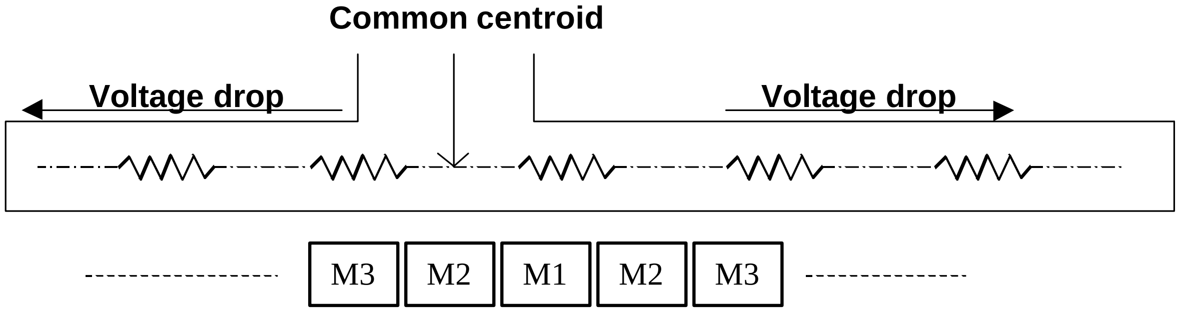
Current Switch DAC



→ current cell
→ transistor matching



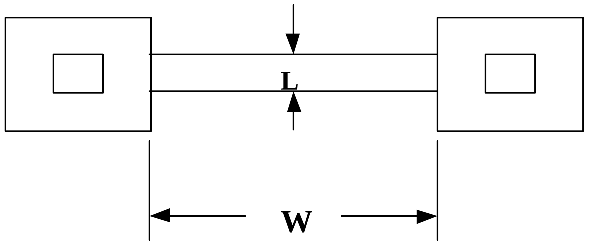




b. Resistor

Resistor type

- *** poly**
- *** well**
- *** diffusion (N+ , P+)**



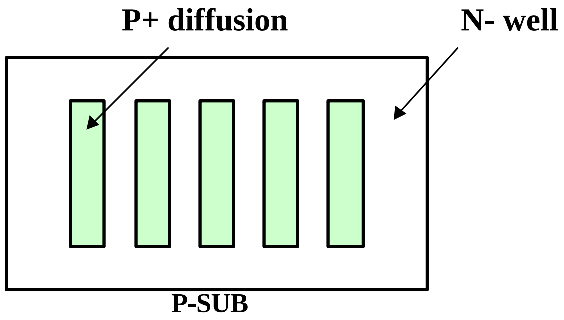
$$R=2R_{cont}+\left(\frac{W}{L}\right)R/\bullet$$

1. poly

Double poly {

- **poly gate**
- **poly resistor → sheet resistor 較大 , 特性較佳 (voltage cofe.)**

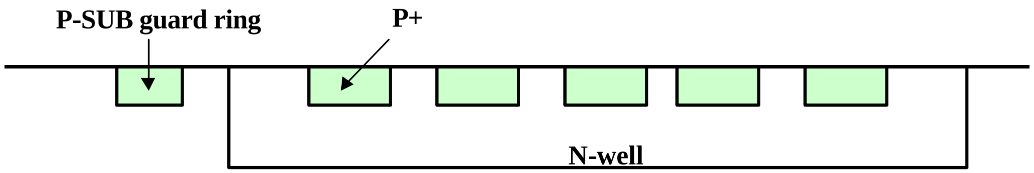
2. well



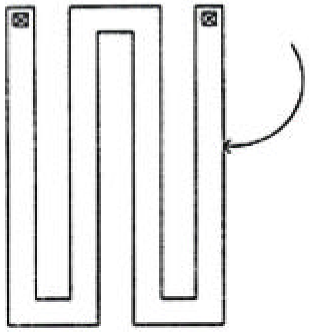
Sheet 最大
Spacing 大
→ 面積最小 ?

3. diffusion

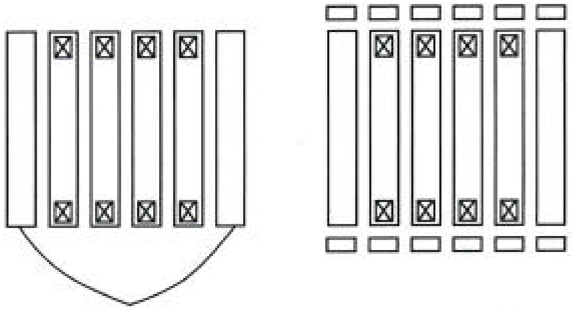
N+ , (if P-sub) → noisy
P+ , in N-well → better
if no double poly process
→ Diffusion is better



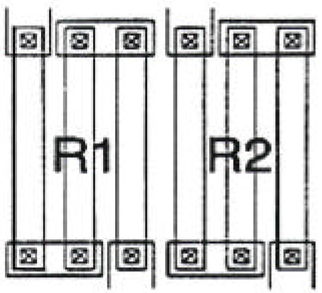
R-string=>resistor matching



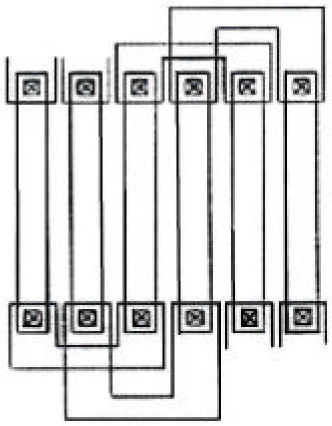
no matching issue
not care absolute value
small size



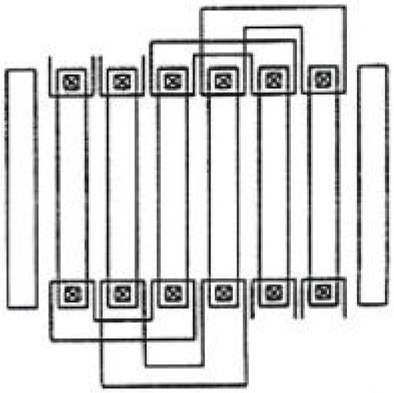
no matching issue
care absolute value



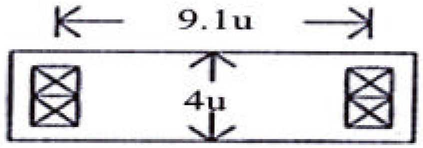
care matching
not care absolute value



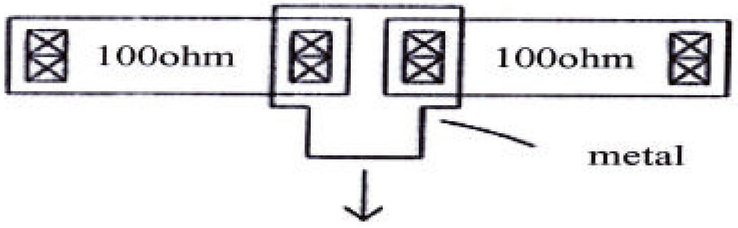
finger layout



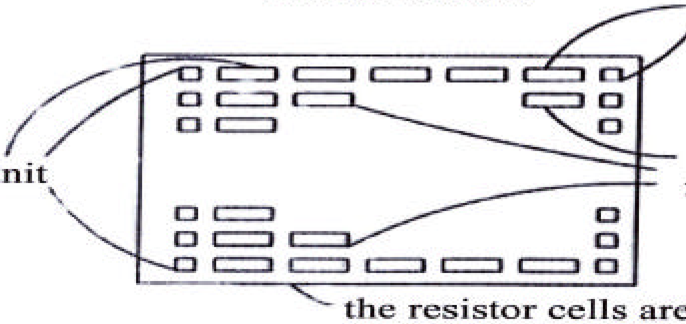
care matching and
absolute value



poly 44 ohm/square
100/44=2.272 square
length=2.272*4=9.1u

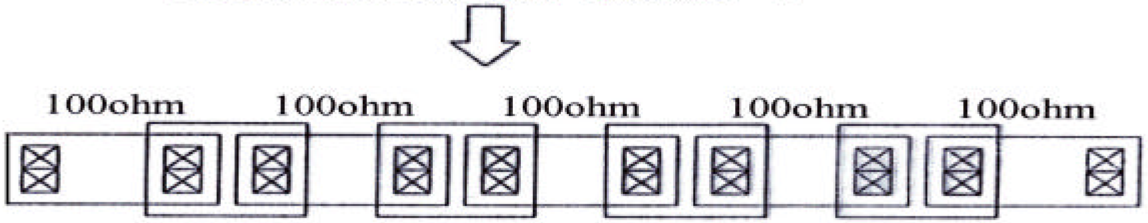


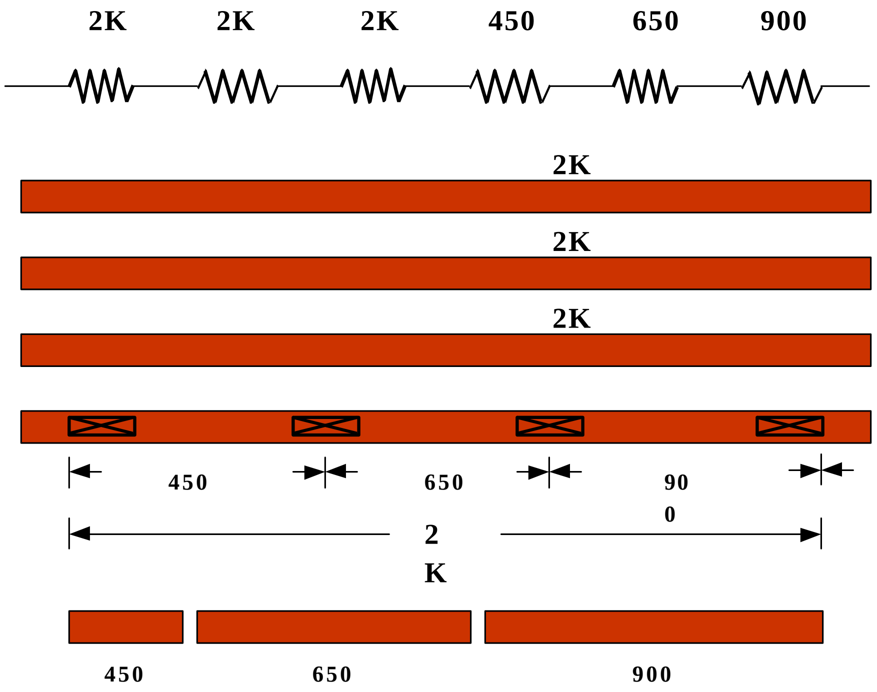
to other circuit



the resistor cells are layouted into square as
possible add the dummy cells at four sides

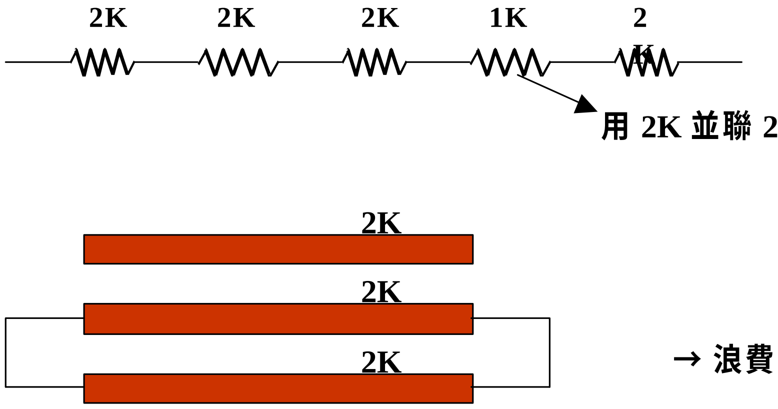
Unit cell layout
for example: 500 ohm=100 ohm *5





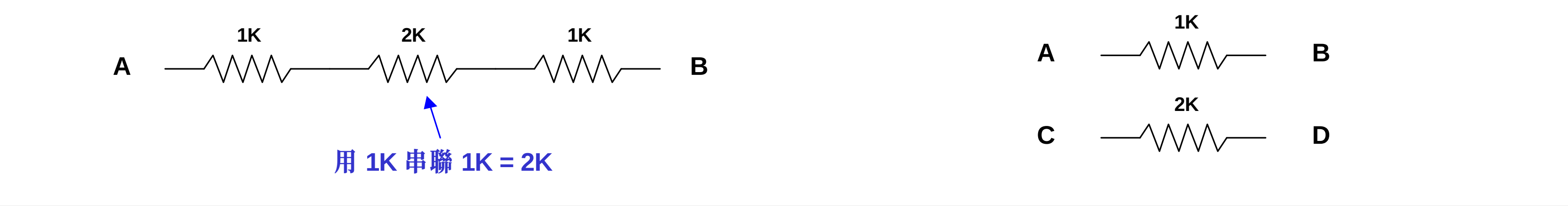
Better

Worse

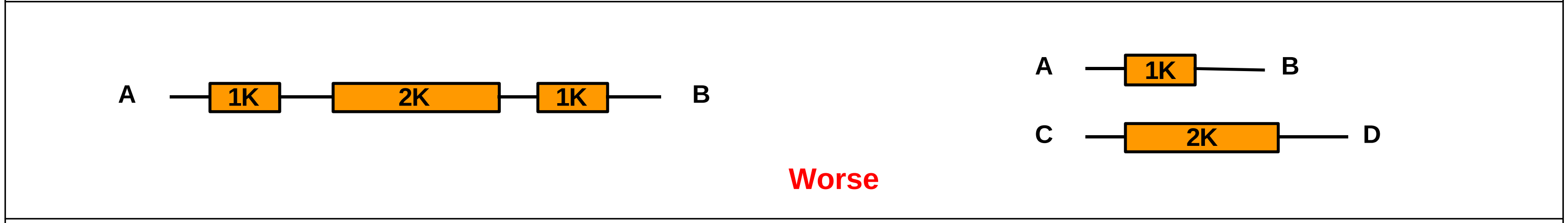


用 2K 並聯 2K → 1K

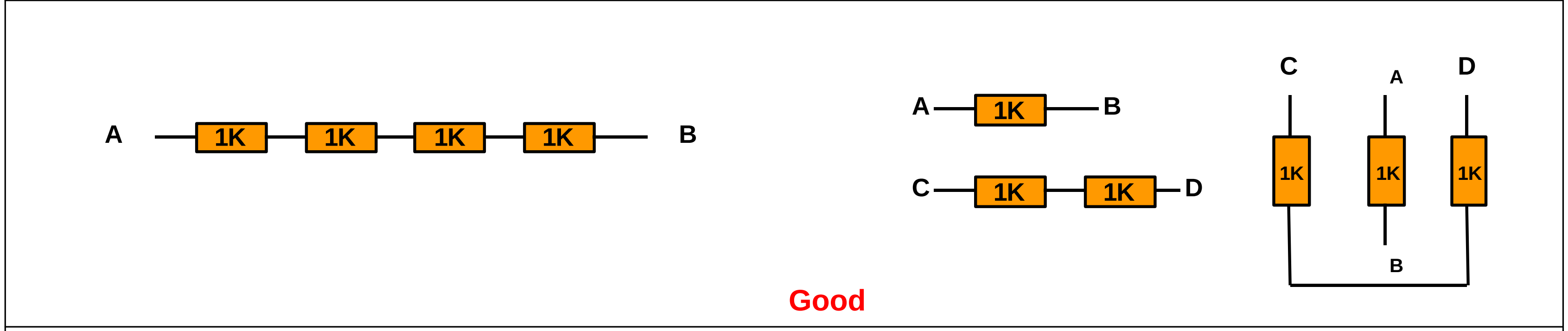
→ 浪費面積



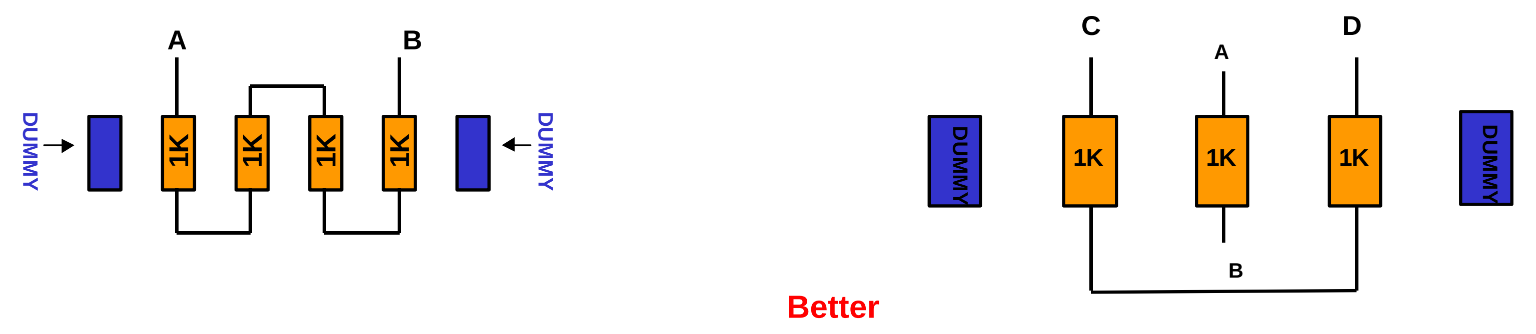
用 1K 串聯 1K = 2K



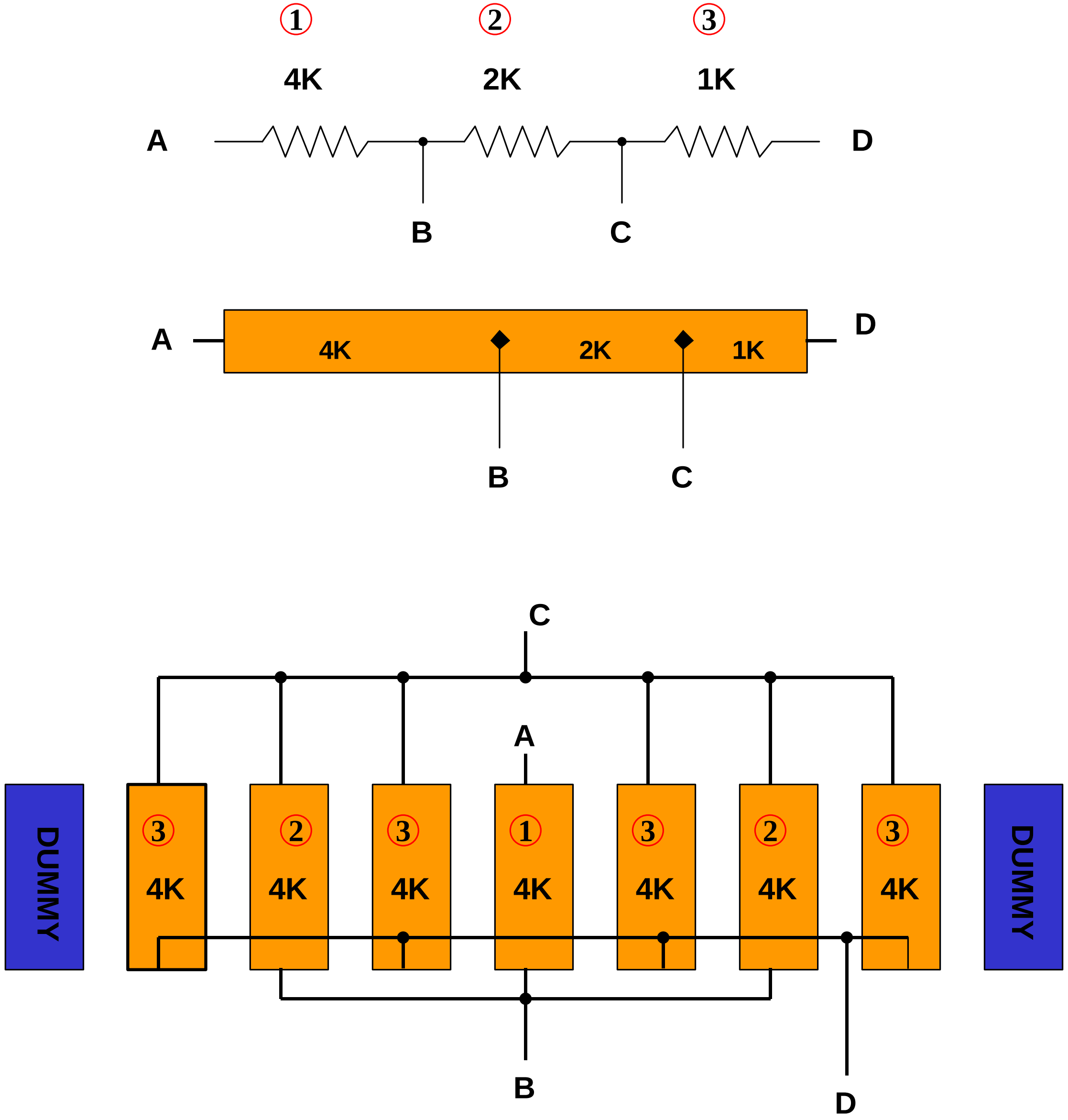
Worse



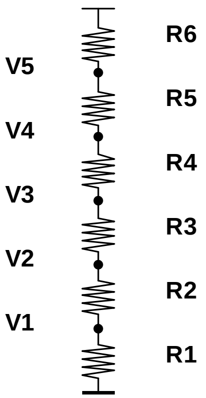
Good



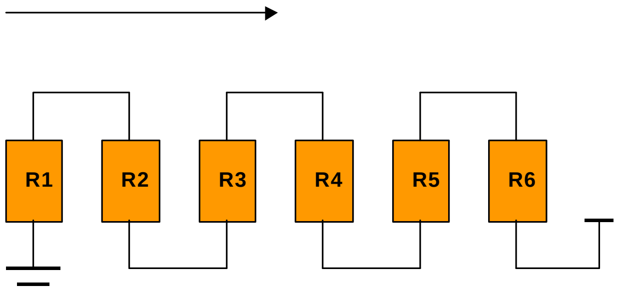
Better

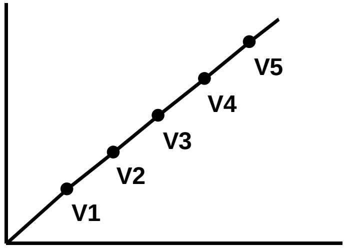

①
②
③
4K
2K
1K
A
D
B
C
A
4K
2K
1K
D
B
C
C
A
DUMMY
③ 4K
② 4K
③ 4K
① 4K
③ 4K
② 4K
③ 4K
DUMMY
B
D

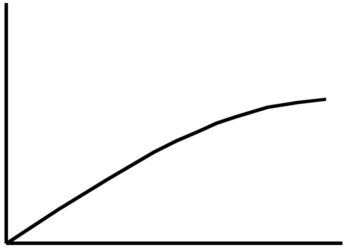
R-string layout



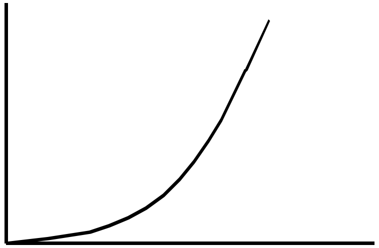
Resistor grading



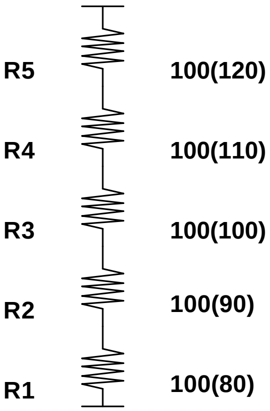


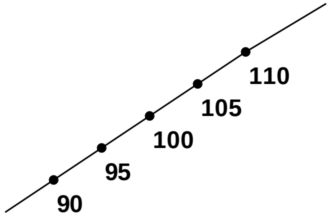


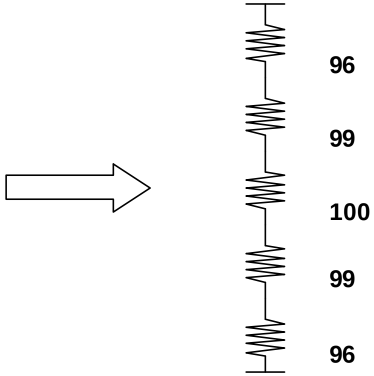
R1>R2>R3>R4>R5>R6

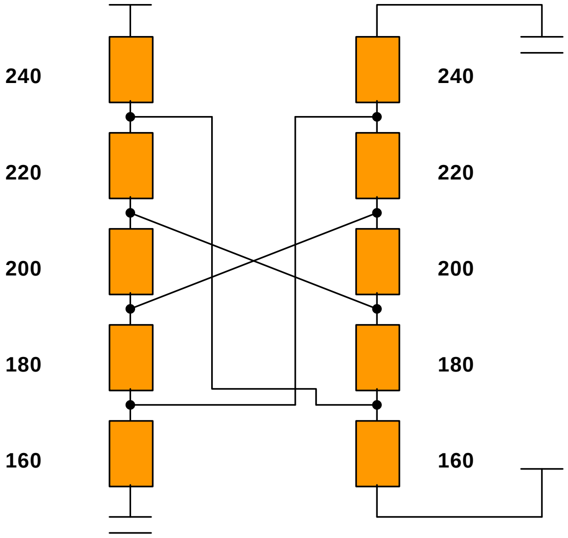


R6>R5>R4>R3>R2>R1



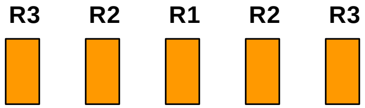


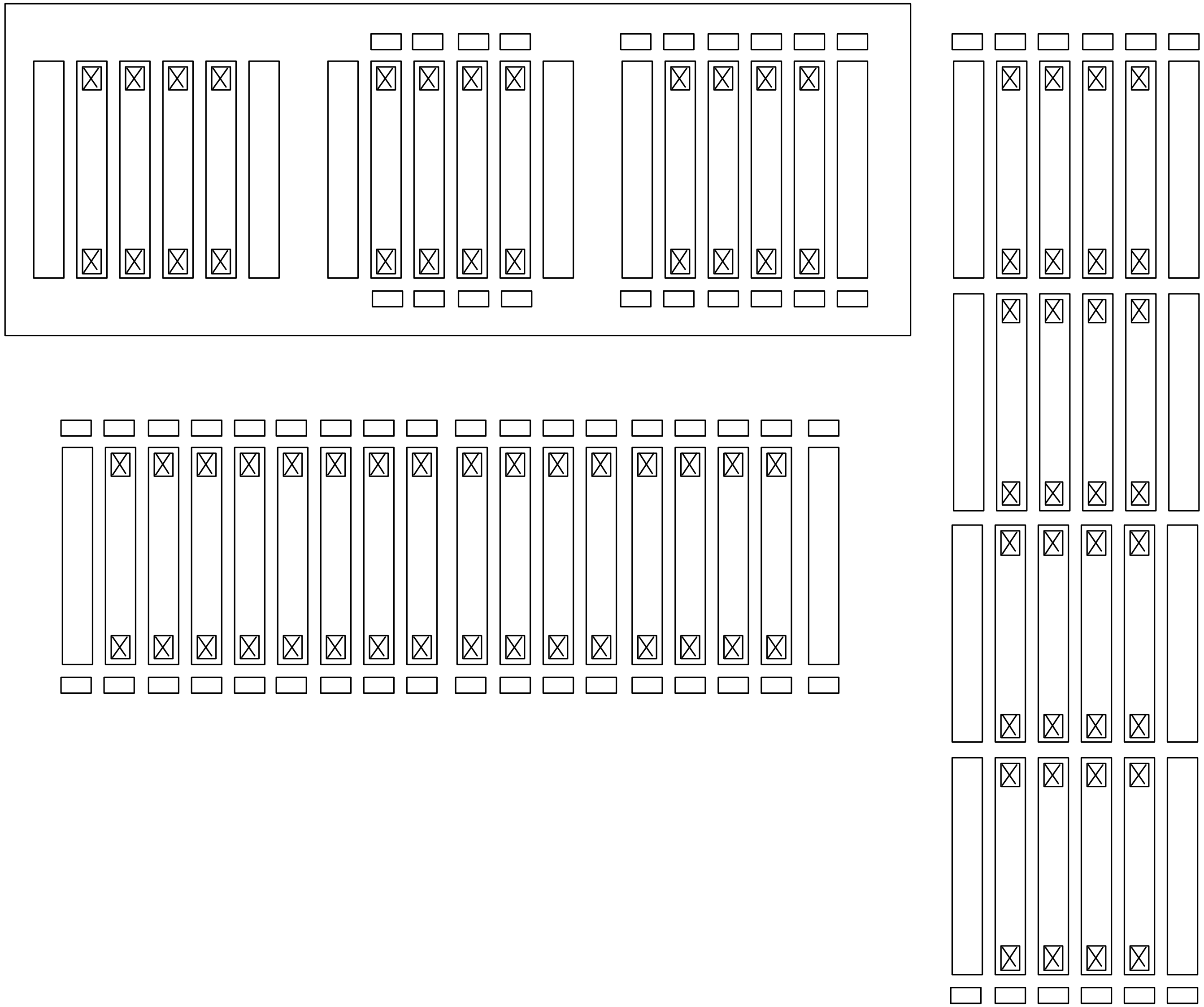




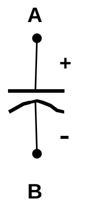
$$160 \,//\, 240 = \frac{160 \times 240}{160 + 240} = 96$$

$$180 \,//\, 220 = \frac{180 \times 220}{180 + 220} = 99$$





c. Capacitor

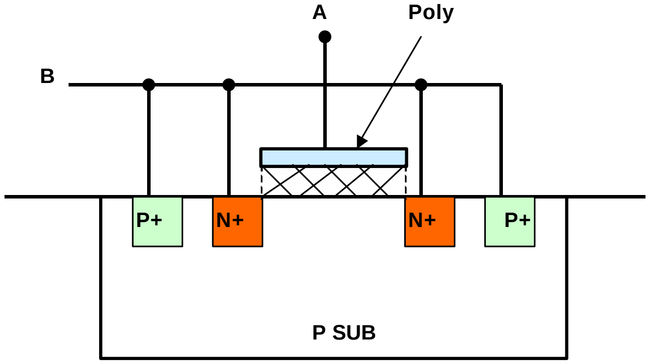


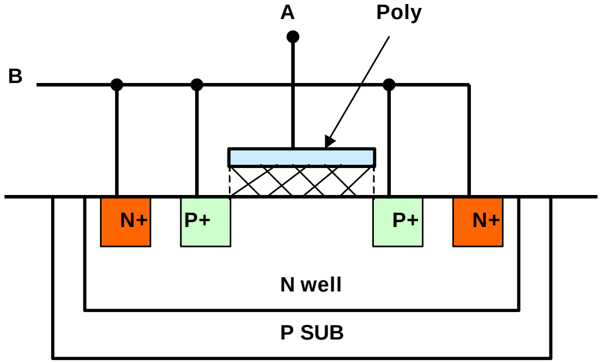
$C = \frac{A}{d}$, $A < 100 \times 100\ \mu^2$

C type

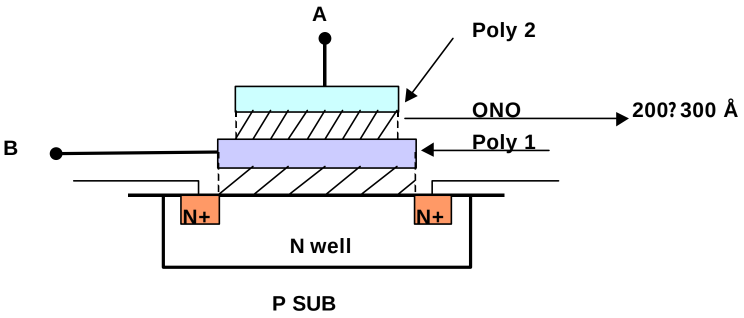
- * Mos
- * Double poly
- * Mmc
- * Sandwich

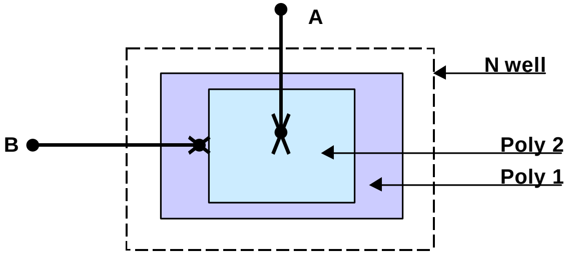
MOS

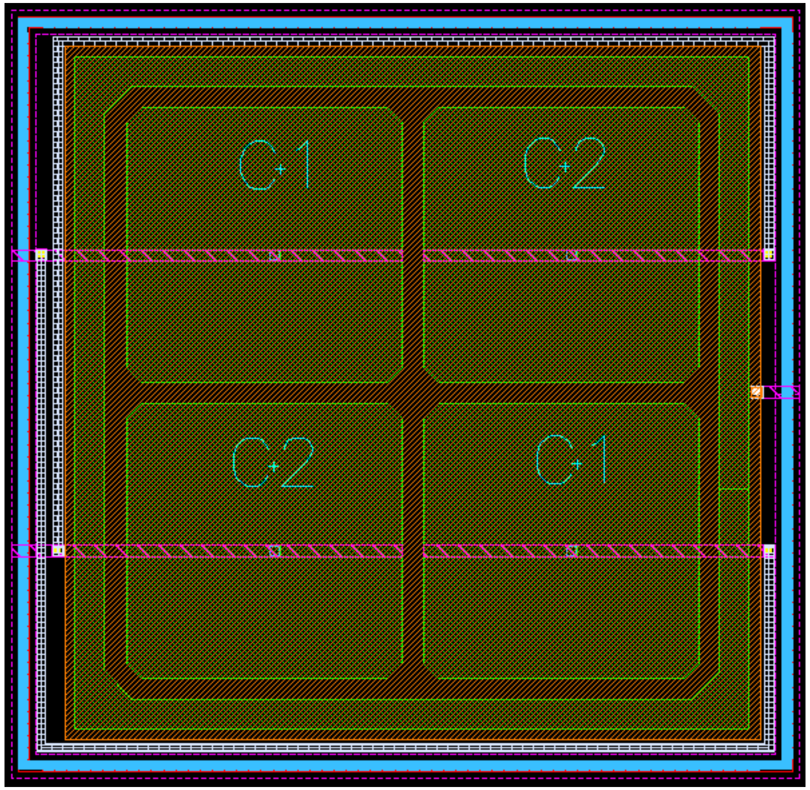




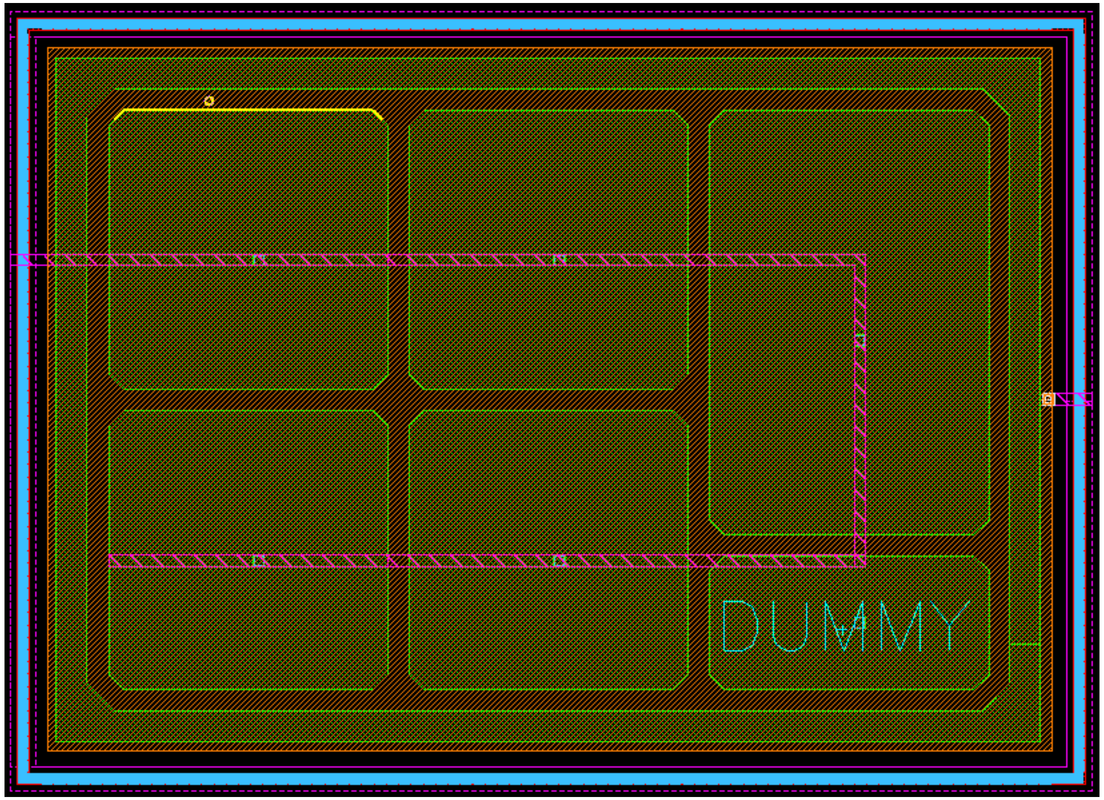
Double poly

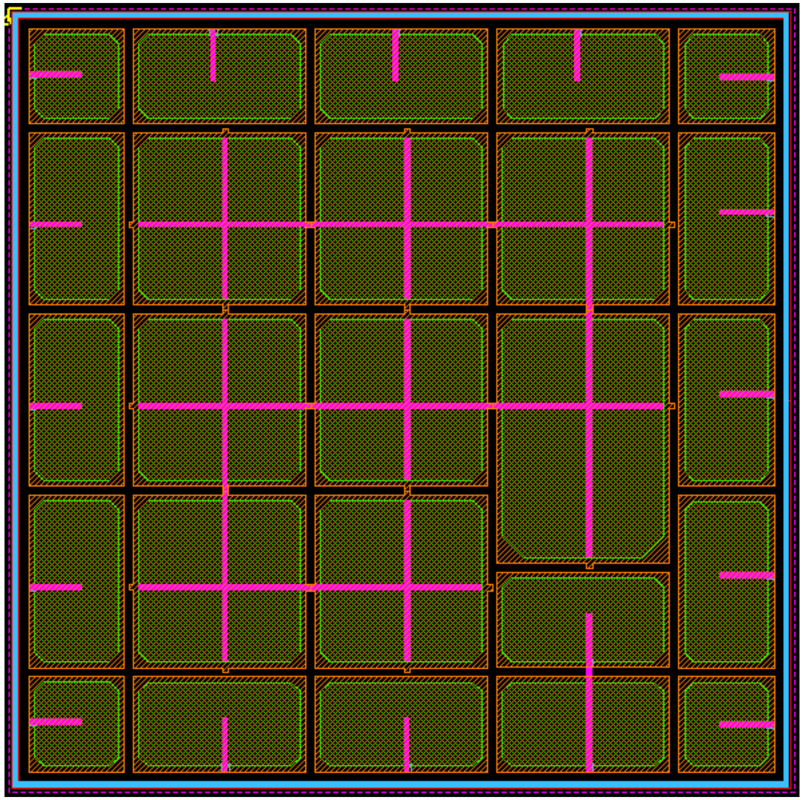




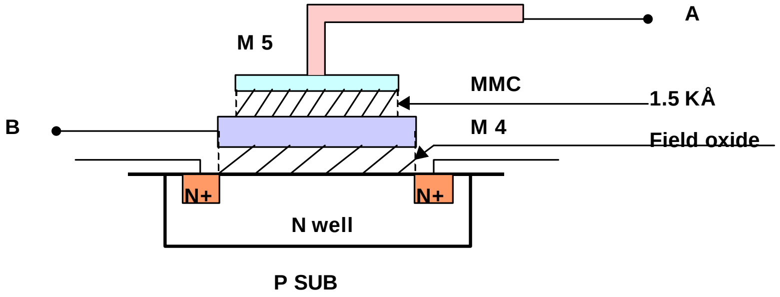


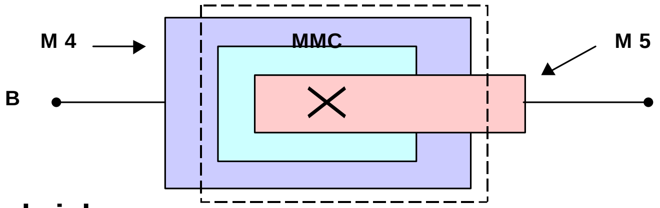
C1
C2
C2
C1


DUMMY

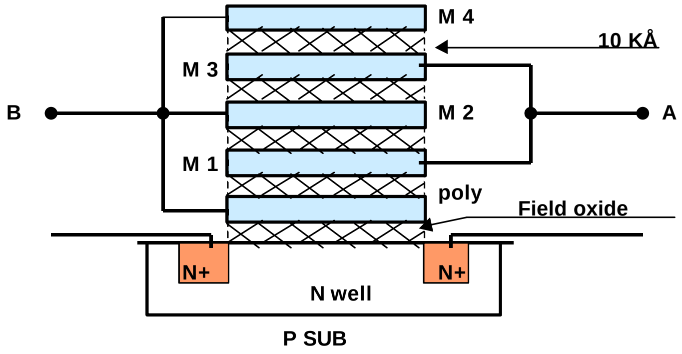


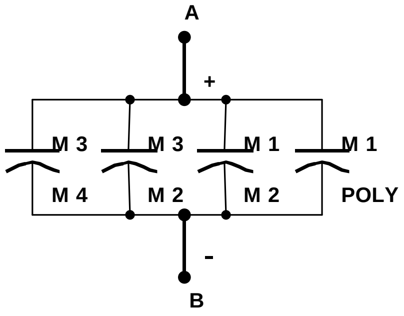
MMC

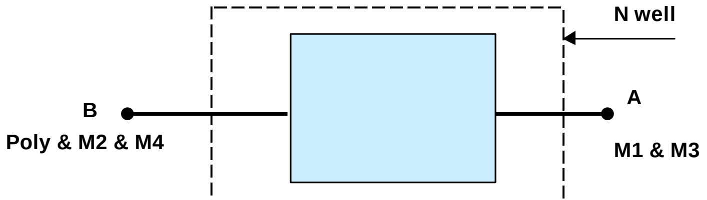


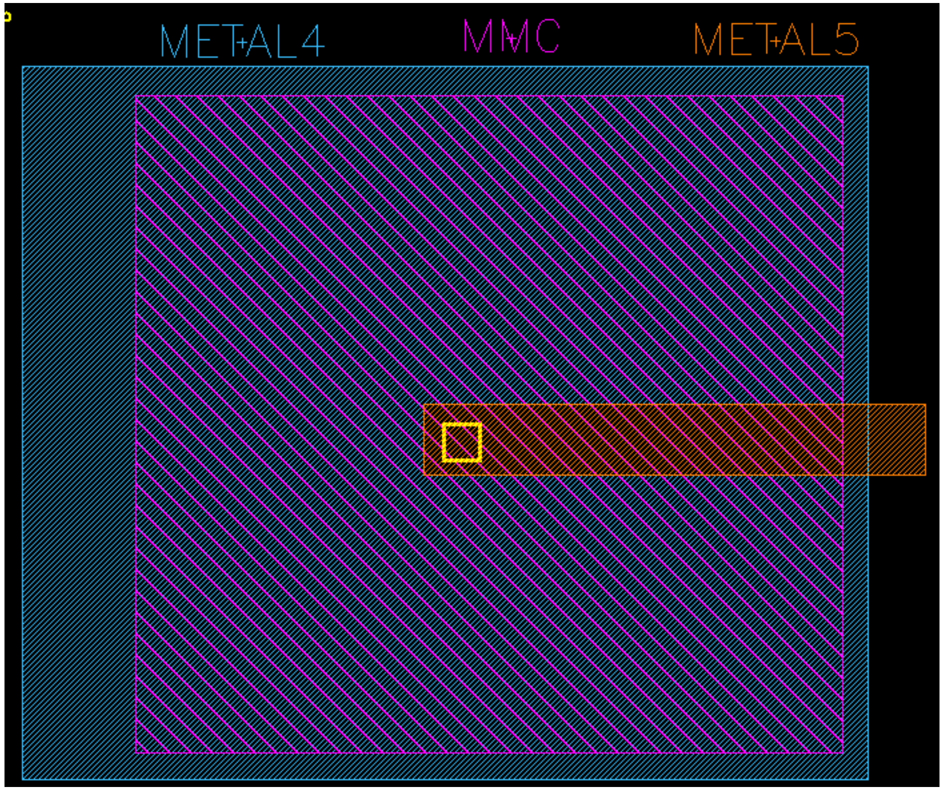


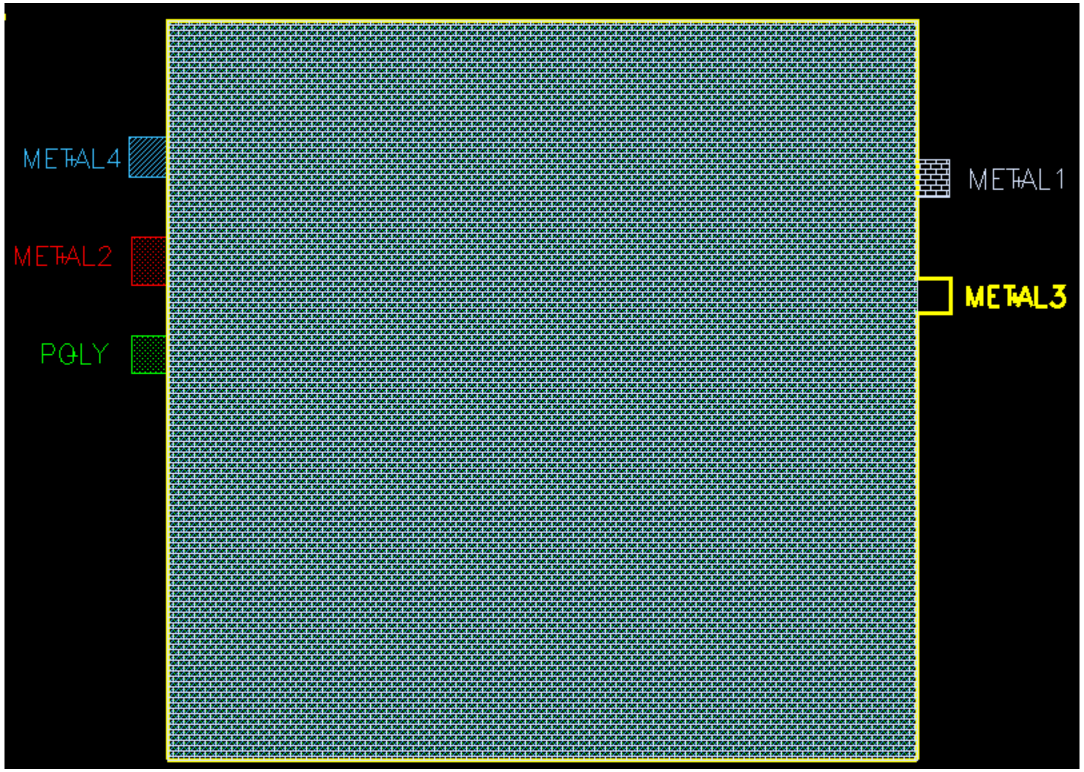
Sandwich





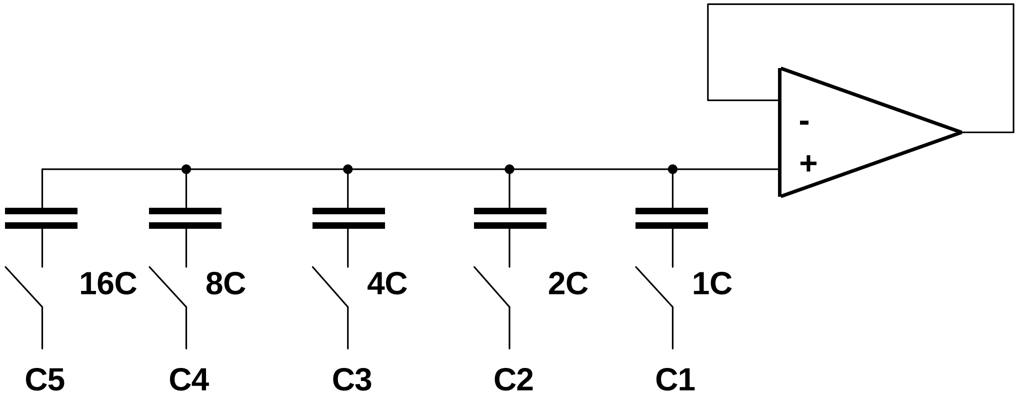



METAL4
MMC
METAL5

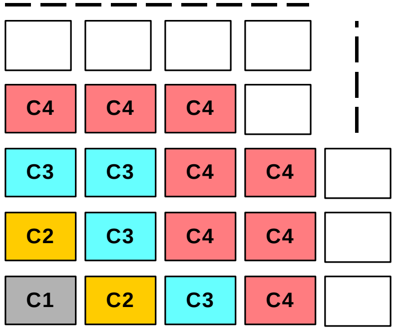

METAL4
METAL2
POLY
METAL1
METAL3

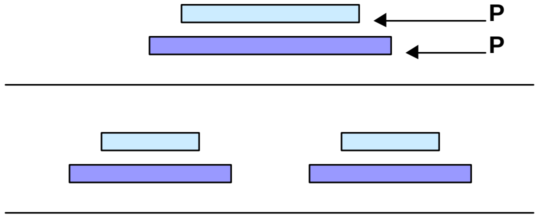
→ **Cap. array**

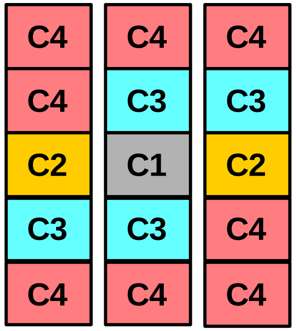
→ **dummy Cell. Cap. Tn well**



Double poly Cap.



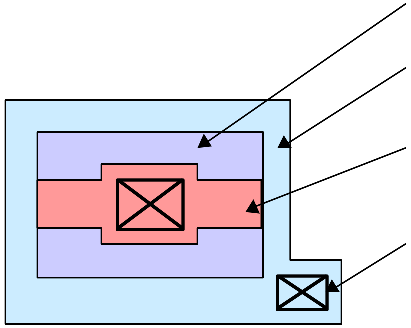


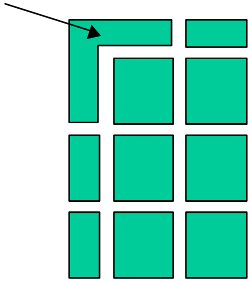


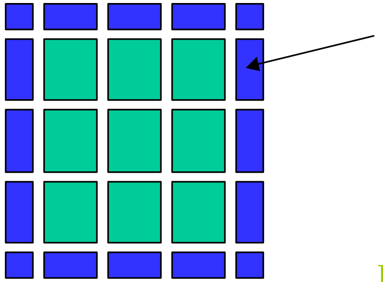
C4	C4	C4
C4	C3	C3
C2	C1	C2
C3	C3	C4
C4	C4	C4

Common centroid layout

Cap. Cell layout



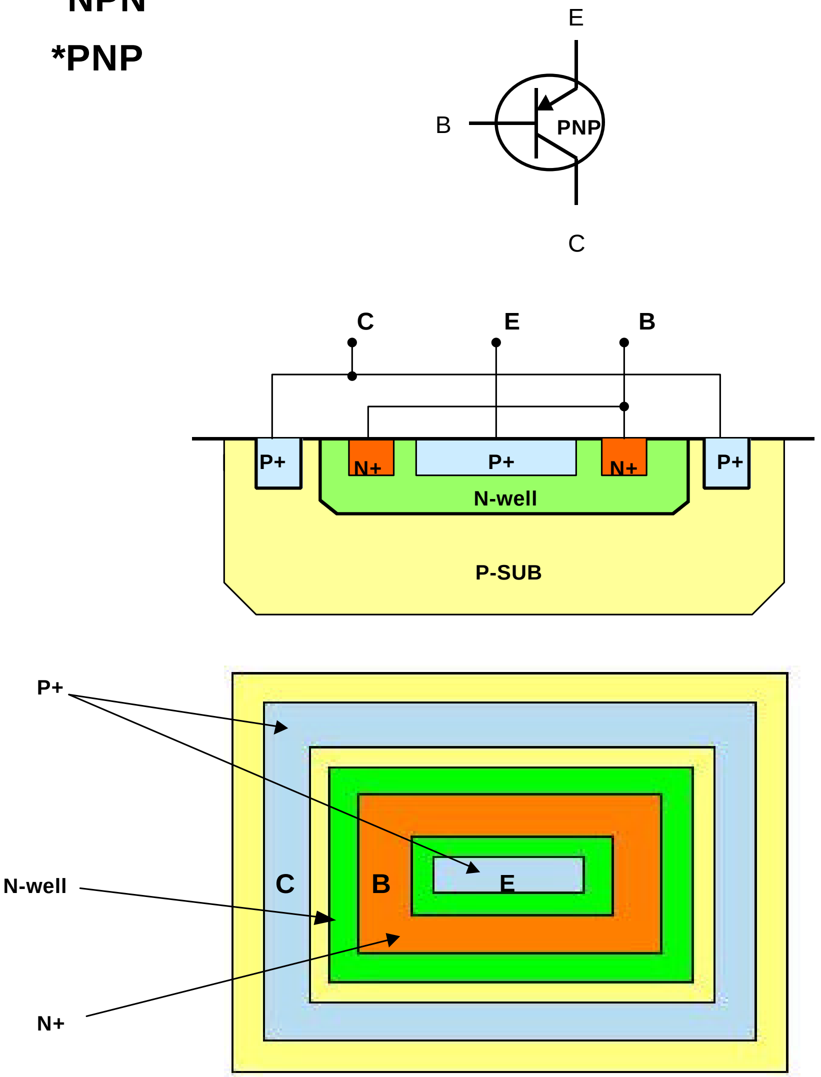


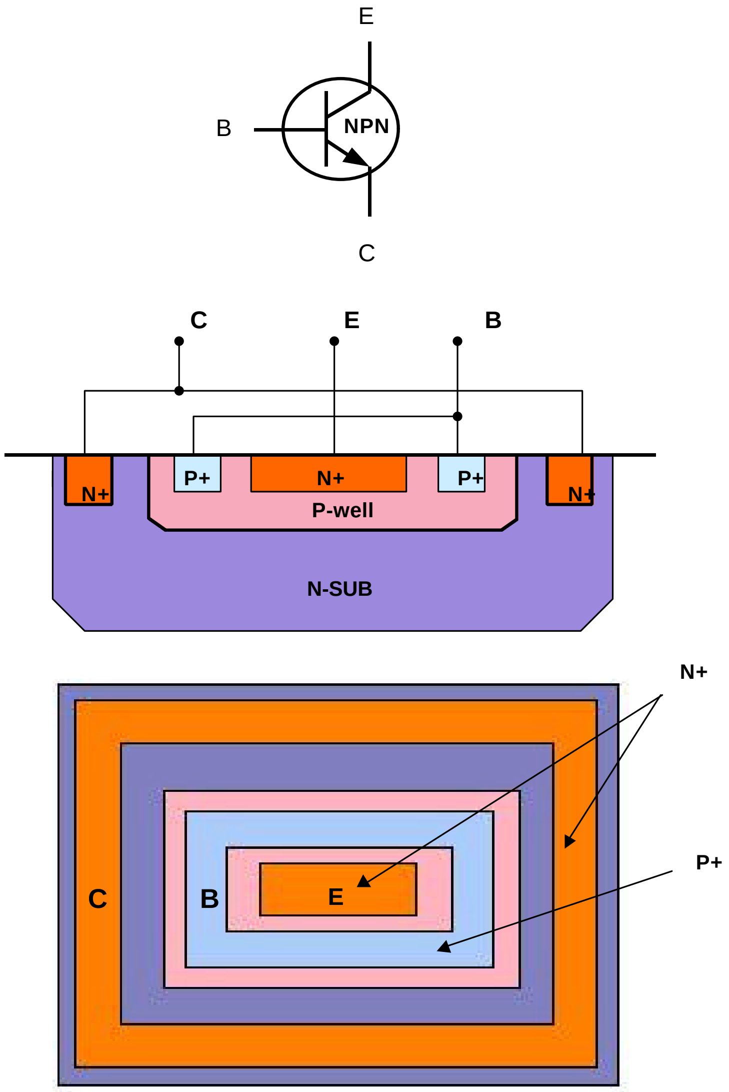


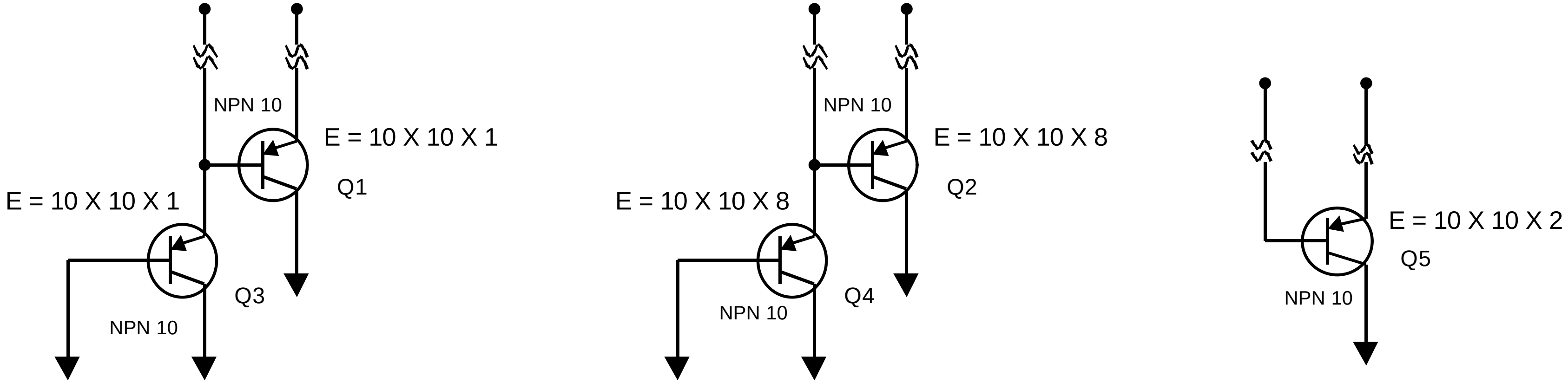
d. BJT

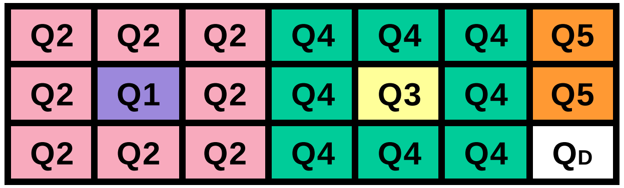
***NPN**

***PNP**


E
B
PNP
C
C
E
B
P+
N+
P+
N+
P+
N-well
P-SUB
P+
N-well
N+
C
B
E

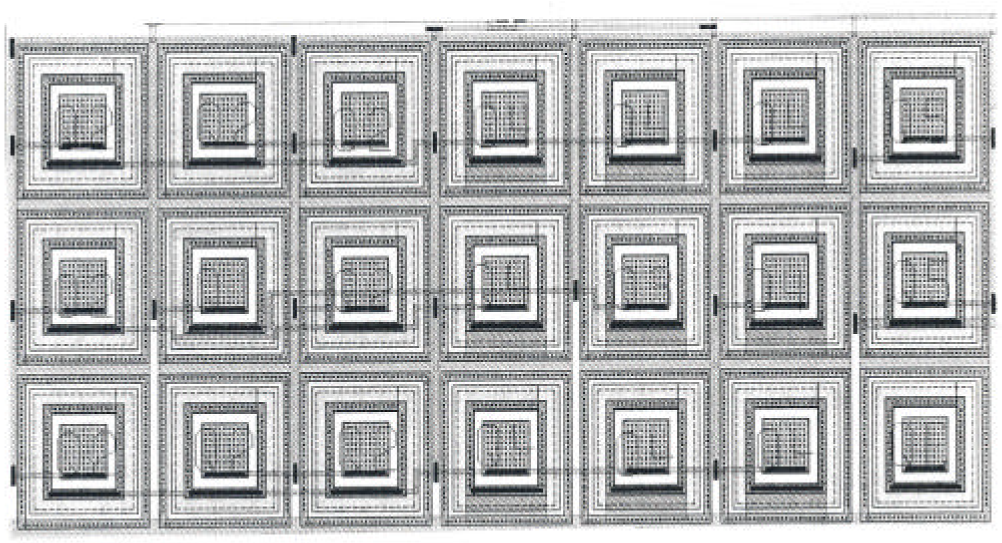

E
B
NPN
C
C
E
B
N+
P+
N+
P+
N+
P-well
N-SUB
N+
P+
C
B
E

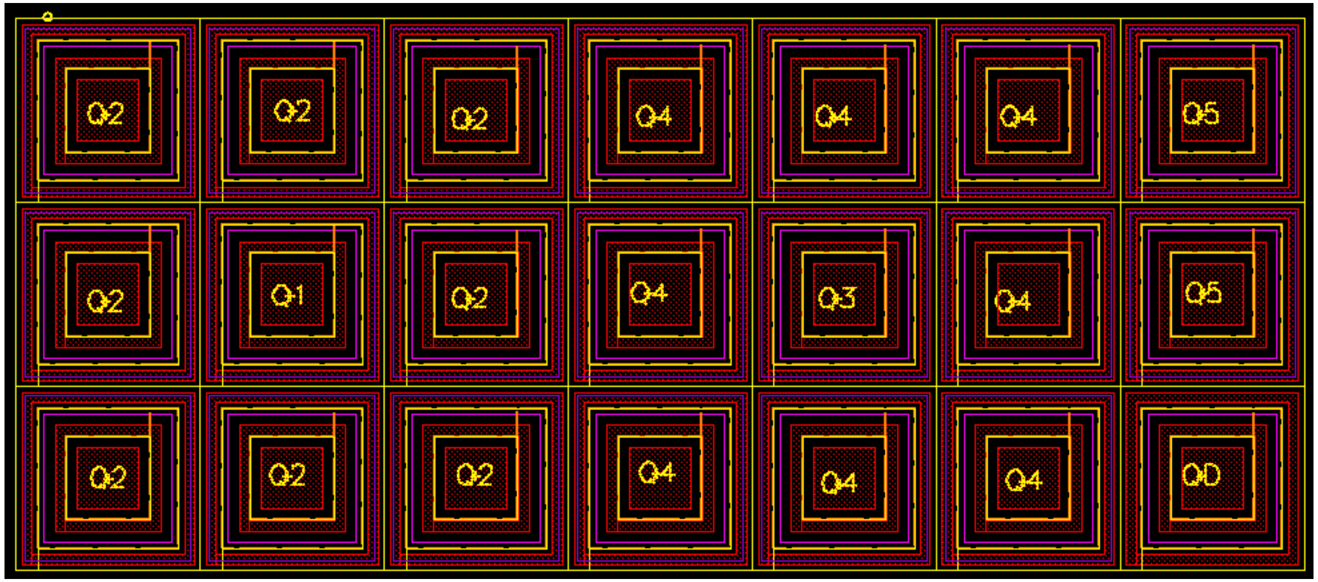




Q2	Q2	Q2	Q4	Q4	Q4	Q5
Q2	Q1	Q2	Q4	Q3	Q4	Q5
Q2	Q2	Q2	Q4	Q4	Q4	Q_D

dummy bjt

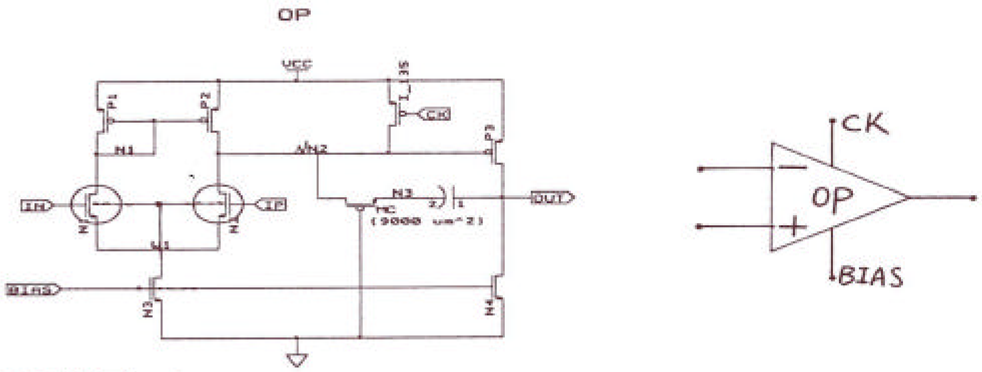



Q2
Q2
Q2
Q4
Q4
Q4
Q5
Q2
Q1
Q2
Q4
Q3
Q4
Q5
Q2
Q2
Q2
Q4
Q4
Q4
QD

e. OP amplifier

ANALOG CIRCUIT 之 OP LAYOUT 注意事項：

1：OP CIRCUIT AND SYMBOL。



2：LAYOUT(附圖一)。

3：說明：

3-1：N1 AND N2 MOS 之 LAYOUT PATTERN 與方向必須一致，且僅量靠近，最好使用 CROSS-LAYOUT，此乃爲避免 MASK PATTERN DEVIATION，而影響 DEVICE OFFSET VOLTAGE。

3-2：P1 AND N1，P2 AND N2 之間連線不允許其他信號線跨過，且 NN2 (HIGH-IMPEDANCE NODE)接至各點必須用 METAL 連接，也不要和其他信號線 COUPLING，連線必須愈短愈好，以達到較好之高頻響應。

3-3：電容之 LAYOUT 須在 WELL 內，此 WELL 接至獨立之 POWER LINE，不可和 OP POWER LINE 共用，電容之 WELL 不可與 N3、N4 MOS 之 WELL 共用，以防止 NOISE COUPLING。

3-4：N1 AND N2 MOS 之 SUBSTRATE 接 W1 NODE，而不是接其他 POWER NODE。

3-5：INPUT AND OUTPUT STAGE 須完全分開，可利用補償電容隔開，以防止 SPURIOUS FEEDBACK EFFECT。

3-6：利用補償電容置於 OUTPUT STAGE P3 AND N4 MOS 之間，使 P、N MOS SPACE 加大，降低 INTERNAL LATCH-UP 機會。

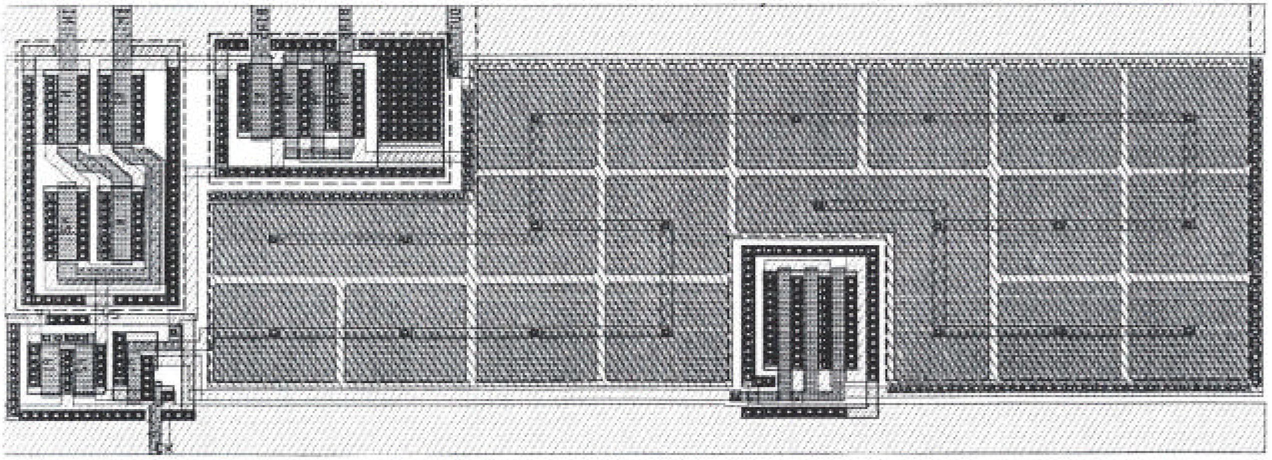
3-7：OP OUTPUT 須接電容之 BOTTOM LAYER (NODE 1)，以防止 NOISE 因電容之 BOTTOM LAYER(NODE 1)誤接至 OP INPUT NODE 而將 NOISE 放大。

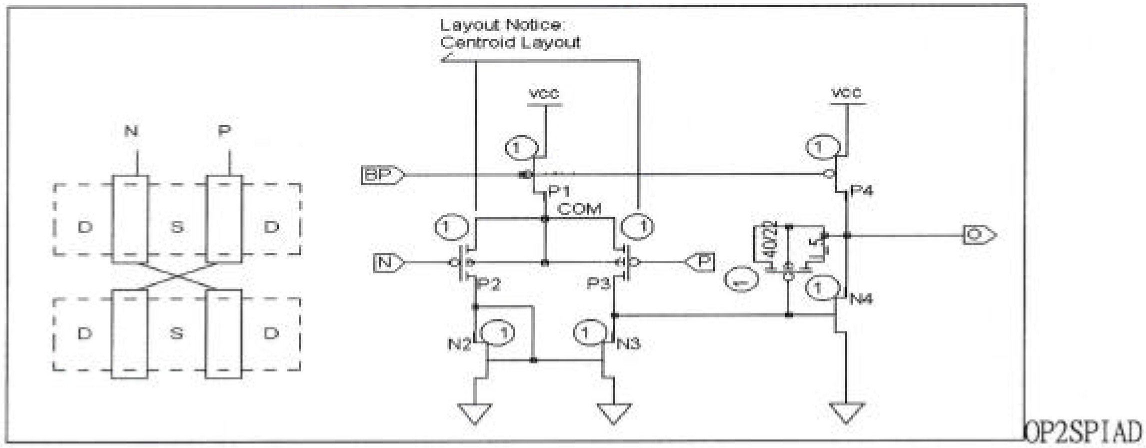
3-10：OP 之輸出信號不允許跨越輸入點，以免造成 FEEDBACK OSCILLATION。

3-11：OP 之 DEVICE LAYOUT 時，宜讓 DRAIN 的面積愈小愈好，主要爲了降低輸出點之寄生電容，及提高 PHASE MARGIN。

3-12：OP 之補償電容原則無規定長寬爲多少 UNIT，但僅量拆成多個 UNIT，而不是一整塊，以防止因製程之天線效應把 TOP LAYER AND BOTTOM LAYER 較 WEAK 處打穿，若有多個單位電容則不會有此情況產生，因電容之面積愈大，所集之電荷愈多，反之則小。

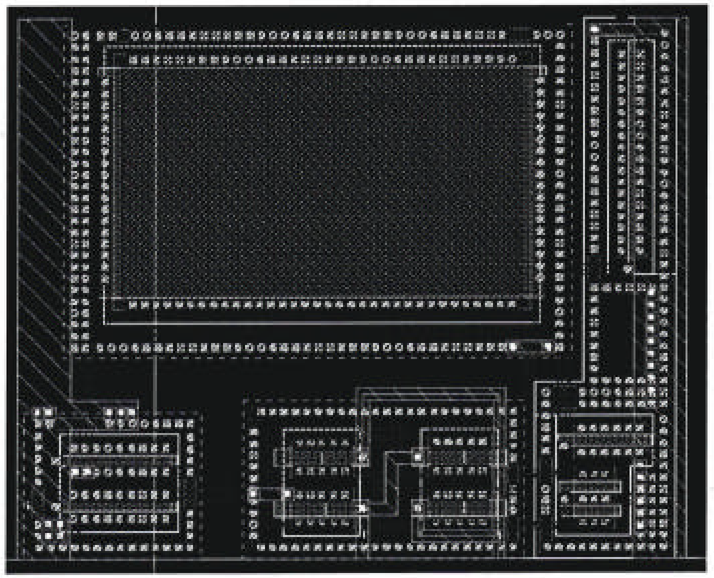
附圖一：

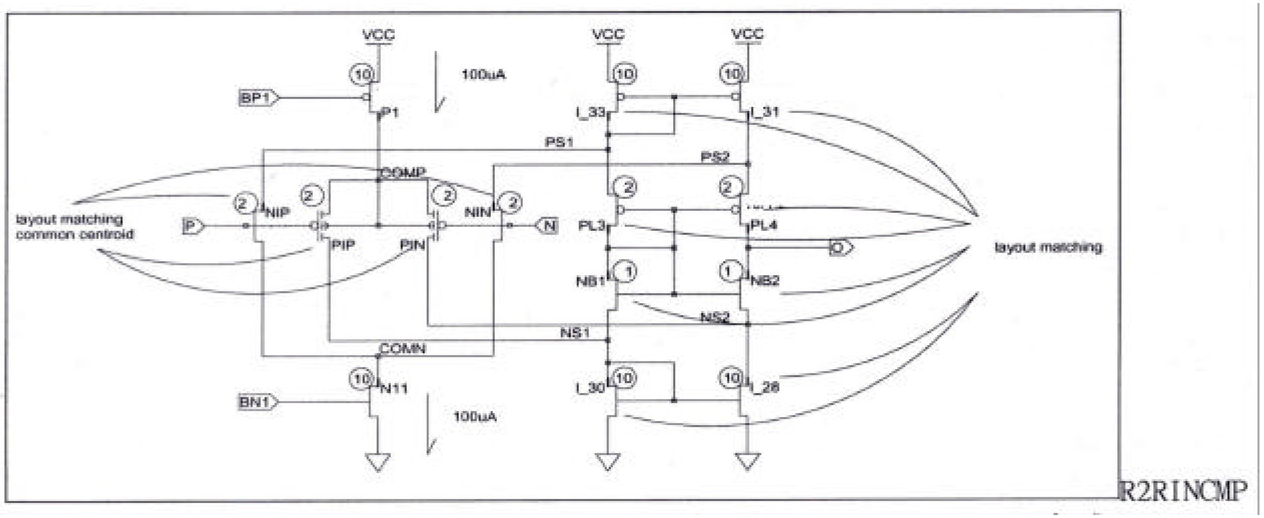




a. OP input stage MOS (P2&P3)是影響OP performance最嚴重的一級，因此一般設計皆不會使用minimum size (for process variation)，且需要以common-centroid方式layout，達到製程漂移最小.

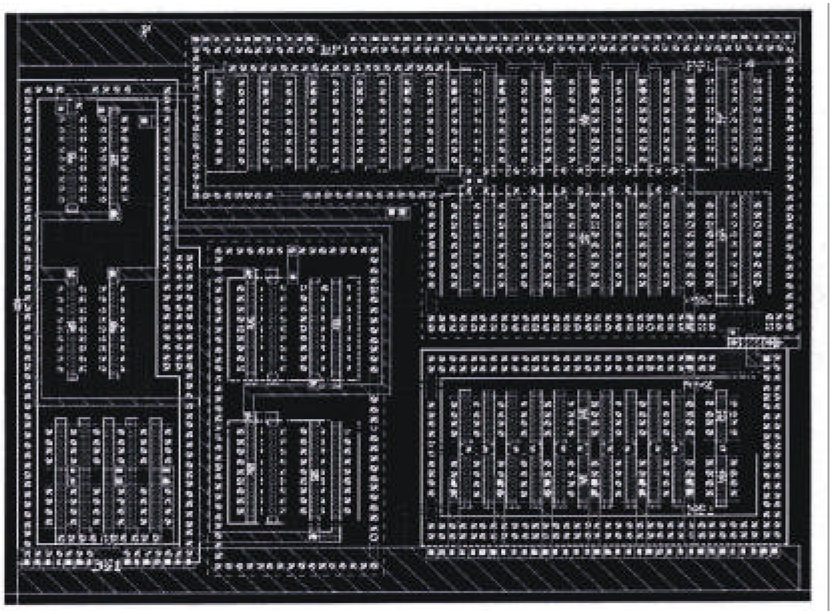
b. 對稱之MOS(N2&N3)，layout 成同一方向會有較好之matching.



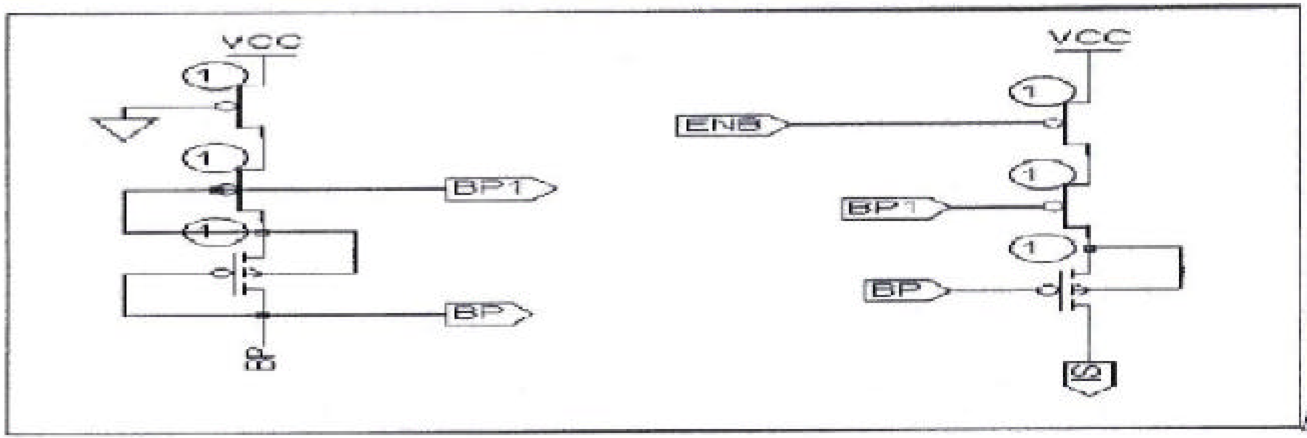


a．Input stage MOS (PIP&IN; NIP&IN)需要個別以 common-centroid 方式 layout，以降低 offset voltage．

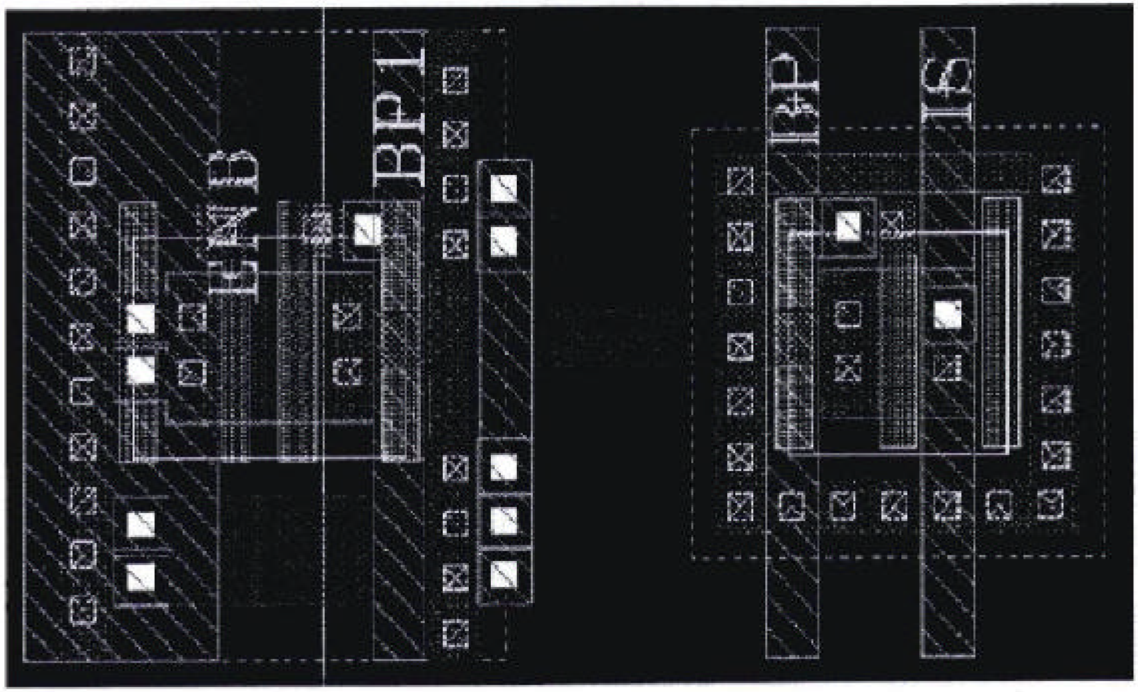
b． 對稱之MOS(1_33 & 1_31 ; 1_30 & T_28 ; PL3 & PL4 ; NB1 & NB2)，亦需 layout 成同一方向互相對稱。

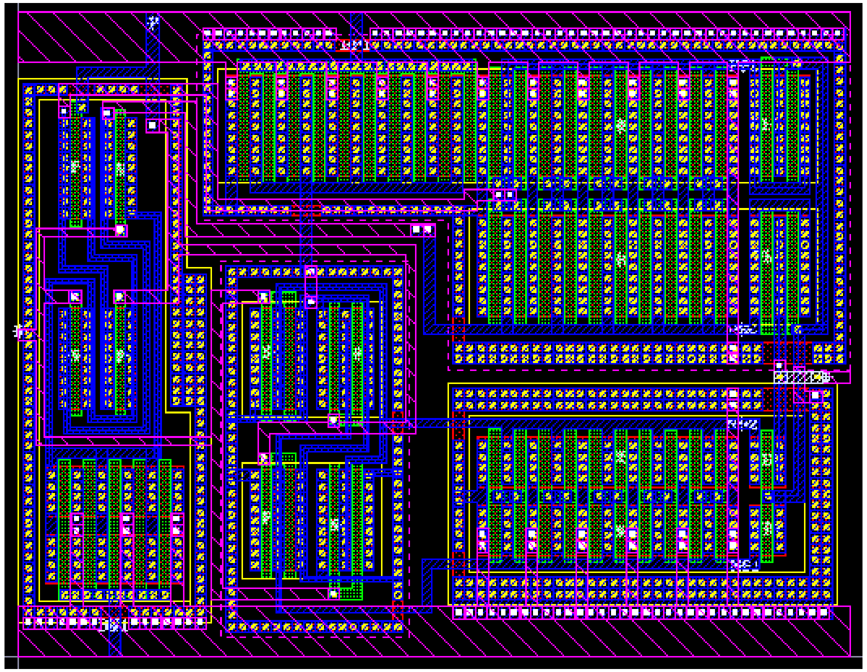


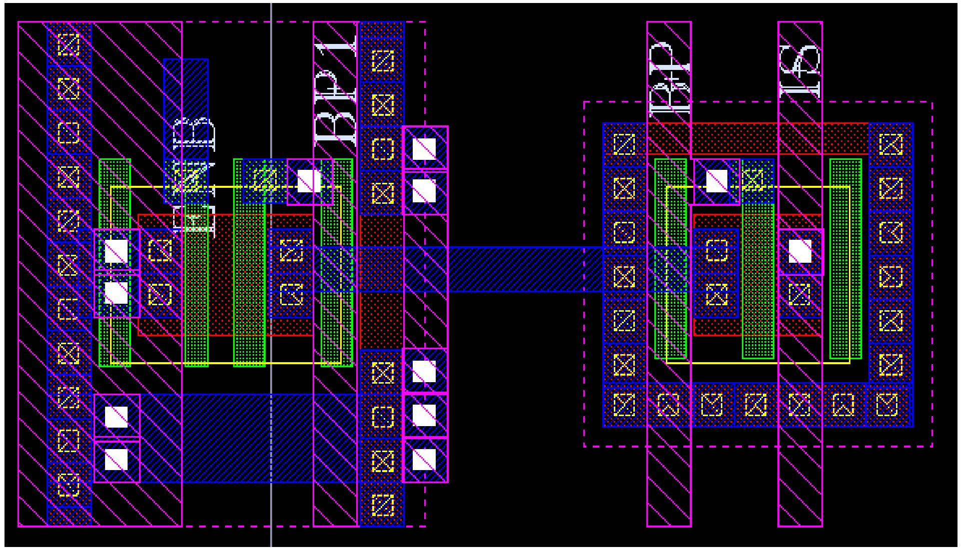
By Johnson Liu / NOVATEK



ADMCELL & ADCELL



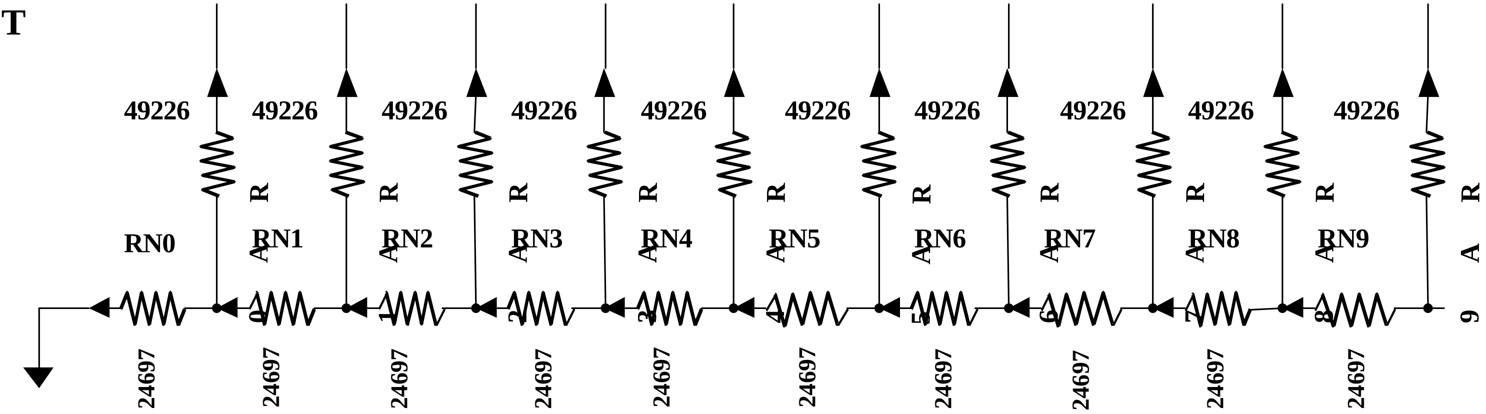



BP1
BP
IS

g. ADC/DAC

DAC LAYOUT 注意事項 :

1. DAC LAYOUT



2. LAYOUT (附圖一)

3. 說明 :

3-1：DAC 擺設以先決定電阻之 LAYOUT 方式，再 LAYOUT 其他 DEVICE，因電阻所用之 LAYER 不同，相對值也不同，而影響 PLAN AND BLOCK SIZE？

3-2：DAC 之電阻 LAYOUT 方式，除非必要勿用 WELL 當電阻 因 WELL 會 COUPLING SUBSTRATE NOISE，若用 WELL 當電阻，其 WIDTH 須大於最小值 5 – 6 μ m，以免在 ETCHING 時 WELL WIDTH 產生增減，阻值也隨之變化，影響 DAC PERFORMANCE，另外在 WELL上面必須覆蓋 METAL 並接至高電位或 VCC，以降低電壓係數以防止 WAFER 在測試時，因 WELL DOPING 低，經光照射，電阻值會降低，且呈現不穩定現象，影響測試準確度？

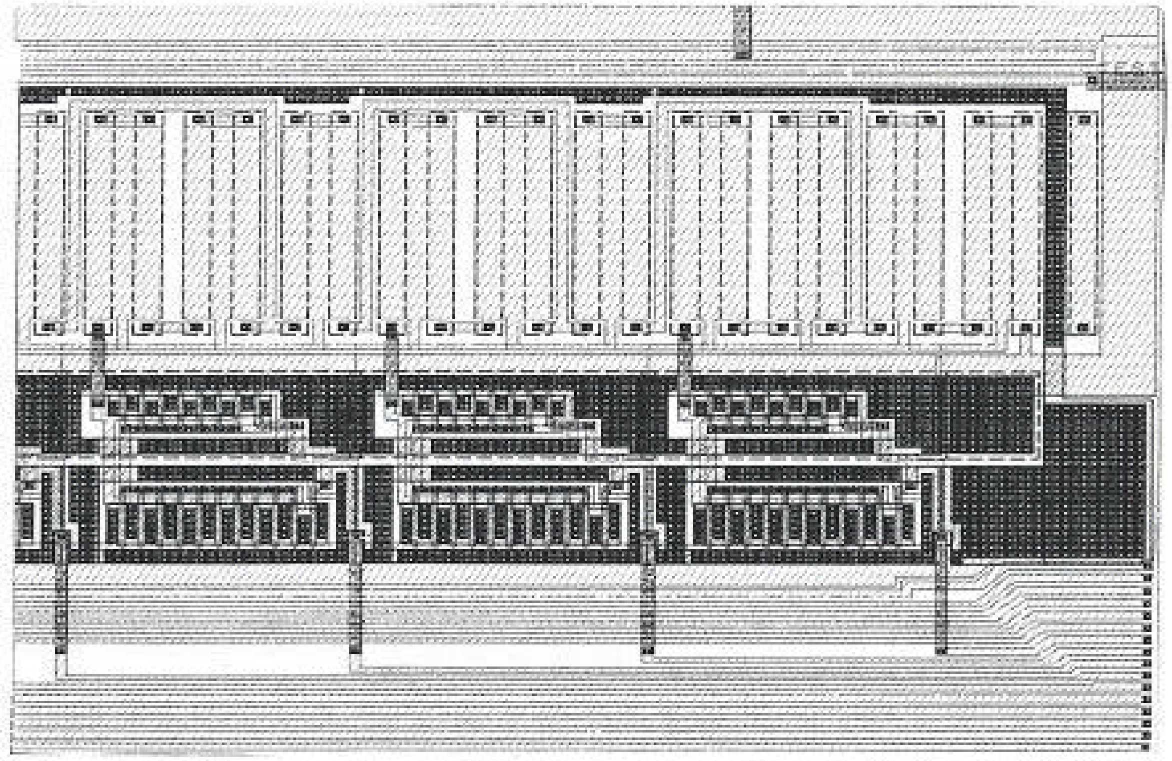
3-3：電阻 之佈局方式與方向，必須對稱且一致，最好是作一組再 COPY 至其他，而電阻四周必須加 DUMMY 防止曝光顯影光之繞射，使得四周電阻與內部電阻之阻值不一？

3-4：DAC之輸出點接至鄰近線路之輸人端必須愈短愈好，最好．其週圍用GND LINE 將其圈住，以隔離其他信號，防止電容效應產生 NOISE 干擾？

3-5：當電阻LAYOUT要求精確，MATCH AND RATIO 時，宜採用 POLY 來 LAYOUT 因其寄生電容最小。

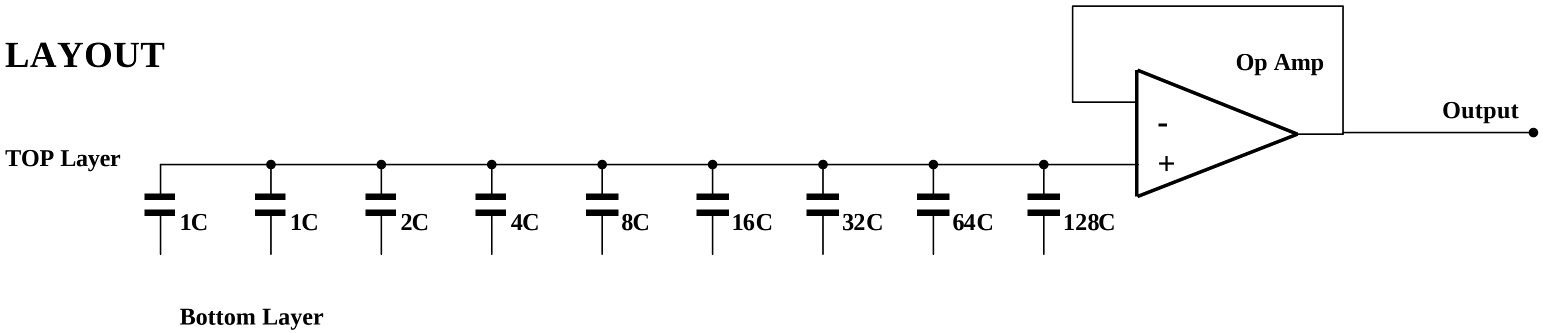
3-6：若 WELL 電阻欲接至 PAD，則必須於外圍環繞 GUARD RING，以防止對其他 CIRCUIT 造成 LATCH - UP。

附圖一



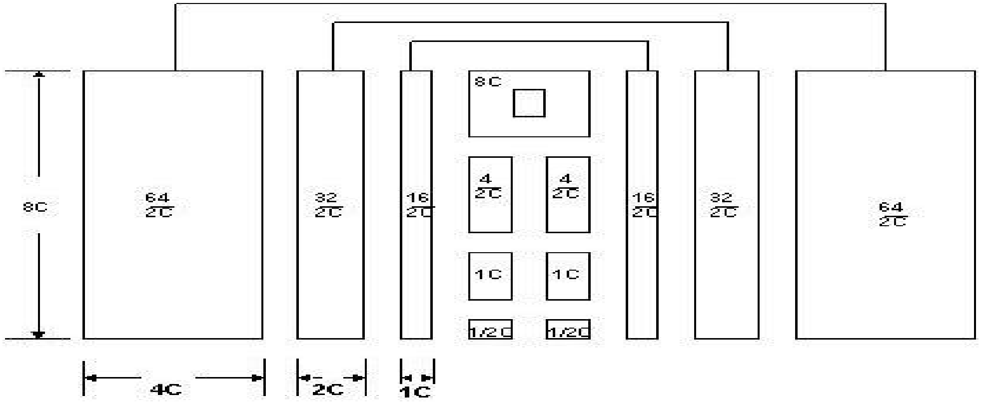
ADC LAYOUT 注意事項 :

1. ADC LAYOUT



2 : 說明 :

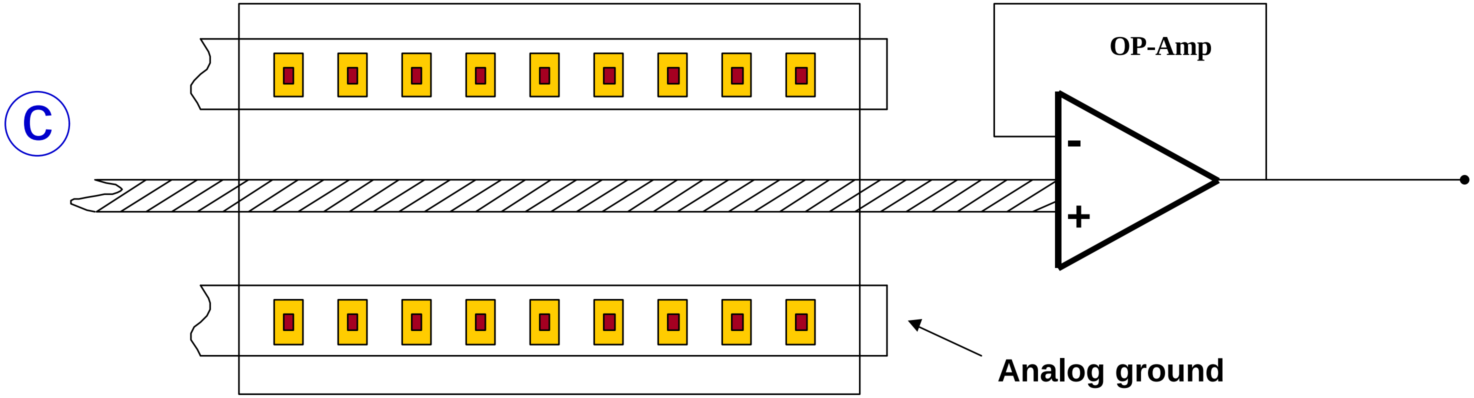
2 –1：ADC 中 CAPACITOR ARRAY 宜盡量排成近似正方形佈局然後將 1C、2C 、4C 、 8C 、 16C 、 64C、 128C 電容拆成兩半左右對稱佈局主要 在避免 PROCESS 變化而影響電容比值？



2–2：ADC CIRCUIT 中電容之比值在佈局時最重要的就是同心圓分佈和均衡，最後在四周加上 DUMMY GUARD RING 使每一個單位電容感受四周的環境變化會一致，以期減少容比值？

2–3：ADC CIRCUIT 中電容之排列佈局必須將電容的 TOP LAYER 連接至 OP CIRCUIT 的輸入端，且接至 OP CIRCUIT(+)輸入端之 METAL 越短越？

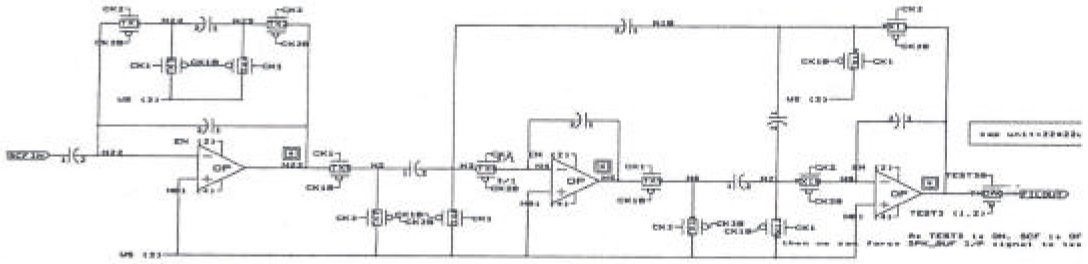
2 – 4 將電容之 TOP LAYER 接至 OP CIRCUIT(+) 這一段之 METAL LAYER 在 POLY Ⅰ上且 POLY Ⅰ接至 ANALOG GROUND，如此可預防 SUBSTRATE NOISE 的 COUPLING？



f. SCF

ANALOG CIRCUIT 之 SCF LAYOUT 注意事項：

1：SCF CIRCUIT。

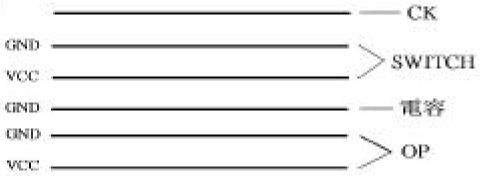


2：LAYOUT(附圖一)。

3：說明：

3-1：SCF LAYOUT PLAN 方式以 OP CELL PLAN 爲第一優先，也就是先決定 OP 大小再擺電容，因電容之佈局可朔性較大。

3-2：OP、SWITCH、電容之 POWER LINE 不可共用，其優先順序是 OP、SWITCH、電容，其佈局方式如下



3-3：各個電容必須用 WELL 圍住，其電位爲獨立之 POWER LINE，且POWER LINE 上不可挖任何 WELL OR SUBSTRATE CONTACT，用 WELL 圍住是把電容與SUBSTRATE 隔開，以防止 SUBSTRATE NOISE COUPLING。

3-4：各 OP CELL 之輸出端必須接電容之 BOTTOM LAYER。

3 - 5：各 OP CELL 之輸入端必須接電容之 TOP LAYER，且不允許跳線或其他信號線跨過？

3 - 6：電容若有多個 UNIT 組成而有不足 1 UNIT須與其他 UNIT 合並以降低電容值之誤差？

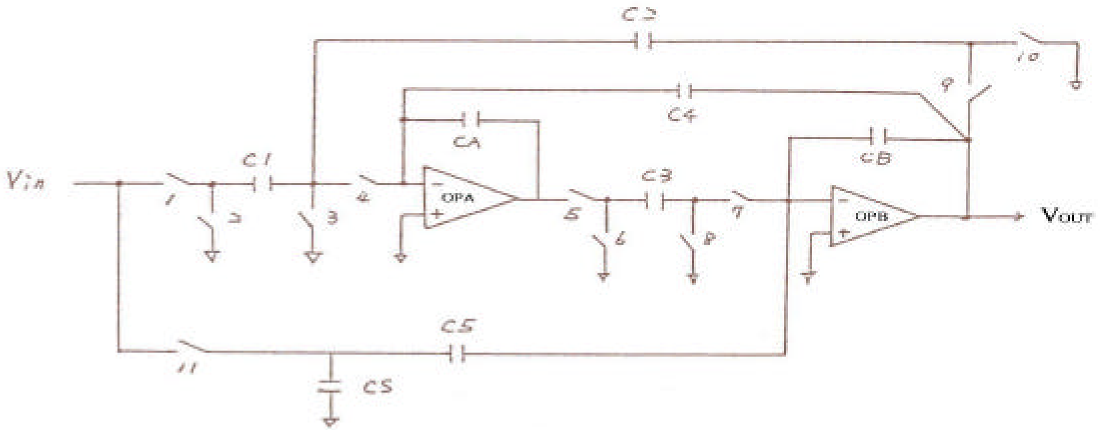
3 - 7：各 OP CELL 之輸入負端之所以接電容之 TOP LAYER，是因為電容之 BOTTOM LAYER 會 COUPLING SUBSTRATE 些許 NOISE 若接 OP 之輸入負端 則 NOISE 會被放大之故？

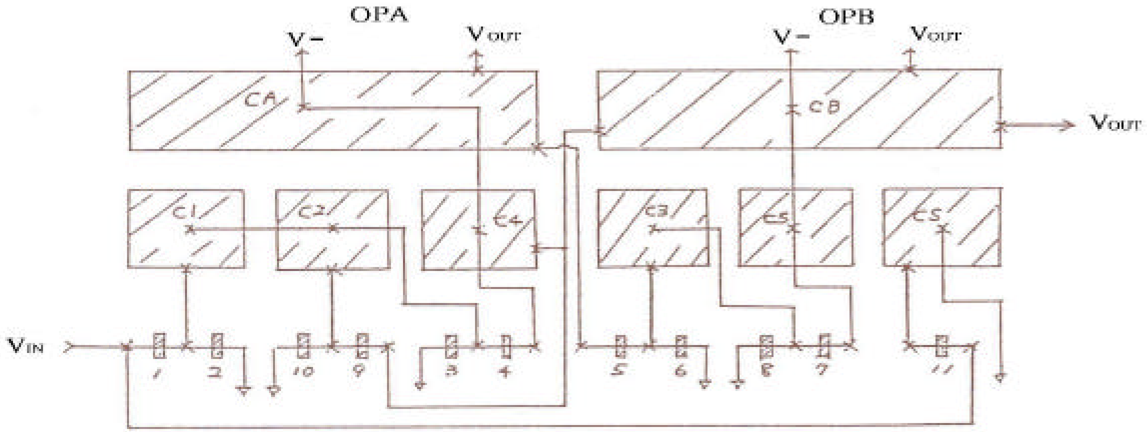
3 - 8：在佈局1 UNIT 電容時，因製程之變化會影響電容值之準確性較好之電容 LAYOUT 方式是 W = L 也就是正方形，並把四角切成 45 度 ETCHING 後電容形狀更一致，以減少圓角誤差，此斜角之大小須與 DESIGNER 討論？

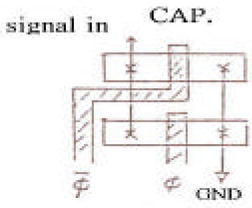
3- 9：OP CELL 之輸出端不允許跨越本身之輸入端以避免造型成 FEEDBACK OSCILLATION？

3-10：避免所有 SIGNAL LINE AND CLOCK LINE 之間信號互相 COUPLING？

3-11：直接連接或經 SWITCH 街至同一個 OP 負端的所有電容，宜盡量靠近並且成同心圓分佈？







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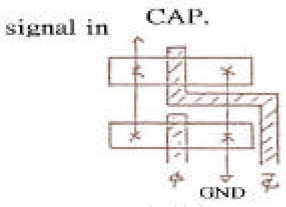
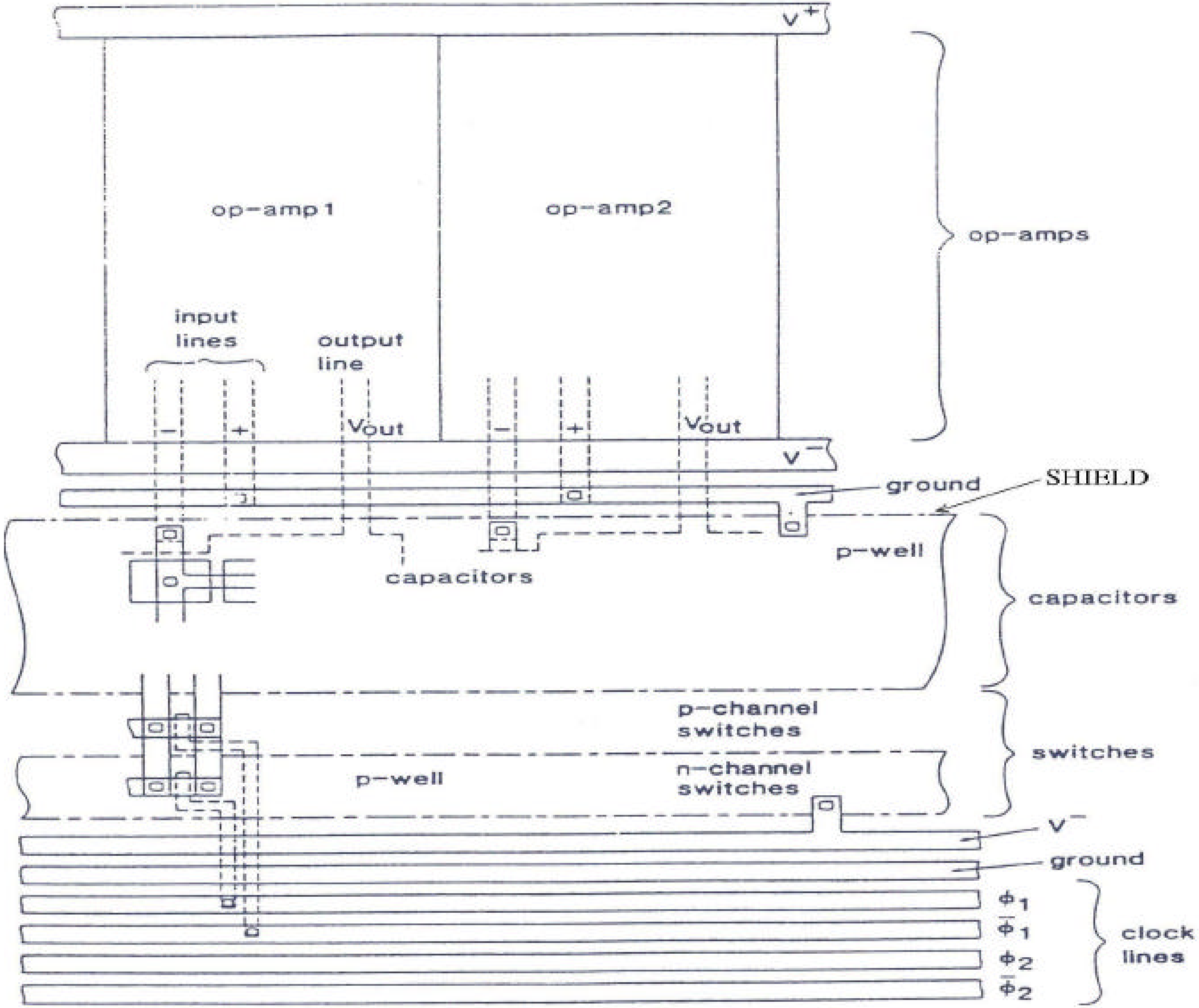


(O)

應該將 CLOCK 跨 GND LINE.


V+
op-amp1
op-amp2
op-amps
input
lines
output
line
−
+
Vout
−
+
Vout
V−
ground
SHIELD
p-well
capacitors
capacitors
p-channel
switches
switches
p-well
n-channel
switches
V−
ground
ϕ_1
$\bar{\phi}_1$
ϕ_2
$\bar{\phi}_2$
clock
lines

ANALOG CIRCUIT LAYOUT 注意事項：

1：若兩條信號線並排非常近時，會因電容效應而產生 CROSS-TALK NOISE，可藉著加大兩信號線間距離來避免此種效應的產生？

2：若當兩條信號線上下交叉通過，或是一排信號線通過一個固定參考電壓，其上下層雖有 THICK-OXIDE 做 ISOLATION，可是有時高頻信號仍會 COUPLE 到另一信號線上，而固定電壓對信號線的 COUPLING 也十分敏感，如此會產生錯誤動作，此時可用 POLY Ⅰ 加在上下兩層信號線間並接至 GND，以產生 SHIELDING 作用，隔離彼此的 COUPLING 現象？

3：若有 ANALOG BLOCK AND DIGITAL BLOCK 同置於 CHIP 中彼此 BLOCK 須用分開且每一 BLOCK 必須各自獨立一條 POWER LINE 如此可避免NOISE COUPLE？

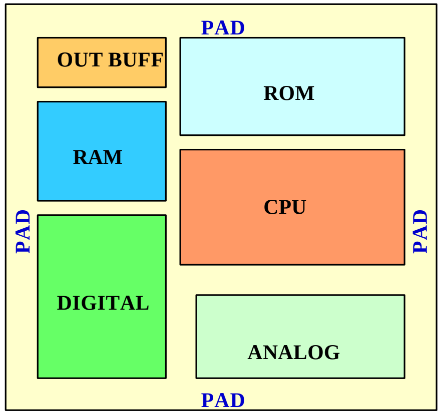
4 : ANALOG BLOCK 四週必須用 VCC OR GND RING 圍住，以防止 DIGITAL BLOCK NOISE COUPLE，此 VCC OR GND LINE 為獨立之 POWER LINE 且不接任何 DEVICE？

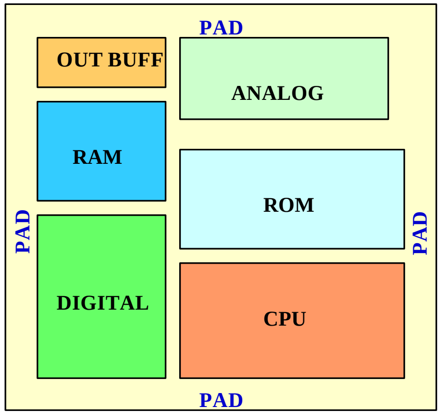
5：ANALOG 內各小 BLOCK 之 POWER 必須從 POWERPAD 處分開獨立連接，此 POWER LINE 不允許挖 SUBSTRATE OR WELL CONTACT，以防止 BLOCK 間 NOISE 經由 SUBSTRATE INJECTION？

3. Floor plan layout guide (noise immunity)

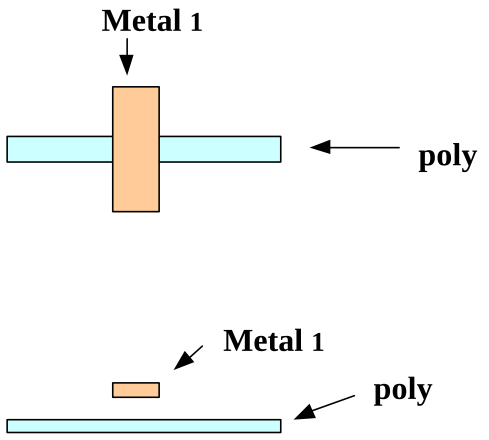
- **coupling from signal line**
- **coupling from substract**
- **coupling from power line**

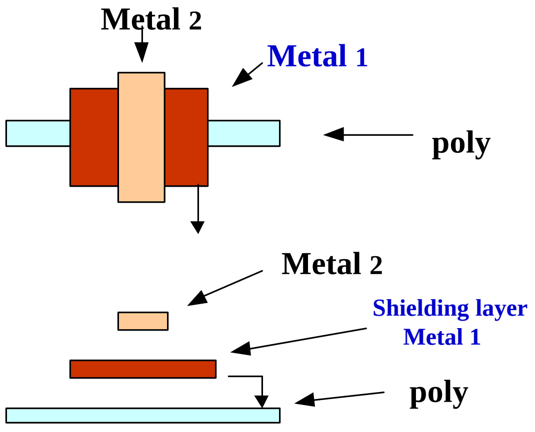
a. coupling from signal line



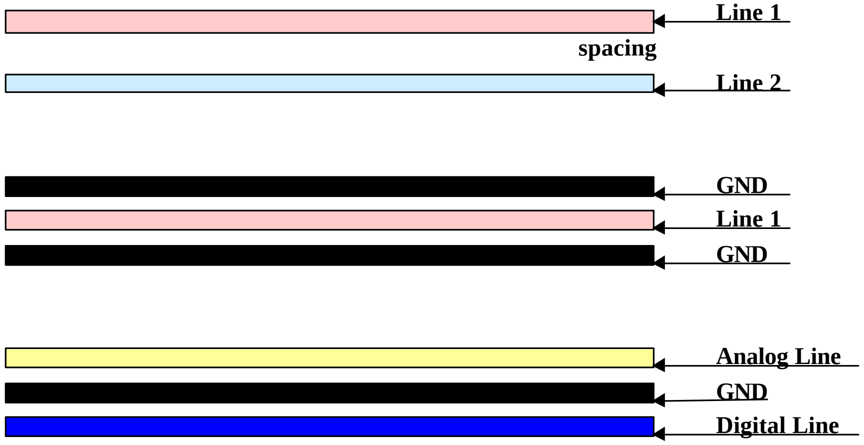


*** Signal line shielding**



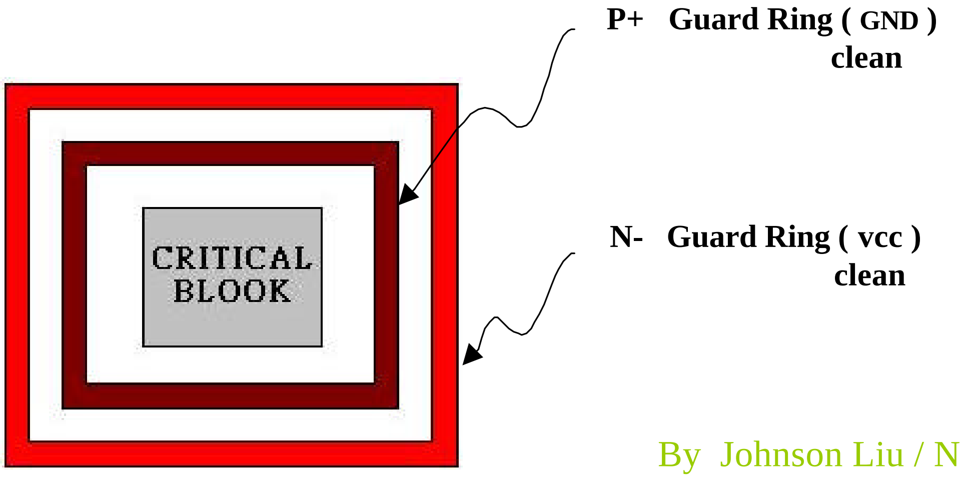


* Far away two signal line



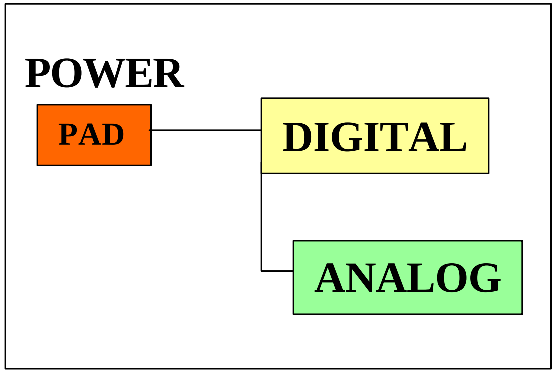
b. Coupling form substract

* guard ring



*well isolation

C. Coupling from power line



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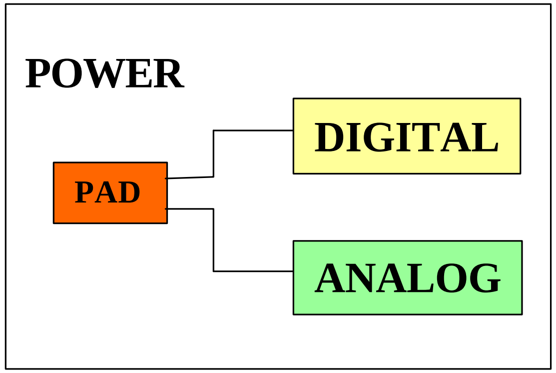

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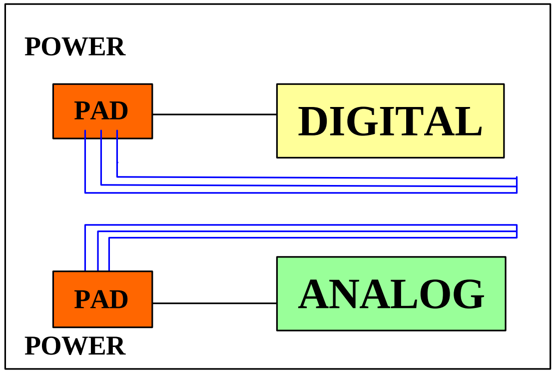

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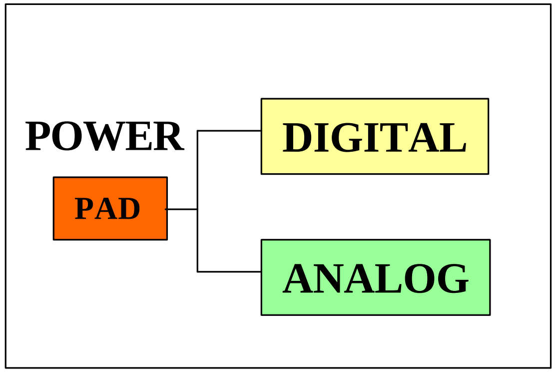

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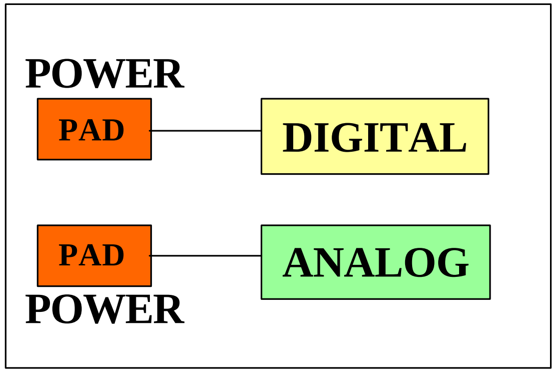

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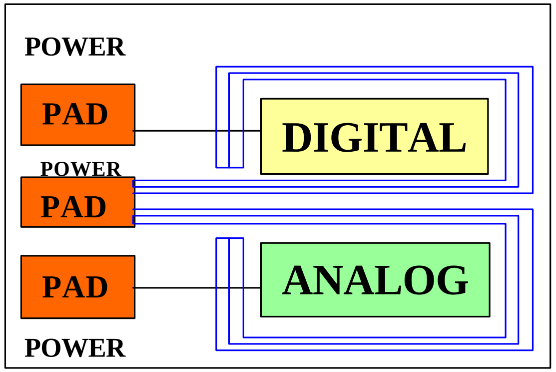

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