

MOSIS Report

ECE 532

A Low Power CMOS Bandgap Voltage Reference

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Abstract

This report is a summary of the student projects completed in ECE 532 – Advanced Analog Electronics at The University of Tennessee. The project included the design, simulation, and layout of a bandgap voltage reference circuit using the AMI C5N 0.5- μm process through MOSIS. Seven different bandgap circuits were submitted for fabrication. In this report, a summary of the design procedure will be given, followed by a detailed design analysis of one of the bandgap designs. The test results for all seven bandgap designs will be shown on all five chips. The designs were simulated using the AMI models verified with characterization data available through MOSIS. Layout was done using the NCSU sub-micron scalable Cadence Design Kit (CDK) within the Cadence design environment.

Introduction

A low power bandgap voltage reference is to be designed, simulated, and fabricated using AMI's 0.5-micron CMOS process (CN5). The nominal supply voltage for the reference is $V_{DD} = 5V$. The current dissipation of the circuit should be $\leq 30 \mu A$ at $50^{\circ}C$. The nominal output voltage of the reference should be around 1.25V. The power supply rejection of V_{DD} should be ≤ -50 dB at 100 Hz. Only one pn-junction diode is allowed to be used in the design.

Circuit Description

Design

With the low power constraint of the specifications and the limitation of only one pn-junction diode, a design using primarily MOS devices had to be chosen. The beta multiplier was an ideal design choice for this project. A weak inversion operation of the beta multiplier current reference was used to generate a PTAT-like current. This current can then be used to provide a reference voltage by being put through a series-connected resistor-diode combination.

The output current of a weak inversion beta multiplier can be greatly influenced by body effect. In order to minimize body effect, a design using a pair of weakly inverted PMOS devices can be used instead of NMOS devices. Refer to *Figure 1* for a schematic of the design.

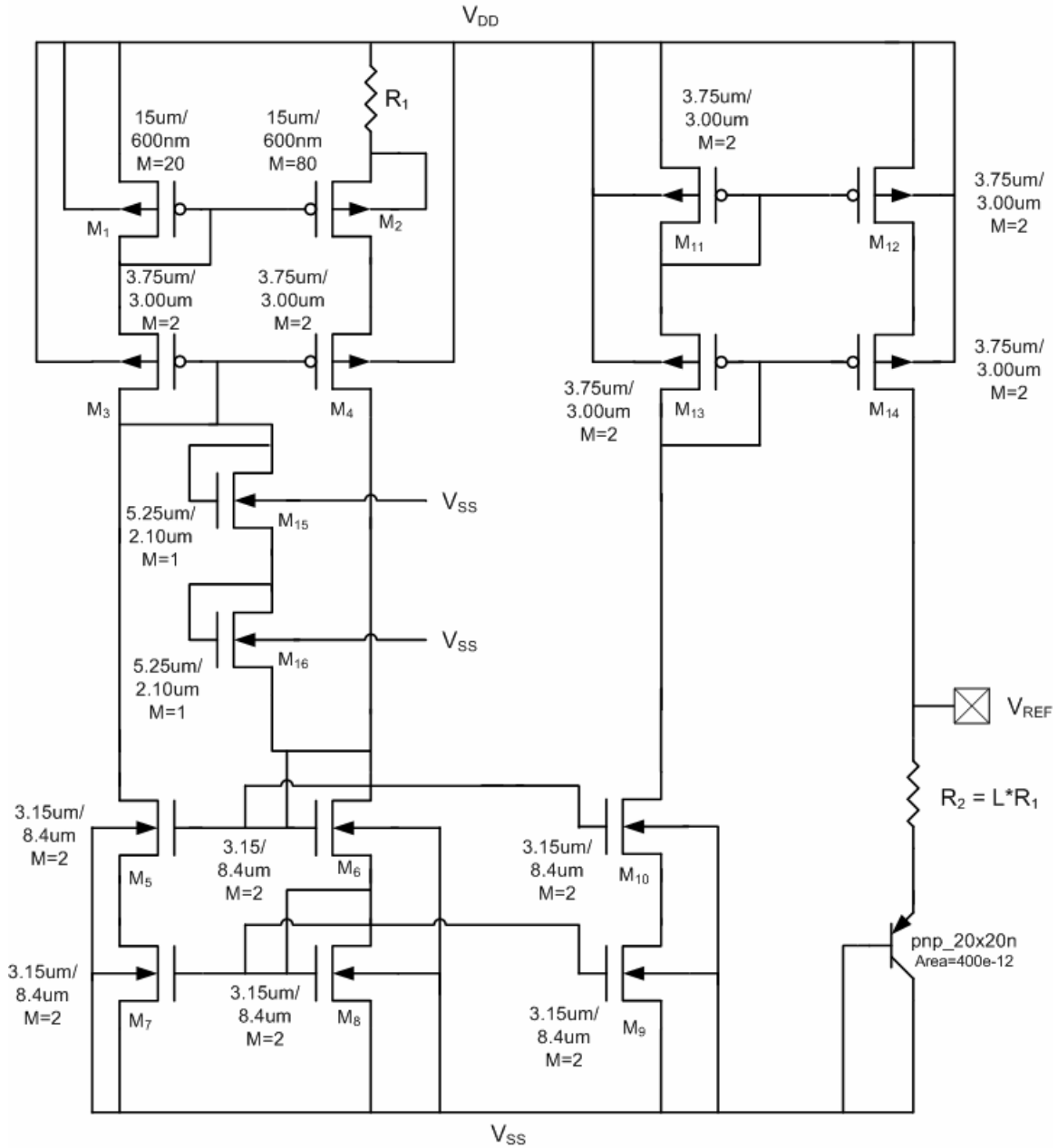


Figure 1 – Design Schematic

The PMOS devices M_1 and M_2 are the two devices that will function in the weak inversion region. All of the other transistors will be functioning in strong inversion in order to reduce the layout area as much as possible.

In order to bias up M_1 and M_2 correctly in the sub-threshold region, the following equation was used.

$$R = \frac{n \cdot V_T}{I_{REF}} \cdot \ln K$$

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The thermal voltage, $V_T = 26 \text{ mV}$ at room temperature. The value of K was chosen to be 4. I_{REF} was picked to be $3\mu\text{A}$, and the value of n for this process was estimated to be 1.3. With all these values, the bias resistor value can be determined. The initial value for resistor turned out to be around $16 \text{ k}\Omega$.

Device sizing for the two weak inversion devices was very important. Trade offs had to be made in order to keep the area of the devices small while still ensuring that the devices stay in weak inversion throughout the 100°C range. By utilizing the following equation, the W/L ratio of the diode connected PMOS device can be calculated.

$$IC = \frac{I_D}{I_s} = \frac{I_D}{I_o \cdot \left(\frac{W}{L}\right)}$$

The reason for calculating the W/L ratio for M_1 as opposed to calculating the W/L for M_2 is because the size of M_2 will be K times larger than M_1 in order to achieve the same current. If the W/L ratio was designed for M_1 in order to keep it in weak inversion then K times that W/L ratio will mean that M_2 would also be in weak inversion. For I process, $I_o = 80\text{nA}$ for the PMOS transistors and $I_o = 200\text{nA}$ for the NMOS transistors. With an $IC=0.075$, the required W/L ratio came out to be 500 for M_1 . M_2 's ratio had to be 4 times larger which means the ratio was 2000.

Because of these large W/L ratios, the usual practice of making L at least four times the minimum was not used in these weak inversion devices. The devices would have been excessively wide even if an L of just $2.1 \mu\text{m}$ was chosen. The final W/L chosen for M_1 and M_2 was $\frac{15\mu\text{m}}{600\text{nm}}$. M_1 's multiplier is 20 while M_2 's multiplier is 80.

Other than the two PMOS devices, M_1 and M_2 that generate the PTAT current, the rest of the devices in the circuit will function in strong inversion. The PTAT current has to be mirrored in order to provide a voltage reference that is relative to ground instead of V_{DD} . The sizing for the rest of the transistors in the bandgap reference was determined similarly to M_1 and M_2 . An inversion coefficient of 20 was chosen for the NMOS devices which resulted in a $W/L = 3/4$. IC of 15 was used for the PMOS devices which resulted in a $W/L=2.5$. With these W/L ratios calculated, the current mirror multipliers were then determined. To better provide accurate current mirrors, matching of the transistors is extremely critical. The m factor for the devices was designed to be two. The mirrors used were also cascode current mirrors which further ensure a more accurate copy of the current.

Once the PTAT current has been properly mirrored to achieve the correct polarity, the reference voltage is simply determined by the voltage across the series-connected resistor-diode combination. The resistor, R_2 , at the output is L times larger than the resistor, R_1 .

$$V_{REF} = I_{ptat} \cdot L \cdot R + V_d = I_{ptat} \cdot L \cdot (nV_T \cdot \ln K) + V_d$$

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With the above expression, the temperature coefficient for V_{ref} can be determined.

$$TC_{V_{REF}} = \frac{1}{V_{REF}} \frac{\delta V_{REF}}{\delta T} = \frac{1}{V_{REF}} \left[L \cdot n \cdot \ln K \cdot \frac{\delta V_T}{\delta T} + \frac{\delta V_d}{\delta T} \right]$$

$$\text{where } \frac{\delta V_T}{\delta T} = 0.085 \text{ mV}/^\circ\text{C} \text{ and } \frac{\delta V_d}{\delta T} = -2 \text{ mV}/^\circ\text{C}$$

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Since the best possible $TC_{V_{REF}} = 0$, the value of L can be determined. An initial calculation was done and $L \approx 13$. With the initial values for the resistors and the device sizes determined, the next step was to produce a schematic with these preliminary values. Entering the device sizes for the transistors was fairly straight forward. However, the resistor was a little different. The HY resistor model was used in schematic because it matches the process's resistor. However, the W/L resistor ratios had to be used instead of resistance values. By choosing the L to be $2.1 \mu\text{m}$, the W was then adjusted in order to reach a resistor value close to the resistor values from the design phase. Simulations of the bandgap voltage were done using the typical MOSFET models from $0^\circ\text{C} - 100^\circ\text{C}$ and the initial results were analyzed. L was adjusted until the temperature coefficient curve became flat ($TC_{REF} \approx 0$). Once a very low TC was achieved, the L ratio was kept the same between the two resistors. The value of resistor, R_I , was adjusted to shift the value of V_{REF} to about 1.25V . After some slight adjustments, the final resistor values were determined based on the results. The startup circuit used for this bandgap voltage reference is very simple. Referring back to **Figure 1**, it can be seen that the startup circuit is just two diode connected NMOS devices, M_{15} and M_{16} , connected between the PTAT current generator and the NMOS current mirror. Once the circuit gets “turned

Layout

Common-centroid, guard rings, and other essential layout practices were utilized in this design. The resistors were laid out very carefully in order to improve their matching. In order to lay out the resistors in common-centroid, the W/L ratio of the resistors had to be adjusted slightly. During the schematic phase of the design, a $W=2.1\mu\text{m}$ was chosen so that only L needed to be varied. Since it is impractical to lay out a single resistor, especially if it is a large resistor, it is essential that the resistor can be divided up into multiple fingers that can later be connected together in series. While the original design for the PTAT generation resistor called for a ratio of $33.5\mu\text{m}/2.1\mu\text{m}$ and the V_{REF} resistor ratio of $372\mu\text{m}/2.1\mu\text{m}$, their L 's had to be adjusted in order to allow for common-centroid layout. In the final design, the ratios were changed to $33.6\mu\text{m}/2.1\mu\text{m}$ and $369.6\mu\text{m}/2.1\mu\text{m}$, respectively. The new lengths are multiples of $16.8\mu\text{m}$. Each resistor element is $16.8\mu\text{m}/2.1\mu\text{m}$. While the PTAT resistor matched the schematic's PTAT resistor exactly, the V_{REF} resistor's length was $2.4\mu\text{m}$ less. Schematic simulations were done using the new length and the results turned out to be exactly what was expected. The performance was not as good as the original length, but it was still within the project specifications.

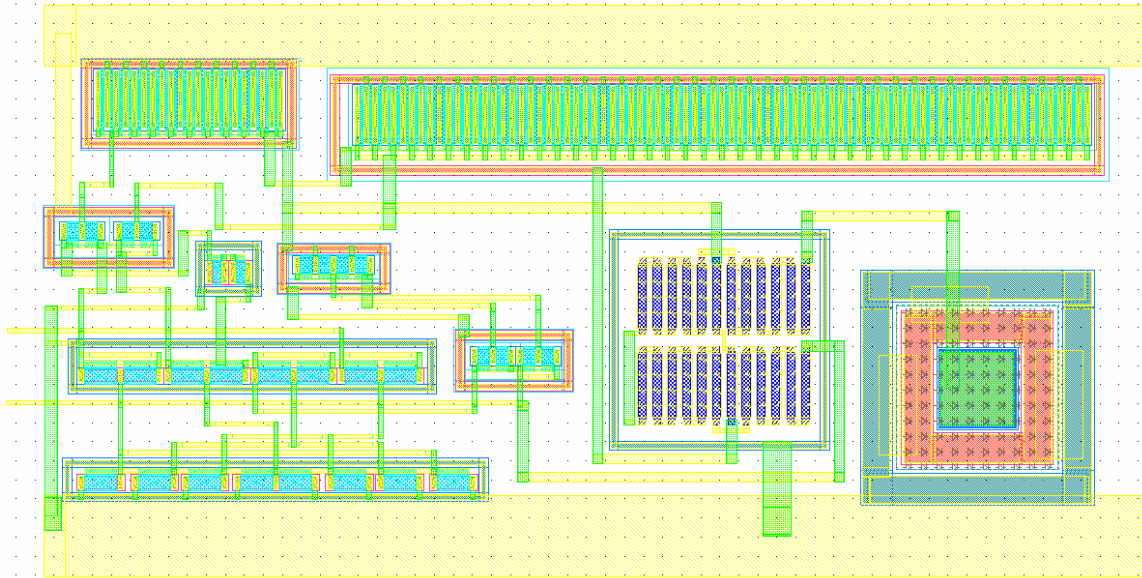


Figure 3 – Layout

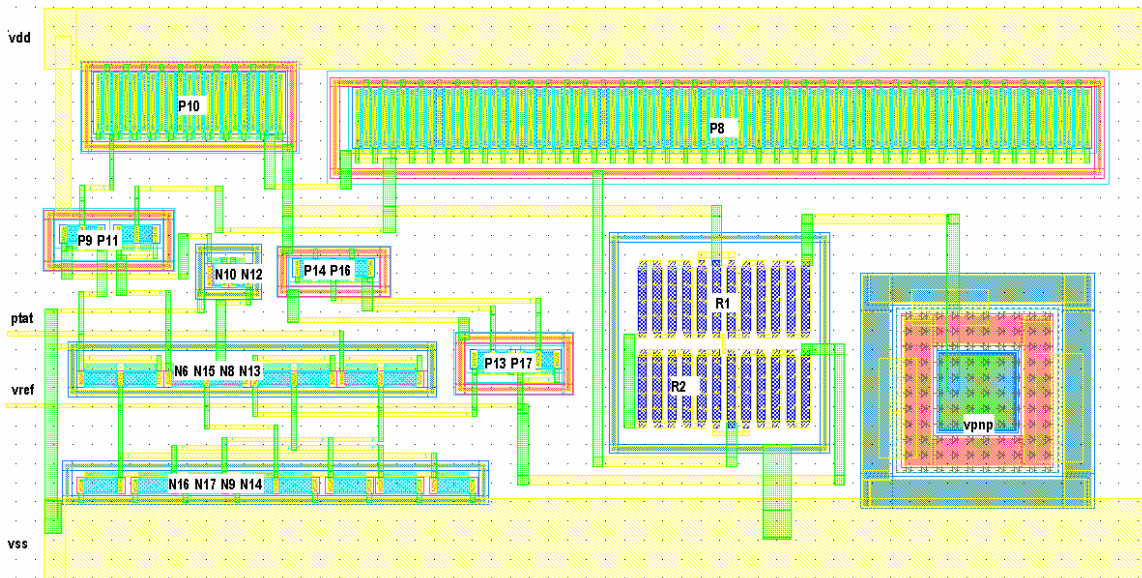


Figure 4 – Labeled Layout

Test Results

1. Room Temperature Test

Seven bandgap circuits were tested at room temperature. All five chips were tested. The results show that all seven BGR circuits were functional. However, there were definitely some chip to chip variations, and even large reference voltage differences in some of the BGR circuits.

Table 1 - Room Temperature Voltage Reference Measurement (V_{dd} = 5V)

Chip 1	V _{ref} with VDD = 5V	Chip 2	V _{ref} with VDD = 5V
BGR1	1.1669	BGR1	1.17782
BGR2	1.14011	BGR2	1.1822
BGR3	1.4615	BGR3	1.4095
BGR4	1.17976	BGR4	1.15488
BGR5	1.14521	BGR5	1.2316
BGR6	1.4051	BGR6	1.2927
BGR7	1.3649	BGR7	1.07709

Chip 3	V _{ref} with VDD = 5V	Chip 4	V _{ref} with VDD = 5V
BGR1	1.1658	BGR1	1.17831
BGR2	1.2052	BGR2	1.1018
BGR3	1.3668	BGR3	1.5611
BGR4	1.13324	BGR4	1.159
BGR5	1.18923	BGR5	1.2433
BGR6	1.5278	BGR6	1.4963
BGR7	1.16619	BGR7	0.9852

Chip 5	V _{ref} with VDD = 5V
BGR1	1.15295
BGR2	1.18155
BGR3	1.7135
BGR4	1.17649
BGR5	1.2327
BGR6	1.4648
BGR7	1.0647

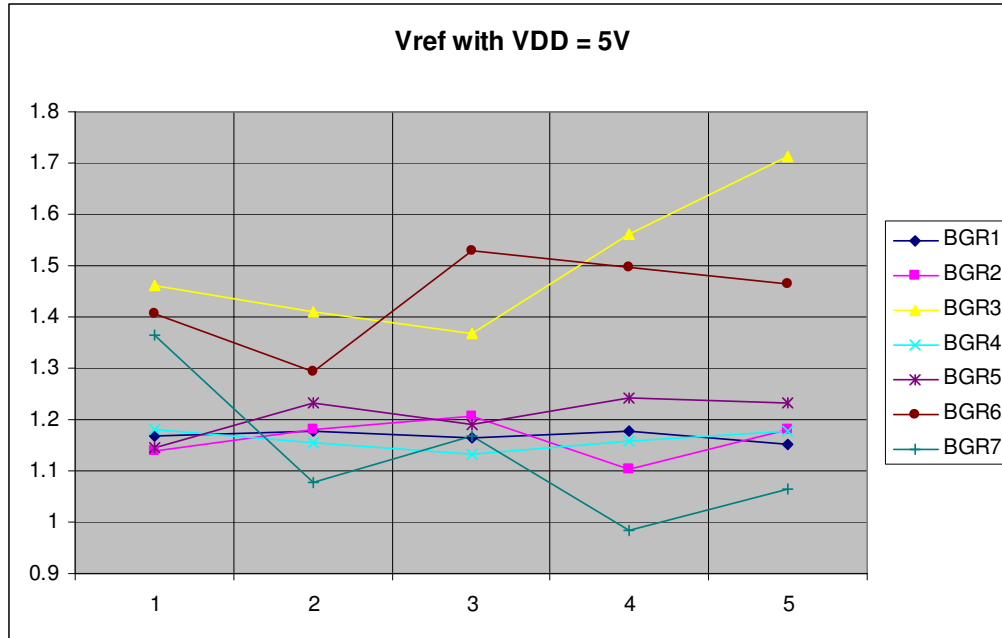


Figure 5 – Room Temperature Voltage Reference Measurement (Vdd = 5V)

2. Power Rail Voltage Change Test Measurement

The power rail voltage was varied from 5V to 4V and 6V. This test would give a general idea on how well the BGR circuits work with the change in supply voltage.

Only chip one was measured.

Table 2 - Reference Voltage Measurements with Supply Voltage Change

Chip 1	Vref (Vdd = 4V)	Vref (Vdd = 5V)	Vref (Vdd = 6V)
BGR1	1.15612	1.16052	1.2876
BGR2	1.13788	1.1395	1.14015
BGR3	1.4612	1.4652	1.5407
BGR4	1.17511	1.17659	1.17702
BGR5	1.1406	1.14521	1.3338
BGR6	1.3958	1.4012	1.4976
BGR7	1.3642	1.3668	1.3751

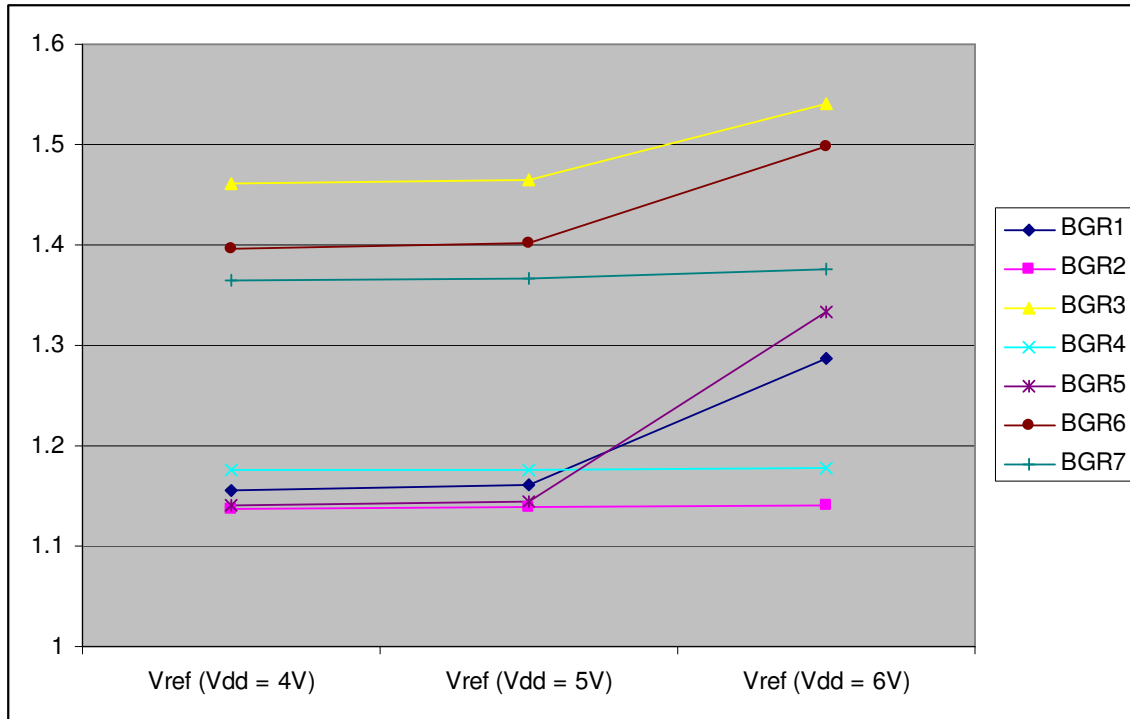


Figure 6 – Reference Voltage Measurements with Supply Voltage Change (Chip1)

The results show that most all the BGR voltages do not change much at a supply of 4V, but some of the reference voltages become noticeably higher with a 6V supply. This is most likely due to the top PMOS pair not remaining in weak inversion with a 6V supply.

3. Temperature Sweep Test Measurement

Two bandgap circuits, BGR2 and BGR4, were tested at various temperatures. Chips two and three were tested. Temperature was swept from -50°C to 150 °C.

Table 3 - Reference Voltage Measurements with Change in Temperature

Chip 2	-50 C	0 C	50 C	100 C	150 C
BGR2	1.18215	1.1806	1.18528	1.19721	1.2198
BGR4	1.15578	1.15412	1.15807	1.17089	1.19461

Chip 3	-50 C	0 C	50 C	100 C	150 C
BGR2	1.2114	1.2054	1.207	1.2155	1.2358
BGR4	1.12557	1.12915	1.13845	1.15359	1.18049

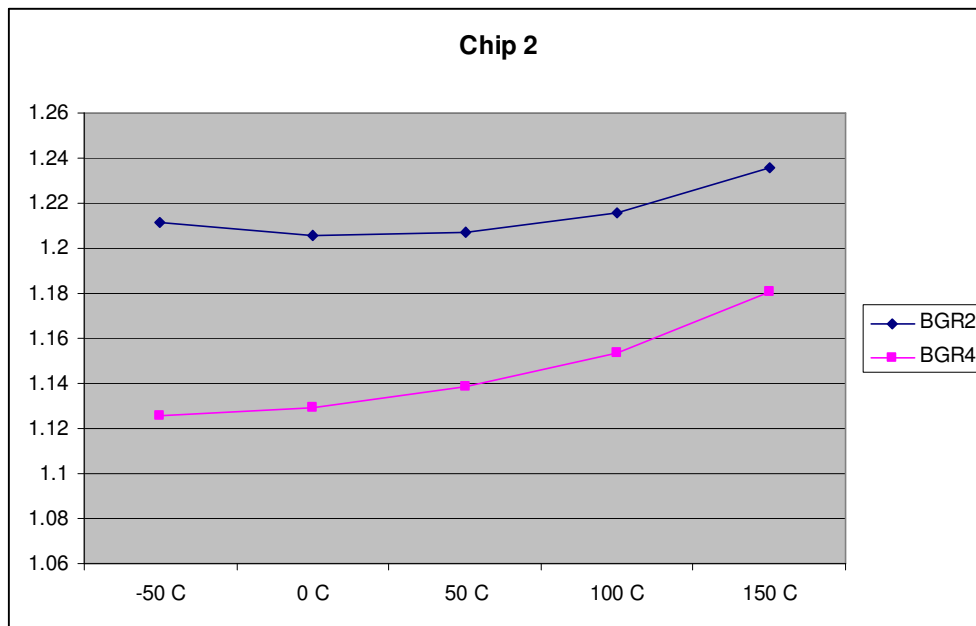


Figure 7 - Reference Voltage Measurements with Temperature Change (Chip2)

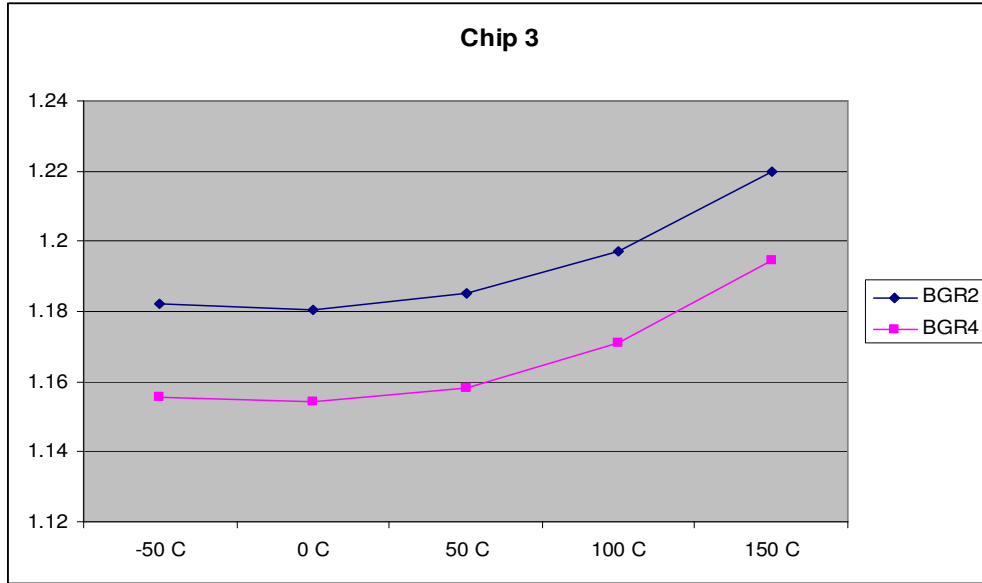


Figure 8 - Reference Voltage Measurements with Temperature Change (Chip 3)

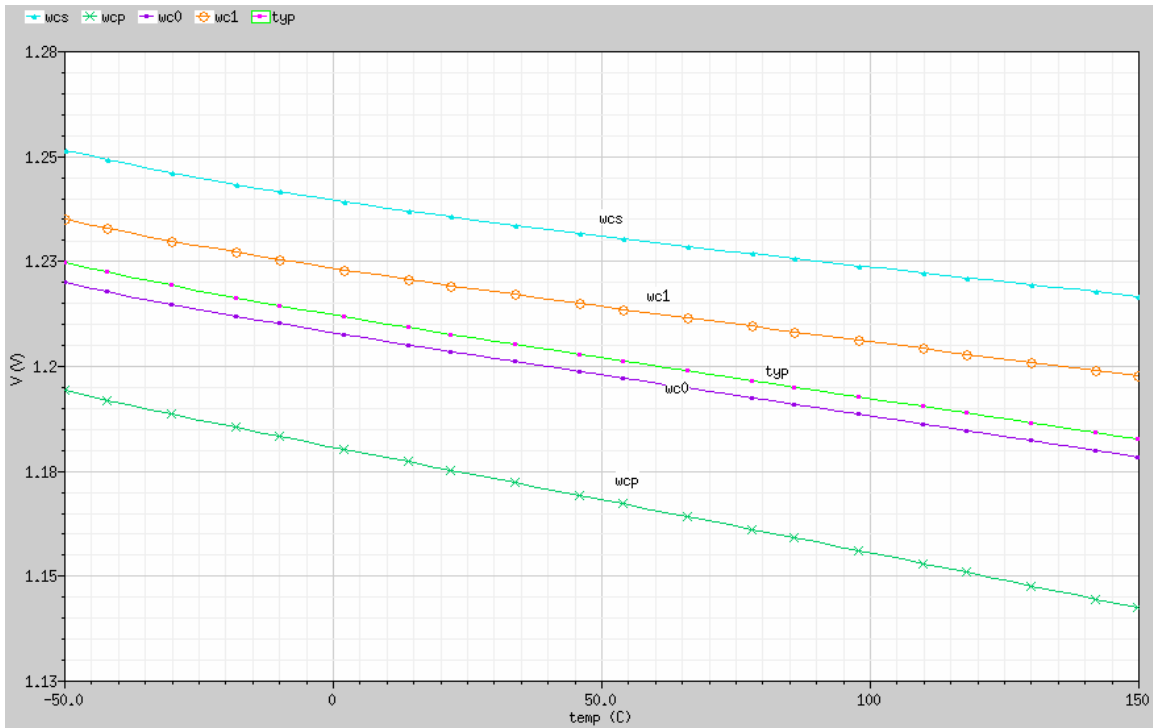


Figure 9 - Reference Voltage Post-layout Simulation with Temperature Change (BGR4)

Figure 9 shows the BGR4 post simulation results with temperature variation. The simulation results are quite different from the measured results. There are several possible explanations for this which includes:

1. Some of the critical matching components have asymmetrical layout. The weak inversion PMOS transistors in BGR4, for example, are not laid out symmetrically due to their large size.
2. The simulation results may not be precise because no Monte Carlo simulation was done for these BGR circuits.
3. The BJT model may need further improvement.

Conclusion

This report summarized the design, layout, and test measurement of the bandgap voltage references completed as an ECE 532 course project at the University of Tennessee. Seven designs were submitted for fabrication, and five chips were fabricated and packaged.

The room temperature testing shows the functionality of all seven BGR circuits on the five chips. The power rail test shows that all seven BGR circuits on chip one will work with a 4V supply voltage, and three of them would also work with a 6V supply. The temperature test was done on BGR2 and BGR4 on chips two and three. The results were somewhat different than the simulation results. This could be due to the asymmetrical layout of the circuit, the lack of Monte-Carlo Simulation, or the deficiency of the BJT model.

Submitting these class projects to MOSIS ultimately enhanced the students' design experience. The measurement results helped validate their understanding of the bandgap voltage reference circuit, and it also aided in developing improvements for future class projects.

Acknowledgement

Special thanks are extended to MOSIS and AMI for their support which made the fabrication of these class projects possible.