A High Accuracy Triangle-Wave Signal Generator for On-Chip ADC Testing

S. Bernard, F. Azaïs, Y. Bertrand and M. Renovell
LIRMM, University of Montpellier - 161, rue Ada - 34392 Montpellier - France
{bernard, azais, bertrand, renovell}@lirmm.fr

Abstract

A general BIST architecture for A-to-D converters involves the integration of both an analog test signal generator and a digital output response analyzer. This paper presents a structure for the internal generation of a linear signal used with the histogram-based test technique. The structure is based on two highly linear ramp generators together with a feedback control circuitry. Results show that the proposed structure preserves the linearity of the ramp generators while accuracy of the triangle-wave is provided by means of a calibration scheme.

1. Introduction

With the growing complexity of digital and analog circuits and the generalization of System-On-Chip (SOC), the price of mixed-signal circuits is being dominated by production testing costs. Indeed, the price of Automatic Test Equipment (ATE) becomes prohibitive because its performances can not easily follow the evolution of the new generation of mixed-signal circuits. Moreover, the poor observability and controllability of these high-complexity circuits demands ever-increasing test time and resources. In this context, Built-In-Self Test (BIST) technique is an attractive alternative to reduce the testing cost. Indeed a BIST technique allows to eliminate expensive mixed-signal tester, reducing the test time and making the accessibility inside the chip easier. Many mature BIST techniques have been proposed over the past years for digital circuits and most of digital designers use today these BIST techniques. The situation is not so advanced for analog and mixed-signal circuits. Many of these mixed-signal circuits includes Analog-to-Digital Converter (ADC) to allow the connection between digital and analog domain. It is essential to define a BIST solution for this component.

In the past few years, many published papers have been concerned with the definition of BIST techniques for ADC. Because one of the most significant constraints for a BIST architecture is the silicon area overhead, we have chosen to divide ADC BIST techniques in two groups according to the required pre-existing circuitry.

The first group concerns techniques dedicated for mixed-signal ICs including both an ADC and a Digital-to-Analog Converter (DAC). Most of these proposed BIST techniques use an all-digital approach. The test is performed by providing a digital stimulus to the DAC and monitoring the digital output of the ADC. The technique proposed in [1] also relies on digital BIST techniques. The digital generation of the stimulus and the digital analysis of the responses are performed using dedicated Linear Feedback Shift Register (LFSR)-based modules. An other all-digital BIST technique presented in [2] needs also a DAC in the same chip than the ADC under test. But in addition, the DAC must be $\Sigma-\Delta$ converter. The noise-shaper properties of this kind of converter are used to generate a pure analog sine-wave from a digital sequence created by a digital oscillator. Then, this signal is applied on the ADC input and the ADC response is analyzed by a digital signal processor (DSP) available in many ICs. It is clear that the viability of all of these techniques depends on a number of prerequisites such that the presence in the original circuit of pre-existing DSP capabilities and mainly the presence of both an ADC and a DAC.

The second group concerns techniques for ICs including solely an ADC. For these techniques, it is obviously not possible to use an all-digital approach. In this context, an original technique has been proposed based on the reconfiguration in test mode to create oscillations in the circuit [3]. Measurements on these oscillations guarantee some tests. Using this original BIST technique, no generation of input stimulus is required. A more classical ADC BIST scheme implies the analog generation of an input stimulus and the digital monitoring of the ADC outputs. In this context, the technique presented in [4] is based on analysis of Least Significant Bit (LSB) of the ADC output code. LSB is the bit that contains the more information on the output code variations because it switches over at each code transition. The operating principle of this BIST technique consists in generating a slow ramp signal on the ADC input and evaluating the time delay between two code transitions. As the input signal is linear, these time delays are proportional to the difference between two successive threshold voltages. The knowledge of all threshold voltages permits to determine some of most important ADC parameters. A more complete evaluation of the converter characteristics can be obtained by means of the histogram test method and BIST analyzers implementing this technique are presented in [5][6].

Concerning on-chip test stimulus generation, only a limited number of BIST solutions have been proposed. Original generators providing single or multi-tone analog signals are described in [7] to make frequency-domain

test of converters. Time-domain testing is addressed in [8][9] with solutions for generating a precise analog ramp signal.
The purpose of this work is to develop a linear analog signal generator used as stimulus generator in ADC testing applications. This generator will form part of a BIST structure to implement the histogram-based test technique. This technique is based on a statistical analysis of the ADC output code [10]. It is actually constituted of three steps. The first step consists in building the experimental histogram that represents the number of times each ADC output code appears for a given input signal. Then, this experimental histogram is compared with an ideal histogram obtained in the case of both ideal ADC and ideal analog input. Note that for a linear input signal this ideal histogram is perfectly flat due to the signal propriety. Finally, the main ADC parameters are extracted from the comparison with the two histograms.
The paper is organized as follows. Section 2 defines a classical example of experimental setup and details the generation requirements needed to ensure accurate ADC characterization. Section 3 recalls the adaptive ramp generator proposed in [11] and discusses the performances achievable using this kind of signal as stimulus for ADC testing. The principles of the triangle-wave signal generation are presented in section 4 and the need of self-calibration to take into account parameter fluctuations is shown. Section 5 discusses the performances of the proposed test generator in terms of slope precision and linearity of the generated signal. Finally, section 6 gives some concluding remarks.

2. Experimental Setup

*I*n the specific histogram-based BIST context, the analog stimulus should respect several constraints.
The first obvious constraint concerns the silicon area of the generator that should be minimal so that the total BIST architecture is economically viable.
The second constraint concerns the quality of the analog test signal. It should exhibit a quality exceeding that of the circuit under test, in order to not degrade the accuracy of the test technique. To illustrate this point, let us consider the example of non-linearity or gain error in the input signal. Applying this signal to a perfect converter, some variations in the code counts (see figure 1) appear in the measured histogram. Even if these variations are due to errors of the input signal, they will be interpreted as Integral Non-Linearity (INL), Differential Non-Linearity (DNL) or gain error of the ADC under test. Consequently, the accuracy of ADC parameter extraction directly depends on the quality of the input signal.

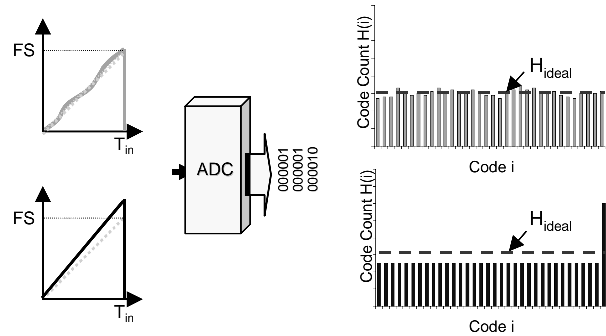

Figure 1. Influence of input signal errors on histogram

To summarize, the development of a test stimulus generator must be conducted with a special attention paid to the linearity and the amplitude of the generated signal while involving minimal silicon overhead.
As an illustration in this paper, we consider the following example of realistic experimental setup. The circuit under test is a 10-bit converter with 2V full-scale range and 20MHz clock rate. We want to perform the histogram test on this converter using 25711 samples collected on a linear input signal. The stimulus frequency is determined respecting the coherence sampling condition. For this specific application, the input signal frequency is set to 10.091kH.

3. Calibrated saw-tooth generator

3.1. Adaptive ramp generator principle

*A*n attractive and simple technique to generate a ramp signal consists in charging a capacitor C with a constant current Ic. The slope of the ramp is defined by the ratio Ic/C.
In order to achieve satisfactory test signal quality in terms of linearity, the authors have proposed in [11] a ramp generator based on a high swing current mirror. The generator presented in figure 2 has been implemented in CMOS 0.35µm technology.

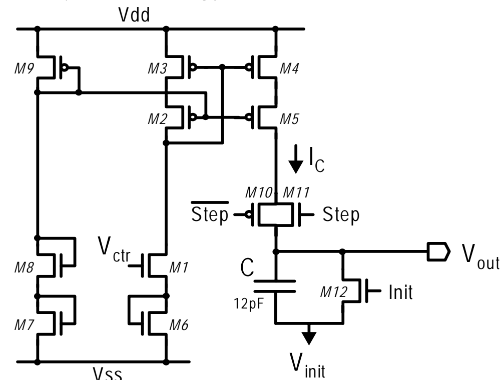

Figure 2. Schematic of the ramp generator

We obtain a ramp signal of 2V amplitude with a duration of 0.1ms and we measure a maximum INL of 60µV. This corresponds to a slope distortion lower than 0.003%. The basic ramp generator therefore exhibits good linearity performance. For illustration, such a good linearity allows the test of ADC up to 13 bits. Indeed, it is commonly accepted that the input stimulus applied on the ADC input should presents a resolution 2 bits higher than the converter resolution. So, expressing the ramp generator linearity in terms of resolution, we obtain linearity higher than 15 bits for the ramp generator (considering a 2V input range), which permits to test a 13-bit converter.
Unfortunately, the constraint of minimal silicon area overhead requires to use small charging current (Ic = 240 nA). Under these conditions, the slope of the ramp is very sensitive to the process variations. For instance, when we perform corner analysis (worst cases of the foundry model card) on our ramp generator, the ramp slope value can vary from 8V/ms to 41V/ms around the expected value of 20V/ms. It corresponds to a slope variation as high as hundred percent, which is clearly unacceptable for an analog test generator. The authors have therefore proposed an adaptive scheme to calibrate the ramp slope.
This adaptive scheme is based on a feedback loop that modifies the charging current according to the comparison between a reference voltage and the ramp amplitude at a fixed delay T_{in}.

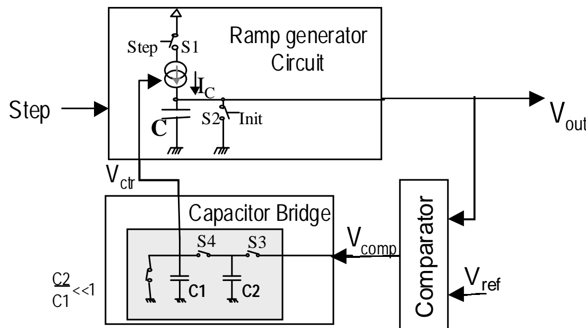

Figure 3. Adaptive ramp generator principle

Figure 3 shows the implementation of this adaptive scheme. The feedback circuitry simply consists of a capacitor bridge controlled by the comparator output. At each cycle the capacitor bridge adjusts the control voltage V_{ctr} of the current generator transistor according to the comparison result. The accuracy of the correction just depends on the capacitor ratio implemented in the capacitor bridge. In the present example, this original architecture can generate after calibration a ramp signal with a slope error lower than 0.6%. In addition our adaptive scheme has little influence on the linearity of the generated signal. Indeed we still obtain a linearity of about 15 bits. With this result we can expect to be able to test converter of 13-bit resolution.

3.2. Limitations

This section presents the limitations of the previously described calibrated ramp generator when used in practical context.
In the histogram test technique, a lot of samples are required to achieve satisfactory statistically results, this technique. All these samples cannot be taken at-speed on only one period. Hence, an analog pattern composed of several periods of ramp signal has to be defined. For instance, with a sample frequency of 20MHz and an input signal frequency about of 10kHz, thirteen periods of the analog input signal are required to collect 25711 samples. Figure 4 shows the obtained saw-tooth signal.

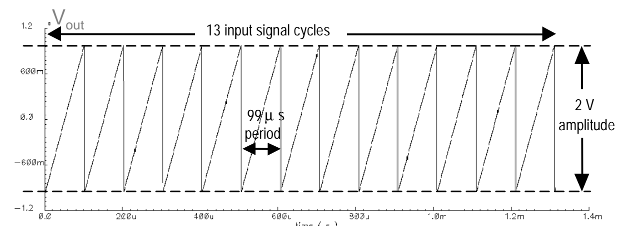

Figure 4. Simulation of an analog pattern for ADC testing

The main problem of this analog pattern arises from the initialization phases. Indeed, using several periods of the ramp signal involves that some samples might be collected in the initialization phase of the saw-tooth signal (see figure 5). These "parasitic" samples inevitably reduce the accuracy of the histogram-based test technique. Indeed, these samples modify the frequency distribution of ADC output code, resulting in a degradation on the accuracy of the extracted ADC parameters.

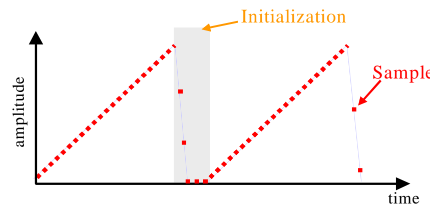

Figure 5. Parasitic samples taken on the saw-tooth signal

In order to evaluate this degradation, we have developed a program in *LABVIEW* that describes an ADC model and performs the histogram test technique on this ADC. Simulation results of our test pattern obtained with *Spectre* are applied on the input of an ideal ADC model, and the resulting histogram is processed to determine the equivalent non-linearity associated to the analog test pattern. For the specific example of this study we measure a maximum DNL value of 0.56LSB and a maximum INL value of 0.98LSB.
Expressing the INL result in terms of equivalent resolution, we obtain 10 bits. This value has to be compared to the equivalent resolution of a single ramp of 15 bits. We

observe degradation that limits the use of the saw-tooth generator to the test of converters with a resolution lower than 9 bits.
In order to increase our application field, it is interesting to investigate other kinds of analog linear stimulus. In particular, we focus on the development of a triangle-wave generator in order to avoid problems related to the initialization of the ramp signal.

4. Calibrated triangle-wave signal generator

4.1. Principe

*I*n the same way as for the ramp generator, a very simple approach to generate triangle-wave voltage consists in charging a capacitor with two opposite constant currents (I and –I).
In practice, we use two generators of I and –2I connected by a switch. This system allows a minimization of the parasitic effects due to commutations. The structure of this generator is presented in figure 6.

Figure 6. Triangle-wave generator

The switch S1 that connects the two current generators is controlled by the Schmitt trigger output with dynamic threshold voltages $\pm V_{TH}$ defined by the expression:

$$V_{TH} = \frac{Vsat \times R1}{R1 + R2}$$

The timing diagram of figure 7 illustrates the operating principle of generator. The first phase consists in initializing the output voltage at V_{init} through the switch S2. As V_{init} is lightly lower than the negative threshold voltage $-V_{TH}$, the comparator output is equal to the positive saturation voltage $+V_{sat}$ and the two generators are connected. Consequently, the charging current I_c is equal to +I and the generator produces a ramp with a positive slope. As soon as the signal amplitude reaches the positive threshold voltage, the comparator output switches to the negative saturation voltage and switches S1 off. Then, the capacitor is charged by a negative current –I and the signal slope is negative. In the same way, when the signal amplitude is equal to the negative threshold voltage, the comparator output switches and the slope of the signal becomes positive. As a result, the repetition of cycles gives a triangle-wave signal between the two threshold voltages $\pm V_{TH}$. Consequently, to generate a signal with amplitude A_{in}, V_{TH} is fixed at $A_{in}/2$.

Figure 7. Timing diagram of triangle-wave generation

Unlike the saw-tooth generator, this triangle-wave generator needs no initialization at each cycle. However because the triangle–wave generator is also based on simple ramp generators, the slopes of the generated signal are very sensitive to the process variations. To illustrate this point, figure 8 shows the maximum slope variations when we perform worst case simulations. Unlike the ramp generator, the variations affect the signal period instead of the signal amplitude that is fixed by comparator threshold voltages.

Figure 8. Influence of process variations on the signal

For the present application, these slope variations correspond to a period variation of 105%. It is clear that we have to reduce these variations in order to use the triangle-wave signal as analog stimulus for ADC testing.

4.2. Calibration

*T*o reduce influence of process variations we reuse the capacitor bridge previously developed for the adaptive ramp generator, but the operating principle is a little different than the one of calibrated ramp generator. Here, the idea is to precisely adjust the value of the 2I current generator so that one period of the triangle-wave signal is generated in a given time T_{in}. Consequently, the purpose consists in increasing (respectively decreasing) the slope of the positive slope ramp if the period of the triangle-wave signal is higher (respectively lower) than the reference value T_{in}.

In practice, the comparator output gives information on the sign of the signal slope at every moment. So, the observation of the comparator output allows us to deduce period of the generated signal. Indeed, suppose the triangle-wave signal period is higher than the reference one T_{in}. The generator has not enough time to generate a complete period. Consequently, after a time T_{in} the slope of the signal is negative and the comparator output is equal to the negative saturation voltage $-V_{sat}$. In the same way, if the period of the generated signal is lower than the expected one, after T_{in} the generator generates a positive slope ramp and the comparator output is equal to the positive saturation voltage $+V_{sat}$. In this context, we can insert the capacitor bridge in the structure so that it adjusts the positive slope through current generator polarization voltage V_{ctr} according to the value of the comparator output. The conceptual structure of the original adaptive triangle-wave signal generator is shown in figure 9.

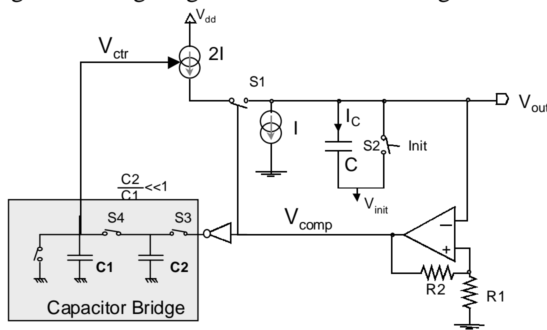

Figure 9. Adaptive triangle-wave generator

This adaptive triangle-wave generator operates according two different modes: a calibration mode and a normal triangle-wave signal generation mode.

In the calibration mode, the charging capacitor is initialized at every period T_{in}. Just before initializing the capacitor C, the capacitor C2 is pre-charged at the opposite value of comparator output V_{comp}. During the initialization phase of capacitor C, switch S3 is turned off and switch S4 is turned on. Then charge distribution between the 2 capacitors C1 and C2 increases or decreases the control voltage according to the sign of C2 charge. At a given iteration of the procedure the resulting control voltage is expressed as:

$$V_{ctrl}(i) \cong V_{ctrl}(i-1) \pm \Delta \qquad \text{(with } \Delta = \frac{C2}{C1} \cdot V_{sat}\text{)}$$

This expression clearly translates how, assuming a very low capacitor ratio, the control voltage is adjusted of a small increment Δ at each iteration.

As an illustration of the calibration procedure, we consider the case of an increase in the period of the triangle-wave due to process variations (see figure 10). The calibration procedure starts with a number of cycles in which the control voltage is progressively augmented of Δ at each iteration, until the signal period reaches the reference time T_{in} within the given amplitude $A_{in} = 2 \times V_{TH}$. Then, the control voltage oscillates around the proper value in the following iterations, indicating that the calibration is completed.

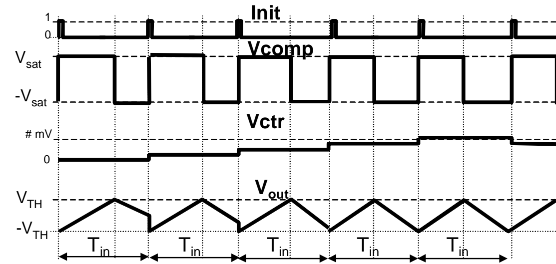

Figure 10. Timing diagram of the adaptive

Once the system is calibrated, we can then use the generator to deliver a triangle-wave signal by continuously iterating the process without any intermediate initialization step. In this case, the *Init* signal is maintained at logic 0 and switch S3 is continuously off.

Note that the correction does not permit to generate a symmetric triangle-wave signal because only one generated current is modified. In fact, it is not a problem because this generator is dedicated to an ADC BIST architecture able to implement histogram-based test technique. The measured histogram actually only depends on the period of the triangle-wave signal used as stimulus and not on the symmetry of the signal.

4.3. Performances and discussion

The auto-calibrated triangle-wave generator has been implemented in CMOS 0.35 technology using two high-swing current mirrors. In practice, the Schmitt trigger uses two precise external resistors. Moreover, in order achieve a very low capacitor ratio C2/C1 while maintaining a low silicon area, we suggest to use only the parasitic capacitors of the transmission gates operating as switches for C2 and we choose 10pF for C1 as illustrated in figure 11. The charging current and the charging capacitor are equal to 240nA and 6pF respectively.

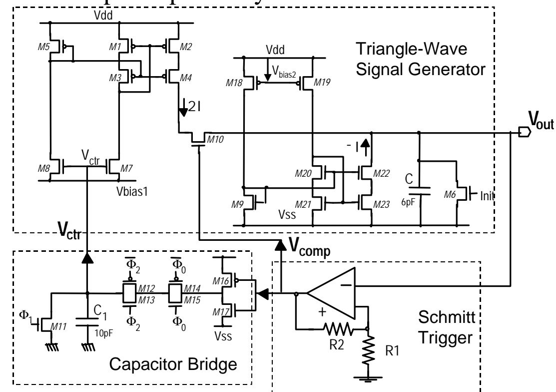

Figure 11. Adaptive triangle-wave generator schematic

Concerning the validation of the operating principle, figure 12 presents simulation results of the calibration phase. We can see that the triangle-wave period calibrates itself to the reference period in less than 10 cycles. Then, we have oscillations of the control voltage around -5mV with an amplitude less than 1mV. Measurements of period once calibrated reveal an average period error of 0.7%, which clearly demonstrates the effectiveness of the calibration scheme to correct the sensitivity of the ramp generator to process fluctuations.

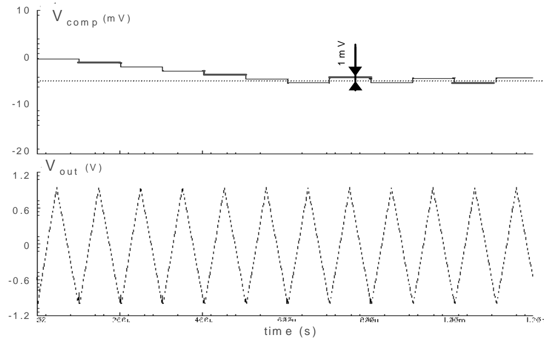

Figure 12. Simulation in calibration phase

Figure 13 presents simulation results in running phase with the same experimental setup: ADC sampling frequency of 20 MHz, histogram built on 27511 samples collected on the analog input signal. The test pattern is constituted by 13 periods of triangle-wave signal and T_{in} is equal 99µs. In this phase there is only one initialization phase at the beginning. After that, the generator is self-running.

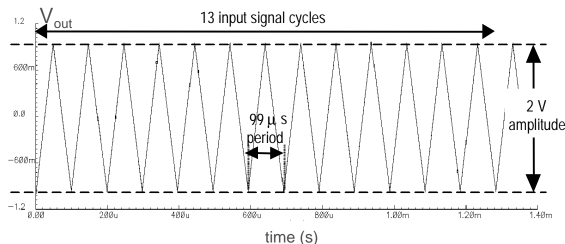

Figure 13. Simulation in running phase

Finally, we apply these 13 periods of the calibrated triangle-wave signal to the ideal converter model and we build up the corresponding histogram. From this histogram, we can now evaluate the DNL and INL seen through the "eyes" of the ADC. We measure a maximum DNL value of 0.14 LSB and a maximum INL value of 0.18 LSB. Consequently, the proposed auto-calibrated triangle-wave signal generator can be used in a BIST architecture dedicated to ADC with resolution lower than 12 bits.

5. Conclusion

In a histogram-based BIST context, this paper has presented two linear signal generators. Using high swing current mirror the ramp generator gives 60µV of non-linearity equivalent to 15bit resolution. In order to make this generator less sensitive to the process variation we have proposed an original adaptive scheme. Unfortunately for the histogram test technique, several successive periods of the signal are needed. Simply using the ramp signal in a saw-tooth generator, some "parasitic" samples collected in the initialization phase reduce the accuracy of the histogram technique. In order to avoid this drawback, we have proposed a second linear signal generator. This triangle-wave generator also needs adaptive circuitry to reduce the process variation sensitivity. However, due to the absence of initialization phase, the analog pattern built with this generator allows to optimize the histogram-based test capabilities.

6. References

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