BIOMEDICAL IC DESIGN

A Major Qualifying Project Report

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By

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Abstract

The purpose of this project was to begin the development and evaluation of a single channel electrophysiologic data acquisition system. The goal was to fabricate a bread board version of the system, develop an integrated circuit layout of the system, and develop a digital interface to the PC. The analog bread board was a single ended second order sigma-delta analog to digital converter and was digitally interfaced to the PC using a National Instruments Digital I/O board. A portion of the system, a switched-capacitor integrator which used a fully differential folded cascode op-amp, was designed using the NCSU 1.6μm process library in Cadence Virtuoso for the integrated circuit.

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1 INTRODUCTION

The goal of this project was to begin the development and evaluation of an electrophysiologic data acquisition integrated circuit proposed Edward Clancy, principal investigator and co-advisor. This IC would be one channel of *n* front end channels of the complete IC proposed. The system in this project would acquire various electrophysiological signals from the body, condition the signal, and then output a 1-bit digital signal with a resolution of 16-18 bits. The purpose of this project was to develop the layout of this system for an IC along with build an analog bread board version of the system for proof of concept and analysis. Along with the construction of an analog bread board version of the system this project also called for the development of the interface between the circuit and PC where the output signal from the system would be digitally filtered and evaluated. Typical electrophysiological signals that would be acquired from the system developed were:

- Heart (electrocardiogram [ECG]),
- Brain (electroencephalogram [EEG]),
- Skeletal muscles (electromyogram [EMG]),
- Peripheral nerves (electroencephalogram [ENG]),
- Eyes (electroneurogram [EOG]), and
- Smooth muscles of digestive system (electrogastrogram [EGG])

Table 1-1 shows typical amplitudes and frequency ranges of several biopotentials.

Biopotential	**Approximate Amplitude Range**	**Frequency Range**
Diagnostic |ECG|	1 mV	0.05-100 Hz
Surface |EEG|	100 μV	0.1-100 Hz
Needle |EMG|	1 mV	100-2000 Hz
Surface |EMG|	1 mV	20-500 Hz

Table 1-1: Typical amplitude and frequency ranges of several common biopotentials [Webster, 1998, p.259]

The challenge that emerges from acquiring electrophysiological signals from the body is the presence of a 60 Hz signal, several volts in magnitude, which is introduced to the body from power lines. The power line is common-mode interference when the electrophysiological signal is acquired from multiple electrodes. This interference is also several orders of magnitude greater than the desired signals, so it is imperative that the 60 Hz signal be eliminated. The biomedical IC design was to implement a second order sigma-delta analog to digital converter (Σ-Δ ADC) with a bipolar differential difference amplifier front end which would eliminate the unwanted 60 Hz signal. If the 60 Hz signal was not common-mode when acquiring the electrophysiological signal from multiple electrodes then there would be no need for the differential difference input. Since interference is common to multiple electrodes, but the electrophysiologic signal is not, it is necessary to have the differential difference front end. Another undesired characteristic that can occur when acquiring electrophysiologic data are offset potentials and low frequency motion artifacts, which if not eliminated could cause the amplifier to saturate which would distort the signal. Figure 1-1 is the block diagram of the single channel electrophysiologic data acquisition system proposed.

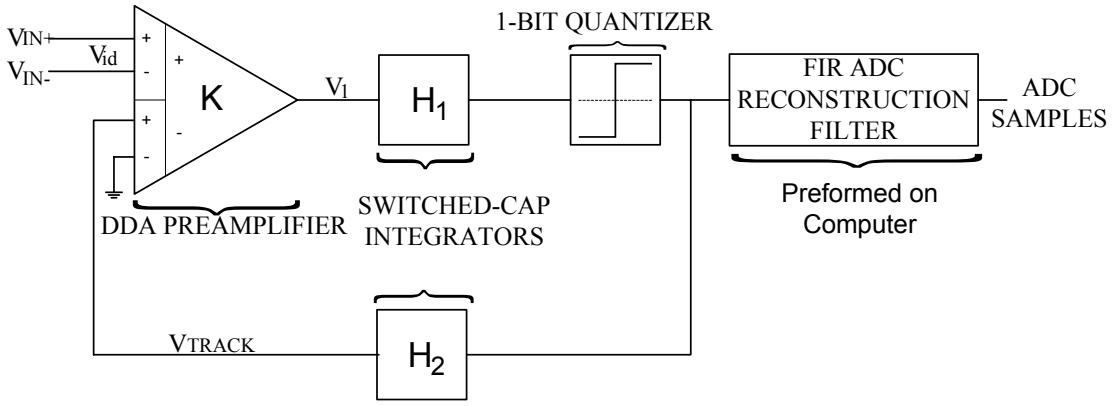


Figure 1-1: Σ-Δ ADC Block Diagram

From figure 1-1, V_{id} was the differential input voltage that would be acquired from bipolar electrode contacts from the body. The goal of the second order Σ-Δ ADC design was to be a bandpass system with selectable gain and frequency response based on the electrophysiological signals from table 1-1. Controlling the transfer functions H1 and H2

via switched capacitors would allow for the appropriate frequency response and gain for the various electrophysiological applications. Incorporating the feedback H2 of the second order Σ-Δ ADC, V_{TRACK} was the voltage from the 1-bit data stream (output of 1-bit quantizer) which would track any potential DC offset associated with the electrophysiological signals, subtracting it from the input signal. The finite impulse response (FIR) reconstruction filtering was performed, non-real time, on the PC using Matlab.

The format of this paper will be separated into two major sections, Analog Bread Board and Integrated Circuit Design, and will end with a conclusion of the project along with recommendations for future work on this system. The Σ-Δ ADC made up the heart of the electrophysiologic data acquisition circuit, so in order to gain a competent understanding of the ADC a first order system was first designed, analyzed, bread boarded, and then evaluated. After adequate evaluation of the first order Σ-Δ ADC the same steps where taken to develop a single ended second order Σ-Δ ADC, which made up the majority of the electrophysiologic data acquisition circuit from figure 1-1. Due to time constraints the differential difference amplifier was not implemented in the second order Σ-Δ ADC. The development of the first and second order Σ-Δ ADC is covered in the analog bread board section. The analog bread board section also covers the interfacing between the Σ-Δ ADC circuit and the computer, along with the design and implementation of the FIR reconstruction filtering preformed on the PC.

As for Integrated Circuit design, building a simple fully differential single output op-amp to obtain basic understanding and knowledge; then base on the performance and results of the op-amp, a more complicated fully differential op-amp with dual outputs will be implemented. After that it will be modified to handle 16 bit resolution ADC output and rejecting low frequency noise that would meet the project requirement. After the completion of designing the op-amp, switched-capacitor integrator will be implemented on top of the op-amp, and it will be the component that would suitable for first and second order Σ-Δ ADC; then the layout design for fabrication process will be implemented based on the schematic design. If it passes the simulation test, then it will be sent to fabrication laboratory to have the chip fabricated.

2 ANALOG BREAD BOARD

The goal for part of this project was to have an analog bread board version of a single-ended input second order Σ-Δ ADC to provide adequate proof of concept of the system proposed. The initial design of the system was have a dual-ended differential difference amplifier input to a second order Σ-Δ ADC, but due to time constraints it was decided to omit the differential difference amplifier to allow for a more complete analysis of the second order Σ-Δ ADC. To develop a second order Σ-Δ ADC the complete design was taken in steps, progressively becoming more complex. The first step was to develop a single-ended input Σ-Δ ADC with a first order integrator for H1, replacing H2 with a shorting wire and resistor matching the input resistor which become the RC time constant of H1. The first order system can be represented as H1 and the 1-bit quantizer with feedback loop from figure 1-1. From the analysis techniques developed through the evaluation of the first order Σ-Δ ADC, the next step was to develop a single ended input second order Σ-Δ ADC introducing H2 as an integrator op-amp into the feedback loop. The second order system can be represented as H1, the 1-bit quantizer, and H2 in the feedback loop from figure 1-1. To analyze the output data from the first and second order Σ-Δ ADC a digital I/O board (NI PCI-6533) from National Instruments was used to acquire the 1-bit stream of data produced from the ADC and saved as a binary file. Matlab was then used to design and perform the FIR reconstruction filtering and analysis of the binary files.

The analog bread board portion of this report is broken down into design and analysis, implementation, and concludes with results. The design and analysis covers the first and second order Σ-Δ ADC along with the FIR filter design. The first part of the design and analysis will cover the first order Σ-Δ ADC. It will begin with an overview of the first order Σ-Δ ADC followed by a DC analysis and then a frequency analysis of the first order system. It was important to perform a DC analysis in order to determine the necessity of a linear of the system. The linearity of the system discussed in this section implies that if a DC voltage is applied to the Σ-Δ ADC then the average value of the output should follow the input voltage. If the system does not produce a linear output following a DC input then when a signal is passed through the Σ-Δ ADC it can produce harmonics of that signal making it difficult to acquire an accurate reading of the input

signal. The DC analysis will cover the importance of a linear system along with determining where a potential DC offset would stem from the first order system. The next section, frequency analysis, covers the important development of a linear model technique for the system in order to derive the transfer functions of the system. The transfer functions acquired from this analysis serve as an important characteristic of the Σ-Δ ADC which demonstrates how the input signal will be passed through the system and the quantization noise associated with ADCs will be pushed into the higher frequency band. As mentioned in the introduction, the design of the biomedical data acquisition system was to be a bandpass system with selectable frequency response via switched capacitors. The frequency analysis of the first order Σ-Δ ADC will demonstrate how the breadboard version of the Σ-Δ ADC systems did not have selectable frequency response but develop the techniques required to determine the frequency response of the second order Σ-Δ ADC. The analysis of the first order Σ-Δ ADC is then followed by the design and analysis of the second order Σ-Δ ADC.

The second order Σ-Δ ADC begins with an overview of the system and then moves to a frequency analysis of the system. From the techniques acquired from the first order Σ-Δ ADC of developing a linear model of the system to analyze the frequency response of the Σ-Δ it will be shown that the second order system was a bandpass system that rejected DC offset. After the design and analysis of the first and second order Σ-Δ ADCs is the design of the FIR reconstruction filter. The FIR section will cover the design of the lowpass filter implemented in Matlab. Following the design and analysis of the systems and FIR filter is the implementation section. The implementation section covers how the first and second order Σ-Δ ADCs where bread boarded along with how the output of the systems where acquired and evaluated on the PC. Following the implantation section is the results.

The results will cover the DC evaluation of the first and second order Σ-Δ ADCs, FIR filter implementation, second order Σ-Δ ADC frequency response, nonlinear least-squares curve fitting, and signal to noise and distortion ratio (SNDR). The DC evaluations will cover the results of passing DC signals, covering the input voltage range of the systems, through the Σ-Δ ADCs and obtaining a plot of the input versus the output

DC values. The results of the DC evaluation are important to determine the linearity of the Σ-Δ ADCs systems.

The FIR filter implementation section will demonstrate how the FIR lowpass filter was used to eliminate the high frequency quantization noise in order to reconstruct the digital signal. The second order Σ-Δ ADC frequency response compares the measured frequency response of the system to the theoretical frequency response to demonstrate how the system follows the theory in the second order Σ-Δ ADC frequency analysis. The nonlinear least-squares curve fitting section will show how a sine wave was fit to the reconstructed digital signal, sine waves where used for testing purposes, to obtain the amplitude and frequency of the digital signal. The measurements of the amplitude and frequency obtained from the curve fitting technique allowed for the comparison of the digital signal to the analog input signal to determine the accuracy of the Σ-Δ ADCs. From the curve fitting technique an error plot was also obtained, the difference between the best fit sine wave and the reconstructed sine wave, which was useful information in determining the signal to noise and distortion ratio (SNDR) of the system. The SNDR section uses the error plot data to evaluate different aspects of the SNDR of the first and second order Σ-Δ ADCs.

2.1 Design and Analysis

This section will go through the design and analysis of the first and second order Σ-Δ ADC. It will begin with the first order Σ-Δ ADC and then build on the concepts of the analysis to work its way up to the more complex second order Σ-Δ ADC. The Design of the FIR reconstruction filter will also be covered. From the design and analysis the implementation of the systems will be covered followed by the evaluation of the systems.

2.1.1 First Order Sigma Delta Analog to Digital Converter

The first step to building up to a second order Σ-Δ ADC was to first breadboard and analyze a first order Σ-Δ ADC. Building up a first order Σ-Δ ADC as a first step allowed for the development of the analytical techniques need to be applied to the second order Σ-Δ ADC. Figure 2-1 is a block diagram of the first order Σ-Δ ADC used.

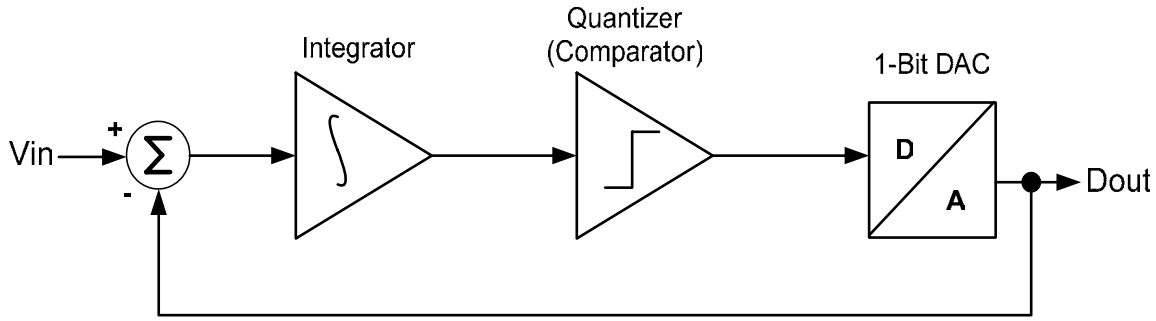


Figure 2-1: First Order Σ-Δ ADC Block Diagram

The input signal, *Vin*, came into the Σ-Δ ADC through a summing junction and was then passed through an integrator. The signal then went through a comparator which acted like a 1-bit quantizer. The 1-bit quantized signal was then passed through a two stage 1-bit digital to analog converter which was the output, *Dout*. The DAC acquired a sample of the output of the comparator on every positive edge of an external clock and produced a 1-bit stream of data that ranged between its positive and negative reference voltages. The output of the 1-bit DAC was also fed back to the summing junction where it was subtracted from the input. "This feedback forces the average value of the quantized signal to track the average input. Any difference between them accumulates in the integrator and eventually corrects itself" (Candy, p.3). Since the output of the Σ-Δ ADC was a 1-bit stream of data which average value represented the input signal it did not directly represent the input signal. To acquire an accurate digital representation of the

input signal the output was be passed through a reconstruction filter which is shown as part of the block diagram in figure 1-1. The reconstruction filter for this application was a finite impulse response (FIR) lowpass filter preformed on the PC, which will be discussed in further detail in the FIR filter section. What was being filter was the high frequency quantization noise of the Σ-Δ ADC. The quantization noise is the difference between the input signal and the 1-bit feedback signal and can also be described as the "round-off" error that accompanies the quantization of an analog signal (Jarman, p.1). In order to shape or push the quantization noise to a higher frequency band to allow for reconstruction filtering the Σ-Δ ADC was sampled at a frequency much higher then the input frequency bandwidth, which is called oversampling. Both the first and second order Σ-Δ ADC used the technique of oversampling. The oversampling can be quantized as a ratio or the oversampling ratio (OVSR) which is given in equation 2-1 where *fs* is the sampling frequency and *fb* is the input signal bandwidth.

$$OVSR = \frac{f_s}{2 f_b} \qquad \textit{eq) 2-1}$$

The effects of shaping the quantization noise will be discussed further in the linear model and analysis section.

From discrete components, a first order Σ-Δ ADC was bread boarded, as shown in figure 2-2. The integrator was a LF356 op-amp with a 1000pF capacitor in its negative feedback path. The quantizer was a LM311 comparator, and the 1-bit DAC was half of a 74HC74 d-flip-flop. The d-flip-flop was clocked with a MTRON 81-14 1 MHz crystal oscillator.

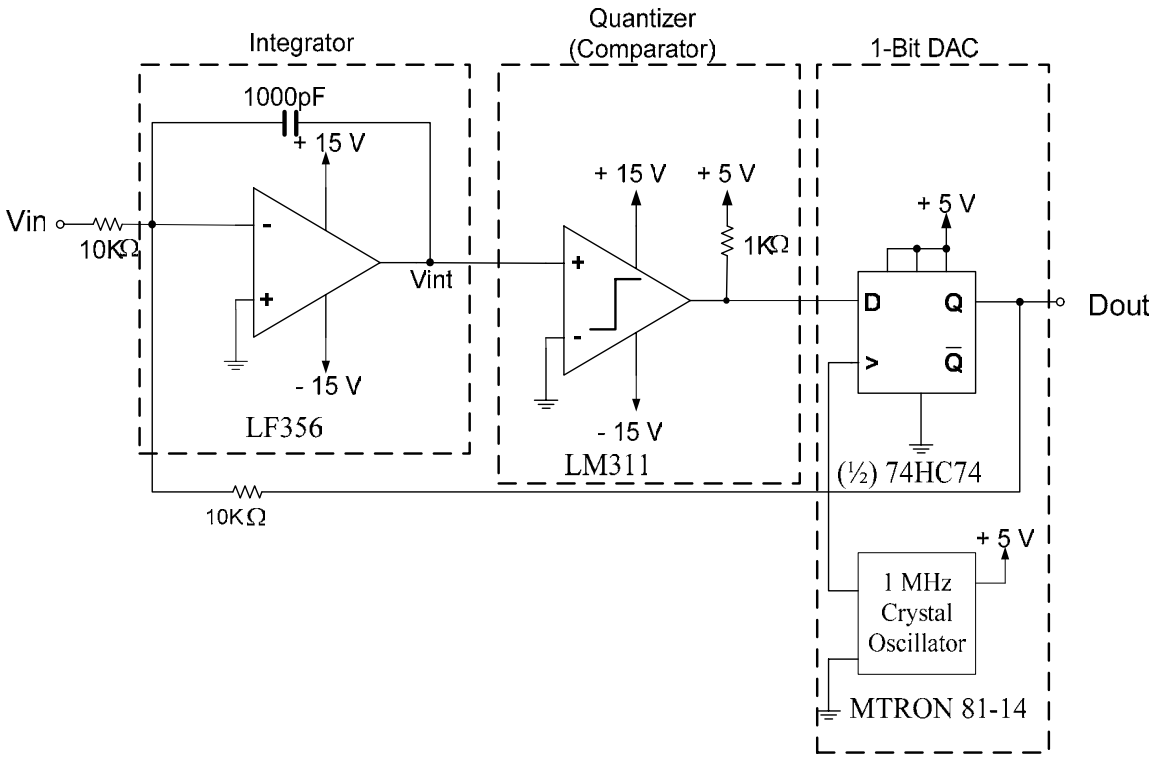


Figure 2-2: Schematic of First Order Σ-Δ ADC

The comparator quantized the signal to a 1-bit stream of data which was represented as 0 and 5 volts. The d-flip-flop then sampled the output of the comparator at the 1 MHz clock frequency and produced a 1-bit stream of data also ranging from 0 to 5 volts. In order to balance the input signal, V_{in}, to have an average value of zero from the feedback loop the input voltage range was between 0 and -5 volts. The following sections will go into more detail on the DC and frequency analysis of the first order Σ-Δ ADC.

2.1.1.1 DC Analysis

It was important as a first step to perform a DC analysis of the first order Σ-Δ ADC to determine the importance of a linear of the system. If the system was not linear it could produce harmonics of the input signal, making it difficult to obtain an accurate reading from the output. A plot of the output voltage versus the input voltage of an ideal Σ-Δ ADC shows a perfectly linear line that passes through the origin, which is represented in figure 2-3 A as the ideal case.

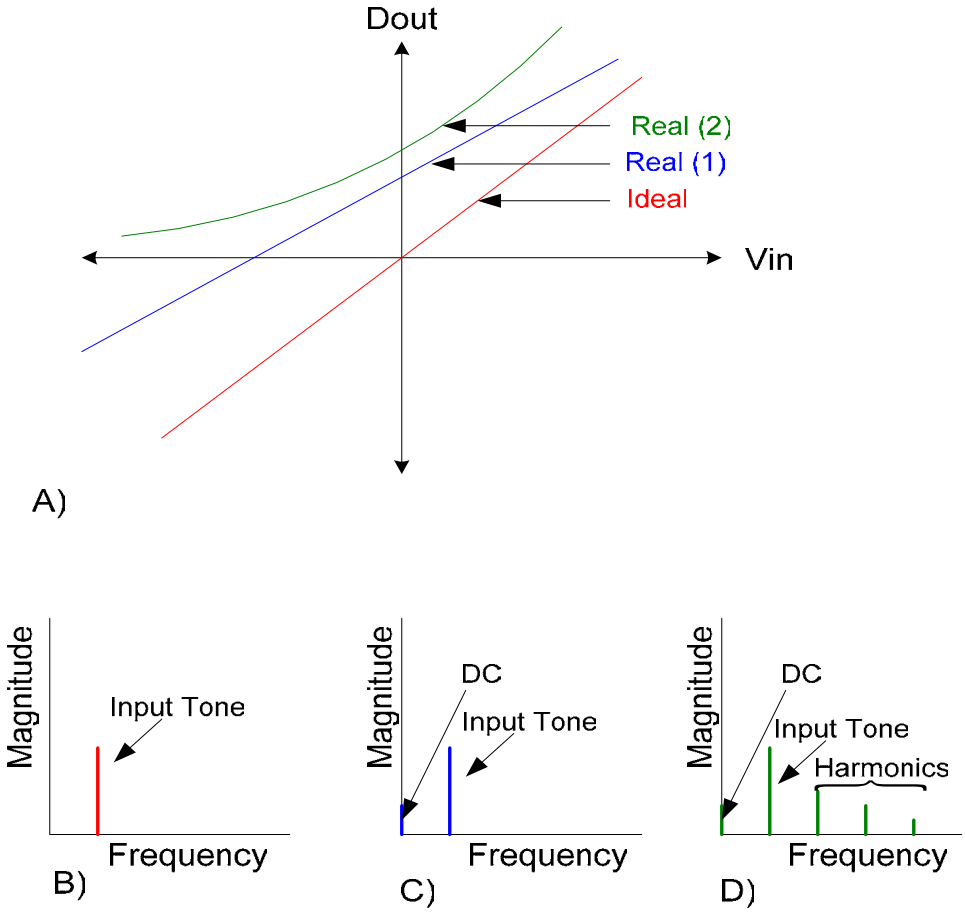


Figure 2-3: A) Dout vs Vin of an Ideal Σ-Δ ADC, and two cases of a real Σ-Δ ADC B) Magnitude Response of FFT of an Ideal Σ-Δ ADC C) Magnitude response of the FFT of Real Case 1 D) Magnitude Response of FFT of Real Case 2

Figure 2-3 A also represents a real case, real (1), of an Σ-Δ ADC where the output voltage, Dout, versus the input voltage, Vin, is linear but has a DC offset. The second real case of an Σ-Δ ADC, real (2), shows a nonlinear system that has a DC offset, also depicted in figure 2-2 A. Figure 2-3 B shows the output magnitude response of the FFT

of an ideal Σ-Δ ADC in which a sine wave was the input. From this figure it can be seen that passing a sine wave through the Σ-Δ ADC produces a single input tone at the frequency of the input sine wave. Figure 2-2 C depicts the output magnitude response of the FFT of the real case 1 of the Σ-Δ ADC, using the same sine wave input example. From this figure it can be seen that due to the DC offset there will be a tone at DC along with the input tone of the input sine wave. Figure 2-3 D shows the second real case of the magnitude response of the FFT, also the same input sine wave. The second real case shows that since the system is nonlinear with a DC offset there will be a term at DC, a tone at the input sine wave's frequency, along with harmonics from the signal. When this system is implemented to acquire electrophysiologic data it would be inappropriate if it was nonlinear and produced harmonics of the input signal, as in the real case 2. If the system produced harmonics of the input signal there would be no way of accurately interpreting the acquired data. It was acceptable for the system to have a DC offset, as in real case 1, because the data acquisition system was a second order Σ-Δ ADC in which the feedback loop tracks any DC offset and subtracts it from the input signal. The second order Σ-Δ ADC will be explained further in following sections. It is now appropriate to analyze the first order Σ-Δ ADC to determine where a potential DC offset could originate.

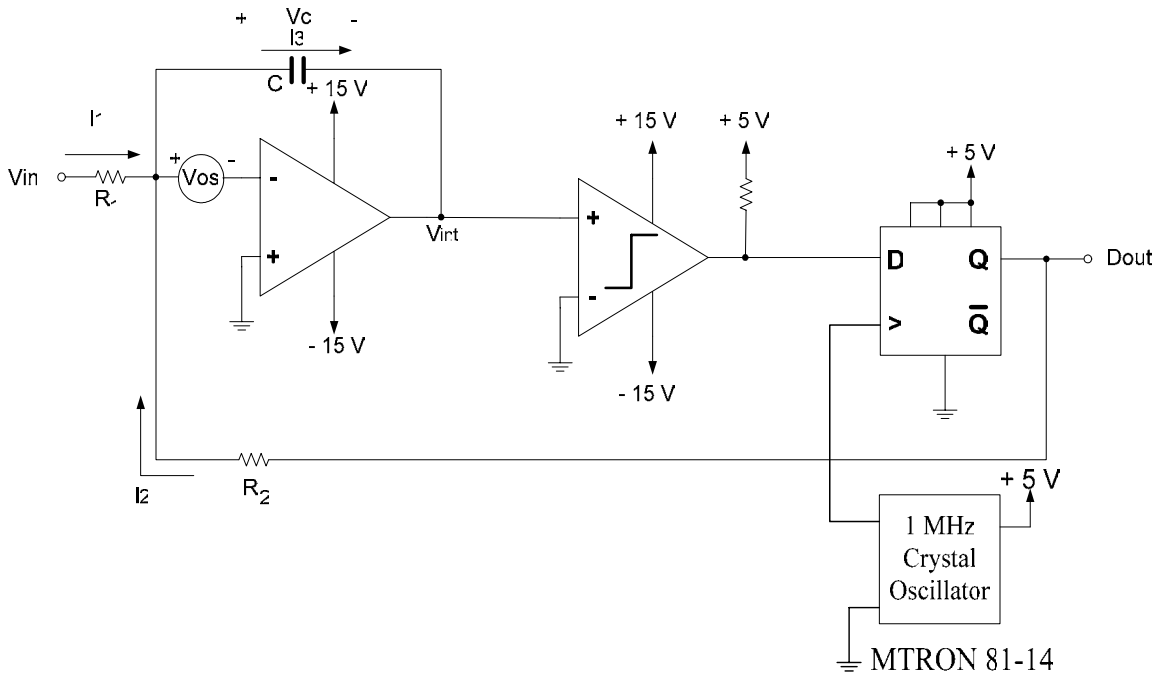


Figure 2-4: First Order Σ-Δ ADC

To explain why the first order Σ-Δ ADC would have a DC offset it was necessary to take a closer look at the circuit itself, figure 2-4, and derive an equation for V_{int} in terms of V_{in} and D_{out}. It should be noted that this derivation introduced an offset voltage, V_{os}, at the negative input of the op amp integrator as a way of modeling the op amp more accurately. The reason for introducing V_{os} was because of imperfections of the op amp used, that is the voltage between the + and – inputs were not a perfect virtual ground as implied by an ideal op amp and would possibly obtain a slight offset voltage. The first step in the derivation of V_{int} was to use KCL, assuming an ideal op amp, to obtain an equation for $I_3(t)$ in terms of $I_1(t)$, and $I_2(t)$, refer to figure 2-4. The equation for $I_3(t)$ was depicted in equation 2-2.

$$I_3(t) = I_1(t) + I_2(t) \qquad \textit{eq) 2-2}$$

From Ohm's law, assuming stable feedback and the polarity of *Vos*, an equation for $I_1(t)$ was derived in terms of the input voltage, offset voltage and R1.

$$I_1(t) = \frac{V_{in}(t) - V_{os}}{R_1} \qquad \textit{eq) 2-3}$$

Derived in the same manner equation 2-4 was of $I_2(t)$ in terms of the output voltage, offset voltage and R2.

$$I_2(t) = \frac{D_{out}(t) - V_{os}}{R_2} \qquad \text{eq) 2-4}$$

Substituting equations 2-2 and 2-3 into equation 2-2, $I_3(t)$ could be rewritten as:

$$I_3(t) = \frac{V_{in}(t) - V_{os}}{R_1} + \frac{D_{out}(t) - V_{os}}{R_2} \qquad \text{eq) 2-5}$$

The next step was to find an expression for voltage across the capacitor of the integrator op amp, $Vc(t)$, which could be expressed as follows:

$$V_c(t) = \frac{1}{C}\int_{t1}^{t} I_3(t)dt + V_c(t_1) \qquad \text{eq) 2-6}$$

It should be noted that in equation 2-6 the initial voltage on the capacitor, $V_c(t_1)$, was disregarded because this was a steady state analysis and the initial voltage on the capacitor was not of importance. It could then be said that $-Vos + Vc + Vint = 0$ so the equation for $Vint(t)$ could be written as:

$$V_{int}(t) = \frac{1}{C}\int\left[-\left(\frac{V_{in}(t) - V_{os}}{R_1}\right) - \left(\frac{D_{out}(t) - V_{os}}{R_2}\right)\right]dt \qquad \text{eq) 2-7}$$

This equation for $Vint(t)$ alone did not explain why the slope and offset were not ideal, to obtain this information it took a little more analysis. Since the concern of this analysis was how this circuit would perform during testing it could be said that $Vint(t)$, on average, was equal to zero. The reason $Vint(t)$ was zero on average was because the output's, *Dout*, average value was equal to the input voltage, *Vin*, which was subtracted from the input through the feedback loop. The subtraction of the output from the input made the average voltage saw on the input of the op amp zero which made the average of *Vint* equal to zero as well. This being the case it could then be said that the total integrand must then equal zero on average. By setting the integrand to zero an expression for *Dout* could then be determined as follows:

$$-\left(\frac{V_{in}(t) - V_{os}}{R_1}\right) - \left(\frac{D_{out}(t) - V_{os}}{R_2}\right) = 0 \qquad \text{Eq) 2-8}$$

$$\frac{-V_{in}}{R_1} + \frac{V_{os}}{R_1} - \frac{D_{out}}{R_2} + \frac{V_{os}}{R_2} = 0 \qquad \text{eq) 2-9}$$

$$-\frac{R_2}{R_1}V_{in} + \frac{R_2}{R_1}V_{os} - D_{out} + V_{os} = 0 \qquad \text{eq) 2-10}$$

From here the expression for *Dout* could be written as shown in figure 2-5:

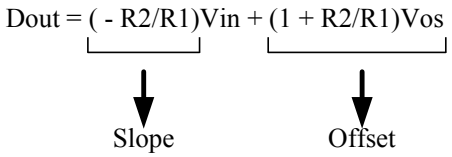


Figure 2-5: Dout Equation

As can be seen from figure 2-5 *Dout* was equal to *Vin* times some constant value plus some offset voltage. Obtaining the formula for *Dout* now allowed the slope to be interpreted as *(-R2/R1)* and the offset as *(1 + R2/R1)Vos*. This conclusion showed that due to the imperfections of the op amp used in the first order Σ-Δ ADC the system obtained an initial DC offset. The linear testing of this system will be presented in the DC evaluation of the first order Σ-Δ ADC in the results section. The following section will analyze the frequency characteristics of the first order Σ-Δ ADC.

2.1.1.2 Frequency Analysis

The next stage of analysis was to investigate the frequency characteristics of the first order Σ-Δ ADC. In order to analyze the first order Σ-Δ ADC in the frequency domain a linear model of the system needed to be developed. The Op amp, which was set up to be an integrator with feedback capacitor, C, and resistors, R1, could be modeled directly as a linear system. The comparator and d-flip-flop produce quantization noise which is the "round-off error that occurs when an analog signal is quantized"(Jarman, David p.1). The quantization noise could be assumed to be random so it is commonly treated as white noise (Jarman, David p.1). Due to the quantization noise produced by the comparator and d-flip-flop they could not directly be modeled as a linear system. There are, however, techniques that have been developed to linearize this portion of the Σ-Δ ADC. Utilizing the "input-independent additive white-noise approximation" of the quantization error, one can get the approximate linear model of the original nonlinear circuit (Norsworthy, Sec. 2.3). Figure 2-6 shows how the first order Σ-Δ ADC was modeled as a linear system.

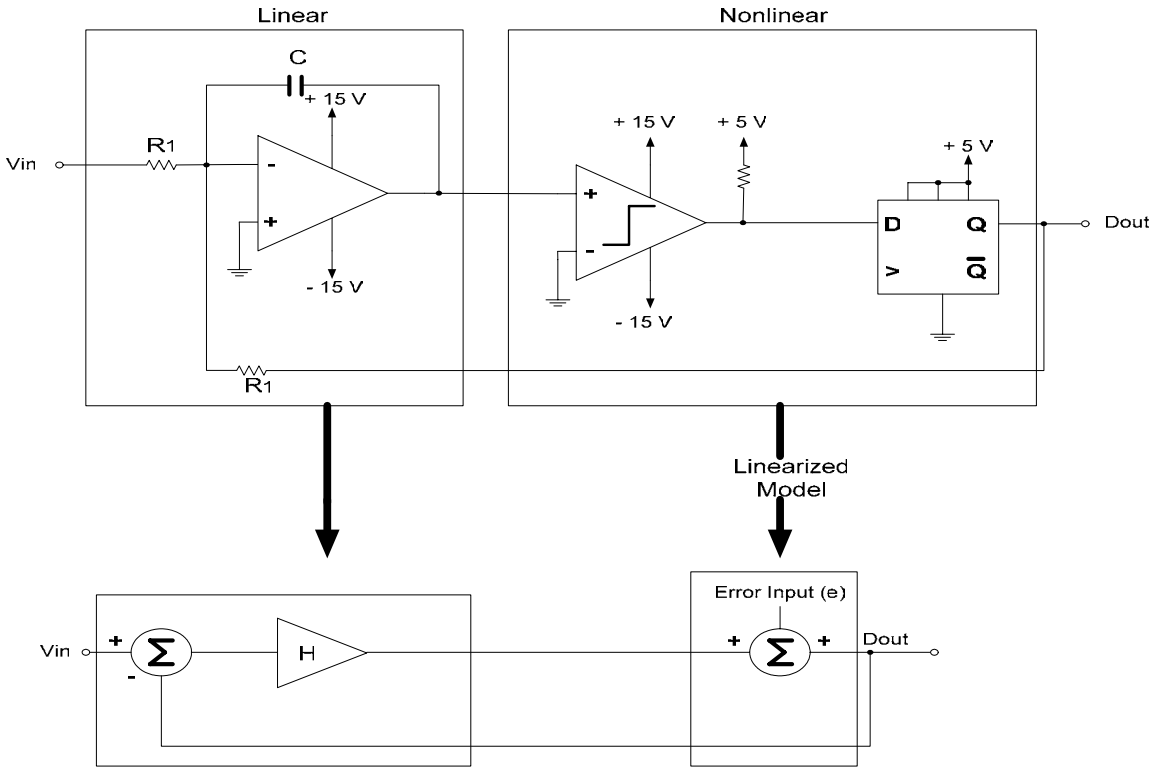


Figure 2-6: Linear Model of first order Σ-Δ ADC

Figure 2-6 shows that the integrator op amp was modeled as a filter with transfer function H = 1/sτ. For the transfer function of the integrator τ was the time constant which was equal to R_1*C. The effect of the comparator and d-flip-flop were modeled as additive noise or an error input. The linear model allowed the additive noise, error input (*e*), to be treated independently from the input, *Vin*, as shown in figure 2-6. From this linear model developed the frequency response of the system could then be determined. To begin the frequency analysis an equation for *Dout* was determined; starting at *Vin* which was added to a negative *Dout* and was then multiplied by *H* and then added to the error insertion. This could be represented as follows:

$$D_{out} = e + H(V_{in} - D_{out}) \qquad \textit{eq) 2-11}$$

Multiplying through by *H* and brining *H*Dout* to the left hand side to factor out *Dout* yielded the equation:

$$D_{out}(1 + H) = e + HV_{in} \qquad \textit{eq) 2-12}$$

Simplifying the above equation yielded:

$$D_{out} = V_{in}\left(\frac{H}{1+H}\right) + e\left(\frac{1}{1+H}\right) \qquad \textit{eq) 2-13}$$

Setting *e=0* and solving for *Dout/Vin* resulted in the following:

$$\frac{D_{out}}{V_{in}} = \frac{1}{1+H} \qquad \textit{eq) 2-14}$$

Equation 2-14 above is Signal Transfer Function (STF) of the system. Now in a similar manner by letting *Vin=0* and solving for *Dout/e* yields the Noise Transfer Function (NTF) of the system:

$$\frac{D_{out}}{e} = \frac{H}{1+H} \qquad \textit{eq) 2-15}$$

Substituting *1/sτ* for *H*, the transfer function of the integrator op amp configuration, into the NTF and STF equations gave:

$$NTF = \frac{s\tau}{1+s\tau} \qquad \textit{eq) 2-16}$$

$$STF = \frac{1}{1+s\tau} \qquad \textit{eq) 2-17}$$

This indicates that the system acted like a highpass filter for the noise and a lowpass filter for the signal. Figure 2-7 is a matlab log-log plot of the theoretical magnitude response of the STF and NTF for the first order Σ-Δ ADC constructed.

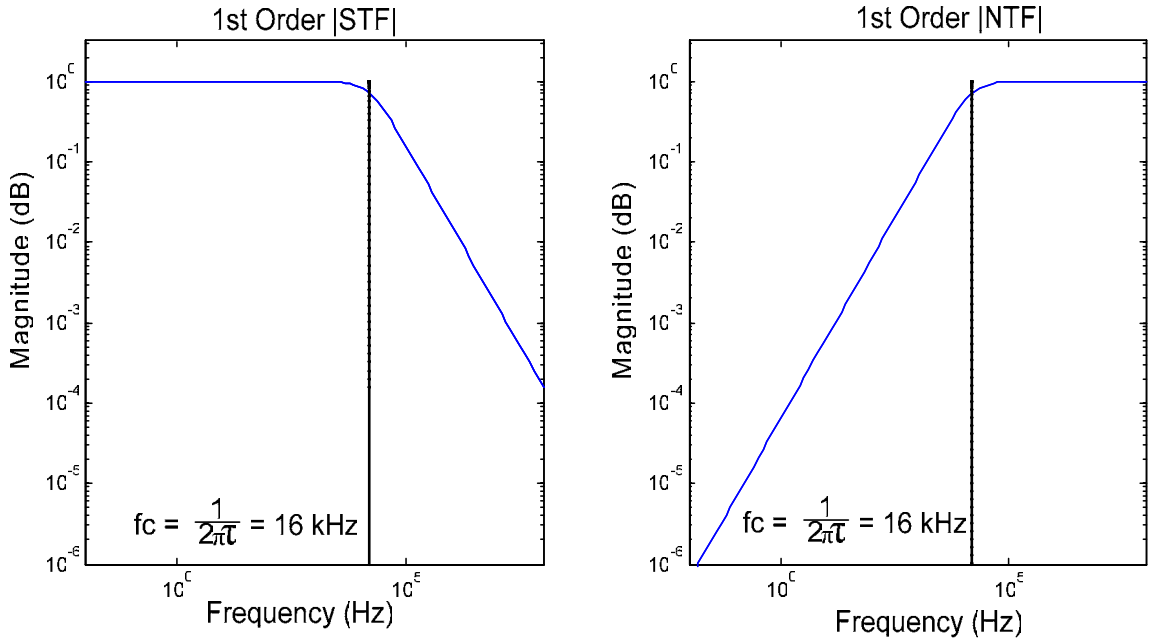


Figure 2-7: First Order STF & NTF Magnitude Response

Note that the cutoff frequency (*fc*) was represented by:

$$fc = \frac{1}{2\pi\tau} \qquad \textit{eq) 2-18}$$

Substituting the values for *R1*, 10kΩ, and *C*, 1000pF, for τ and solving for the cutoff frequency for this system yielded 15915 Hz ≈ 16 kHz. It can be seen that the cutoff frequency, *fc*, is much higher then any of the frequency bands of the electrophysiological signals from table 1-1. The cutoff frequency was chosen to be much higher to assure no attenuation of the input signal.

Another way to examine the effects of the STF and NTF was to look at the power spectrum of the input signal, *Vin*, and the quantization noise, *e*. Figure 2-8 depicts how the effects of the STF and NTF were seen only by the input voltage and quantization error respectively. Part A shows how a sine wave input signal is ideally a single impulse and the quantization noise is white noise. In this same part it also shows how these signals are passed though the STF and NTF. Part B shows how the impulse from the input signal is passed and how the white noise takes on the frequency response of the

high pass filter from the NTF. The effect of the NTF is considered to shape the white noise, which pushes it out to the higher frequency bands. Part C shows how when these two signals are combined at the output *Vin* is left intact and unpolluted from the quantization noise, but how there are still high frequency components that need to be digitally filtered out for a completely clean signal in a given bandwidth.

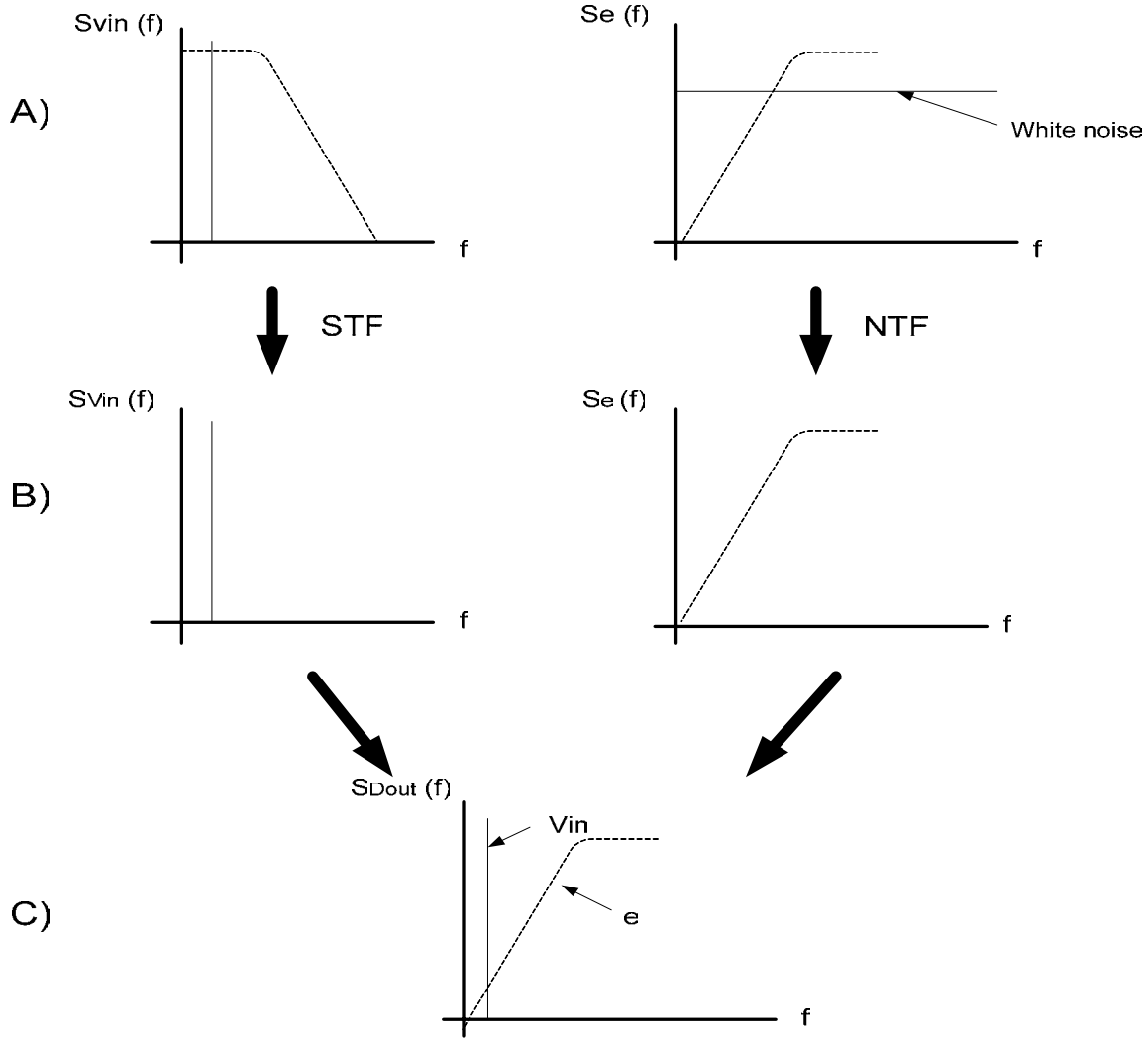


Figure 2-8: Power Spectrum Response of NTF & STF

This analysis showed how the frequency response of an Σ-Δ ADC passed the frequency band of interest, while pushing the quantization noise into the higher frequency band. It could be seen that by changing the values for R1 and C, the cutoff frequency for the STF and NTF could be designed to accommodate the input frequency band of interest. This concept is what will allow the final implementation of the data acquisition

system to have programmable frequency bandwidths by controlling the R1 and C equivalents with switched capacitors.

2.1.2 Second Order Σ-Δ ADC

The second order Σ-Δ ADC was very similar to the first order Σ-Δ ADC with the introduction of an additional integrator op-amp in an additional feedback loop. This additional feedback loop was taken from the inverting output of the d-flip-flop, $\overline{Q}$, and fed back to the summation node of the first integrator. Both of the op amp integrator's positive inputs were set at +2.5 V which set the maximum usable range of the input signal to be between 0 and 5 V. Figure 2-9 is the schematic of the second order Σ-Δ ADC.

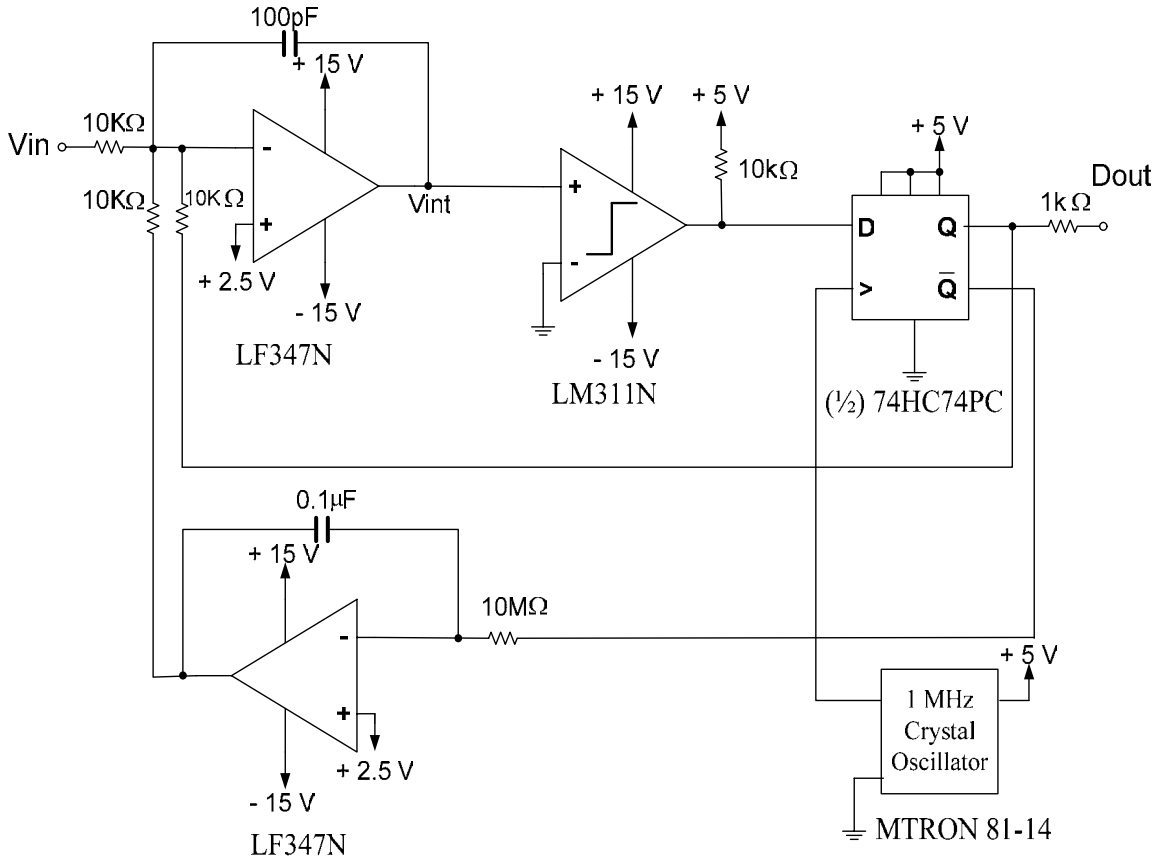


Figure 2-9: Second Order Σ-Δ ADC Schematic

The second order Σ-Δ ADC operated very similarly to the first order Σ-Δ ADC and it could be seen that by breaking the op amp feedback loop and setting the positive input of the op amp in the front end back to ground you would be left with the first order Σ-Δ ADC with a different RC time constant. The introduction of the feedback op amp was an integral part of the design for the acquisition of electrophysiologic data. As

mentioned in the introduction there can be motion artifacts and DC offsets associated with electrophysiologic data that must be eliminated so as not to saturate the op amp to its positive rail and allow proper amplification of the signal, if necessary, with out distortion. The purpose of the op amp in the feedback loop was to track any DC offset present in the input signal, *Vin*, and subtract it from the input signal. The output of the feedback op amp took on any value it needed to in order to have all of the DC current associated with the input signal run through the 10 kΩ at the output of the feedback op amp; thus allowing the input signal to be centered around 2.5 V at the input of the front end op amp. The maximum input range of the system was 0 to 5 volts because like the first order Σ-Δ ADC the output of the d-flip-flop balanced the input so on average it is zero. Since the output range of the d-flip-flop is 0 to 5 volts if the input voltage exceeded that limit then the output could no longer balance it to average to zero. The following section will cover the frequency analysis of the second order Σ-Δ ADC. The analysis will show how the second order Σ-Δ ADC was a bandpass system as mentioned in the introduction along with illustrating how the feedback op amp rejected any DC offset.

2.1.2.1 Frequency Analysis

Similar to the first order Σ-Δ ADC it was beneficial to represent the Σ-Δ ADC as a linear model in order to analyze the frequency response of the signal transfer function (STF), noise transfer function (NTF), and with the second order Σ-Δ ADC the feedback transfer function (FTF) of the feedback integrator. Figure 2-10 was the linear model for the second order Σ-Δ ADC. It should be noted that the "input-independent additive white-noise approximation" was used to derive a linear model for the second order Σ-Δ ADC (Norsworthy, Sec. 2.3).

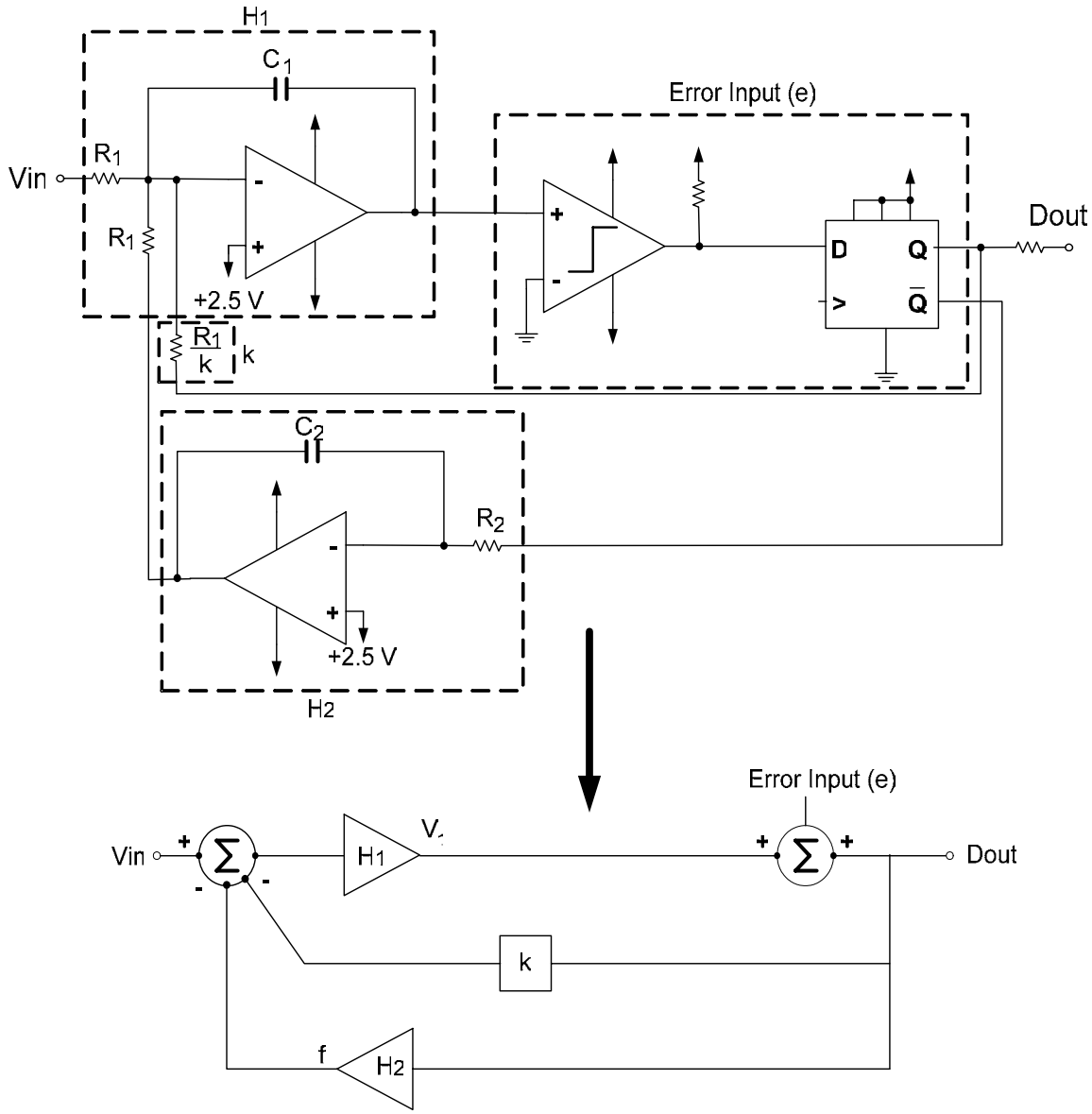


Figure 2-10: Second Order Σ-Δ ADC Linear Model

The linear model was comprised of a summation node at the input, H_1 which was the transfer function of the first integrator ($\frac{1}{s\tau_1}$), summation node of the error insertion from the comparator and d-flip-flop, a feed back constant *k*, and a feed back transfer function H2 ($\frac{1}{s\tau_2}$) from the second integrator in the feedback loop. These were the same H1 and H2 depicted in figure 1-1 of the block diagram of the data acquisition system. The first step in deriving the STF and NTF was to derive an equation for V_1, the voltage at the output of the integrator with transfer function H_1. This can be seen by equation 2-19.

$$V_1 = \frac{-1}{s\tau_1}(-V_{in}) + \frac{-1}{s\tau_1}(f) + \frac{-k}{s\tau_1}(D_{out}) \qquad \textit{eq) 2-19}$$

Factoring out the $\frac{-1}{s\tau_1}$ simplified this equation, seen in equation 2-20.

$$V_1 = \frac{1}{s\tau_1}[V_{in} - f - kD_{out}] \qquad \textit{eq) 2-20}$$

The next step was to derive an equation for the voltage at the output of the second integrator, *f*, which was given in equation 2-21.

$$f = \frac{1}{s\tau_2} D_{out} \qquad \textit{eq) 2-21}$$

Next the equation for the output is given in equation 2-22.

$$V_1 + e = D_{out} \qquad \textit{eq) 2-22}$$

To get an equation for the output voltage (D_{out}) in terms of the input voltage (V_{in}) and the error insertion (*e*) equation 2-22, first solving for V_1, and equation 2-21 were substituted into equation 2-20. This new equation is given in equation 2-23.

$$D_{out} - e = \frac{1}{s\tau_1}\left[V_{in} - \frac{1}{s\tau_2} D_{out} - kD_{out}\right] \qquad \textit{eq) 2-23}$$

Solving equation 22 for *d* yielded equation 23.

$$D_{out} = \left[\frac{s\tau_2}{s^2\tau_1\tau_2 + s\tau_2 k + 1}\right] V_{in} + \left[\frac{s^2\tau_1\tau_2}{s^2\tau_1\tau_2 + s\tau_2 k + 1}\right] e \qquad \textit{eq) 2-24}$$

From equation 2-24 the STF and NTF could be extracted as shown in equation 2-25 and 2-26.

$$STF = \frac{s\tau_2}{s^2\tau_1\tau_2 + s\tau_2 k + 1} \qquad \text{eq) 2-25}$$

$$NTF = \frac{s^2\tau_1\tau_2}{s^2\tau_1\tau_2 + s\tau_2 k + 1} \qquad \text{eq) 2-26}$$

From equation 2-25 it could be seen that with the introduction of the feedback integrator the STF become a bandpass filter as apposed to the lowpass filter response of the first order Σ-Δ ADC. The magnitude response of the STF is given in figure 2-11.

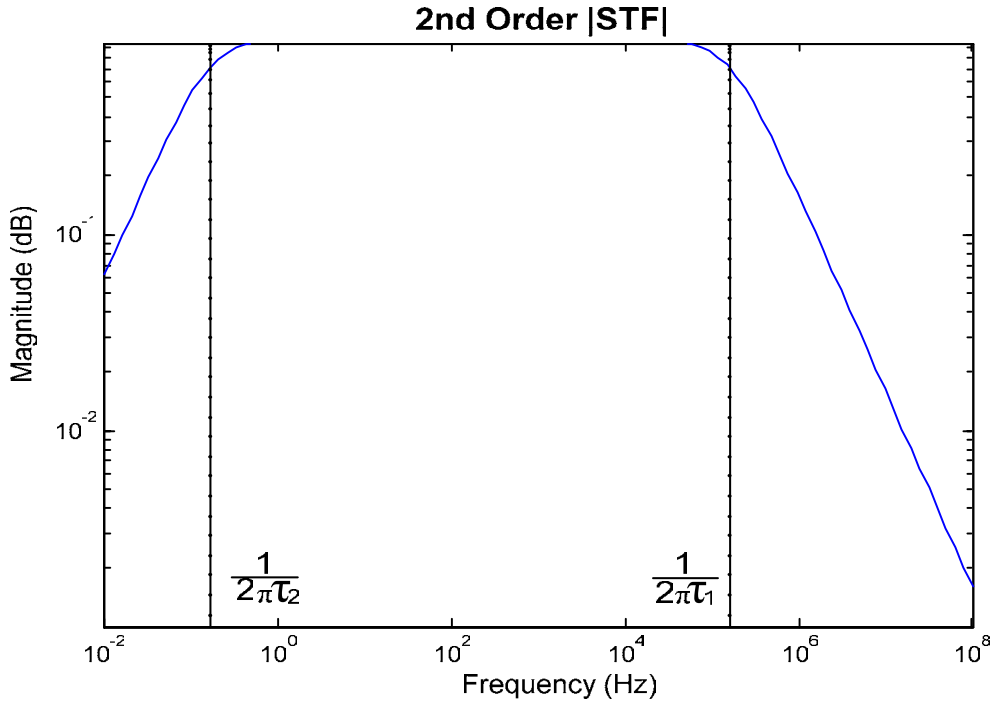


Figure 2-11: Magnitude Response of Second Order STF

This figure was produced using matlab to plot the magnitude response of the STF from the RC values used in the second order Σ-Δ ADC. It could be seen that the time constant τ_2 set the low cutoff frequency and τ_1 set the upper cutoff frequency. The time constant $\tau_1 = R_1C_1$ where $R_1 = 10k\Omega$ and $C_1 = 100pF$ which gave a time constant of 1 μsec and a cutoff frequency of 159.15 KHz. The time constant $\tau_2 = R_2C_2$ where $R_2 = 10M\Omega$ and $C_2 = 0.1\mu F$ gave a time constant of 1 sec and a cutoff frequency of 0.159 Hz. When deciding on appropriate time constants for the second order Σ-Δ ADC the typical frequency ranges of common biopotential signals were examined, table 1-1, and set to encompass all of the signals. From this table it can be seen that the typical frequency range that would be dealt with were between 0.05 Hz and 2000 Hz. When

deciding on the time constants, τ_1 was set to be well above the highest input frequency that would be encountered to allow for the lowpass FIR filtering to take care of the high frequency noise. The time constant τ_2 for this version of the second order Σ-Δ ADC was chosen based on the highest value capacitor and resistor available in the lab, but will need to be adjusted in future work on the system to the an appropriate cutoff frequency. From equation 2-26 the magnitude response of the NTF was plotted using matlab, and is shown in figure 2-12.

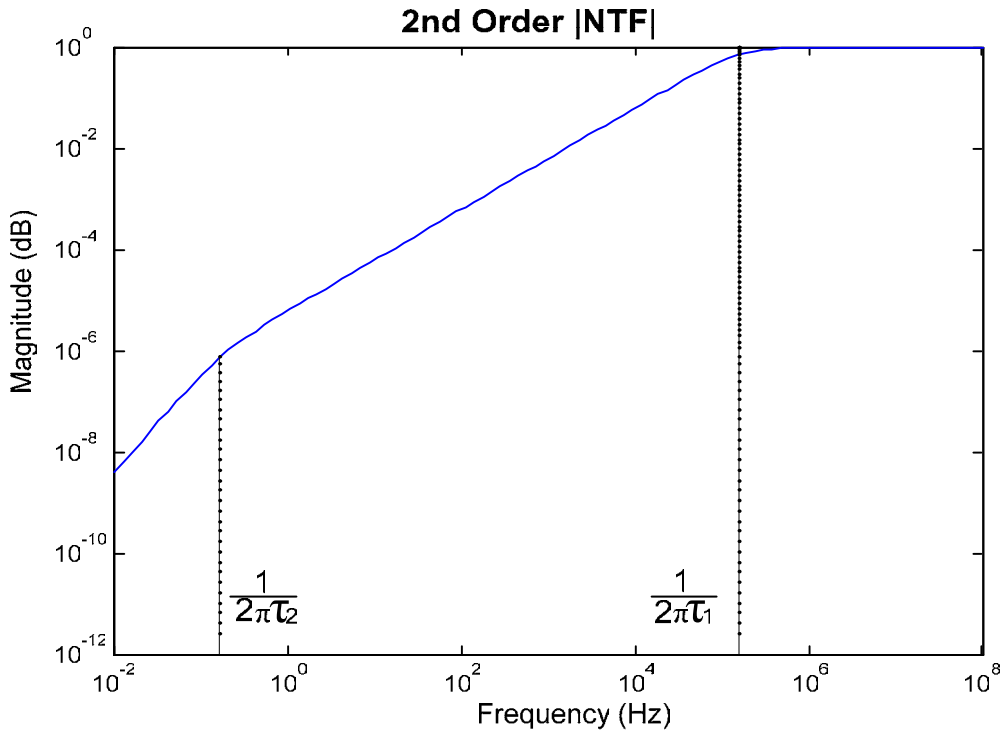


Figure 2-12: Magnitude Response of Second Order STF

From this figure it can be seen that the NTF is a highpass filter that has two distinct stages in the cutoff slope. The high cutoff frequency was determined from the time constant τ_1 and it could be seen that before the time constant τ_2 there was a greater slope than between τ_2 and τ_1. This change of slope between τ_2 and τ_1 was due to the fact that the transfer function is second order, equation 2-26, so each time constant has a point where it is dominant in the frequency response. The effect of the NTF highpass filter was to shape the quantization noise into the higher frequencies as discussed in the first order Σ-Δ ADC frequency analysis.

Offset potentials and low frequency motion artifact signals often can be associated with electrophysiologic signals producing undesirable affects. To eliminate the offset potentials and low frequency signals the second integrator in the feedback loop of the Σ-Δ ADC was introduced. This integrator was used to track these undesirable affects and feed them back to the input of the first integrator thus subtracting them from the input signal. To analyze how this tracking was accomplished the transfer function at the output of the feedback integrator, $|f/V_{in}|$, was derived. For the case of this analysis the feedback transfer function was called FTF. To derive f in terms of V_{in} and e equation 2-21 was solved for D_{out} then substituted into equation 2-24, which yielded equation 2-27.

$$f = \left[\frac{1}{s^2\tau_1\tau_2 + s\tau_2 k + 1}\right] Vin + \left[\frac{s\tau_1}{s^2\tau_1\tau_2 + s\tau_2 k + 1}\right] e \qquad \textit{eq) 2-27}$$

Setting e to zero gave the equation for f/V_{in}, FTF, as shown in equation 2-28.

$$FTF = \frac{1}{s^2\tau_1\tau_2 + s\tau_2 k + 1} \qquad \textit{eq) 2-28}$$

From this equation it could be seen that the FTF exhibited the behavior of a second order lowpass filter. Figure 2-13 is the matlab plot of the magnitude response of the FTF.

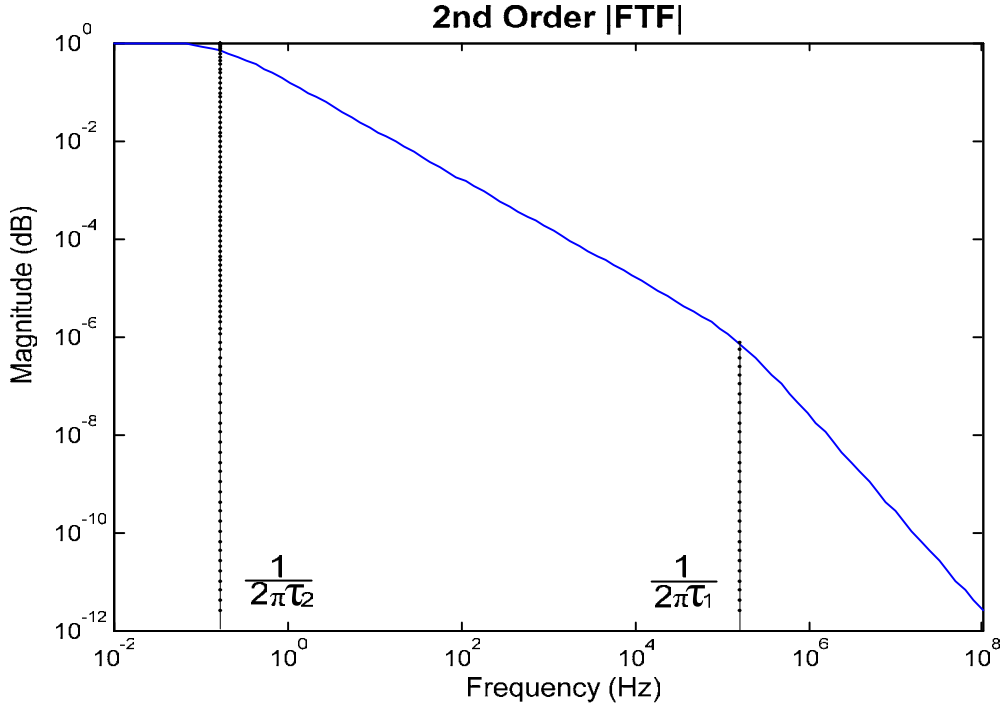


Figure 2-13: Magnitude Response of Second Order FTF

Like the NTF if can be seen that the FTF had two distinct stages in the cutoff slope. The lowpass filter effect of the FTF allowed the undesired signals to be passed back to the input to be subtracted while rejecting the desired signal. Another way to illustrate that the second order Σ-Δ ADC rejected the DC was by evaluating the STF, equation 2-25, at DC which yielded STF = 0/1 = 0 thus rejecting DC. Both methods of analysis are affective in illustrating the rejection of DC.

When deriving the equations for the STF, NTF, and FTF it could be seen that there was the introduction of constant *k*. The constant *k* was the ratio between the resistors in the feedback loop, from the *Q* output of the d-flip-flop, to R_1. The constant *k* was used to control the magnitude response of the transfer functions. For *k = 1* there was no attenuation or amplification in the passband, for k < 1 there was amplification in the passband, and for k > 1 there was attenuation in the passband. To illustrate the effect of *k*, figure 2-14 is the magnitude response of the STF where k = 0.5, 1, and 5.

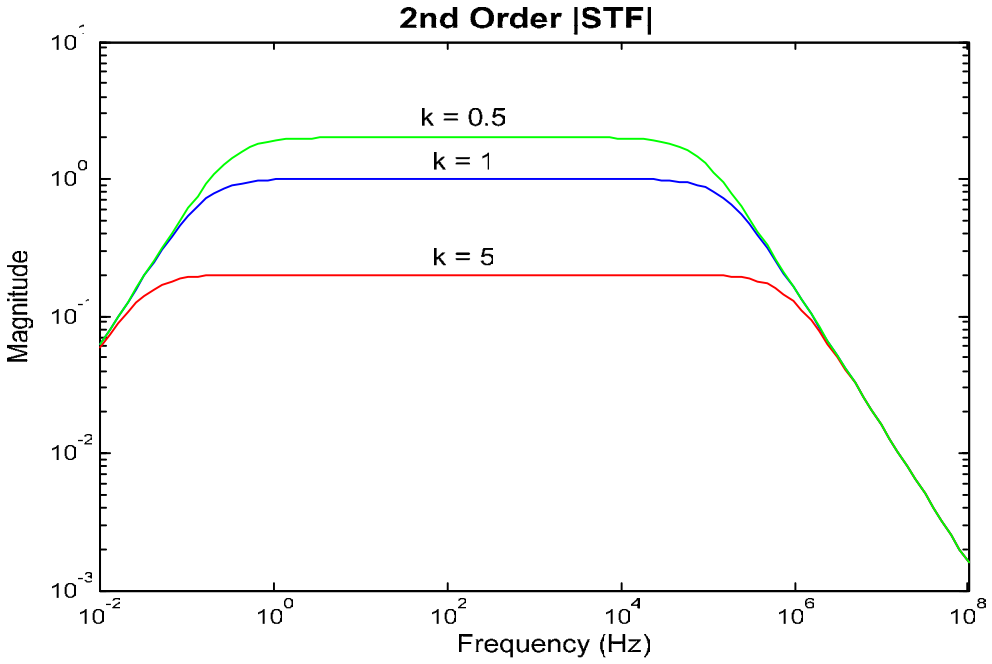


Figure 2-14: Magnitude Affects of Constant k

For this version of the second order Σ-Δ ADC, *k* was chosen to be 1. For future implementations of the second order Σ-Δ ADC it might be desirable to set k < 1 to allow for amplification in the passband.

The frequency analysis showed that the second order Σ-Δ ADC behaved as a bandpass system that rejected any potential DC offset of the input signal. It could be seen

that by adjusting the RC values for the time constants of H1 and H2 the corner frequencies could be controlled for a desired frequency band of the system. It was also shown that the second order system obtained the option for amplification or attenuation of the input signal by controlling the resistor value in the feedback loop from the Q output of the d-flip-flop. This analysis supported the desired characteristics of the electrophysiologic data acquisition system. The evaluation of the frequency response of the second order Σ-Δ ADC demonstrates how closely the system follows this analysis.

2.1.3 Finite Impulse Response Filter

The Σ-Δ ADC implemented made use of over sampling, clocking the d-flip-flop at 1MHz, in order to push the quantization noise associated with the comparator and d-flip-flop to high frequencies relative to the input signal bandwidth. To filter out the high frequency quantization noise a digital low pass filter was applied to the signal once it had been brought into the computer. To accomplish this lowpass filtering, finite impulse response (FIR) filtering was preformed using Matlab.

For the digital filtering required to reconstruct the digital signal there where two types of digital filters looked at, FIR filtering and infinite impulse response (IIR) filtering. FIR filtering was chosen over IIR filtering for a number of reasons. A major draw back with IIR filters is that because they are recursive, that is "the output is calculated using input and previous values of the output," if there were any roundoff errors calculating the output then that error would be fed back into the input compounding on itself (Rose, 2003). The dependency on previously calculated values with IIR filtering can be seen from its general formula where n is the order, a_i and b_i are the output filter coefficients, $Y(k)$ is the output sequence, and $X(k)$ is the input sequence:

$$Y(k) = a_0X(k) + a_1X(k-1) + \ldots + a_nX(k-n) + b_1Y(k-1) + b_2Y(k-2) + \ldots + b_nY(k-n) \quad \textit{eq) 2-29}$$

FIR filters are nonrecursive, "because the output is calculated using the current and past input, but not previous values of the output" (Rose, 2003). This nonrecursion can be illustrated from the general formula of a FIR filter with n is the order, a_i is the output filter coefficients, $Y(k)$ is the output sequence, and $X(k)$ is the input sequence:

$$Y(k) = a_0X(K) + a_1X(k-1) + \ldots + a_nX(k-n) \quad \textit{eq) 2-30}$$

The advantage of the FIR filter not being dependent on previously calculated values is that the roundoff error occurs in the form of a start up transient, the first *n-1* points, which will not accumulate. An IIR filter would also have a start up transient due to round off error, but this error would accumulate. Another attractive feature of the FIR filter compared to the IIR filter is that a FIR filter can be designed with linear phase. Since the application of this project was dealing with biomedical signals it was desirable to only have a pure time delay, which a linear phase filter provided. The one draw back to

using FIR flitering over IIR filtering was that IIR filters typically achieve the desired magnitude response with a fewer number of taps then a FIR filter. This draw back was acceptable though due to the ease of implementation of the FIR filter compared to the IIR filter and the rest of the desired properties of the FIR filter. The design that was finally implemented was a linear-phase FIR filter using the Hamming windowing method.

It was desirable to examine the frequency-domain characteristics of some of the main windowing functions to determine the proper approach in the filter design. Table 2-1 is the frequency-domain characteristics of some more common window functions, where *n* is the number of taps.

Type of window	**Approximate transition width of main lobe**	**Peak sidelobe (dB)**
Rectangular	$4\pi / n$	-13
Barlett	$8\pi / n$	-27
Hanning	$8\pi / n$	-32
Hamming	$8\pi / n$	-43
Blackman	$12\pi / n$	-58

Table 2-1: Frequency-Domain Characteristics of Some Window Functions (Proakkis p. 628)

Comparing the transition widths of the different windowing functions the rectangular method had the narrowest transition width which meant it would need the fewest number of taps to achieve the desired filtering. The disadvantage of this method was that its peak sidelobe is only -13 dB which would not offer adequate attenuation of the high frequencies being rejected. The Blackman windowing method offered the greatest attenuation with peak sidelobes at -58 dB but also had the widest transition width out of the windowing methods for a set number of taps. The Hamming windowing method was thus chosen because it offered the best combination of attenuation in the stop band, -43 dB, and a reasonable transition width for a set number of taps.

The FIR filter chosen from Matlab's Signal Processing Toolbox was the `fir1`. The default setting of the filter is to have a magnitude response of 0 dB in the passband. The function call used was `b = fir1(n,Wn)`, where `n` was the order of the lowpass FIR filter and `Wn` was the normalized cutoff frequency, returned a row vector `b` containing the `n+1` coefficients. By default the `fir1` function used the Hamming-window method and was a

linear-phase filter (Matlab Help). For this design Wn = fc/(fs/2) where fc was the cutoff frequency and fs was the sampling frequency, both in hertz. To demonstrate the filter design figure 2-15 depicts the magnitude response of a FIR lowpass filter whose cutoff frequency was 1200 Hz, sampling frequency was 1 MHz, and *n* was 10000.

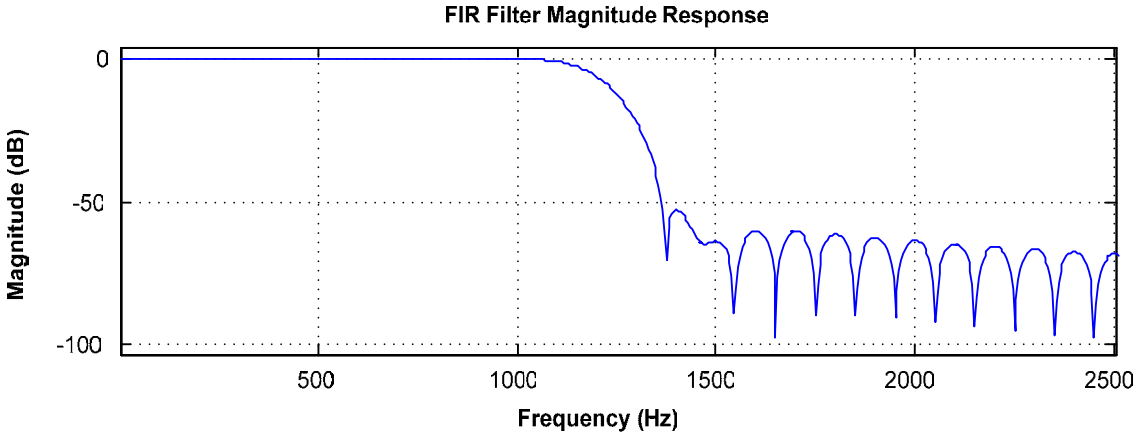


Figure 2-15: FIR Lowpass Filter Magnitude response

From figure 2-15 it can be seen that the peak sidelobe was just below -50 dB down, which exceeded the average peak sidelobe from table 2-3. Further analysis of the passband showed that there was indeed a tiny bit of rippling effect, which was to be expected. Figure 2-16 is magnification of the passband in figure 2-15.

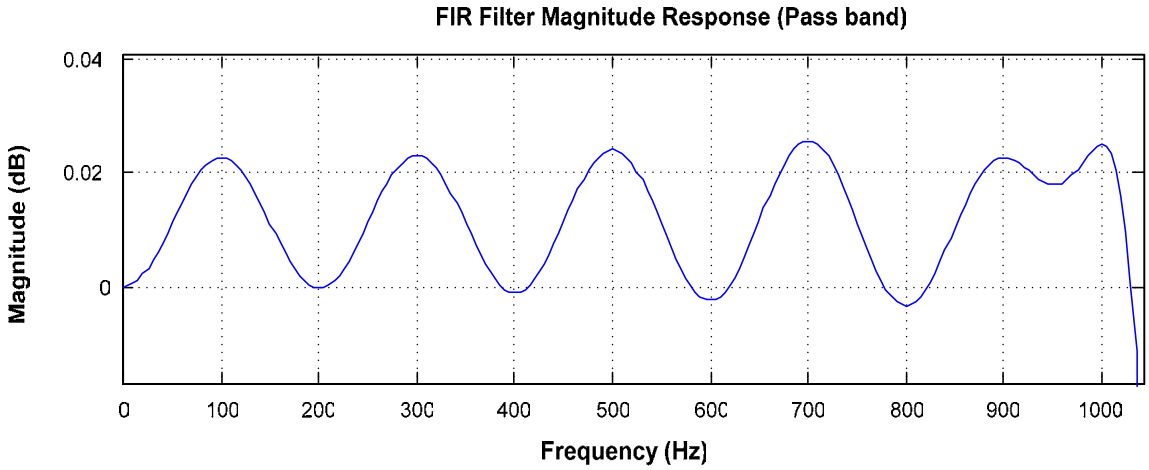


Figure 2-16: Magnified View of Pass Band

From figure 2-16 it can be seen that there is indeed a slight ripple effect between 0 and about 0.02 dB. This small ripple effect was due to the windowing filter design method, known as Gibbs phenomenon (Proakis p.259). Figure 2-17 depicts the phase

response of this same filter. It can be seen that the phase response was linear over the entire range of frequencies.

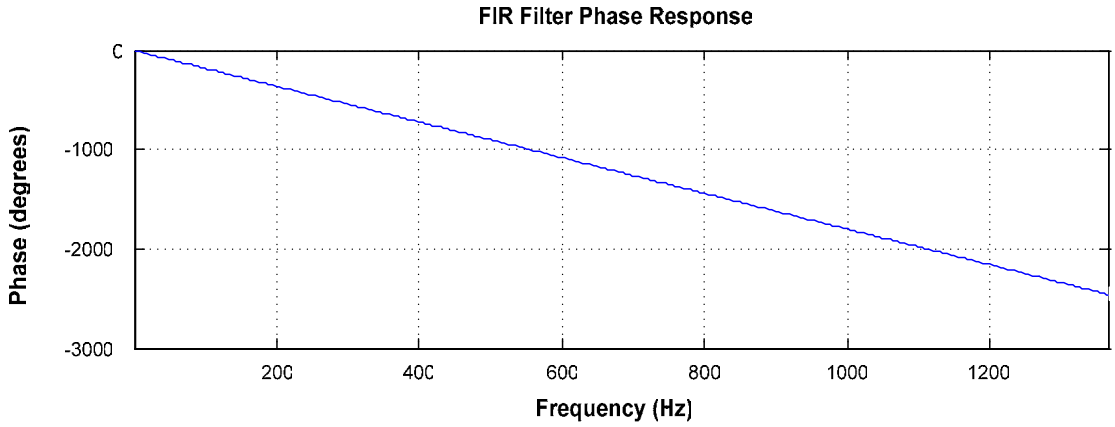


Figure 2-17: FIR Phase Response

For implementation of the electrophysiologic data acquisition system the cutoff frequency will need to be set for the appropriate input frequency bandwidth. From figures 2-15 and 2-16 it can be seen that that a cutoff frequency of 1200 Hz would be good for passing a frequency bandwidth up to 1000 Hz. This indicated that for a 10000 order FIR lowpass filter setting the cutoff frequency 200 Hz above the highest frequency in a given frequency bandwidth would be adequate. When the FIR filter was used to evaluate the digital output of the Σ-Δ ADCs the order used was 10000.

2.2 Implementation

This section covers the implementation of the first and second order Σ-Δ ADCs along with how the output signals where acquired and evaluated by the computer.

2.2.1 First Order Σ-Δ ADC

The first order Σ-Δ ADC was breadboarded with all discrete components. The +15V, -15V, and +5V rails were generated from a Tektronix PS2521G Programmable Power Supply, and the ground connection came from the connector block of the digital I/O board. For all the supply pins bypass caps of 0.1μF were connected to ground. The op amp used was a monolithic JFET input operational amplifier, National Semiconductor LF356BN. The voltage comparator used was a National Semiconductor LM311N and the Dual D-type Positive Edge-triggered Flip-flop was a 74AC74PC. The clock used for the D-flip-flop was a 1MHz crystal oscillator, M-Tron 89-14. For testing purposes the input sine wave was generated with a Hewlett Packard 33120A 15 MHz Function / Arbitrary Waveform Generator. The maximum input voltage range for this setup was between 0 and -5 volts, and when the input was a sine wave it was centered at -2.5 volts. Figure 2-18 is a digital photo of the first order Σ-Δ ADC setup when it was fully connected.

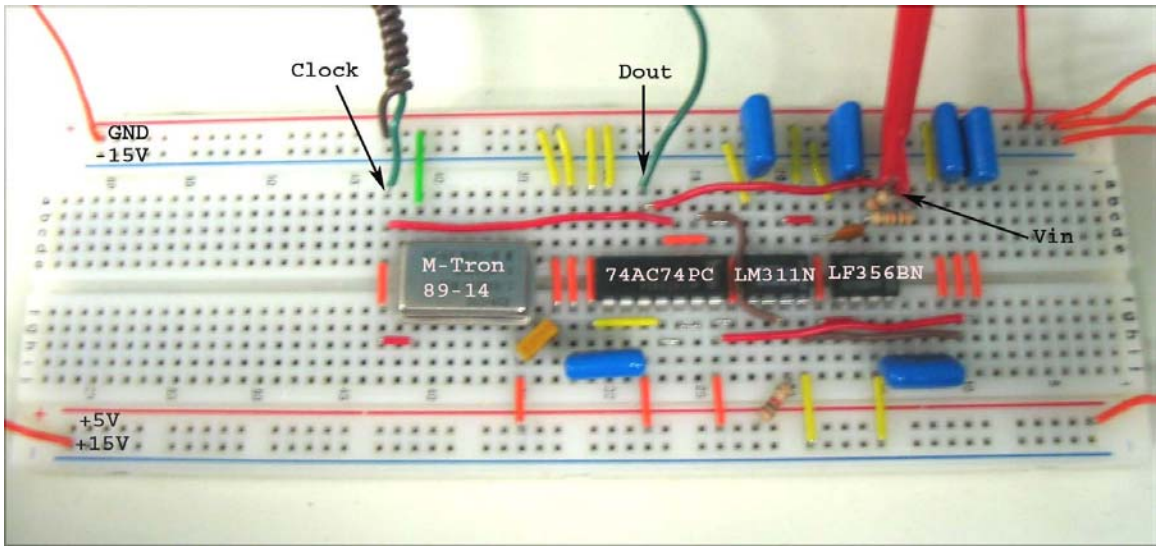


Figure 2-18: First Order Σ-Δ ADC Configuration

2.2.2 Second Order Σ-Δ ADC

The second order Σ-Δ ADC was breadboarded with all discrete components. The +15V, -15V, and +5V rails were generated from a Tektronix PS2521G Programmable Power Supply, and the ground connection came from the connector block of the digital I/O board. The +2.5V rail was generated by passing the +5V rail through a voltage divider and was not effected because no current was drawn from the rail. The op amps used were two of the JFET-input quad operational amplifiers, LF357N. The voltage comparator, and Dual D-type Positive Edge-triggered Flip-flop, and clock used for the second order Σ-Δ ADC were the same as the first order Σ-Δ ADC because the only difference between the two systems was the introduction of the feed back op amp. The maximum input voltage range for this setup was between 0 and +5 volts. Due to the DC rejection characteristic of the second order Σ-Δ ADC the input voltage could obtain any offset. Figure 2-19 is a digital photo of the second order Σ-Δ ADC setup when it was fully connected.

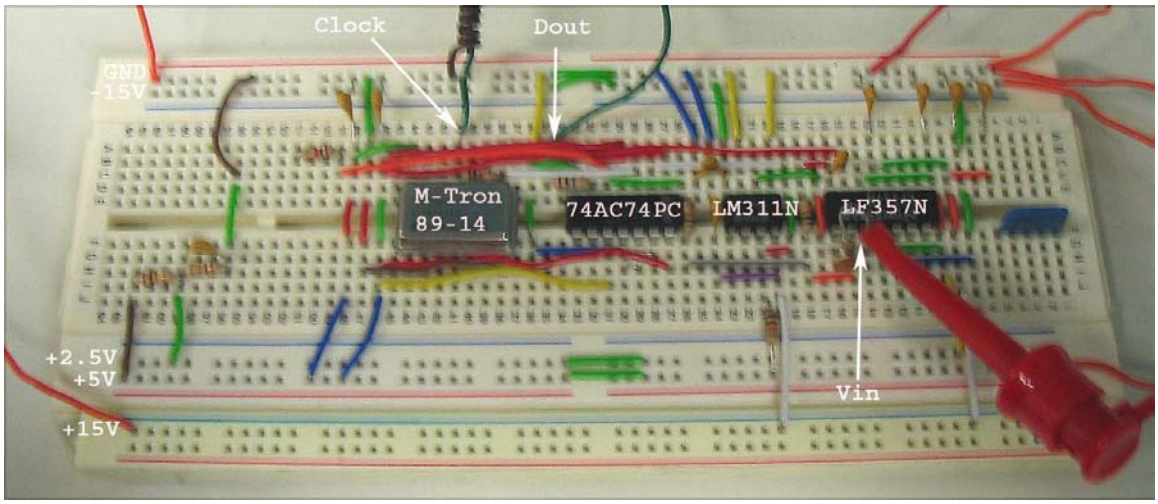


Figure 2-19: Second Order Σ-Δ ADC Configuration

2.2.3 Data Acquisition

The hardware used for this implementation was a digital I/O board, cable, and connector board. The major qualification when searching for the digital I/O board was that it be capable of handling an external clock of 1MHz or higher (for future applications), which would be taken from the clock on the Σ-Δ ADC. The National Instrument PCI-6533 (DIO-32HS) digital I/O board was eventually chosen for this application. This board had 32 digital I/O lines, at 5 V TTL/CMOS, and with a 2.5 MHz maximum input rate for an 8-bit word was more than sufficient to handle the clock speed of 1 MHz. The maximum input rate of 2.5 MHz allowed the option to increase clock speed of the Σ-Δ ADC for future applications if necessary. To interface with the Σ-Δ ADC, the National Instrument SH68-68-D1 Shielded Cable and SCB-68 Noise Rejecting, Shielded I/O Connector Block was used. Figure 2-20 depicts the shielded I/O connector block. Wires were then used to connect the ground, clock, and output signal from Σ-Δ ADC to the connector block. Since the output signal of the Σ-Δ ADC was only one bit it was connected to the first bit of one of the three 8 bit channels of the connector block. The ground wire coming out of the connector block was wrapped around the clock wire to add extra shielding when the wires were outside the connector block connecting to the Σ-Δ ADC.

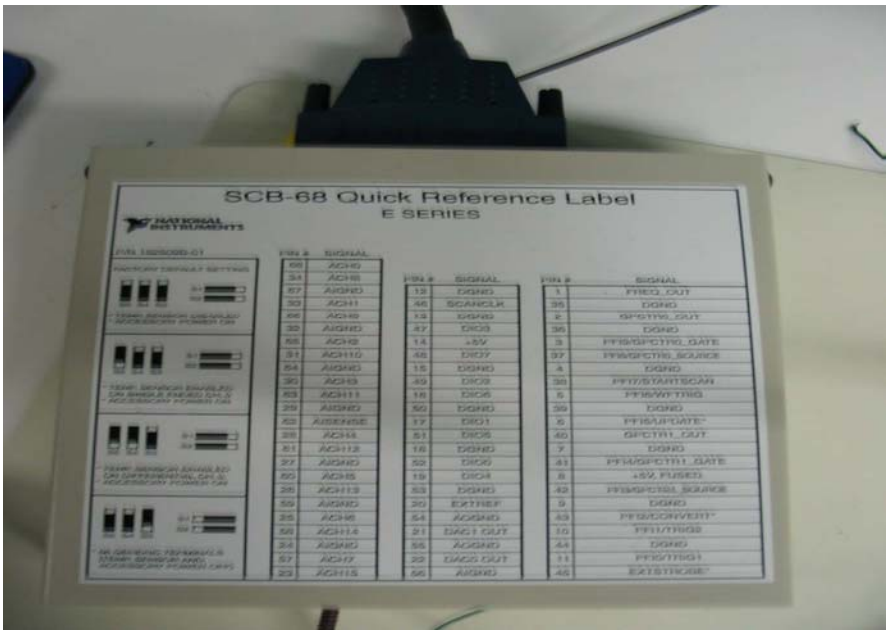


Figure 2-20: Shielded I/O Connector Block

2.2.4 Labview

Labview was used in conjunction with the digital I/O board, cable, and connector block to acquire the output data from the Σ-Δ ADC. Code to perform this operation was downloaded from National Instruments web page under NI Developer Zone → Example Code. The code used performed continuous pattern input while streaming to a binary file, one digital sample per byte. Once the appropriate connections where made from the Σ-Δ ADC to the connector block the following parameters had to be set: device number, channels, clock source, scans to read at a time, and buffer size. Figure 2-21 depicts the front panel of the labview program once the parameters where set.

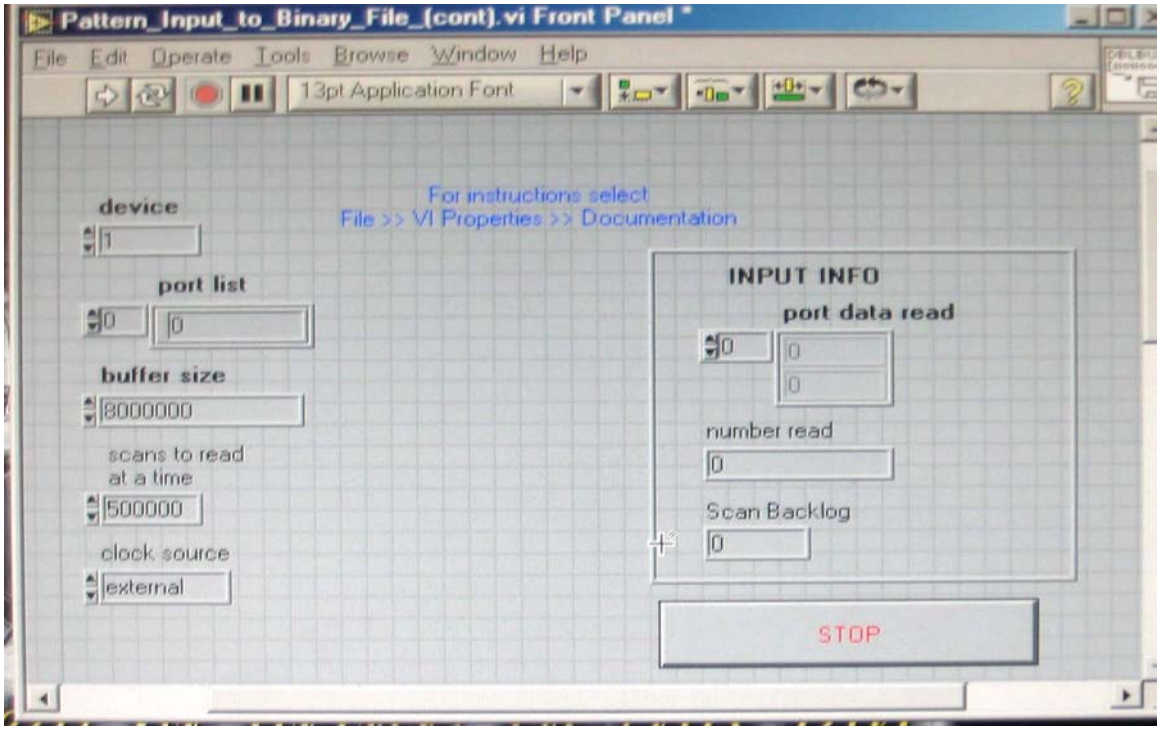


Figure 2-21: Labview Setup

2.2.5 Matlab

Matlab was used once the data from the Σ-Δ ADC was brought into the computer to perform FIR filtering and further evaluation of the signal. The mfile coding can be found in Appendix A.

2.3 Results

This section presents the results of the evaluations preformed on the first and second order Σ-Δ ADC. It will cover the DC evaluation of the first and second order Σ-Δ ADC, FIR filter implantation, second order Σ-Δ ADC frequency evaluation, and an evaluation of the signal to noise ration of the systems.

2.3.1 DC Evaluation

This section covers the DC analysis preformed on the first and second order Σ-Δ ADC. It was important in determining the linearity of the systems to determine if they would distort an input signal.

2.3.1.1 First Order Σ-Δ ADC

From the DC analysis of the first order Σ-Δ ADC it was shown that the system should have a linear DC response with a DC offset due to the imperfections of the op amp integrator. To perform this evaluation a number of DC voltages were applied to the Σ-Δ ADC, covering the full range of the input voltages of the Σ-Δ ADC being 0 to -5 volts. The average value of the output to the Σ-Δ ADC represented the input voltage, so a multimeter was used to read the output. The multimeter was used to measure the DC value of the output signal because it "averag[s] the input by integrating it over a fixed period"(Hertz). The results of the measurements can be found in table 2-2. From a first glance of the data in table 2-2 it can be said that *Vout* followed *Vin* implying linearity.

Vin (volts)	**Vout (volts)**
-0.399	0.3975
-0.7976	0.7954
-1.1967	1.1936
-1.594	1.59
-1.993	1.988
-2.392	2.386
-2.791	2.785
-3.19	3.183
-3.589	3.582
-3.988	3.98
-4.387	4.378
-4.786	4.777

Table 2-2: Vin vs Vout

To take a closer look at these data, Matlab was used to obtain a scatter plot. The scatter plot showed that *Vout* vs *Vin* was indeed linear but to determine its exact slope and offset the polyfit function was implemented to obtain a linear least square best fit line for the data points. Figure 2-22 shows the best fit line along with its slope and offset for the data, which were -0.9983 and -0.0011 respectively.

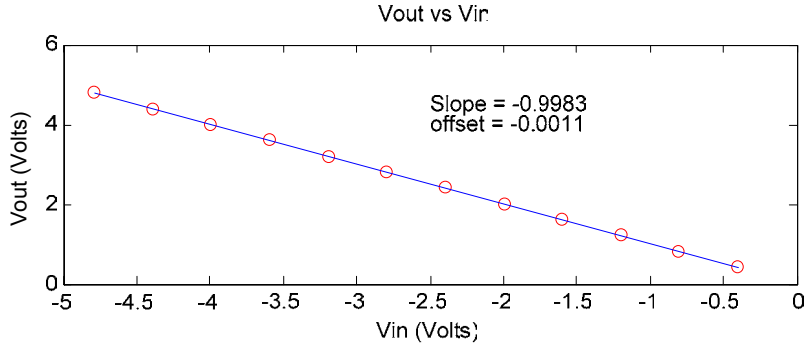


Figure 2-22: First Order Σ-Δ ADC - Vout vs Vin

Finding the difference between the data points and the best fit line produced a new data set, which can be used to obtain the error plot shown in figure 2-23. The pattern of the scatter plot, which is emphasized by the superimposed line, characterized the quantization "noise" or "error" of the system. There is also some error introduce from the limited resolution of the multimeter used for testing. There was no indication from figure 2-23 that the system was nonlinear.

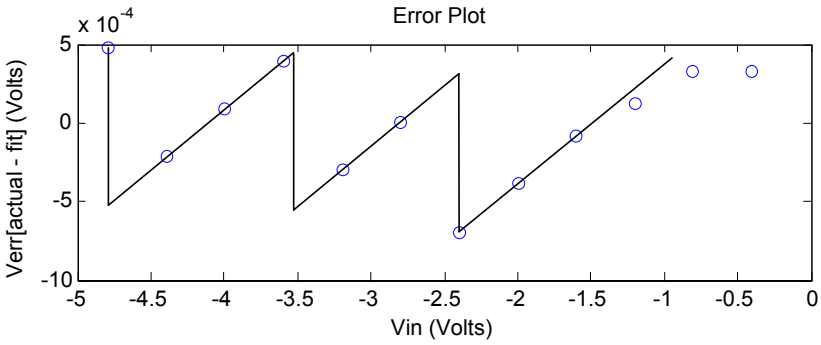


Figure 2-23: First Order Σ-Δ ADC - Error Plot

In the circuit tested R1 and R2 were both 10KΩ, but due to the fact that they had a ±5% tolerance they produced a slope not equal to unity. From figure 2-5 it could be seen that the *slope = -R1/R2* and that the *offset = (1+R2/R1)Vos*. The value for *R1/R2* could be seen to be 0.9983 from the equation of the slope and *Vos = offset / (1+R2/R1)*. *Vos* could then be calculated to be -.55mV by dividing -0.0011, the offset, by (1 + 0.9983). It should

be noted that the linear least square best fit line gave the values for the slope and offset. The calculated offset voltage fell within the specifications of the LF356, which has a typical *Vos* of 3 mV and a maximum *Vos* of 10mV. This evaluation concluded that the first order Σ-Δ ADC followed the real case 1, from figure 2-3, and was linear with a DC offset. The tools for this evaluation were applied to the second order Σ-Δ ADC.

2.3.1.2 Second Order Σ-Δ ADC

A DC evaluation was preformed for the second order Σ-Δ ADC, similar to that of the first order Σ-Δ ADC. There had to be a slight modification made to the second order Σ-Δ ADC in order to do this evaluation. Figure 2-24 is the schematic of the modified second order Σ-Δ ADC used to perform the DC evaluation.

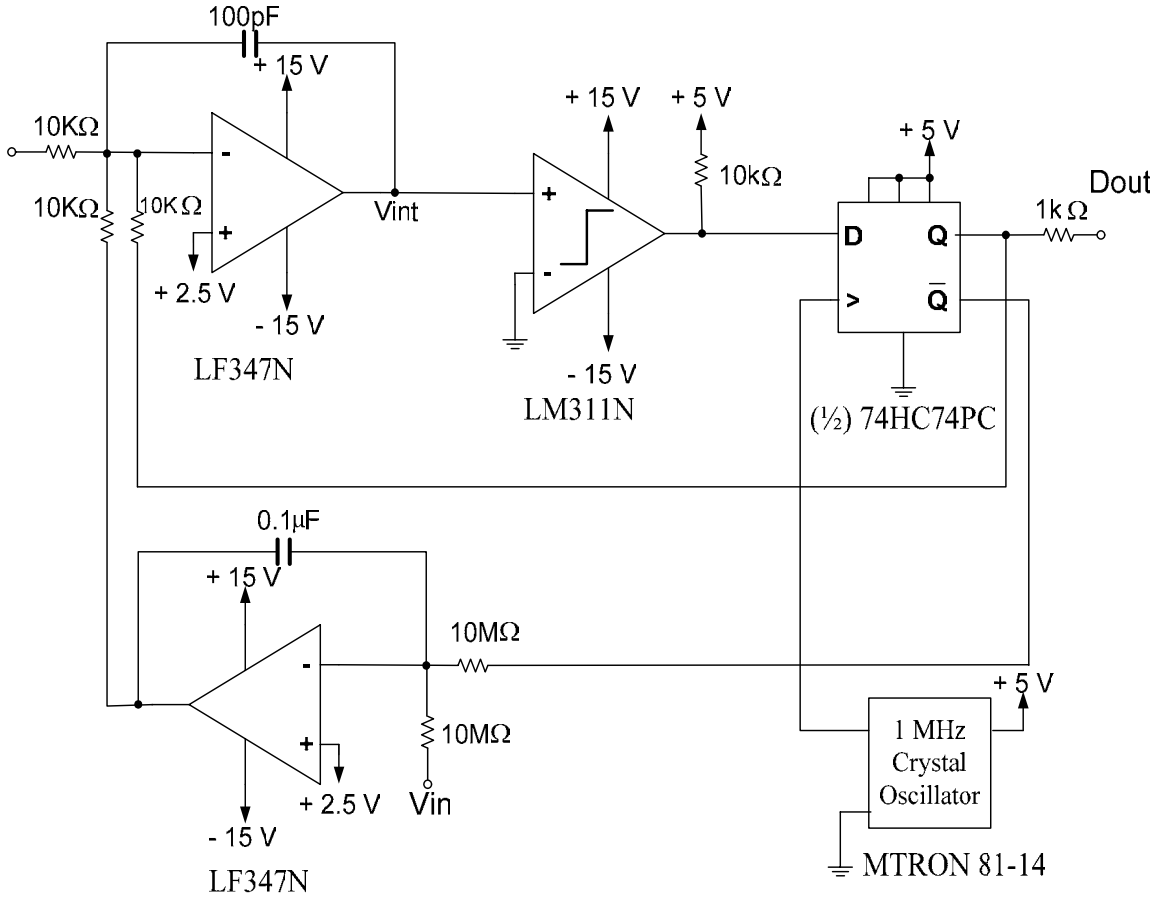


Figure 2-24: Schematic of Second Order Σ-Δ ADC for DC Evaluation

As can be seen in figure 2-24 a 10 MΩ resistor was added to the input of the feedback op amp as the input, and the original input at the 10 kΩ was left floating. The reason this had to be done was that the feedback op amp was used to subtract out any DC

component of the input signal. To perform this evaluation the Hewlett Packard 33120A 15 MHz Function/Arbitrary Waveform Generator was used to produce the DC input voltage, while the Hewlett Packard 3458A Multimeter was used in conjunction to read the DC value inputted. The reason the multimeter was used with in conjunction with the function generator was that it allows for a much more accurate reading of the DC voltage due to its higher resolution. The DC voltage was then applied to the input of the second order Σ-Δ ADC, *Vin*, and the output, *Dout*, was read into the computer with labview taking 500k samples of the output signal. Matlab was then used to calculate the mean value of the output signal to obtain the DC representation. Figure 2-25 is the plot of the second order Σ-Δ ADC's DC response, with a matlab generated linear least square best fit line.

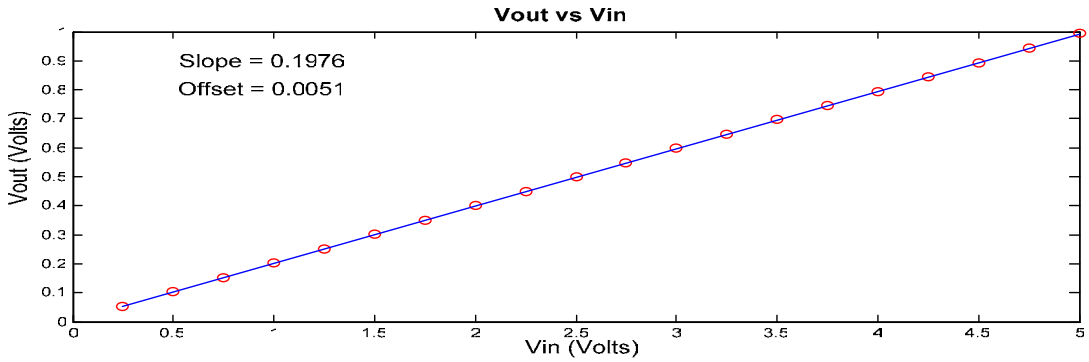


Figure 2-25: Second Order Σ-Δ ADC -Vin vs Vout

As can be seen the output scale was between 0 and 1 volts and the input voltage was between 0 and 5 volts. Taking the difference between the output data and the best fit line the error plot was then produced, shown in figure 2-26.

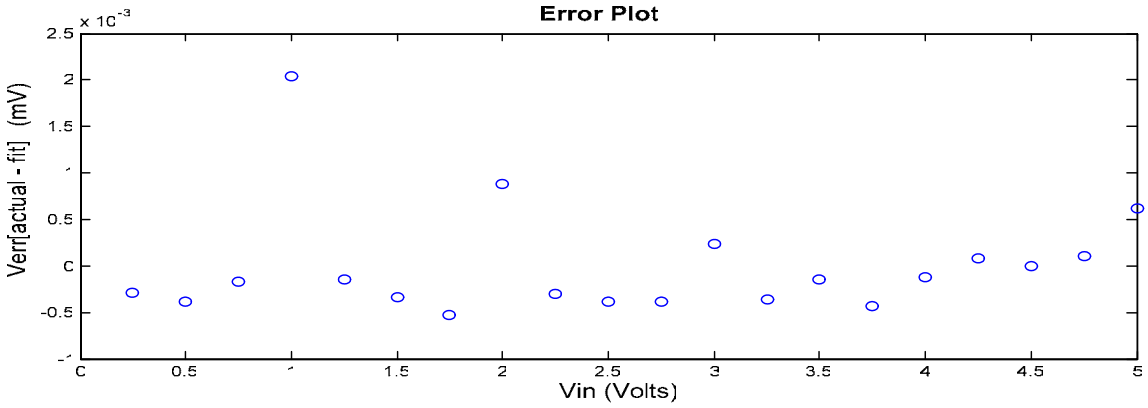


Figure 2-26: Second Order Σ-Δ ADC - Error Plot

This error plot showed that the second order Σ-Δ ADC was linear, discarding the results at the input voltages of 1V, 2V and 3V. The variance of these points with the rest of the data was not determined. This conclusion suggested that the system would not distort the signal.

2.3.2 Finite Impulse Response Filter Implementation

To demonstrate the effects of the FIR filter example presented in the FIR Filter Design section, a 1 kHz sine wave with a 3.2 V peak-peak amplitude and -1.1 Vdc offset was applied to the input of the first order Σ-Δ ADC converter. Labview was then used to read in 500000 samples of the output data. It should be noted that Labview sampled *Dout* once per clock cycle, 1 MHz, (after Dout was stable) and read a digital bit which was set to 1 when *Dout* was high and 0 when *Dout* was low. Figure 2-27 is a time domain representation of the first 2 msec of the unfiltered data, which consisted of all 1's and 0's representing the sine wave input. Due to the high frequency quantization noise it is difficult to make out the sine wave from this figure.

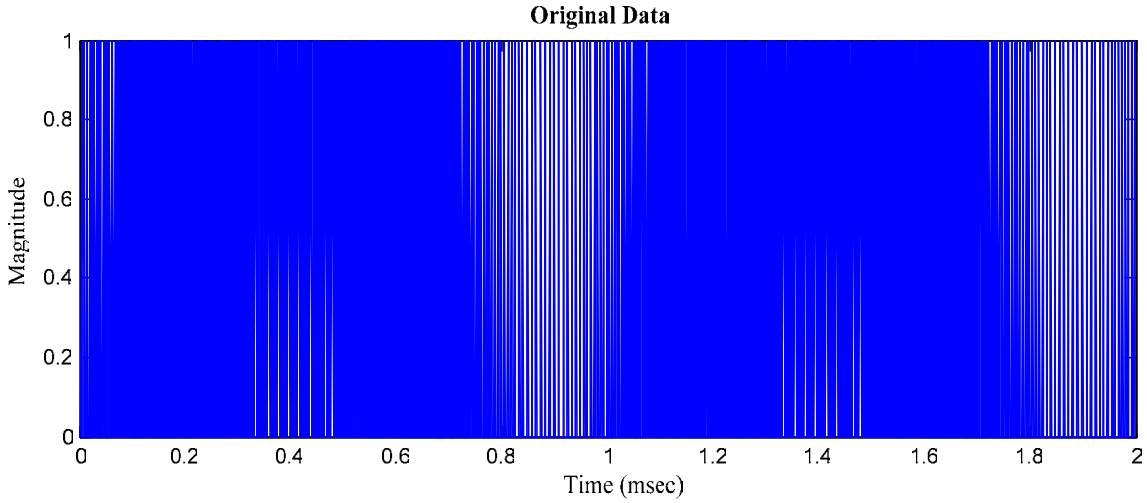


Figure 2-27: 2 msec Sample of Unfiltered Data

To illustrate the high frequency quantization noise further, figure 2-28 depicts the FFT of the unfiltered data on a log log frequency plot. It can be seen from this figure that the high frequency noise increased in amplitude with frequency. The increasing of the noise in the higher frequencies was the effect of the noise-shaping highpass filtering caused by the NTF. The effects of the lowpass filtering caused by the STF could also be seen in this figure as low amplitude, close to 0 dB, noise in the low frequency passband.

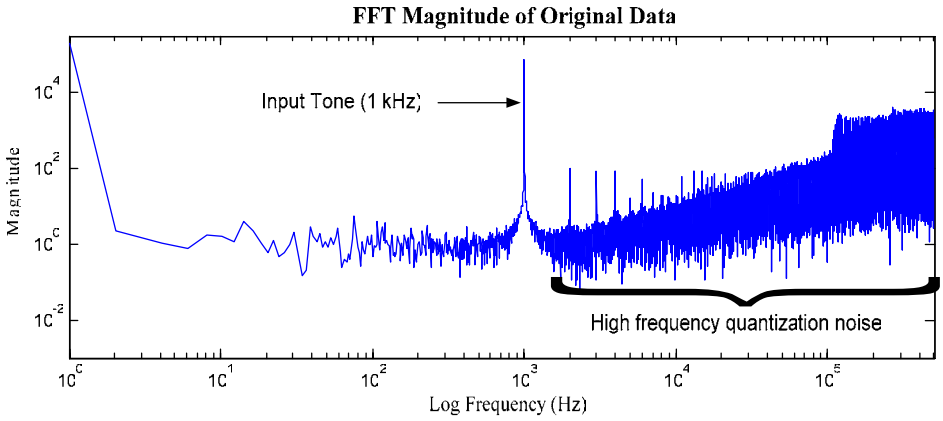


Figure 2-28: FFT of Unflitered Data

This signal was then passed through the designed lowpass FIR fliter using the command `y = filter(b,1,data)`, where `b` were the coefficients computed from the `fir1` function. Since there was a start up transient associated with FIR filtering the first `n+1` points (n = order and order = taps + 1) were removed from the beginning of the filtered data and after the filtering takes place. To account for the start up transient and phase delay the unfiltered data was changed to start at 1 + n/2 and end at end – n/2. Figure 2-29 is the first 2 msec of the filtered data, after the removal of the start up transient.

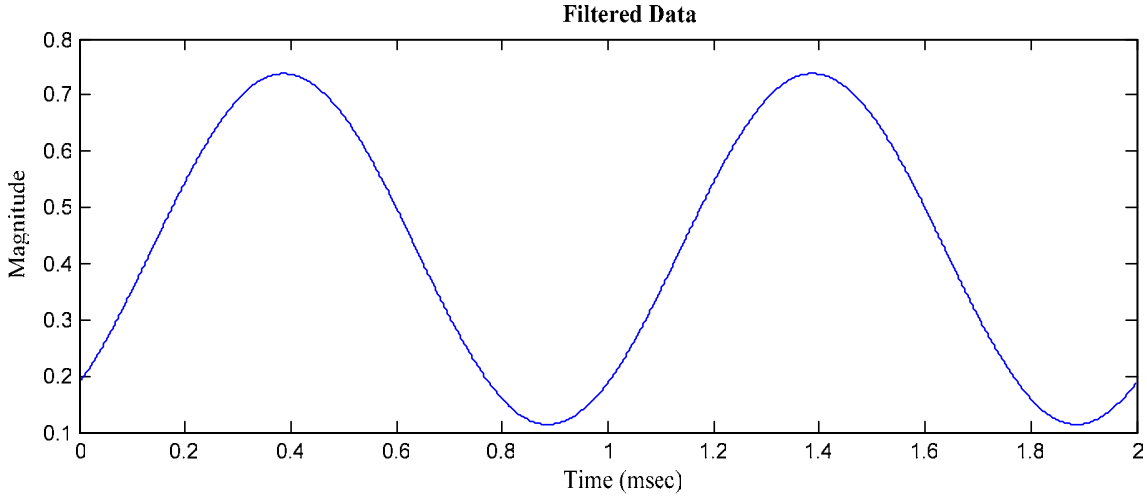


Figure 2-29: 2 msec Sample of Filtered Data

This figure illustrated that after the removal of the high frequency quantization noise the input sine wave can be seen. To represent these same data in the frequency domain figure 2-30 is the FFT of the filtered data, also after the removal of the start up transient.

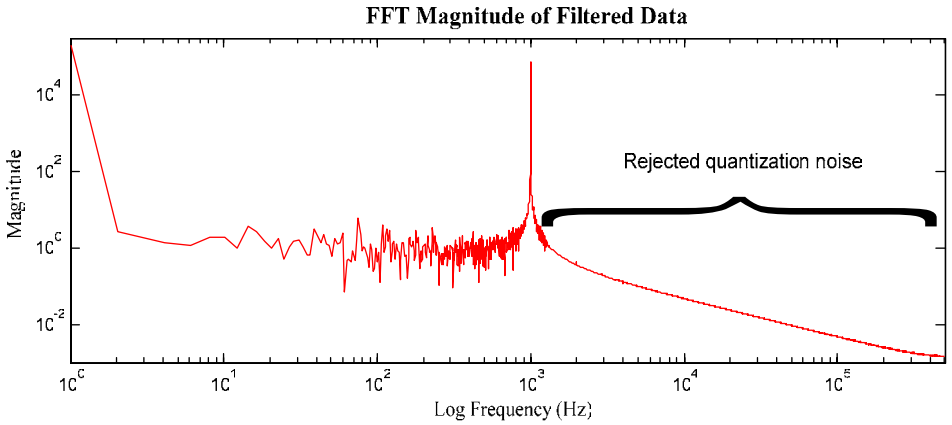


Figure 2-30: FFT of Filtered Data

In comparing this figure with figure 2-28 the affects of the FIR lowpass filter could be seen. All of the high frequency quantization noise was successfully filtered out, leaving the input signal without any attenuation. In this example the FIR lowpass filter's cutoff frequency was specially set to this input signal, but in the actual implementation the FIR filter would be designed to accommodate a wider passband for the varying input signals with different frequencies.

When comparing the filtered data to the unfiltered data in the FFT frequency domain it was noticed that the signals didn't match up exactly in the passband frequencies. This observation is depicted in figure 2-31.

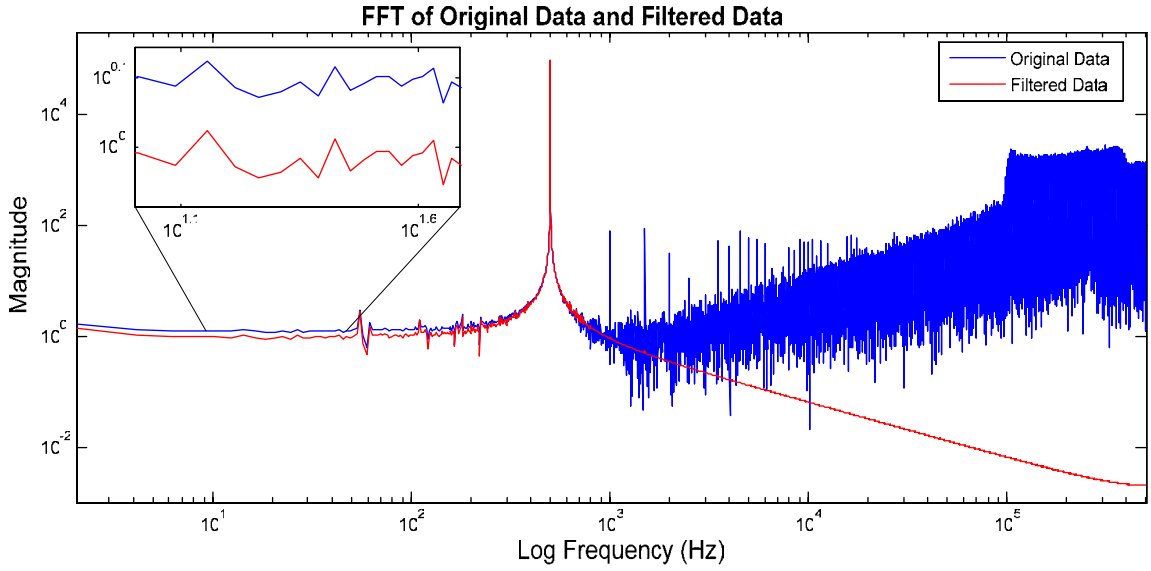


Figure 2-31: FFT Comparison of Filter and Unfiltered Data

It can be seen that the two passbands differ by about 11 dB from each other. The variance of the passbands also was different for each signal. In some cases the passband of the filtered data would be above the unfiltered data and other times it would be, as depicted in figure 2-31, the unfiltered data would be above the unfiltered data. The reason for the difference in the passband when comparing the filtered and unfiltered data was not determined, but it was decided for this stage of development this was not a crucial issue and could be looked into further in future work if necessary.

2.3.3 Second Order Σ-Δ ADC Frequency Response

To get a sense of how well the second order Σ-Δ ADC followed the analysis of frequency response, in particular how closely it followed the STF, a number of input sine waves at different frequencies were inputted and then the amplitude of the output filtered data was reordered. The input sine wave had an amplitude of 2 Vpk-pk. Figure 2-32 is a Bode plot of the frequency response of the second order Σ-Δ ADC along with the theoretical STF.

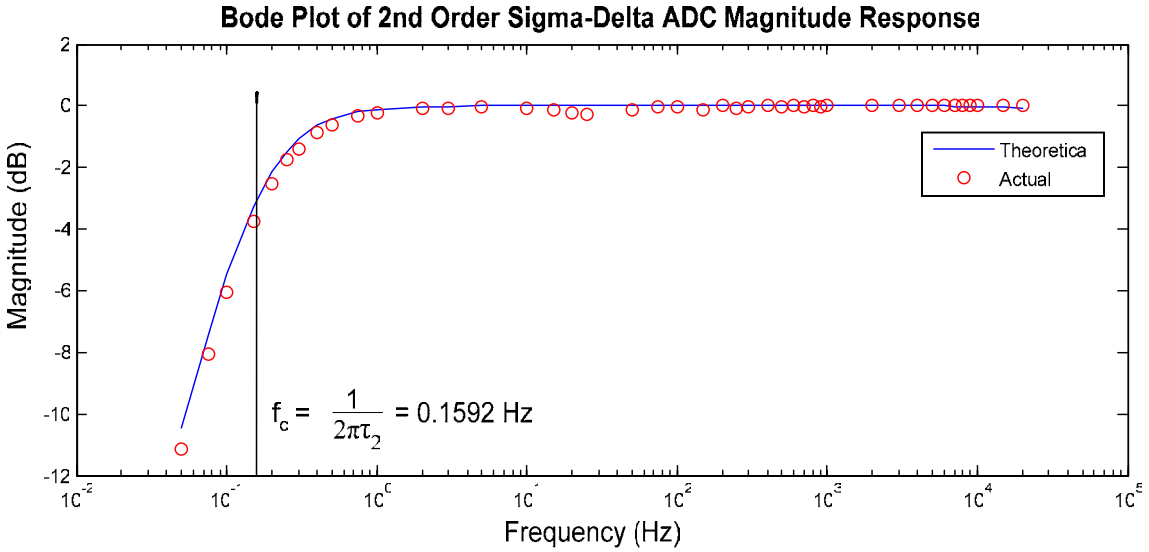


Figure 2-32: Bode Plot Second Order Σ-Δ ADC Frequency Response

It should be noted that in determining the Bode plot the amplitude response was normalized to 0.3982 volts, which was an average value of the passband amplitude. Comparing figure the theoretical STF bandpass filter with the acquired frequency response it can be seen that for the lower frequency range the response of the second order Σ-Δ ADC followed very closely with the theoretical predictions. When the system is implemented in future applications for a cutoff frequency that is more appropriate for electrophysiologic signals, this evaluation showed that the response of the system will perform as expected.

2.3.4 Nonlinear Least-squares Curve Fitting

To measure the accuracy of the output data from the Σ-Δ ADC after filtering it was fit to a sine wave to determine the actual offset, amplitude, and frequency of the filtered data. To fit a sine wave to the filtered data the lsqcurvefit Matlab function was implemented to find a non-linear least squares best fit sine wave. This function produced a best guess for the offset, amplitude, frequency and phase. To give an example of this process the filtered sine wave, used in the FIR implementation section, the best fit offset = 0.4260 V, amplitude = 0.3123 V, frequency = 999.9911 Hz. These data show that the filtered data were a very accurate representation of the input sine wave. The amplitudes of the input sine wave and the filtered sine wave could be compared by there ratios of their voltage windows. For the input signal it was a 3.2 V peak-peak, or 1.6 V amplitude in usable range of 0 to 5 V. The filtered signal's amplitude was 0.3123 V in a 0 to 1 V range, since the data from the Σ-Δ ADC was only a 1-bit signal. The ratio for the input signal, 1.6 V / 5 V, was 0.32 and for the filtered data, 0.3123 V / 1 V, it was 0.312. Computing the percent error or attenuation:

$$100 * (0.32-0.3123) / 0.32 = 2.4\%$$

This error was due to the fact that the amplitude response was not ideally 1, which was seen in the magnification of the passband of the FIR filter in the FIR Filter Design section. With a percent error of 2.4% and an estimated frequency of 999.991 Hz this showed to be an accurate first order Σ-Δ ADC converter. The graphical representation of the best fit sine wave to the filtered data is represented in figure 2-33.

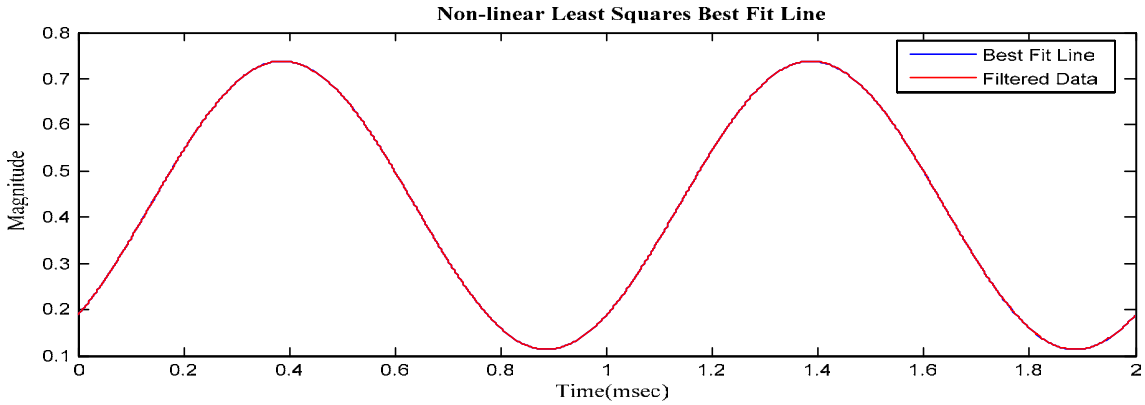


Figure 2-33: 2 msec of Best Fit Curve and Filtered Data

This figure depicts the best fit sine wave plotted on top of the filtered sine wave. As can be seen it was very difficult to distinguish any difference between the two wave forms. To illustrate the difference between the two wave forms their difference is taken (best fit – filtered data) and plotted versus time which is depicted in figure 2-34.

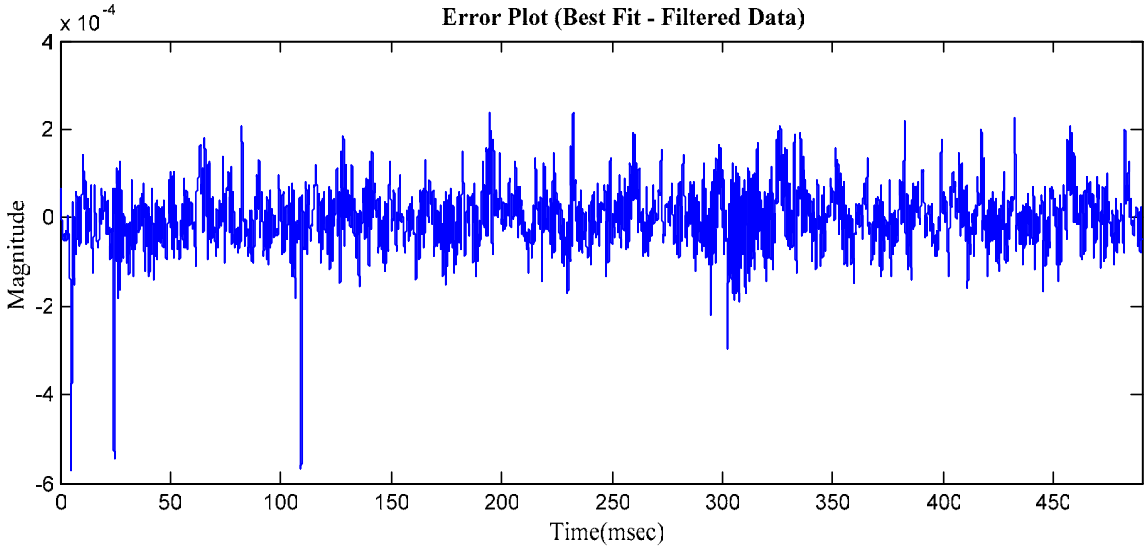


Figure 2-34: Error Plot (Best fit curve - Filtered Data)

It can be seen from this figure that error is between -0.02 and 0.02 mV. Having Matlab compute the non-linear least squares best fit curve and error plot were useful tools in analyzing different effects of the signal to noise and distortion ratio SNDR. The following section will analyze the SNDR, which makes use of the error plot to make the calculations.

2.3.5 Signal to Noise and Distortion Ratio

The signal to noise and distortion ratio calculated in this section was the ratio of the amplitude of the input signal to amplitude of the noise signals. The equation used for the SNDR was:

$$SNDR = 20\log_{10}\left(\frac{A}{E\_rms}\right) \qquad \textit{eq) 2-31}$$

The equation for *E_rms* was:

$$E\_rms = \sqrt{(mean(bfit - fd))} \qquad \textit{eq) 2-32}$$

The value *bfit* was the best fit sine wave and *fd* was the filtered data. It should be noted that the SNDR calculations preformed here were not precise, that is they did not exclude harmonics present in the input sine wave used for testing which is why it was a measure of the noise and distortion. Figure 2-35 is the FFT response of the first order Σ-Δ ADC in which a 1 kHz sine wave was inputted. From this figure the harmonics of the input tone mentioned can be seen. The source of these harmonics was not traced down, but a possible reason was due to the 12-bit resolution of the function generator being used for testing.

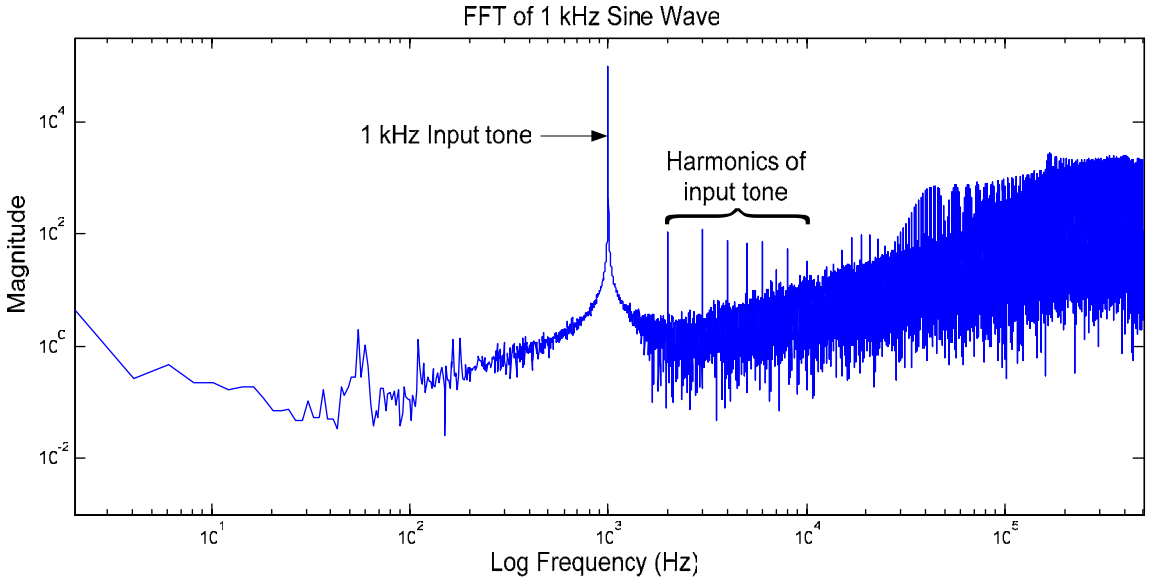


Figure 2-35: FFT of 1kHz Sine Wave

To illustrate the affect of the harmonics on the SNDR a 500 Hz sine wave with 2 V peak-peak amplitude was applied to the second order Σ-Δ ADC. The 500 Hz sine wave was then passed through the FIR lowpass filter, with order 10000, a number of times, increasing the cutoff frequency each time. From this data the SNDR was then calculated for each cutoff frequency. Table 2-3 represents this data with the cutoff frequency starting at 700 Hz up to 2 kHz.

fc (Hz)	SNDR (dB)	fc (Hz)	SNDR (dB)	fc (Hz)	SNDR (dB)	fc (Hz)	SNDR (dB)
700	87.2743	**1050**	67.2494	**1400**	64.7428	**1750**	61.0598
750	86.5597	**1100**	65.4978	**1450**	64.4056	**1800**	61.0622
800	86.0256	**1150**	64.8934	**1500**	63.481	**1850**	61.0465
850	85.349	**1200**	64.8038	**1550**	62.3124	**1900**	61.0297
900	82.8107	**1250**	64.7865	**1600**	61.4846	**1950**	61.0078
950	76.306	**1300**	64.7579	**1650**	61.1259	**2000**	60.9481
1000	70.7241	**1350**	64.7668	**1700**	61.0504		

Table 2-3: Cutoff frequency vs SNDR for 500 Hz Input Sine Wave

From this table it could be seen that with the increase of the cutoff frequency the SNDR decreased. Figure 2-36 illustrates SNDR as a function of the cutoff frequency, *fc*.

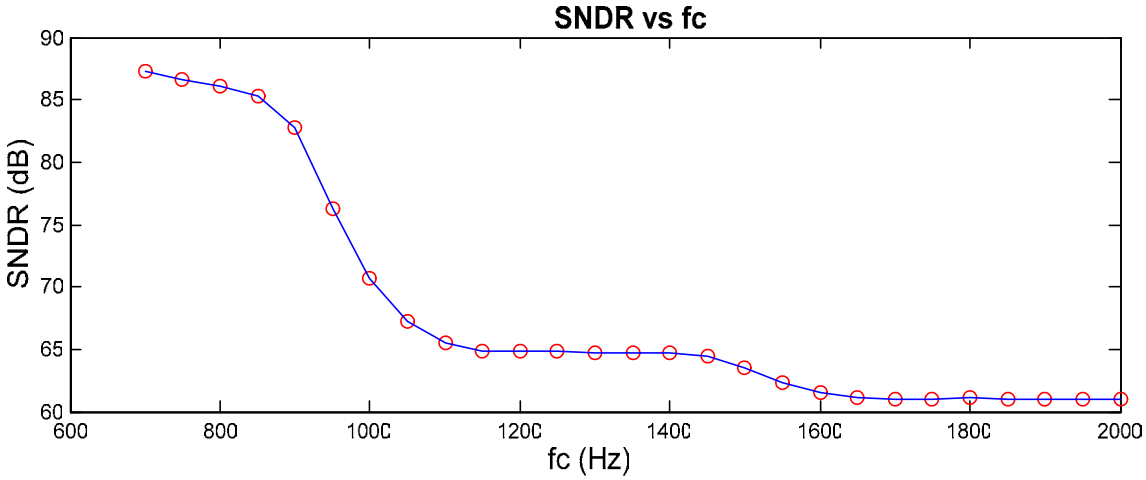


Figure 2-36: SNDR vs Cutoff Frequency

It can be seen that when the cutoff frequency moved past the first harmonic, 1000 Hz, there was a dramatic drop off in the SNDR values. There is another dip in the SNDR values after the second harmonic, 1500 Hz, ass well. This shows how the SNDR evaluation was effected by the harmonics of the input signal.

To evaluate the performance of the first and first order Σ-Δ ADCs the SNDR was calculated for both over a wide range of frequencies. Table 2-4 is the data collected for the amplitude and SNDR of the first and first order Σ-Δ ADCs over a certain frequency range.

		First Order Σ-Δ ADC		Second Order Σ-Δ ADC	
fin (hz)	**fc (Hz)**	**Amplitude (V)**	**SNDR (dB)**	**Amplitude (V)**	**SNDR (dB)**
5	100	0.4004	61.3592	0.3959	69.6694
25	100	0.3884	62.1832	0.3849	70.8169
50	200	0.3959	62.0757	0.3922	70.6343
75	300	0.4002	61.541	0.3965	69.6142
100	300	0.3999	63.5712	0.3966	70.306
150	300	0.3963	67.4193	0.3926	75.2909
200	400	0.4021	67.5316	0.3984	74.6665
250	400	0.3977	83.8462	0.3944	86.8755
300	500	0.4002	82.5238	0.3965	86.3097
400	600	0.4022	87.8415	0.3985	84.9905
500	700	0.4001	87.9695	0.3969	87.2743
600	800	0.4021	86.1392	0.3985	85.8288
700	900	0.4007	84.6201	0.3972	85.2593
800	1000	0.402	84.0787	0.3985	84.581
900	1100	0.4009	82.8362	0.3974	82.8585
1k	1200	0.4016	81.1974	0.398	83.0327
2k	2200	0.4018	74.794	0.3983	75.4392
3k	3200	0.4017	69.5408	0.3983	70.1482
4k	4200	0.4016	66.4894	0.3983	66.8398
5k	5200	0.4012	63.2842	0.3982	64.8988
6k	6200	0.4016	61.0431	0.3982	62.4709
7k	7200	0.4015	58.0543	0.3982	60.1994
8k	8200	0.4016	56.3126	0.3982	58.4905
9k	9200	0.4016	54.1606	0.3982	56.5957
10k	10200	0.4011	53.1438	0.3983	55.0532
15k	15200	0.4016	47.7813	0.3988	49.3774
20k	20200	0.4016	41.3828	0.3998	45.5879

Table 2-4: Amplitude and SNDR for First and Second Order Σ-Δ ADC

Note that *fin* was the input frequency and *fc* was the cutoff frequency of the lowpass FIR filter, both in hertz. The input signal was a 2 V peak-peak amplitude for both Σ-Δ ADCs. It could be seen that the SNDR of the first and second order Σ-Δ ADC for the frequency range of 5-100 Hz were lower then the frequency range of 150 – 2k Hz. The reason the lower frequency SNDR values were lower was because the cutoff frequency of the FIR filter was above the harmonic values of the input signals. It could also be seen that the SNDR's of the first and second order Σ-Δ ADC both began to decrease past 2 kHz. The reason for this decrease in SNDR was the input signal was getting more and more into the high frequency quantization noise. Table 2-4 also shows that SNDR values for the first and second order Σ-Δ ADC were very close until they start to decrease in the higher frequency range. It can be seen that second order Σ-Δ ADC's SNDR values in the higher frequency range were greater then that of the first order Σ-Δ ADC. This observation could be explained by looking at the NTFs of both systems, shown in figure 2-37.

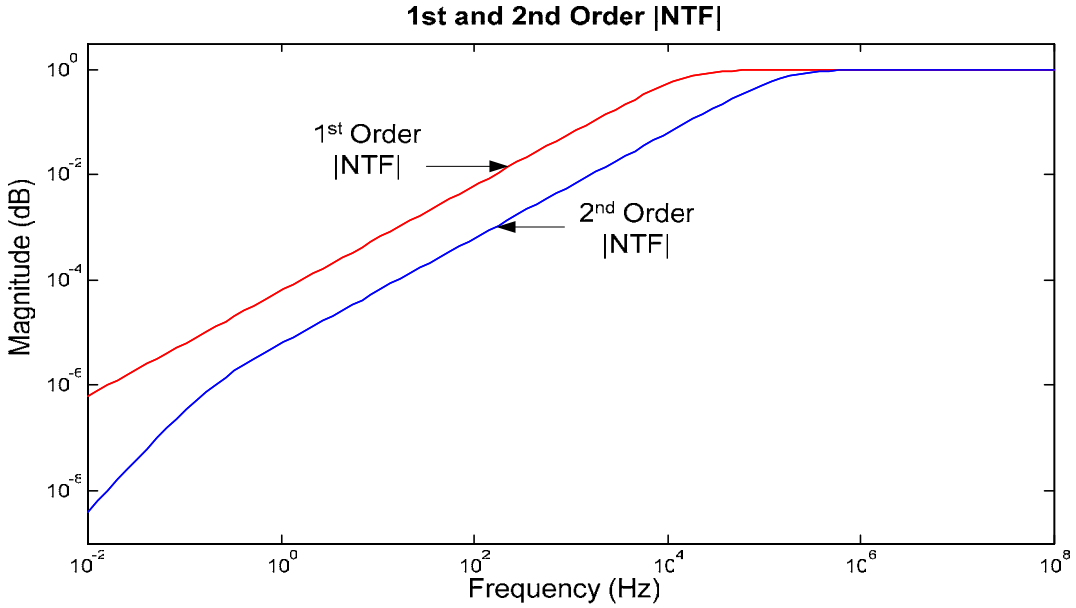


Figure 2-37: Comparison of the First and Second Order Σ-Δ ADC's |NTF|

Figure 2-37 shows that increasing the order of the Σ-Δ ADC also increased the order of the NTF highpass filter. By comparing the two transfer functions of the Σ-Δ ADCs it could first be seen that the cutoff frequency of the NTF highpass filter of the second order Σ-Δ ADC is higher then that of the first order Σ-Δ ADC. The fact that the cutoff frequency of second order NTF highpass filter was higher then the first order

indicated that it would push the quantization noise into higher frequencies then that of the first order system. The second order NTF highpass filter also had a much sharper cutoff towards the end of the cutoff slope due being a second order fitler. This effect helped push the quantization noise into higher frequencies better then the first order system. So due to the fact that the second order Σ-Δ ADC pushed the quantization noise into higher frequencies compared to the first order Σ-Δ ADC it made sense that the SNDR values for the second order system would be larger in higher frequencies then that of the first order system.

Another evaluation preformed was to find the SNDR ratios for a set number of input frequencies keeping the cutoff frequency of the FIR filter fixed. For this evaluation the frequency bandwidth for the needle EMG signal, 100 – 2000 Hz, was tested fixing the cutoff frequency of at 2200 Hz. This evaluation was preformed on the first and second order Σ-Δ ADC, with an input voltage of 2 Vpeak-peak. Table 2-5 is the data of the SNDR versus the operating frequency for both the first and second order Σ-Δ ADCs.

Operating Frequency (Hz)	SNDR	
	1st order	2nd order
100	62.2434	66.1949
200	60.8231	64.078
300	60.438	63.4656
400	60.2225	62.1932
500	60.7227	60.7006
600	59.7451	59.7003
700	59.6732	58.927
800	60.9264	61.4849
900	60.9518	60.6284
1000	61.939	59.9491
1100	66.9942	65.2471
1200	74.5814	74.5093
1300	74.2971	74.9781
1400	74.1664	75.0087
1500	74.6812	74.3805
1600	74.6308	75.4074
1700	75.4763	74.3744
1800	74.0698	75.0793
1900	74.6393	75.3699
2000	74.794	75.4393
Note: cuttoff frequency was 2200 Hz		

Table 2-5: SNDR vs Operating Frequency

Figure 2-38 is the plot of this data.

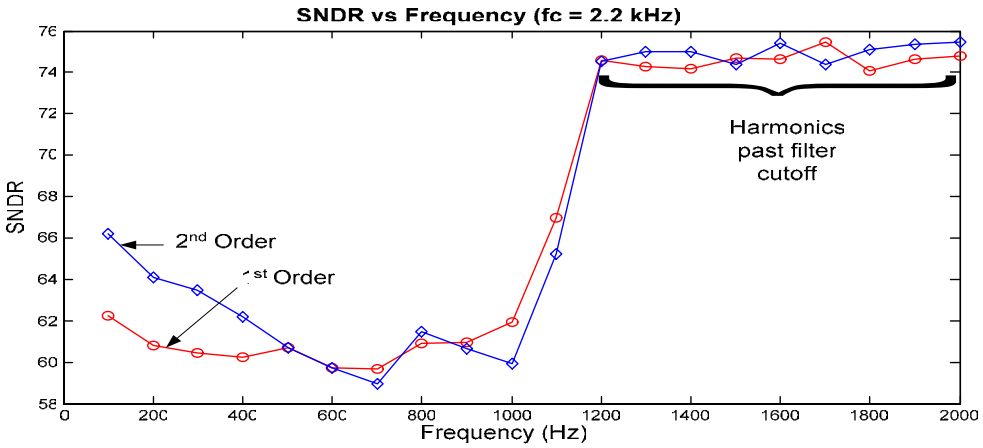


Figure 2-38: SNDR vs Input Frequency

Figure 2-38 further illustrated the effects of the harmonics on the SNDR value. It could be seen that after 1200 Hz the SNDR increased by around 24 dB, which showed that once the harmonics of the input signal passed the cutoff frequency it had a dramatic effect on the SNDR. Since the effects of the harmonics led to a somewhat inclusive evaluation of the SNR of the Σ-Δ ADC systems it was beneficial to take a more qualitative approach to determine if the second order Σ-Δ ADC would truly have 16 bits worth of resolution. Taking a look at the FFT of the 500 Hz input after FIR filtering with a cutoff frequency of 2200 Hz, figure 2-39 shows that the noise floor was 99.8 dB below the input tone.

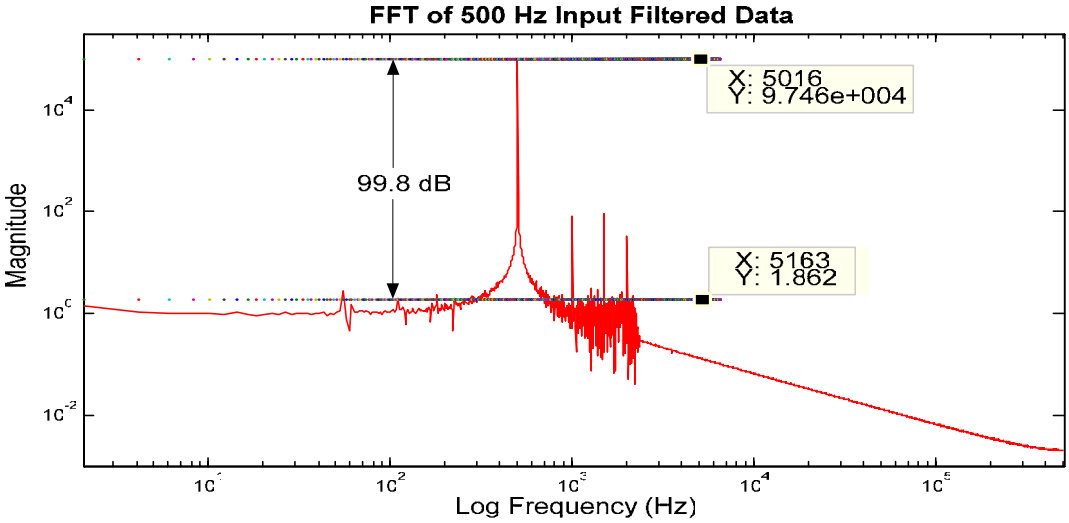


Figure 2-39: FFT of 500 Hz Input Filtered Data

Figure 2-39 shows that ignoring the harmonics of the input signal the noise floor was well below the input tone signifying that the second order Σ-Δ ADC did have a resolution of 16 bits. Although an accurate evaluation of the SNR of the systems was not able to be

obtained due to the harmonics of the signal, the process for obtaining those values was developed. In future work if the harmonics could be eliminated the method for obtaining SNR values for the Σ-Δ ADC systems has been developed.

3 INTEGRATED CIRCUIT DESIGN

Second goal of this project was to integrate all the breadboard components together and scale down into one single IC. However, due to time constraint, and have a better understanding of Σ-Δ ADC algorithm on both Analog Breadboard and IC Designs, the chip was decided not to be fabricated, although switched-capacitor integrator was the only component the being designed, and simulated. Since it is used in both 1st and 2nd order of Σ-Δ ADC, so it is an important part for the chip. The design, simulation, and testing were performed on the Computer Aided Design Software, Cadence Virtuoso. Since the IC was intended to be fabricated under MOSIS design processes, NCSU 1.6μm process library and SpectreS simulator were used in order to correspond to the fabrication process. For more information about MOSIS design process, please visit http://www.mosis.com.

The report for IC design will be broken down into Design and Analysis, Implementations and Results, Layout Design, and Final Simulation and Comparison.

In Design and Analysis, the first section will introduce the basic knowledge of Metal Oxide Semiconductor Field Effect Transistor (MOSFET). After the basic explanation of a transistor, simulations of the differential inputs single-ended output op amp that was chosen from the reference book (Martin p.296) would be discussed and examined. The reason to simulate an op amp from a reference book, because it could be a good foundation to design the op amp for the switched-capacitor integrator and it would be a practice simulation to get familiarize with the CAD software.

In Implementations and Results section, the design process of the Fully Differential Folded Cascode op amp (FDFC) as well as the transistor sizing process would be discussed. Also the simulation results for components of the op amp would also be investigated. After that the design, simulation and analyzation of the switched-capacitor integrator will be examined in this section.

All the design in the sections above were designed in schematic level, however, the fabrication process requires the layout level design, so transformation from layout level design was required to transform from schematic level design, and this transformation will be discussed in this section.

In Final Simulation and Comparison section, the simulation of the layout design was examined and compared with the simulation obtained in schematic level design.

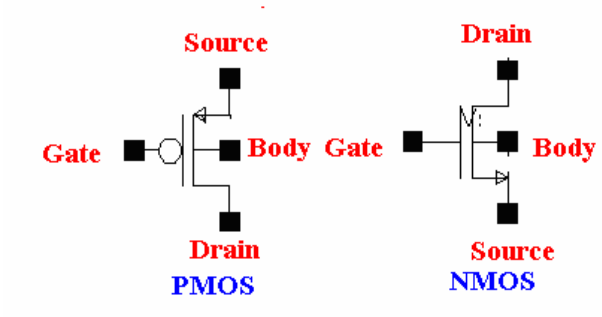
The conclusion and Future work of IC design will be discussed in the last two sections along with the conclusion and future work of Analog Breadboard Design.

3.1 Design and Analysis

This section will go through the fundamental knowledge of MOSFET, so reader would have basic knowledge about MOSFET. Then the differential single-ended op-amp, also known as Folded Cascode (FC) op amp, would be introduced, simulated and analyzed. Base on the performance of the FC op amp, the FDFC op amp would be implemented.

3.1.1 Transistors

The most popular technology for realizing microcircuits makes use of Metal Oxide Semiconductor Field Effect Transistor (MOSFET). MOS circuits use two complementary types of transistors, n-channel and p-channel. N-channel devices conduct with a positive gate voltage while p-channel devices conduct with a negative gate voltage. Moreover, electrons are used to conduct current in n-channel transistors, while holes are used in p-channel transistors (Martin p.16-18). The symbols of PMOS and NMOS in Cadence are represented as below,



There are three major characteristics for PMOS and NMOS. These characteristics are named as, cutoff, triode, and active. These three characteristics are controlled by the gate, drain, source, and threshold voltages. Threshold voltage is the minimum gate to channel voltage needed for n or p carriers in the channel to exist. The relationship and

behavior of gates, drain, source, and threshold voltages can be shown in Table 3-1 (McNeill). With different configuration and different combinations of PMOS and NMOS, they can work as resistors, capacitors, amplifiers, etc.

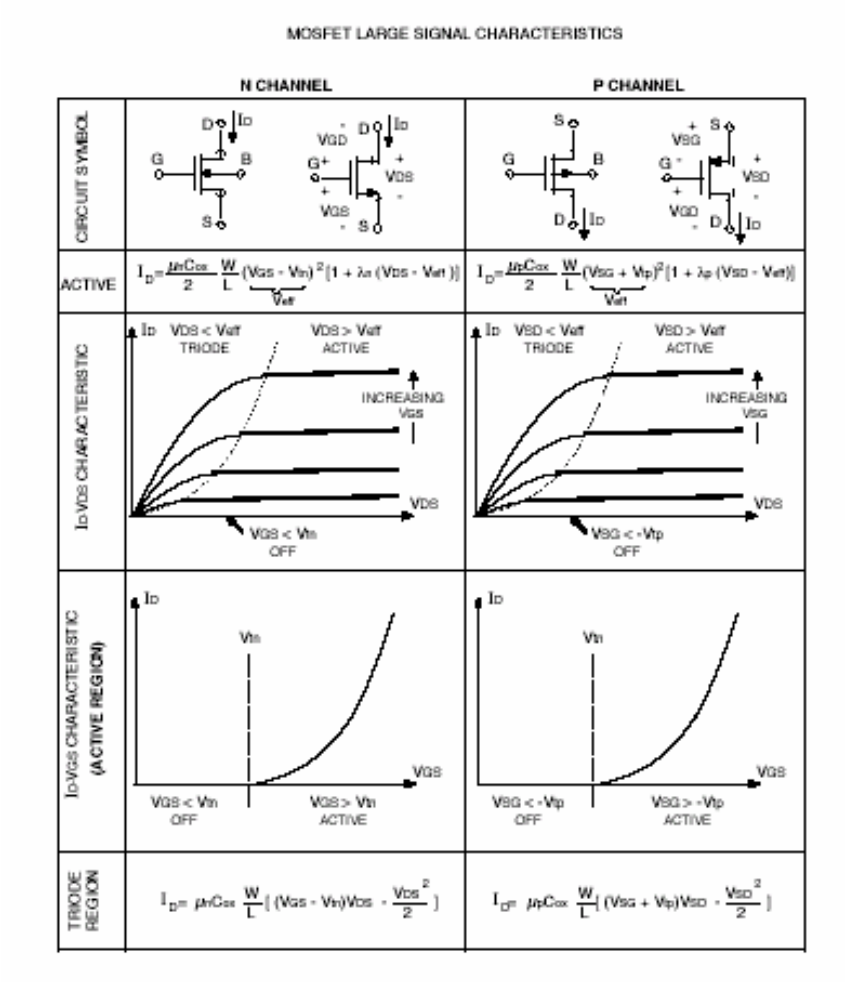


Table 3-1: Characteristic of PMOS and NMOS

3.1.2 Folded Cascode (FC) Op amp

The first step was to obtain an existing op-amp design that was suitable to the project application as a reference, and the Folded Cascode op amp was chosen as the reference (Martin p.296). Although FC op amp was a differential inputs and single ended output op-amp, this op-amp was a good foundation for implementing a fully differential op-amp. The reason to choose this op amp was because all the current mirrors in the op amp were wide swing cascode current mirrors. These mirror resulted in high output

impedance for the mirrors, thereby maximizing the DC gain of the op-amp. The schematic of Folded Cascode Op-amp is shown in Figure 3-1.

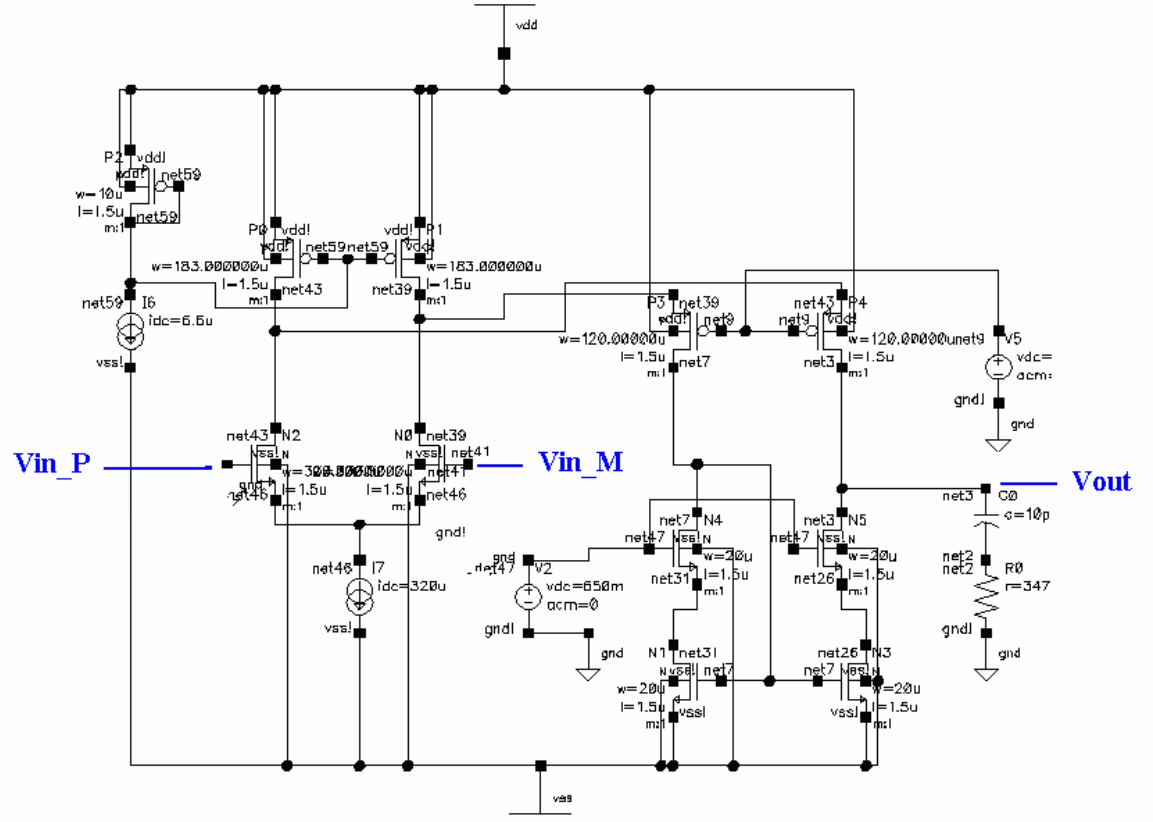


Figure 3-1: The schematic of Folded Cascode Op-amp

This op amp was built and simulated in Cadence. Since this op amp was only a reference, the current sources were not concerned in the op amp. the only concern was the opan loop gain, as the gain has a great impact on the bit resolution of the ADC, the impact will be discussed later on. DC analysis was performed and showed that there was small offset voltage appeared at the output while the differential inputs was set equal to zero (Figure 3-2). DC analysis is set to sweep at the inputs in a range of voltages; then observe the behavior of the output signals. In this analysis, the input voltage was sweep from -2.5V to 2.5V to obtain the behavior of output voltage. Figure 3-2 is the zoomed-in version of DC Analysis, offset voltage was obtained when the input voltages were 0V. The cause of offset voltage will be discussed in the next section.

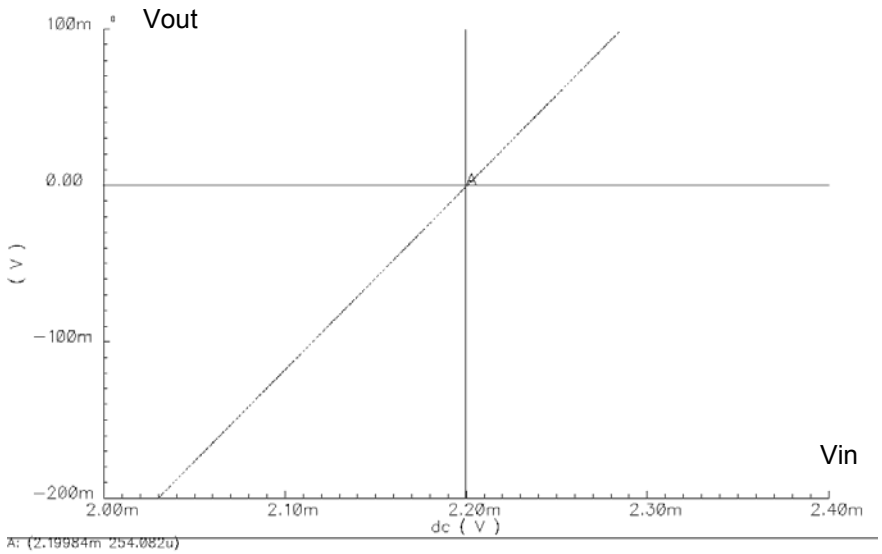


Figure 3-2: DC Analysis of FC op amp; offset = 2.2mV

AC analysis indicated that the open loop gain of the op-amp was not high enough (61dB ≈ 1122) for the project application (Figure 3-3). Since the desired open loop gain for 16 bits resolution for the ADC is calculated as below,

$$\frac{1}{gain} = \frac{1}{2^N}$$, where N is the number of bits (Martin p.564) *eq)3-1*

$$\frac{1}{1122} >> \frac{1}{2^{16}}$$

Therefore, the gain requires at least 90dB, so modification of the op amp is needed.

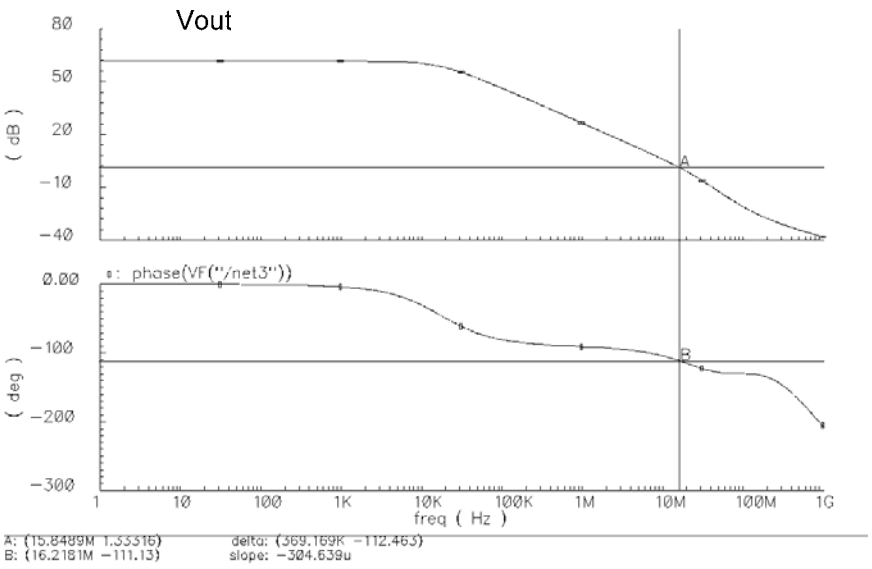


Figure 3-3: AC Analysis of FC op amp; the gain = 61dB and phase margin = 68º

To confirm the simulated gain and the expected gain of the op amp, the following equation was carried out from the reference book. The equations are referred to the op amp in Figure 3-1 to calculate the open loop gain of the op amp (Martin p.269).

Av = gain

Gm1 = the transconductance of differential pair N0, N2

Z = impedance to ground seen at the output node

$$A_V = \frac{V_{out}(s)}{V_{in}(s)} = g_{m1} Z_L(s) = \frac{g_{m1} r_{out}}{1 + s r_{out} C_L} \qquad \textit{eq) 3-2}$$

Rout = output impedance of the op amp

As frequency increases, the load capacitance dominates, and then Av can be simplified as follow,

$$A_V = \frac{g_{m1}}{sC_L} \qquad \textit{eq) 3-3}$$

The calculated gain = 70dB while the simulated gain was only 61dB

3.2 Implementations and Results

This section will introduce the design process of the FDFC op amp in detail as well as the process of choosing the correct sizes of the transistors. There are lots of modifications towards to FDFC op amp comparing to the FC op amp. Also the current sources that appeared in FC op amp would be replaced by other combinations of transistors, which is known as current mirror, to generate the same currents for the op amp. Further discussion will be held in later sections.

3.2.1 Transistor Sizing

Since there were gain variations between the reference and the simulated gain, also the gain did not meet the minimum requirement, it was necessary to re-design the op amp, and modify the sizes of the transistors based on the design of FC op amp. In order to keep a transistor in its active region, it has to meet the following requirement,

$V_G > V_t$

$V_{effective} = V_G - V_t$

$V_{DS} > V_{effective}$

, where V_{DS} = drain to source voltage, V_G = gate voltage V_t = threshold voltage.

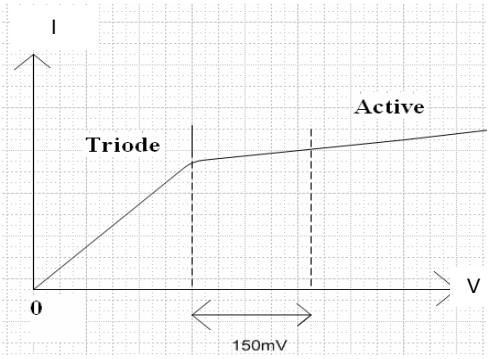


Figure 3-4: MOSFET behavior: Drain voltage vs. Current

Therefore, the following parameters are set for the FDFC op-amp design in order to keep the transistors in active region.

$V_{effective} = V_G - V_t \approx 200mV$

$V_{DS} \approx 350mV$

The parameters for the transistors from Cadence are as follow,

V_{tn}	V_{tp}	μ_n	μ_p	C_{ox}
.65V	-.85V	640 m^2/Vs	268.45 m^2/Vs	1.1345E-3pF/(um)^2

The parameters obtained from FC op-amp are as follow,

The supply voltage = ±2.5V

Current source = 320uA

Based on the parameters from FC op amp, the threshold voltage, and the desired $V_{effective}$ and V_D, then the sizes of the transistors of FDFC op amp could be calculated. The simple structure of FDFC op amp was designed in Figure 3-5. The figure is only used to show how to develop the sizes of the transistors, thus, only half of the op-amp is shown for better illustration; the whole op-amp design is shown in the next session.

Substitute the parameters into Square Law below and solve for W/L; the sizes of the transistors can be obtained.

$$I_D = \mu_n C_{OX} \frac{W}{L}[(V_{GS} - V_{tn})V_{DS} - \frac{V_{DS}^2}{2}] \qquad \textit{eq)3-3}$$

Use transistor P1 in Figure 3-5 as example, when Vdd =2.5V and Id = 320uA, the voltage across drain to source is assumed = .35V, V effective = .2V. W/L can then be solved by plugging in all the values into Square Law.

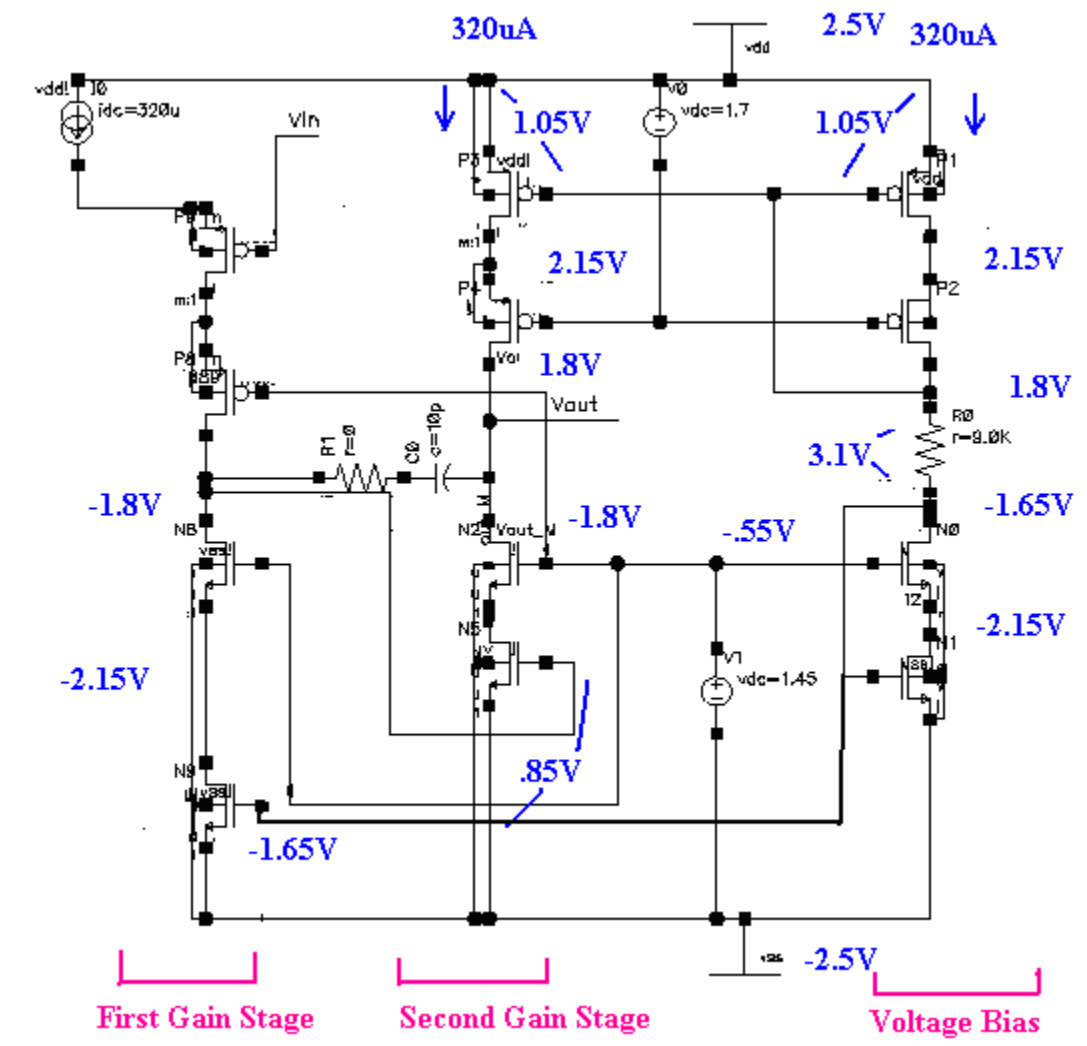


Figure 3-5: ½ of FDFC Op-amp

For better accuracy, DC sweep on the width of the transistor in Cadence to obtain the best width with the set up in Figure 3-6. The rest of the sizes of the transistors are shown in Figure 3-7.

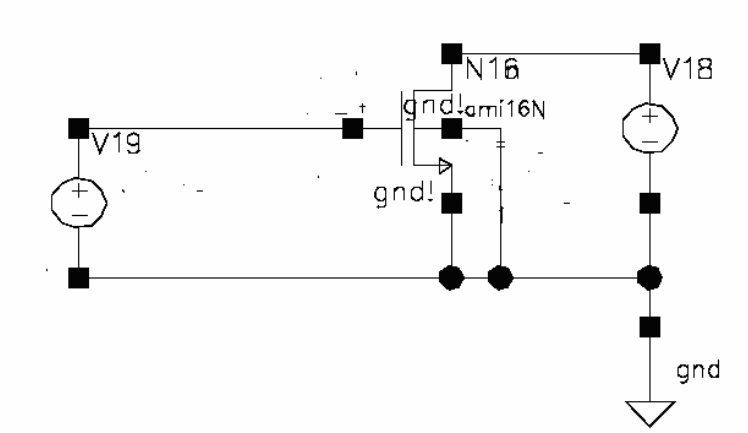


Figure 3-6: An example to obtain the desired size of the NMOS by using DC sweep

3.2.2 Fully Differential Folded Cascode (FDFC) Op amp with ideal Common-Mode Feedback Circuitry (CMFB)

It is desirable to keep the signals fully differential in most analog applications. Fully differential signals imply that the difference between two lines represents the signal component (Martin p.414), and the advantage with using of FDFC op amp is to help reject noise on those input signals. Regarding our project applications, the noise coming from the input signals will affect both signal paths. The noise that affects both input paths is identical, and will be rejected by this differential characteristic. In other words, the noise will have no effects on the differential signals since both sides of the signals see the same noise. This fully differential version op amp is essentially two copies of the FC op amp. Although the fully differential op amp will consume more space for layout design than single-ended output op amp, fully differential op amp can provide twice amount of voltage swing on the signals than single-ended output op amp. For example, if single ended signals are limited to ±1V, then the maximum swing of the signal is 2V. However, it is 4V for fully differential op amp. (Martin p.414) Therefore, the maximum of the signal swing for FDFC op amp is 5V and FC op amp is only 2.5V

However, one drawback of using FDFC op-amp is that a common-mode feedback (CMFB) circuit must be used. The CMFB stabilizes the common-mode voltage, which is about half way between the power-supply voltages. The CMFB also limits the maximum voltage swing on the output signals.

At this early stage of design status, two Voltage Control Current Source (VCVS) were used as the substitutes for the CMFB, so the CMFB would keep the op amp performed correctly. Regardless of some of the limitations just mentioned, the op amp could reject the common noise coming from the input signals. Figure 3-7 is the schematic of the FDFC op amp.

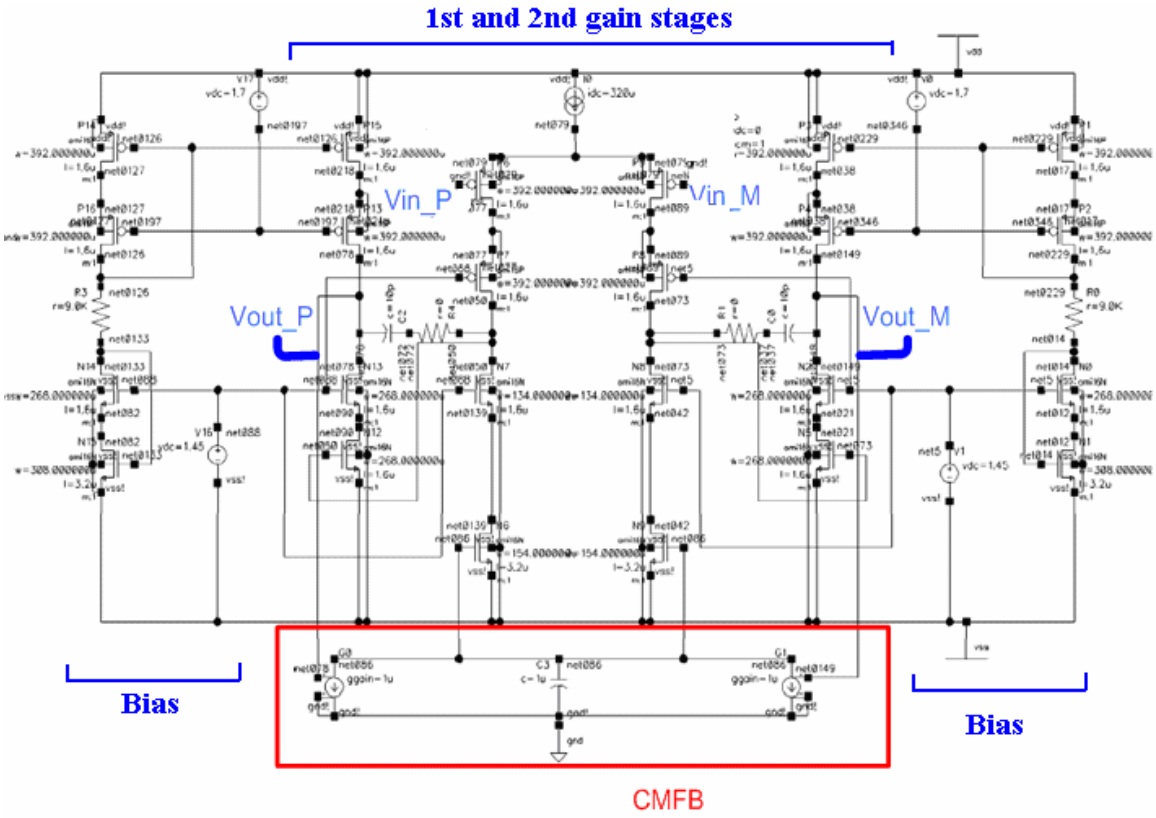


Figure 3-7: Schematics for Fully Differential Folded-Cascode Op amp with ideal CMFB

Figure 3-7 is the schematic of FDFC op amp with ideal CMFB. This op amp configuration was only for performance testing, so notice there are current sources and voltage sources in the op amp at this stage; they will be replaced after the performance testing performed. All the functionalities of each individual transistor will be discussed in the next section.

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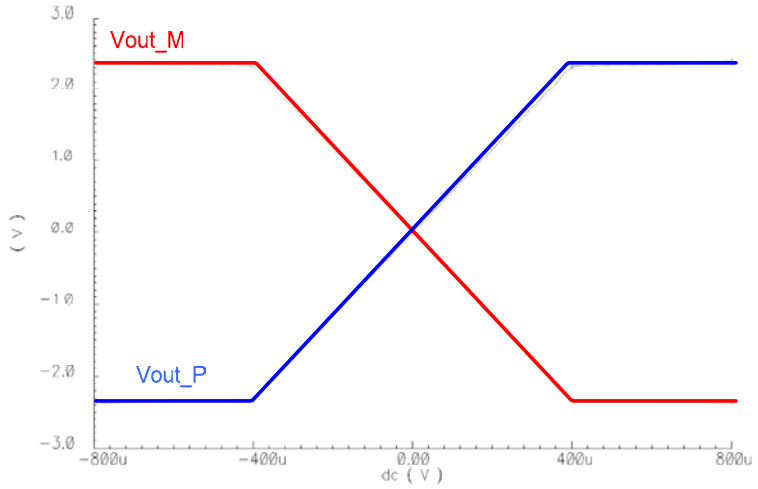


Figure 3-8: DC Analysis of FDFC Op amp

With the re-sized transistors op amp, the performance of the FDFC op amp was simulated using DC Analysis and AC analysis.

Figure 3-8 shows that the FCFB Op-amp functioned correctly, because the CMFB pulls the output voltages back into 0V when the inputs were 0V.

Figure 3-9 shows the performance of the op amp. AC analysis shows that the open loop gain = 96dB, which was capable for the project application as 16 bit resolution was needed. The relationship between bit resolutions and open loop gain is shown below,

$$\frac{1}{gain} = \frac{1}{2^N}$$

$$\frac{1}{70k} = .000014 \le \frac{1}{2^{16}}$$

, where N is the number of bits (Martin p.564) *eq)3-4*

Also the unity gain frequency = 9.3MHz, and the phase margin = 70º, which showed that the op amp was stable under its operating condition.

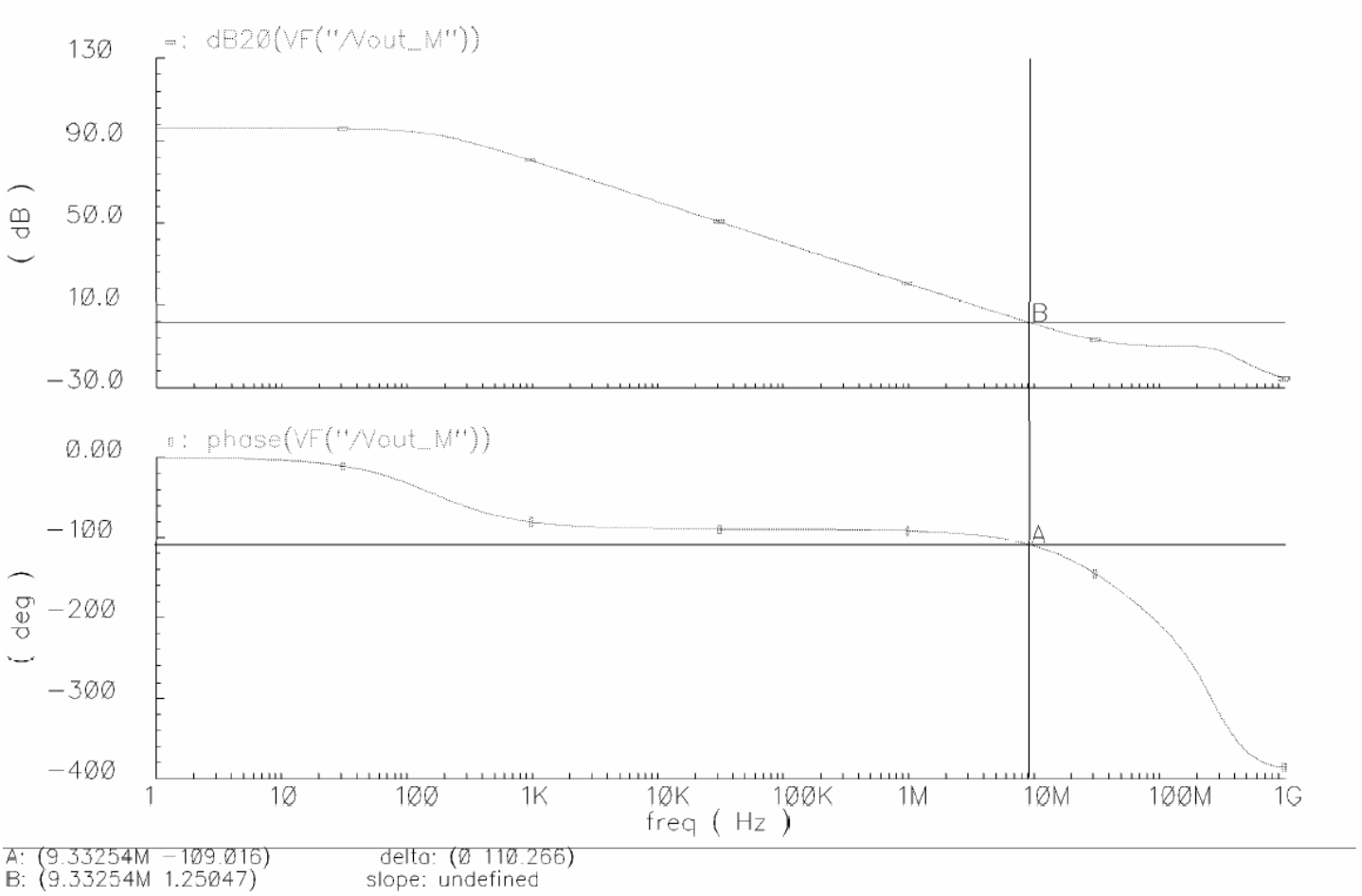


Figure 3-9: AC Analysis of FDFC Op amp

3.2.3 Fully Differential Two stage Cascode Op amp with designed Common-Mode Feedback Circuitry (CMFB)

After the open loop gain of the op amp was taken care of, the ideal components will be replaced one by one. Firstly, the CMFB would be replaced from VCVS to a real circuitry. As stated in the last section, the purpose of having CMFB when using fully differential op amp is to retain the common-mode voltage. As shown in Figure 3-10, a feedback path from the op amp outputs is used to limit the common-mode voltage. The output signal is compared with the reference voltage. The CMFB sees difference and controls the common-mode. Figure 3-10 also shows the top level schematic of the whole op amp design.

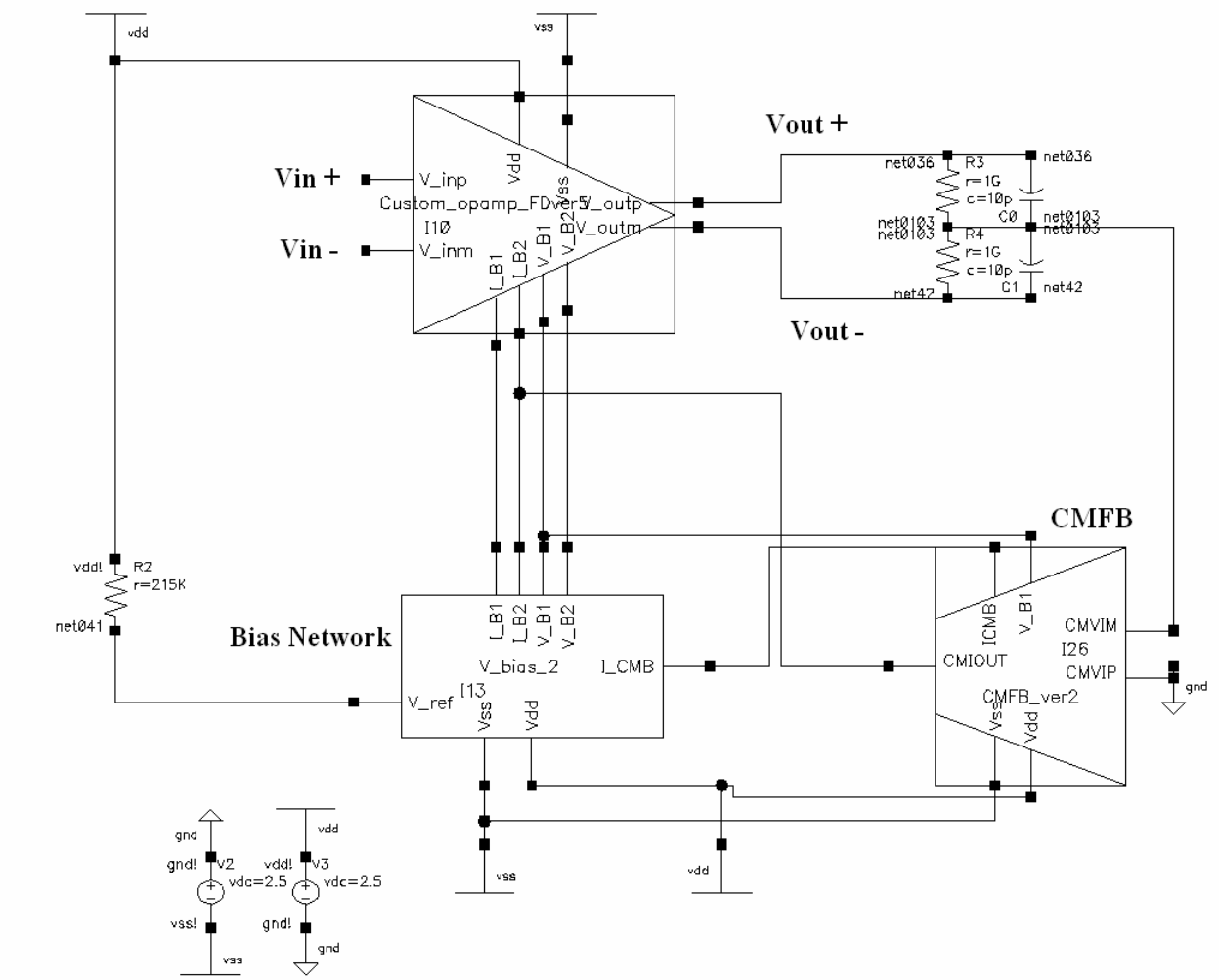


Figure 3-10: Top view of Fully Differential Two stages Cascode Op amp with designed CMFB

Two 1GΩ resistors were placed at the outputs in order to trick the simulator so that it would know two capacitors are in series, it is unnecessary in real application. R2 was used as R_{bias} so that the bias voltages for the whole system could be adjusted based on the resistance values.

3.2.3.1 Input Offset Voltage

If the inputs of the op-amp are tied together, the output voltages ideally would be 0V. Zero offset is hardly to achieve in actual applications as the structure of the op-amp is not perfectly symmetric and there could be some minor errors with sizing in the fabrication process. The offset voltage is due to the mismatched loads, differences in transistor sizes, and threshold voltages. The minimal offset voltage that is acceptable

depends on the op-amp application. In this project, 2nd order of Σ-Δ ADC would subtract the DC offset of the system, so minimal offset voltage is tolerable.

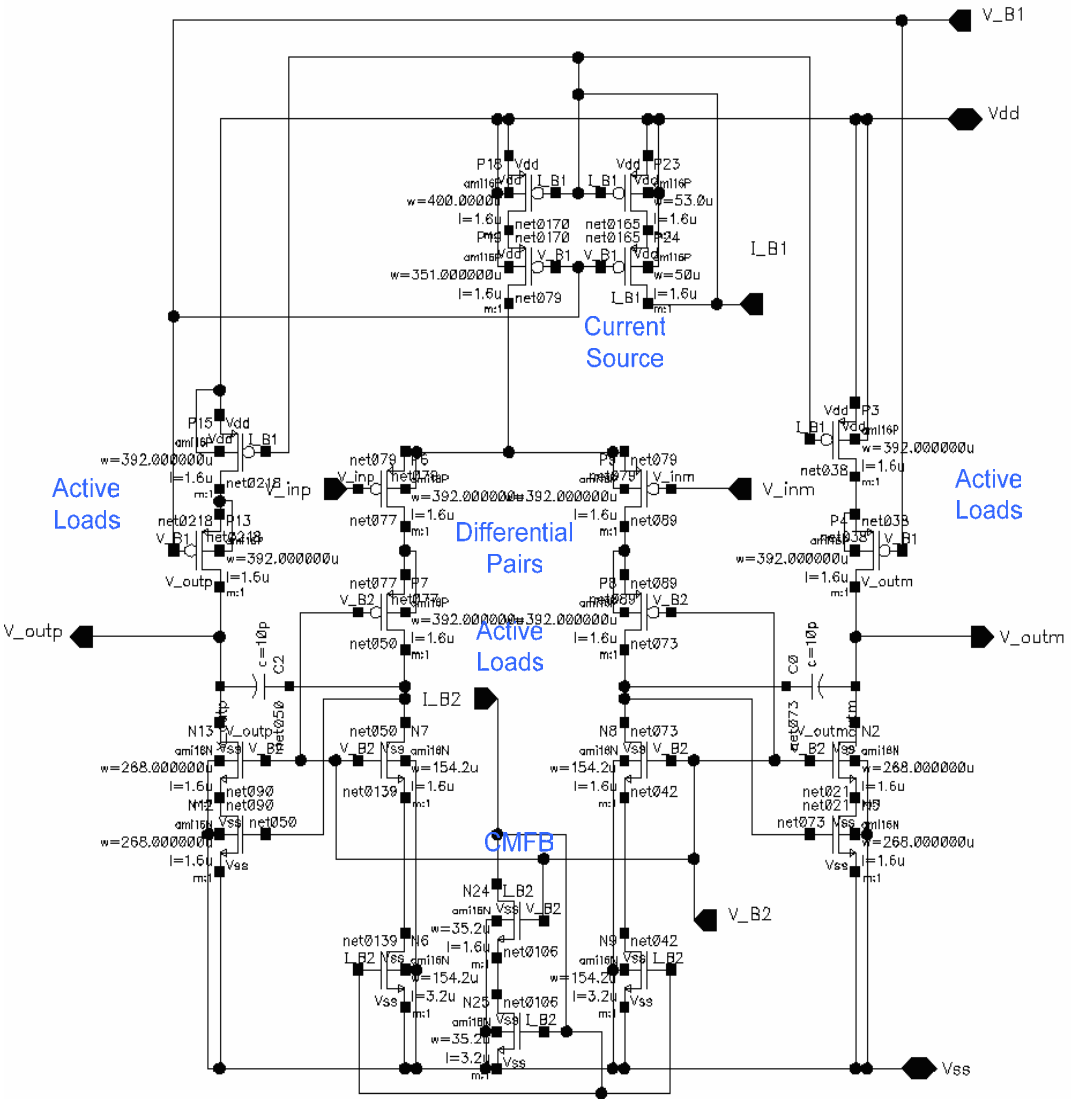


Figure 3-11: Schematic view of Fully Differential Two stages Cascode Op amp

3.2.3.2 PMOS Current Source

To provide a Bias current to the differential pair, transistors P18, P19, P23, and P24 (Figure3-11) were used as current source for the op-amp P23 and P24 were used to deliver 40µA to the op-amp. P18 and P19 current mirrored 40µA to 320µA by the ratio of the sizes of the transistors.

3.2.3.3 Differential Pairs

The PMOS input differential pairs served as the first stage of the amplifier (P6 and P9 in Figure 3-11) that was designed to draw 160μA from the current source when in equilibrium. The transistors were equally sized on both ladders of transistors to provide the same output ability.

3.2.3.4 Active Loads

P7, P8, N7, N8, P3, P4, P15, and P13 (Figure3-11) were served as active loads. They were used to increase the output impedance as they cascode together with other transistors. N5 and N12 were the 2nd gain stage of the op amp.

3.2.3.5 Capacitor Compensation

To set the correct pole for the amplifier, capacitors with two 10pF capacitors were added to the outputs, which is also known as Miller compensation. Also N2 and N13 (Figure3-11) were cascode with N5 and N12 (Figure3-11) to increase the output impendence of the 2nd gain stage.

3.2.3.6 Common-mode Feedback components inside the op-amp

N24 and N25 (Figure 3-11) served as the current mirrors for CMFB so that the op-amp would function properly. For example, if the voltage of either one of input transistor ladder goes down, without the CMFB the output voltage would go even lower because of the imbalanced voltages on the other side of transistor ladder. In this case, the job of CMFB is to limit the drop of the voltage on either side of transistor ladder when the input voltages are changing. CMFB would adjust the gate voltage of the transistors N6, N9, so it would balance voltage levels for both transistor ladders.

The AC analysis is shown in Figure 3-12 that the open loop gain = 96dB and $f_T = 9.3MHz$, which was the same result with using ideal CMFB.

Phase margin = 55º shows that the op-amp is stable throughout its working range.

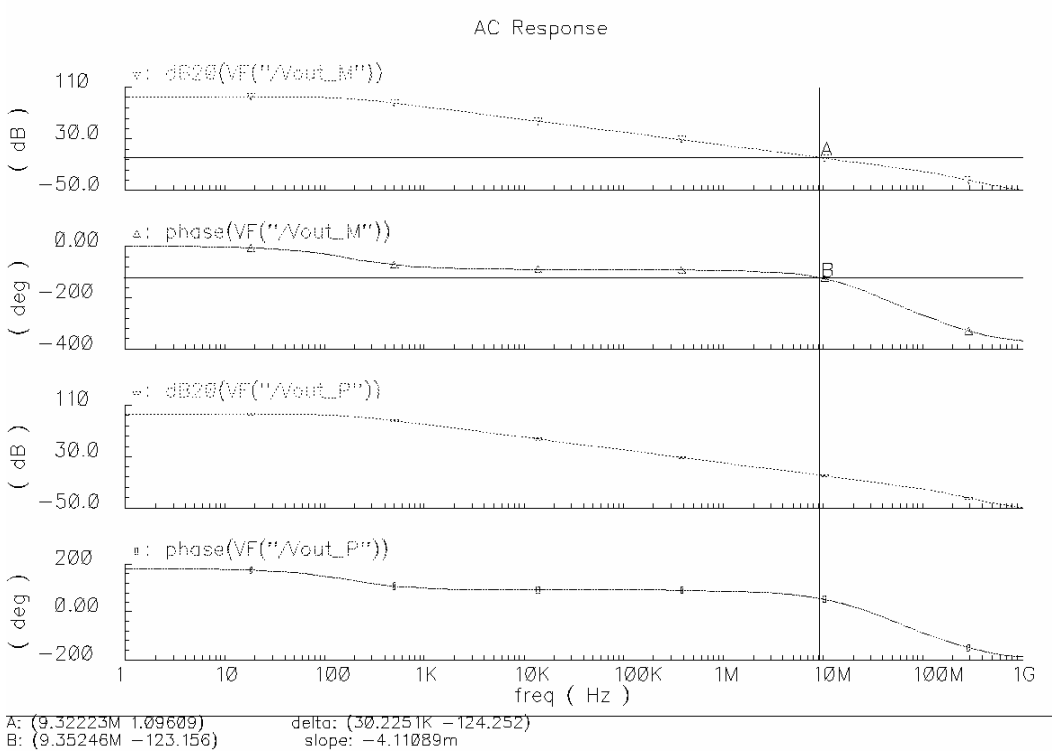


Figure 3-12: AC analysis for FDFC op amp

The DC response of the op-amp is shown in Figure 3-13 as the Common-mode (CM) voltage swings from -2.5V to 2.5V. Notice the CMFB functioned probably.

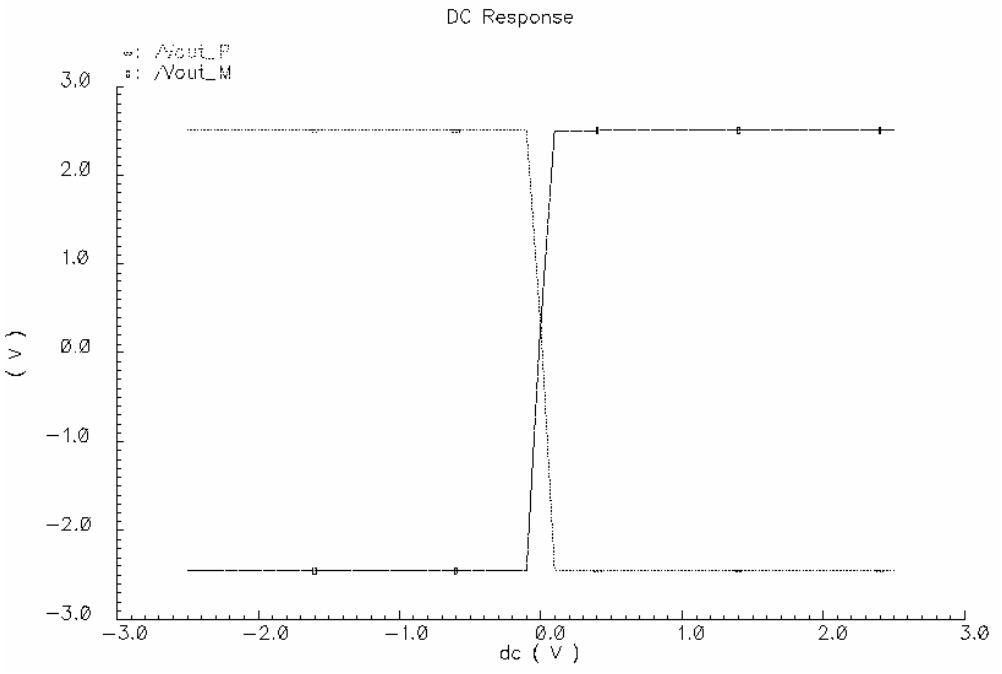


Figure 3-13: DC Response of FDFC op-amp

3.2.4 Bias Network

In order to have the transistors stay in active region, gate voltages were supplied from a separate block of circuitry, instead of building next to the op amp. Voltage sources are not preferable to implement close to the op-amp area as it would increase the fabrication error. Thus, a separate area for implementing the bias voltage network is necessary. The schematic level view of Bias Network is shown in Figure 3-14.

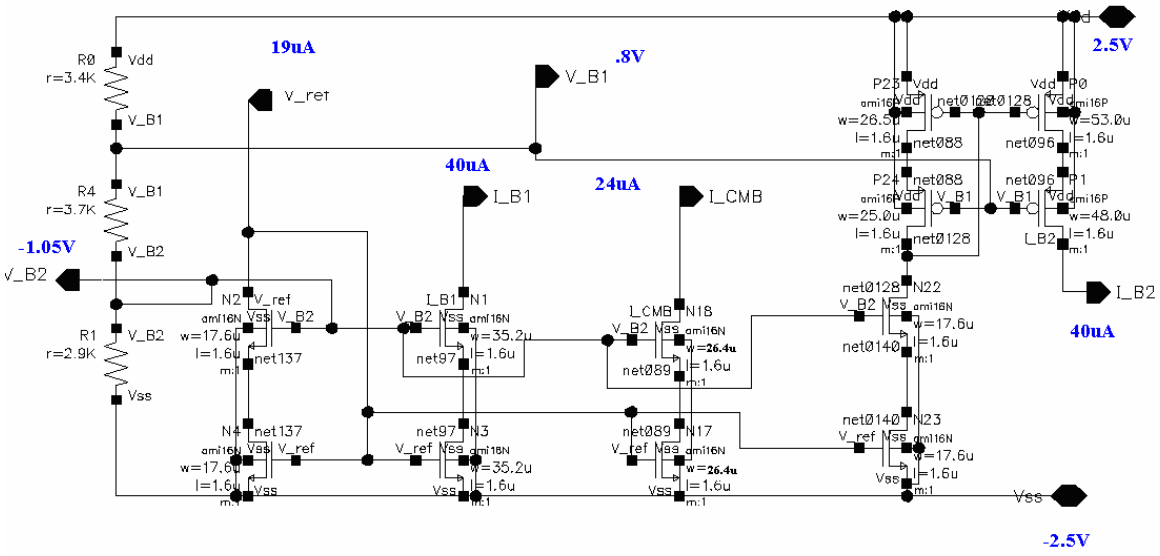


Figure 3-14: Schematic level view of Bias Network

V_B1 supplied .8V to keep the PMOS P3, P14 (Figure 3-11) in active region while V_B2 supplied -1.05V to keep the NMOS in N2, N8, N7, N13, and N23 (Figure 3-11) in active region for the op-amp.V_B1 and V_B2 were generated by using voltage divider with R0, R4, and R1. V_ref is controlled by the R2 (Figure 3-10), so as the V_ref changes, all the supplies voltages and currents that fed into the op-amp would change. The V_ref was the precaution when some minor errors for the sizes of the transistors occurred during fabrications. I_B1 was to supply current to the op-amp for the current

source. I_B2 was to supply current to the CMFB route into the op-amp as the base current to maintain N25, N6, and N9 (Figure 3-11) in active region.
I_CMB was to supply current to the CMFB op amp for the current source.

3.2.5 Common-mode Feedback (CMFB) Circuitry

After the Bias was separated from the op amp, the CMFB will be designed; Figure 3-15 is the schematic of the whole CMFB design. The major component of the CMFB is an op amp that served as a comparator comparing to the difference of the output signals and the reference voltage.

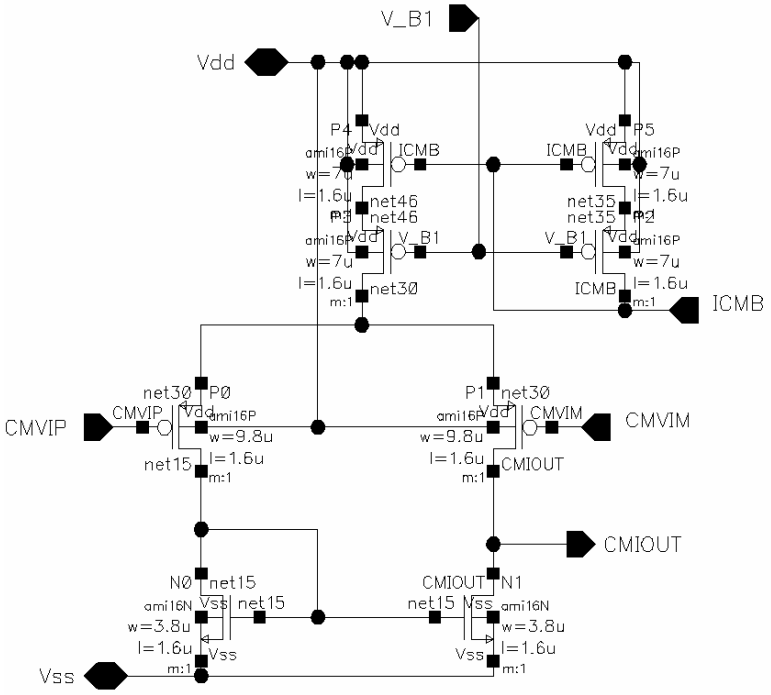


Figure 3-15 : Schematic of CMFB differential op amp with single-ended output

The reference voltage was preset to ground. If there was a difference between output voltages, then the CMFB draws a proportion current to adjust the transistor (N9, N6 in Figure 3-11) inside the op amp so that it limits the flow of the currents. P2, P3, P4, P5 in Figure 3-15 are used as current source to provide 20μA of current to the op amp. P0 and P1 in Figure 3-15 were the differential pairs and served as a gain stage for the CMFB op amp. N0 and N1 in Figure 3-15 are the active loads for the differential pair. The open

loop gain is shown in Figure 3-16. Although the gain is insignificant, it has enough gain to achieve the goal of being a comparator and balance the common-mode voltages.

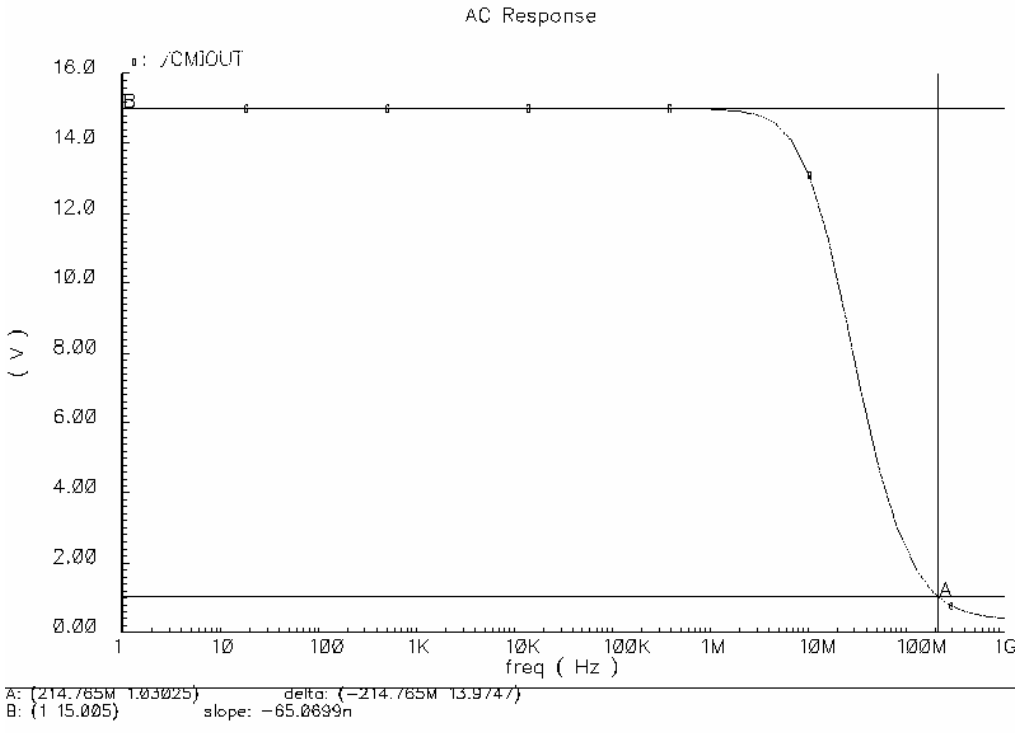


Figure 3-16 : AC Response of CMFB op amp

CMFB circuitry would hold the common-mode voltage from -1V to .7V. Figure 3-17 shows that when CM voltage is set to 0 V, then the differential-mode voltage was sweep from -2.5V to 2.5V, the common-mode voltage would then stay at zero.

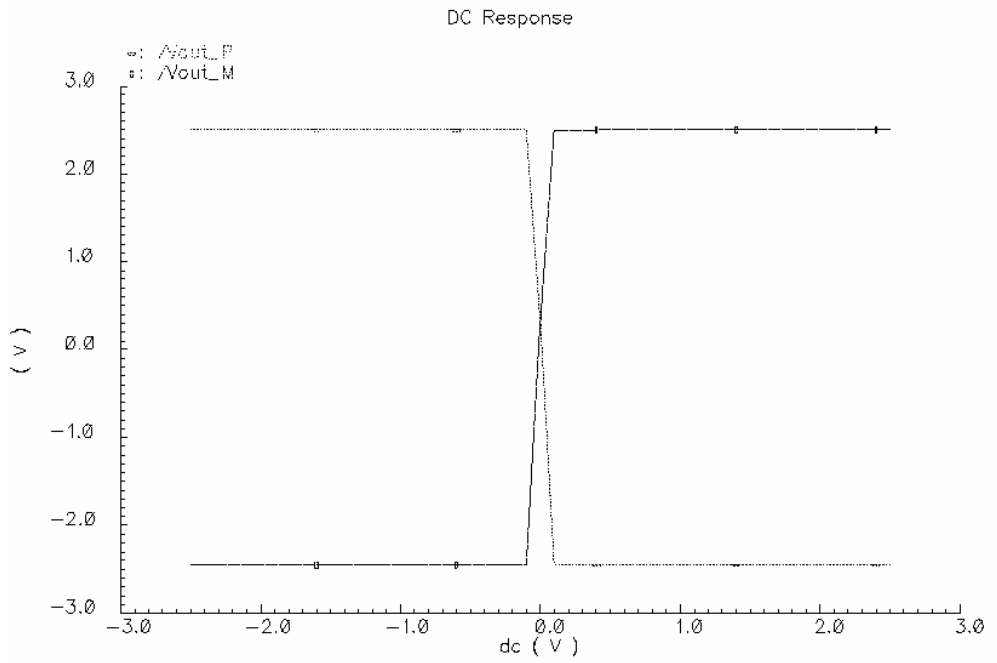


Figure 3-17: DC Response of FDFC op amp with CMFB, sweeping the CM voltage

Figure 3-18 shows the same response without CMFB connected (disconnect the CMIOUT). Without CMFB, the output would drift away at 0V.

Another advantage of having CMFB is that the offset voltage could be minimized by adjusting the reference voltage of the CMFB. Even though the structure of the op amp was asymmetry, the reference voltage could reduce the offset voltage.

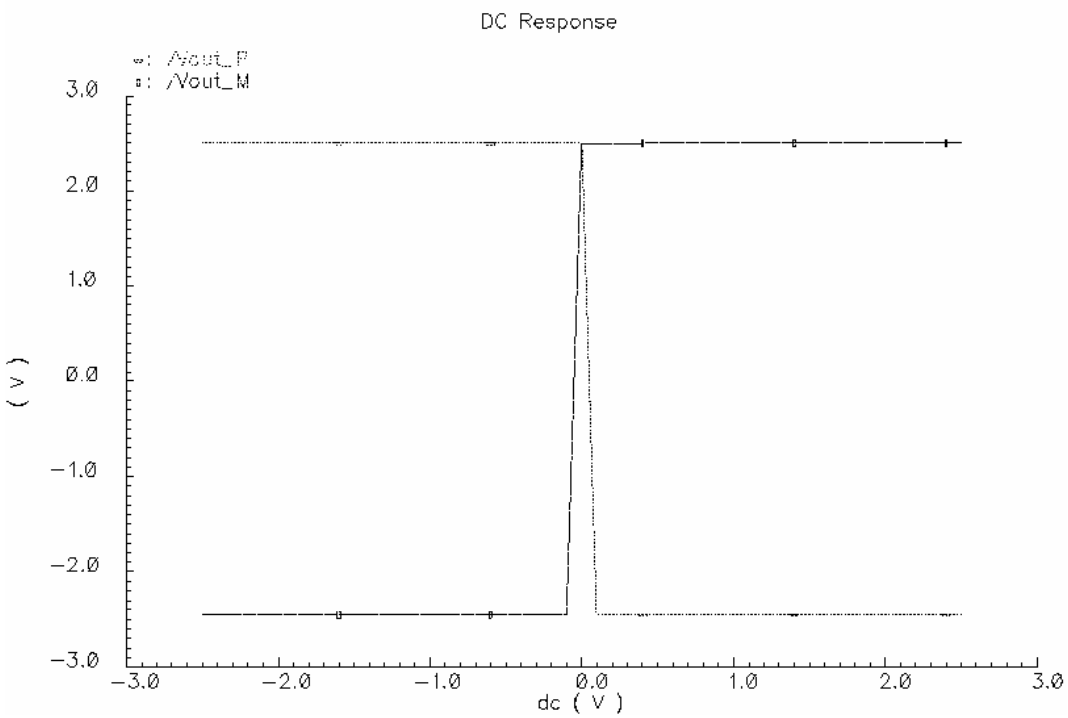


Figure 3-18: DC Response of FDFC op amp without CMFB, sweeping CM voltage

3.2.6 Switched-Capacitor Integrator

After the completion of the FDFC op amp design switched-capacitor integrator is ready to be implemented. Switched-capacitor circuits have become very popular due to their accurate response as well as good linearity and dynamic range. Accurate discrete time frequency is obtained since filter coefficients are determined by capacitance ratios which can be set precisely in an integrated circuit (Martin p.394). The advantage of using switched-capacitor is that the settling time and the frequency response could be easily be adjusted by using different capacitance ratio. Also switched-capacitor integrator can reduce the size of the chip than using simple RC integrator, which would cost less to fabricate because size is costly in IC manufacture industry.

An ideal op-amp was used for the first approach to design this integrator. Using MOSFET as switches is because they have high off resistance with little charge leakage and a relatively low on resistance. Thus it would introduce no offset voltage when it turns on.

The schematic level view of the switched capacitor integrator with using ideal op amp is shown in Figure 3-19. The ideal op amp was used to ensure the switch capacitor integrator functioned correctly under ideal environment. The ideal op amp was set up in Figure 3-20. The ideal op amp used about one third of the transconductance of the differential pair of FDFC op amp designed in the last section. Further explanation on the clock timings and the transistor sizing will be discussed in the next section.

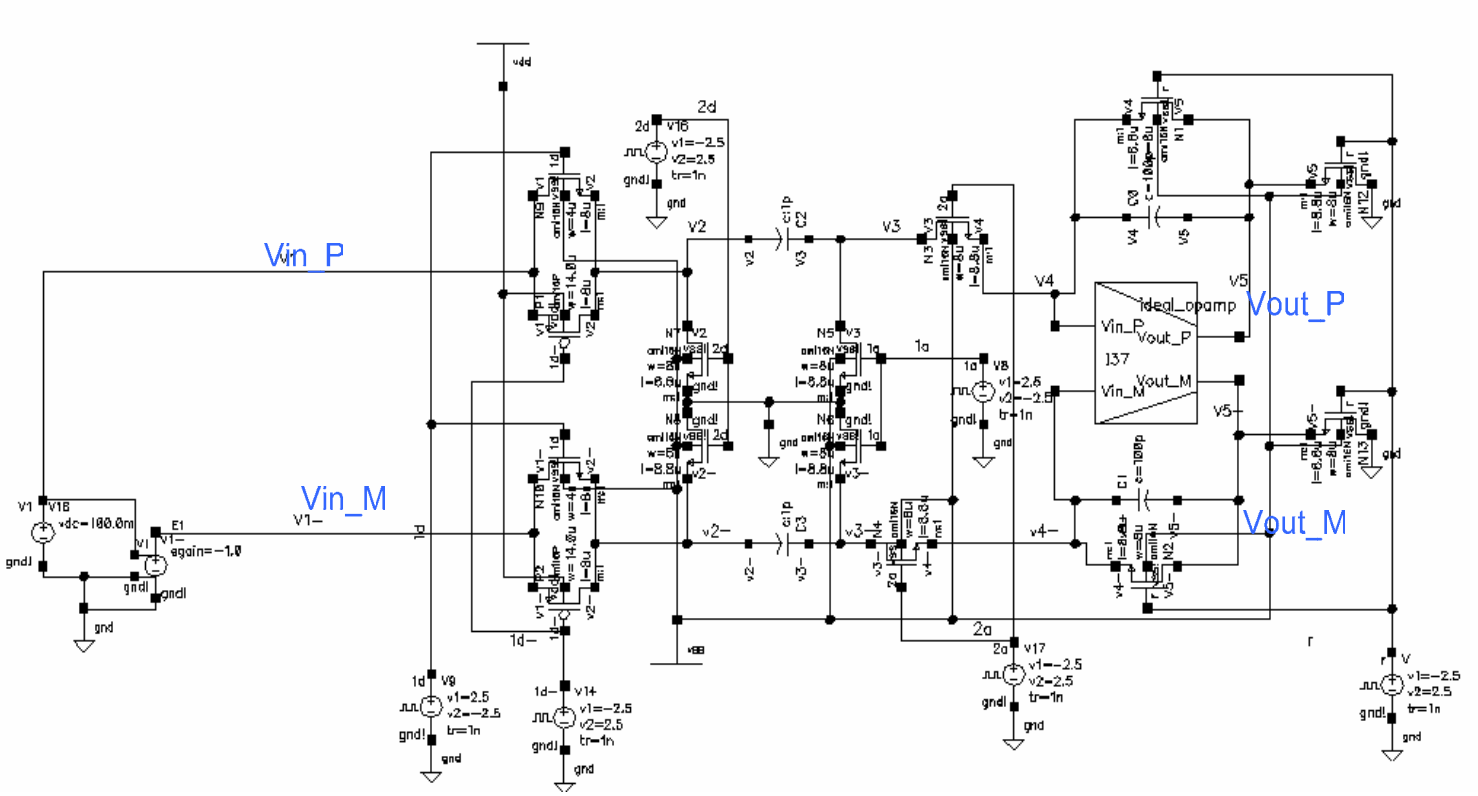


Figure 3-19: The schematic level view of the switched capacitor integrator with using ideal op amp

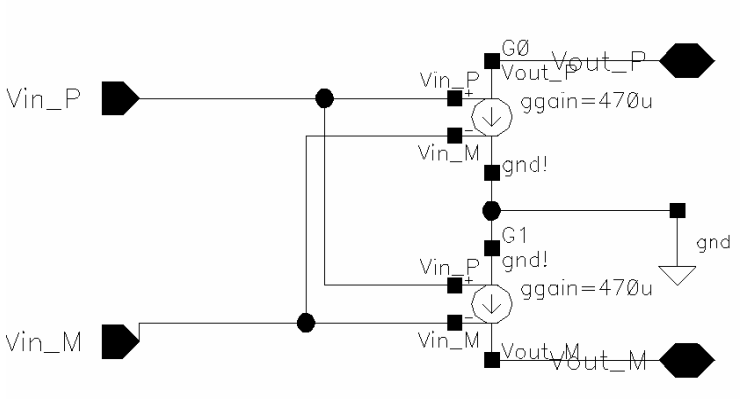


Figure 3-20: The schematic level view of ideal op amp

3.2.6.1 Timing for Switched-Capacitor Integrator

The clock timings were set as in Figure 3-21. These clock timings were used to control the power for the gates of the transistors. If the clock is “high”, then the transistor would be turned on, and allowed data to pass through. One constraint for the clocks was that it was essential to have at least one pair of non-overlapping clocks in switched-capacitor circuits, so the data would not be lost when they are transferring from one MOSFET to another. In other words, it would guarantee the charge is not inadvertently lost. Also the pulse width has to be wide enough for the capacitors to discharge. (Martin p.394) The reason of setting the time constant in such way will be discussed in the next section.

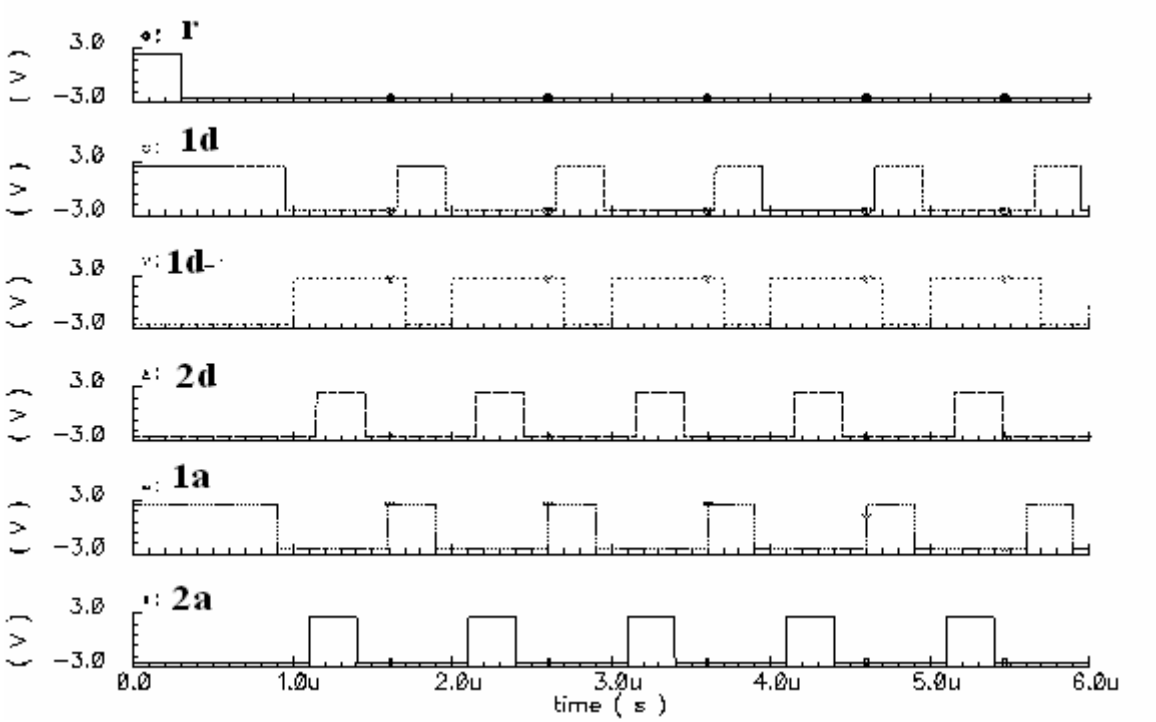


Figure 3-21: Timing for the Switched-Capacitor circuit

The timing of the first 1us was used to reset and initialize the switched capacitors. Timing r in Figure 3-21 was used to reset the C0, and C1 (Figure 3-19), so both input nodes of the op amp would go to 0V. Timing 1a and 2d (Figure 3-21) switched on to reset C2 and C3 (Figure 3-19), after that the whole circuit was ready to function. Timing 1d and 1d- switched off N9, P1, N10, P2, so C3 and C2 (Figure 3-19) were charged up. In the mean time, timing 2a switched on N4 and N3 (Figure 3-19), so the op amp would ready to take the input signals. Then timing 2d switched on N7, and N8 (Figure 3-19), so that the currents on the top plates of C2 and C3 (Figure 3-19) were discharged, however, the bottom plates of C2 and C3 (Figure 3-19) could not discharge instantly. Thus the bottom plates would have the opposite voltage whatever the top plates had. Then the op amp took those voltages as input signals. The output signals of the op amp then feedback to the inputs through C0 and C1 (Figure 3-19). As the inputs signals of the op amp decay as the capacitors discharge, the output signals decay at the same rate. N9, P1, N10, P2 (Figure 3-19) switched on again on the next clock cycle to take another set of input signals, and the process repeated. The specification of the timing is as follow:

Timing	Time delay (µs)	Pulse width (µs)	Period (µs)
R	0	.3	Nil
1a	.9	.7	1
1d	.95	.7	1
1d-	1	.7	1
2a	1.1	.3	1
2d	1.15	.3	1

Table 3-2: Timing specification for Switched-Capacitor Integrator

3.2.6.2 Sizing Transistors and Setting up the time constant

As the project goal is to achieve the ADC with 16 bit accuracy, the proper capacitance, resistance of the transistors had to be set up. To determine the resistance that was needed to achieve 16 bits accuracy with using 1pF capacitor for the switched-capacitor integrator. Looking at the capacitor when it discharged in Figure 3-22, when the capacitor discharges, the voltage drops with exponential behavior. The number of bits that the switched-capacitor integrator could handle depending on the time that the capacitor required to discharge, as shown in Figure 3-22.

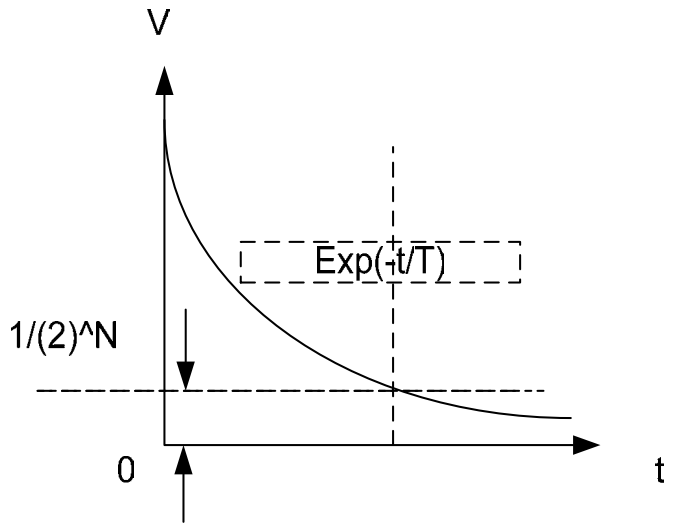


Figure 3-22: the relationship between N bits and switched capacitor integrator RC set up

Assuming τ = 1, and set t = 300ns

$$\frac{1}{2^N} = e^{-t/\tau}$$

$$2^{-16} = e^{-300n}$$

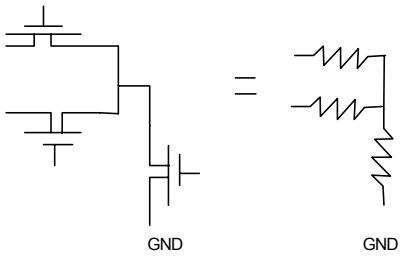
$$\ln(2^{16}) = 11.09$$

$$\frac{300ns}{11.09} = 27ns = T(clock\_period)$$

$$(Total\_resis\tan ce) * 1pF = 27ns$$

$$Total\_resis\tan ce = 27k\Omega$$

eq)3-5



The total resistance of transistors = 27kΩ

The reason to set time = 300ns was for the clock timing in each pulse, the general requirement for the clock frequency should be at least five times lower than the unity gain frequency of the op-amp. (Martin p.395&537) Using the transistors set up in Figure 3-23 to find the desired resistance for P1, N9 and P2, N10 (Figure 3-19). V10 was swept from -2.5V to 2.5V to determine the voltage drop across the transistors, since a small current source (10μA) was used, the resistance of the transistors could be calculated. The reason that the resistance could be calculated in such way because the transistors set up for switched capacitor circuit is equivalent to a resister circuit. The total resistance for the switched capacitor is 27kΩ. It is better to have the resistance evenly distributed on P1,

N9, N7; then N3, N5 rather than having one large transistor with high resistance and small resistances on other transistors. Thus, P1, N9, N7 would have ~14 kΩ load, and N3, N5, N7 would have ~13kΩ load; same set up for the bottom half of the circuit in Figure 3-19.

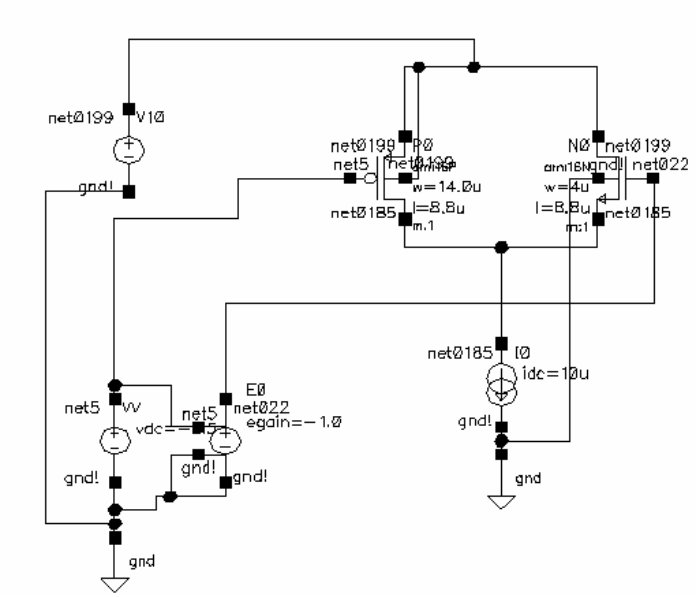


Figure 3-23: Schematic level view of simulating the total resistance for Switched-capacitor Integrator

3.2.6.3 Performance of the Switched-Capacitor with Ideal Op-Amp

±0.5mV DC was used as inputs to test our design by transient analysis. Transient Analysis is to get the output behavior given in a certain time range. Therefore, the output signals including start-up transient of the circuit could be observed. If the inputs were DC, then the integrator output signals should be a straight line with one output climbs up and another output goes down steadily. The outputs are shown in Figure 3-24.

Vin_P and Vin_M are the inputs of the integrator; Vout_P and Vout_M are the outputs of the op amp. The voltages of Vin_P-Opamp and Vin_M-Opamp are the inputs of the op amp.

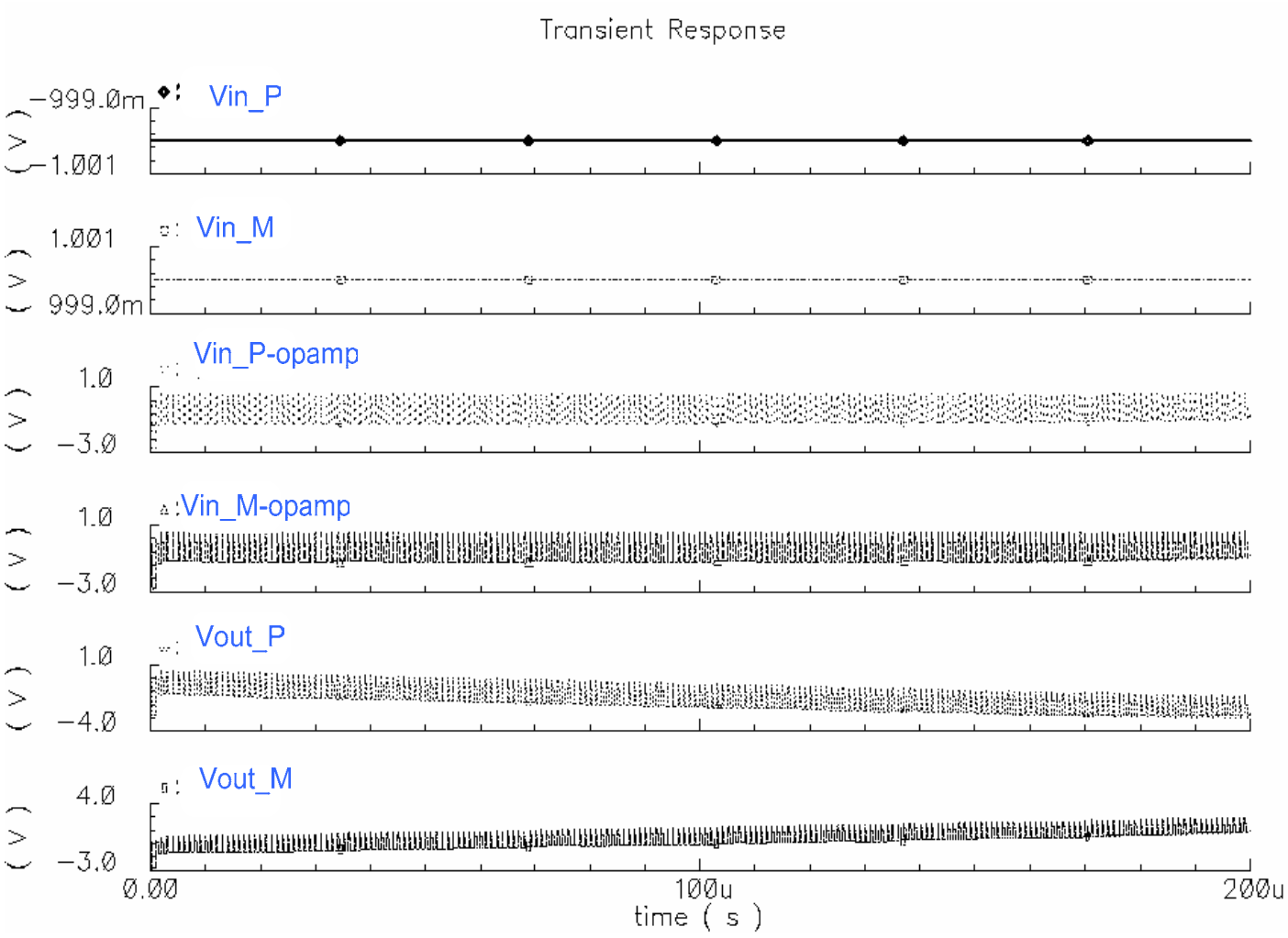


Figure 3-24: Transient Response of Switched Capacitor Integrator with Ideal Op amp

Since this integrator is a discrete time integrator, so the output signals increment in a constant step size, because the input signals were controlled by the clock cycles. As it hit the rising edge of the clock 2a (Figure 3-21), then the op amp would accept the inputs that were discharged from the capacitors. The gain depends on the ratio of the capacitances. Figure 3-25 is the zoom-in version of Figure 3-24 to have better illustration on the signals.

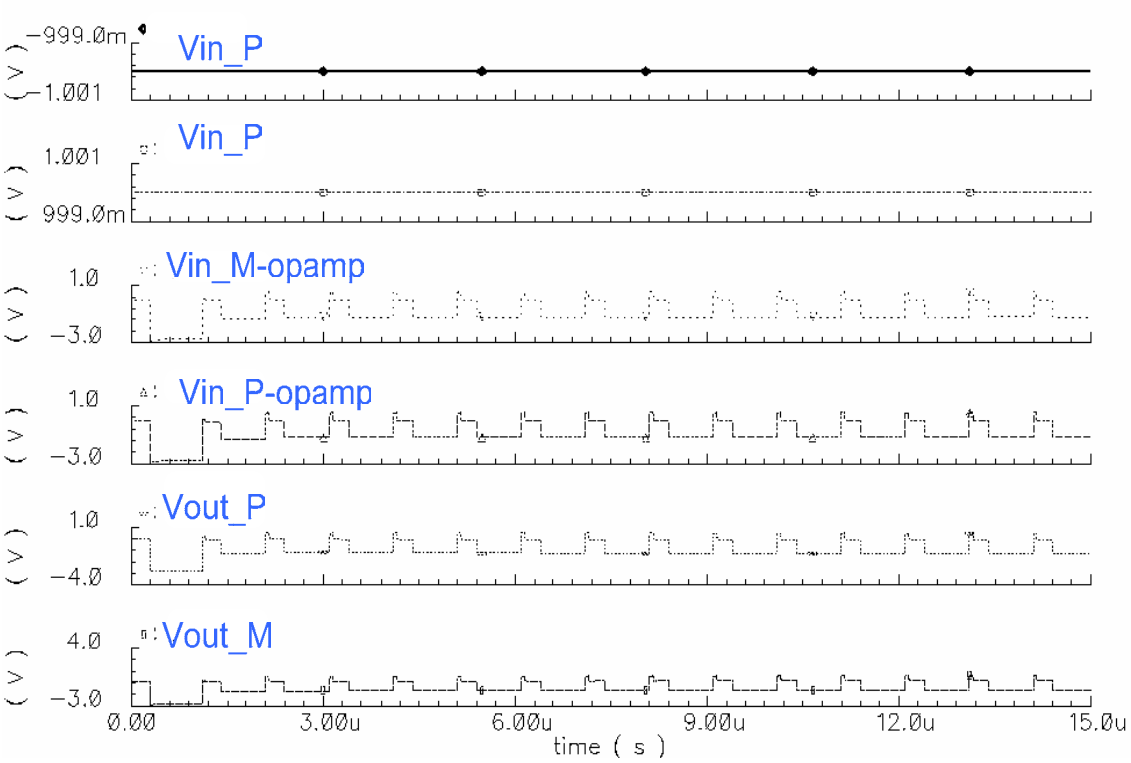


Figure 3-25: Zoomed in Version of Figure 3-24

3.2.7 Switched-Capacitor with FDFC op-amp

After the switched-capacitor integrator succeeded with the ideal op amp, FDFC op amp was then replaced. The top view of our switched-capacitor integrator is shown in Figure 3-26. The integrator was tested with the same configuration; the results of the integrator came out the same. Figure 3-27 is the transient response showing there was start up transient last approximately 18.4µs. Lastly, notice that the time for Vout_P to hit the rail is longer than the time for Vout_M, that is because of the offset voltage is a bit higher than 0V.

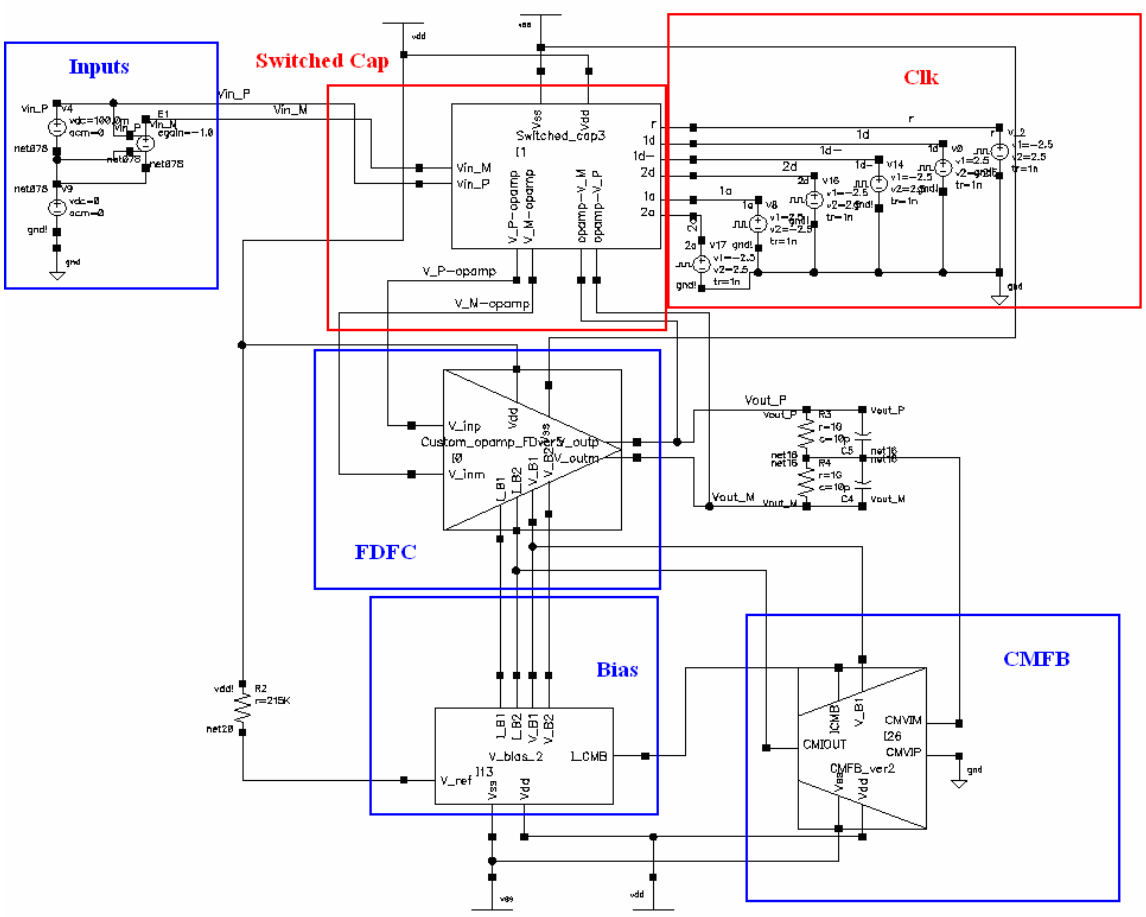


Figure 3-26: Top level view of the switched-capacitor integrator with FDFC op amp

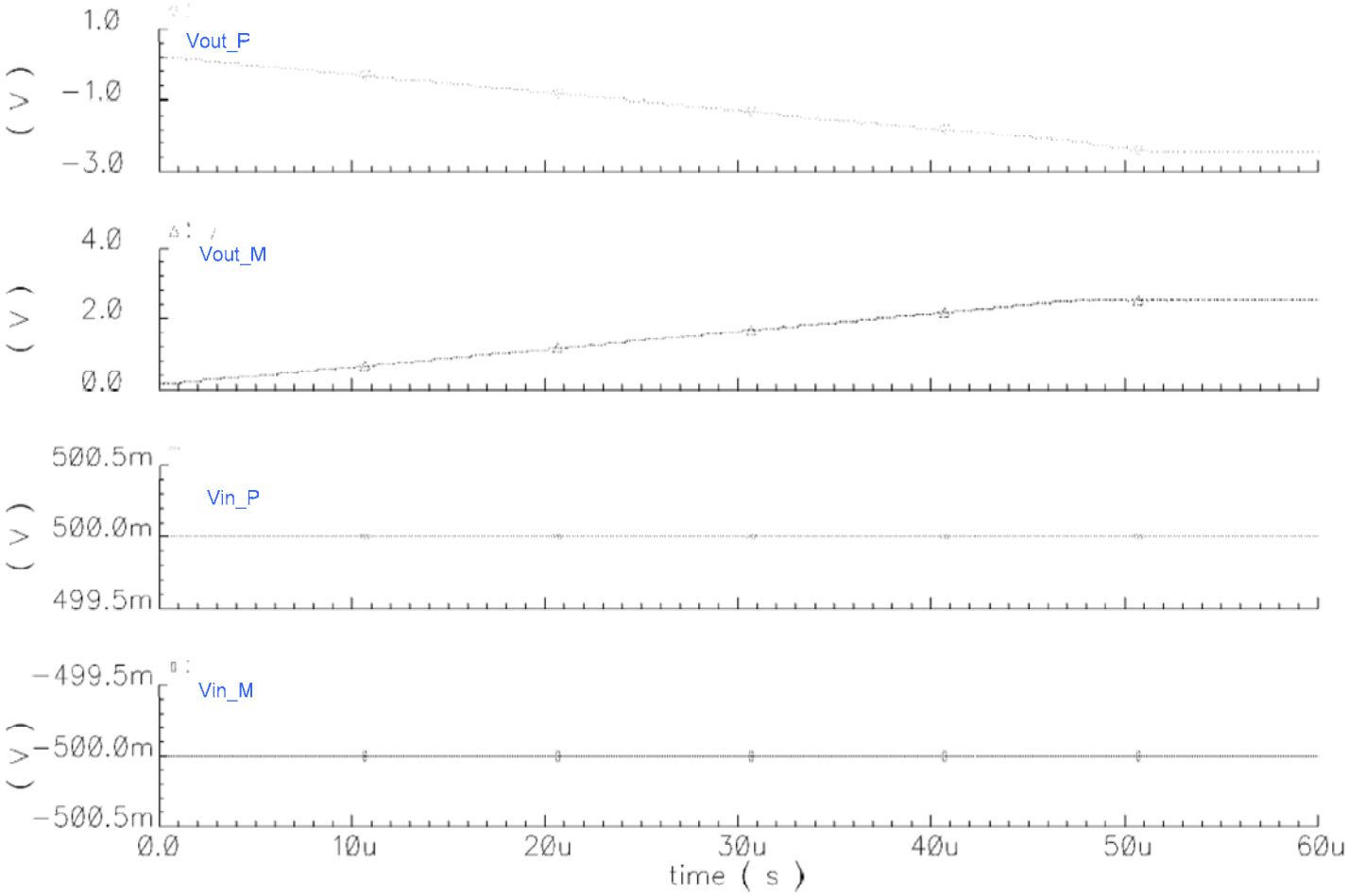


Figure 3-27: Transient Responses of the switched-capacitor integrator with FDFC op amp

To ensure the switched-capacitor integrator functions properly, the transient difference was simulated between Vout_P and Vout_M to verify the timing in each gap from two outputs are identical. Figure 3-28 shows the timings are identical as the output step incremented steadily.

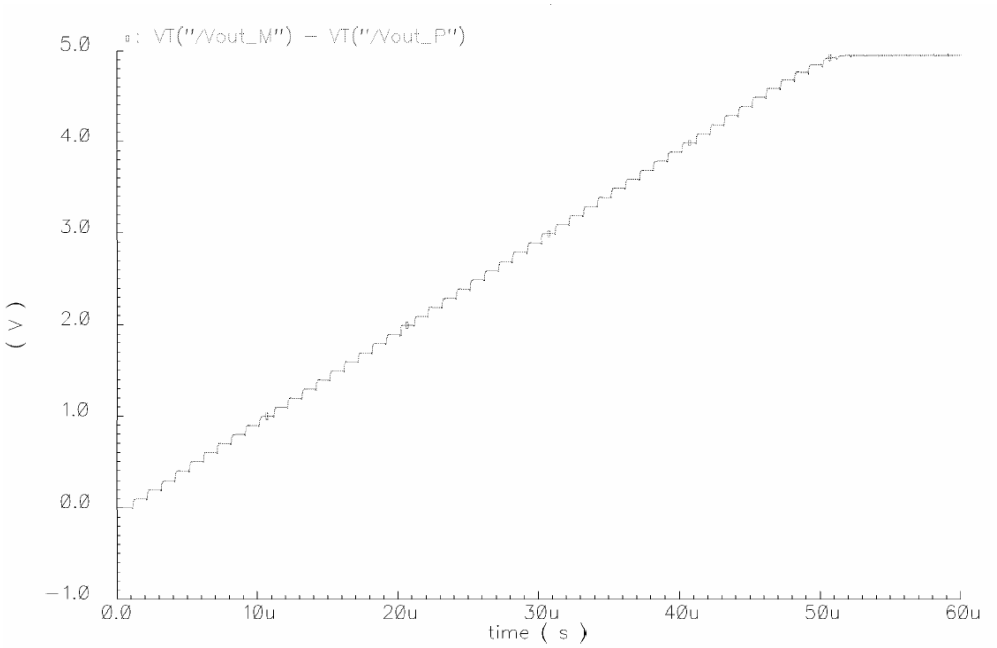


Figure 3-28: Transient output Differences of the Switched-Capacitor Integrator

Since the output signals were controlled by the clock cycles, as it hit rising edges of the clock, then the output signals change. To ensure there is enough settling time between each output increments in order to deliver the data correctly, each of the last data point before the increment at the output signals were recorded and had a linearity check on those points. This is important because the settling time is determined by the ratio of the capacitances, and if there is not enough settling time between the increments, then the data that is being delivered would no longer be correct. If the settling time is too long or uneven in between, then it would affect the sampling rate and the frequency response.

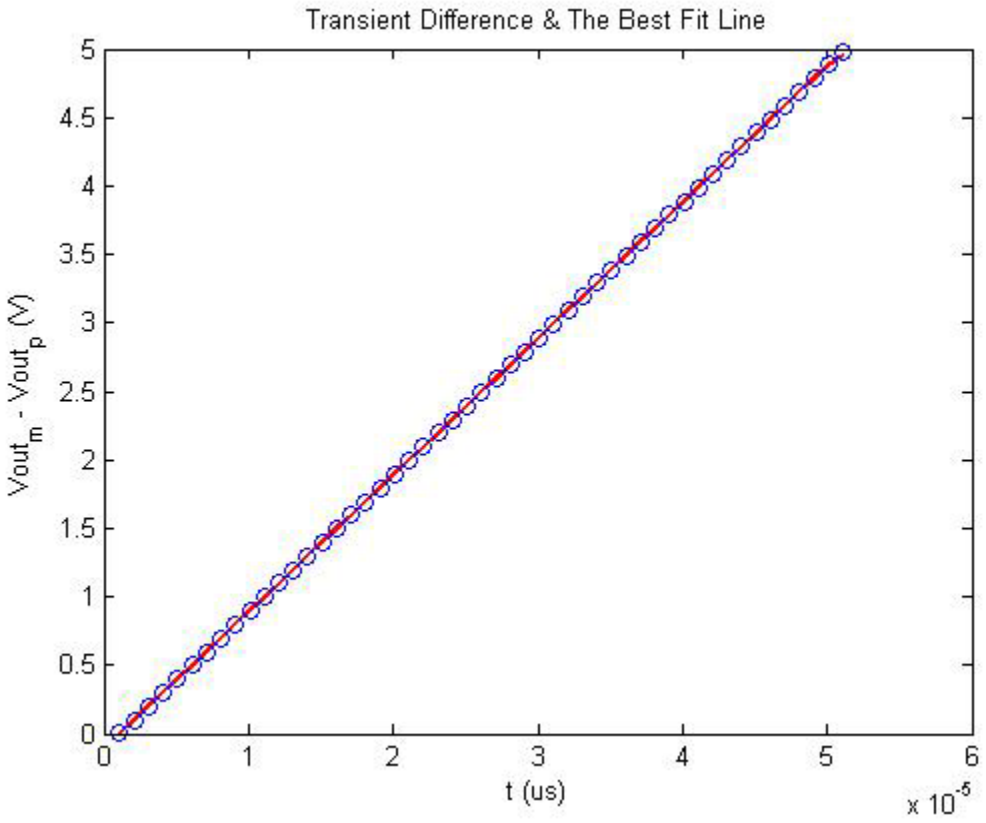


Figure 3-29: The last data point before each output increments and the best fit line of the points with using root mean square method

The error plots between the actual data points and the best fit line are shown in Figure 3-30 and 3-31. The errors occurred before 1us in Figure 3-30 was caused by the start up transient of the switched-capacitor circuit, and the start-up transient was caused by initializing the capacitors. The errors occurred starting from 5us was because as the output signals approached to ±2.5V, the outputs voltages were limited by the supply voltages. Figure 3-31 shows the errors were greatly reduced if the startup transient was discarded.

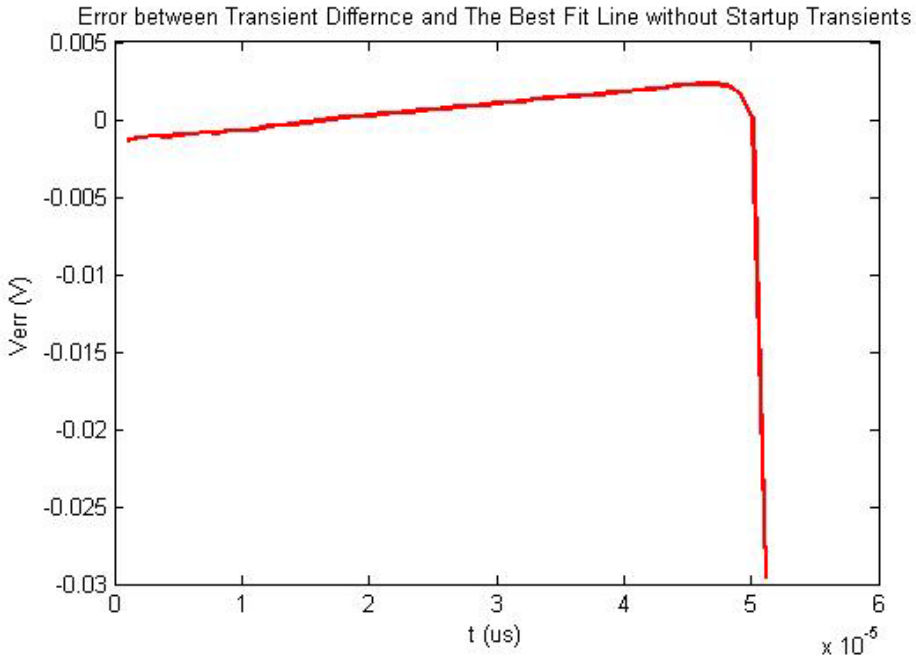


Figure 3-30: Error plot between transient difference and the best fit line with start-up transient

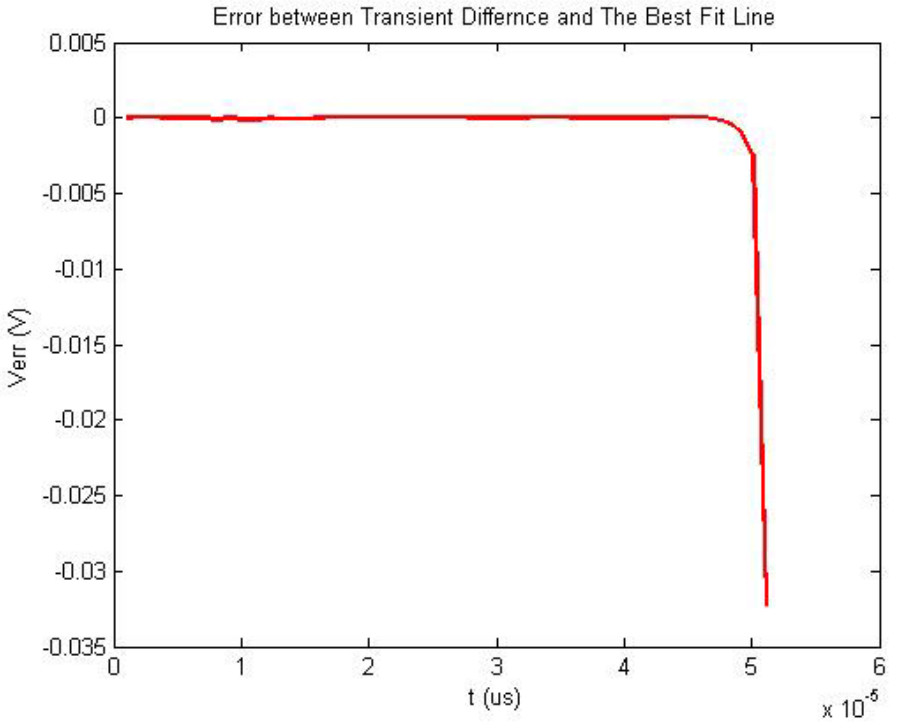


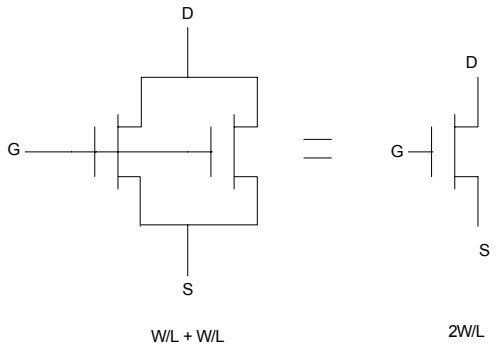
Figure 3-31: Error plot between transient difference and the best fit line without start-up transient

3.3 Design Layout

As previously mentioned, the NCSU 1.6μm process library is used so the design can be fabricated through MOSIS. There is a set of design rules that have to be followed in order to fabricate the IC. For example, the minimum space between each transistors, the minimum width for the gate of a transistor, etc. The detail design rules can be found at http://www.mosis.com/Technical/Designrules/scmos/scmos-main.html.

3.3.1 Design and Analysis

There are several modifications towards the schematic level design in order to have better results and benefits to the IC. Firstly, the sizes of the large transistors have to be modified into smaller transistors in order to lower the parasitic capacitance within the transistors. Any conductor placed above the silicon surface can potentially induce a parasitic channel. (Hastings p.131) Larger size of transistor has larger parasitic capacitance because the area of the gate of the transistor is large enough to become a plate of capacitance, and parasitic capacitance would lower the frequency responses, and it would affect the performance of the op-amp. Using multiple smaller sized MOSFET in parallel can reduce the effect of parasitic capacitances. The smaller size of transistor, the better frequency response it is, however, the tradeoff is that it would increase the sizes of the IC. Also the design rule requires the dimensions of the design to be the factor of .4um; in other words, any dimension that is not multiple of .4um would violate the design rule.



3.3.2 Sample PMOS and NMOS

Figure 3-32 shows the cross-section of a simple PMOS, and is then simulated in Cadence shown below the cross section PMOS. The layout design of the whole circuit is

similar to this process. Since P substrate is used in NCSU 1.6μm process, so no n-well is needed for NMOS and the layout design is shown in Figure 3-33.

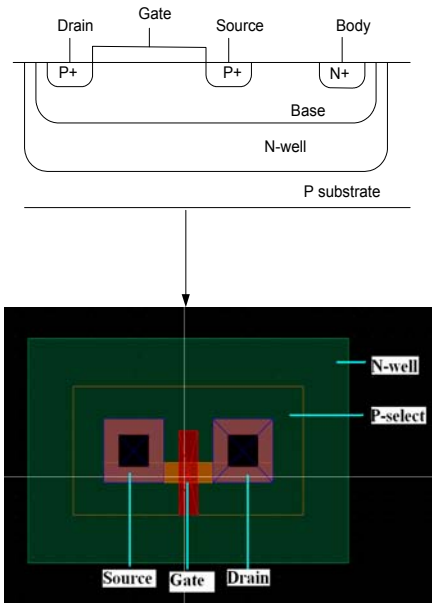


Figure 3-32: Cross-section view and layout (Body not shown in this figure) of a PMOS

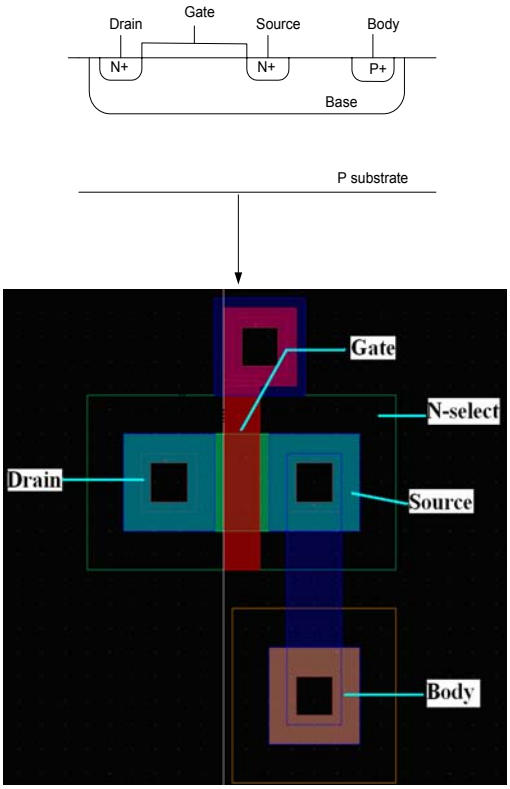


Figure 3-33: Cross-section view and layout (Body if connected to Source) of a NMOS

3.3.3 Design Layout of CMFB

In the layout design process, guard ring was used as the body for PMOS. There are two advantages of using guard ring. Firstly, it could separate the PMOS in the CMFB layout from other components in the design, so it minimized the interference from other components; secondly, it provided more contacts from the body to supply voltages (Vdd). The modified schematic and the layout for CMFB are shown in Figure 3-34.

Since P2, P3, P4, and P5 in Figure 3-34 are cascode, so the contacts between them were not necessary. Another change in the CMFB is that the sizes of P0 and P1 were too large, so P0 and P1 were broken down into four smaller transistors. Figure 3-34 also shows that the guard ring was used as body for the PMOS.

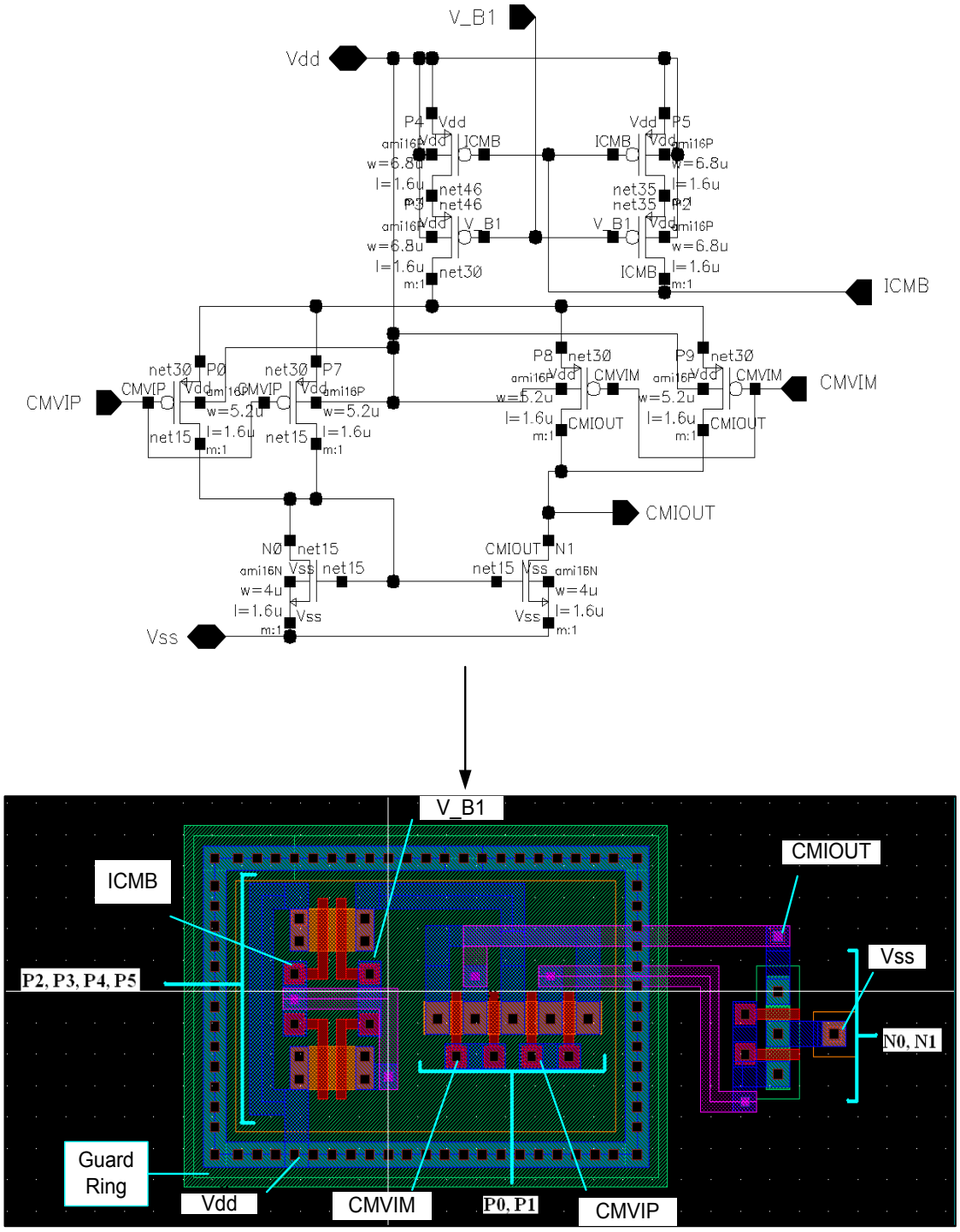


Figure 3-34: Schematic to layout of CMFB

3.3.4 Design Layout for Bias Network

The layout design for Bias Network is similar to the layout of CMFB; however, since the resistors that were used in schematic level design took too much space compared with using transistor as resistors, so the resistors were replaced by three transistors for more efficient layout design. However, accuracy for the resistance values could be an issue during fabrication process. Another key point was that since the voltages were generated by the current mirrors, therefore, the transistors were better to build as close as possible to minimize the fabrication error.

The modified schematic and the layout design of Bias Network are shown in Figure 3-35.

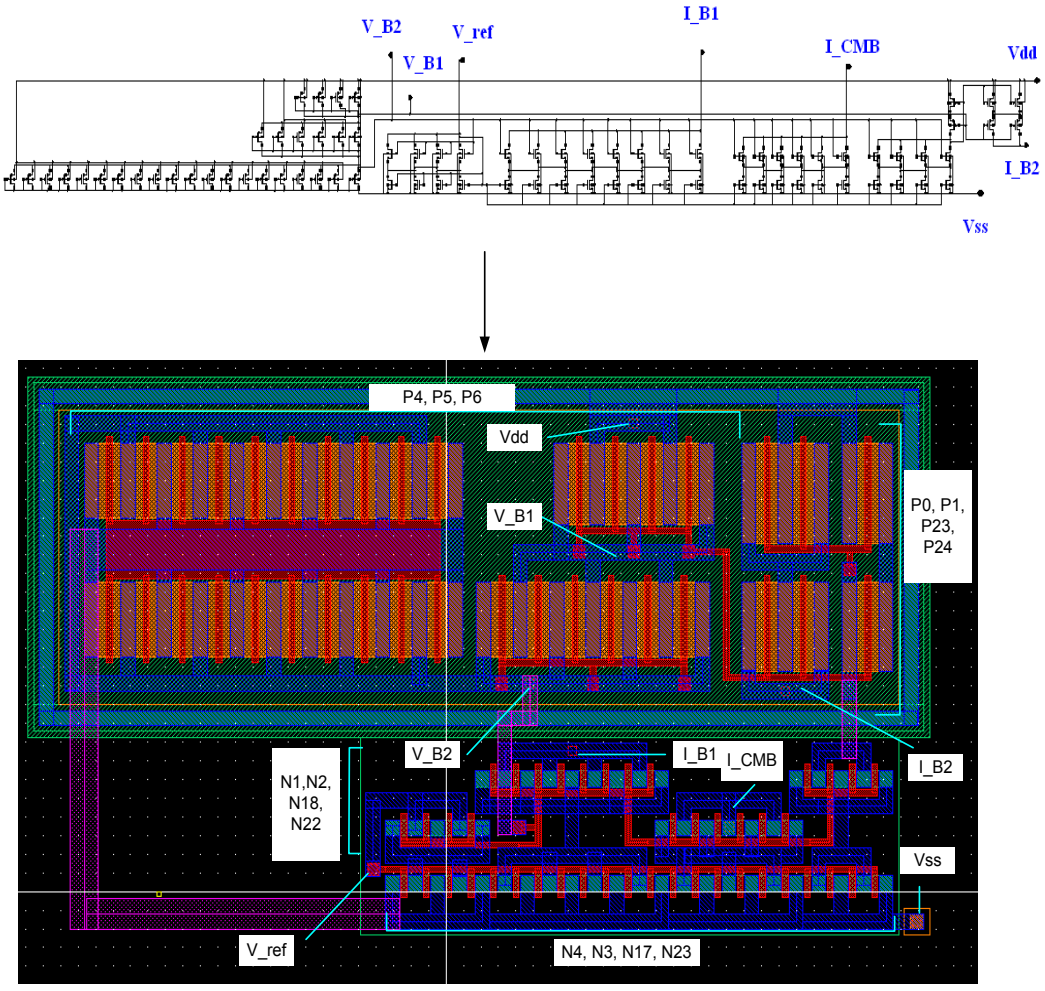


Figure 3-35: Schematic to Layout Design of Bias Network

3.3.5 Layout of FDFC op amp

The layout for the FDFC op amp included two 10pF capacitors (C0, C2), the size of each capacitor is $130 um^2$ and it was split into 4 parallel smaller capacitors to lower the parasitic capacitance. The sizes of the capacitors could be minimized even more by using transistor capacitor. However, the linearity of the capacitor performance might be an issue later on, so these capacitors made by sheets of poly1 and poly2 layers were used and known as double poly capacitors. All the transistors in FDFC op amps were replaced with smaller parallel transistors to increase the frequency response and lower the parasitic capacitance. The total size of the op-amp is 581.2um * 501.2 um. Figure 3-36 shows the modified schematic and the layout of the FDFC op amp.

The capacitance between two layers can be calculated by the following capacitance specification between the layers. The specifications of other parameters can be found in http://www.mosis.com.

Capacitance Parameters	N+ACTV	P=ACTV	POLY1	POLY2	METAL1	METAL2	N_WELL	UNIT
Area (substrate)	269	299	36		24	14	60	aF/unit sq
Area (N+ACTIVE)			1083	691	49	25		aF/unit sq
Area (P+ACTIVE)			1066	684				aF/unit sq
Area (POLY)				590	44	22		aF/unit sq
Area (POLY2)					45			aF/unit sq
Area (METAL1)						36		aF/unit sq

Table 3-3: Capacitance between Layers in SpectreS library

The Calculation of Capacitance between layers is as follow,

The target capacitance = 10pF, as the capacitance between Poly1 and Poly2 is 561aF/unit

$10\,pF = 10000000aF$

$$\frac{10000000aF}{590af\,/\,unitsq} = 16949\,\mu m^2$$

$16949\,\mu m^2$ = area of poly1 overlaps poly2 to generate 10pF.

The length of the square $= \sqrt{16949\,\mu m^2} = 130\,\mu m$

Then the capacitors is split into four with two 66^2um sq. and two 64um sq.

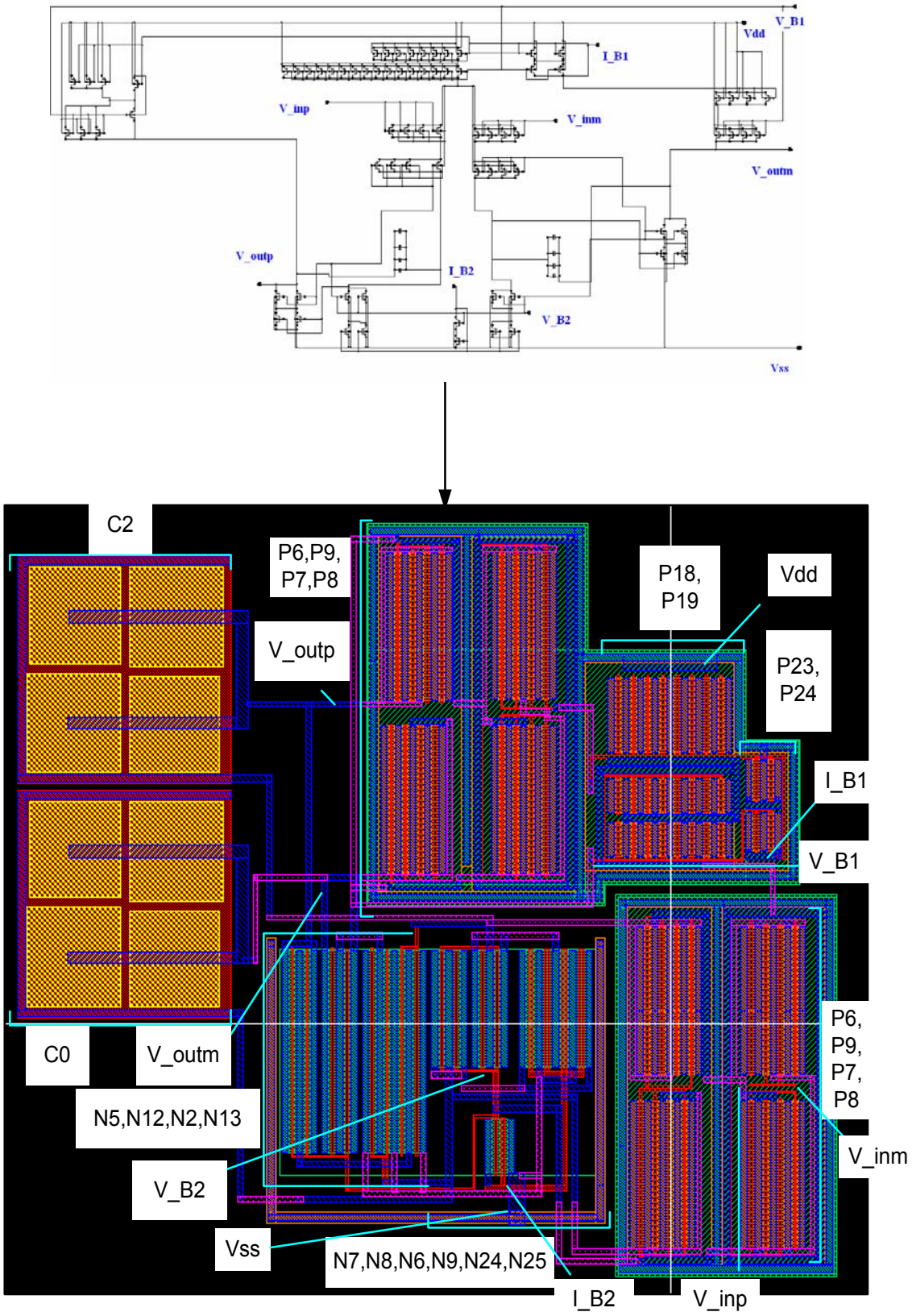


Figure 3-36: Schematic to Layout Design of FDFC op-amp

3.3.6 Layout of Switched Capacitor Integrator

As shown in Figure 3-37, the capacitors occupied large amount of space comparing to the sizes of the transistors that were used in this circuit. High linearity of the capacitance is essential in this circuit as the bits resolution depends on the ratio of the capacitance that was discussed in last chapter. Also some transistors in this circuit were cascode, so they could share the same active layer; therefore, only one layer of contacts was needed between drain and source of the transistors. For example, transistors N7, N5, shares the same contacts between the gates in Figure 3-37. The advantage of this configuration was to save space and minimized the fabrication error.

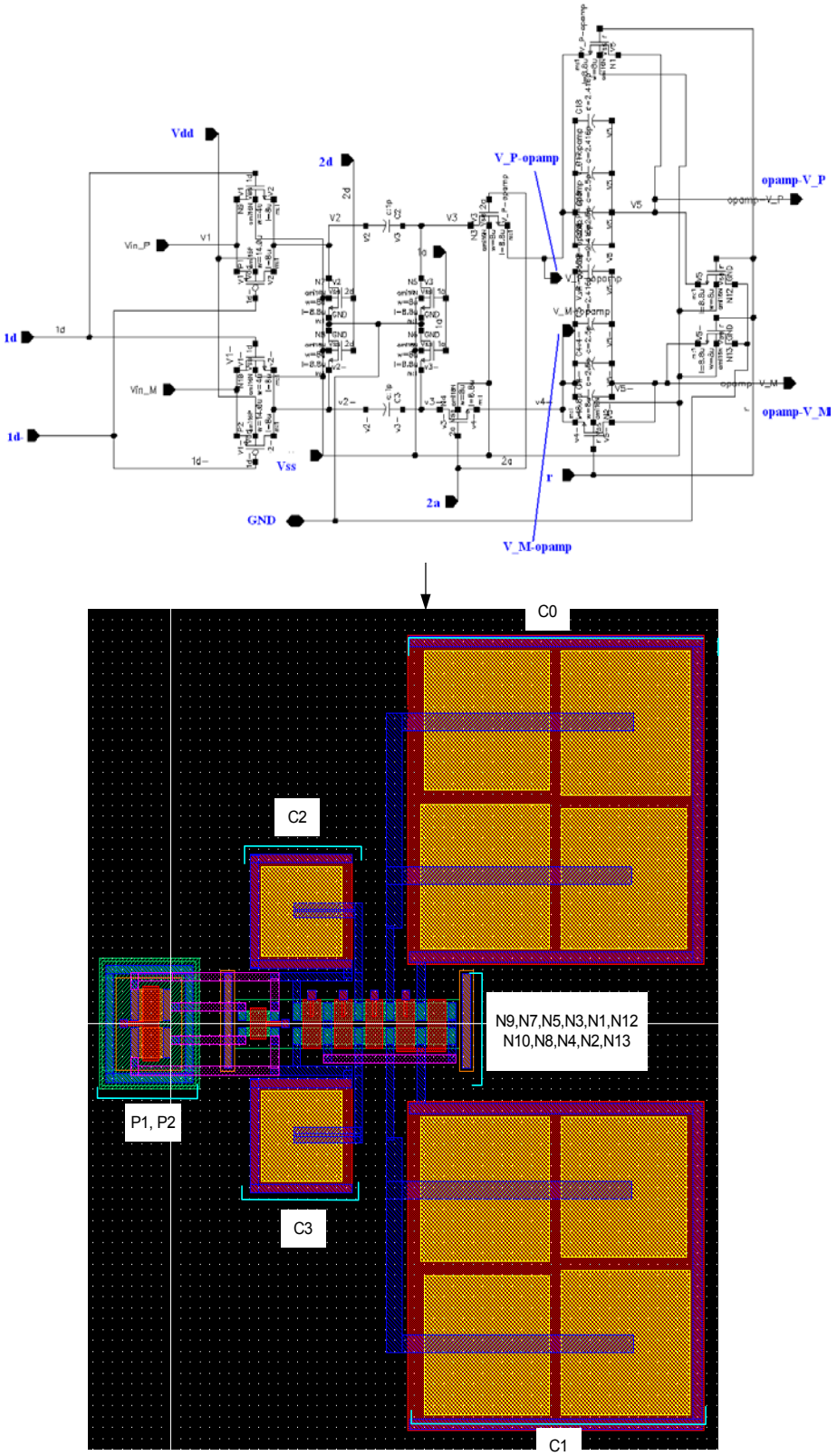


Figure 3-37: Schematic to Layout Design of Switched-Capacitor Integrator

3.4 Final Simulation and Comparison

After completing the layout design, the final simulation to examine any errors and differences between the schematic level design and layout level design. The simulation using layout design is as follow,

The performance of the FDFC op amp is shown in Figure 3-38

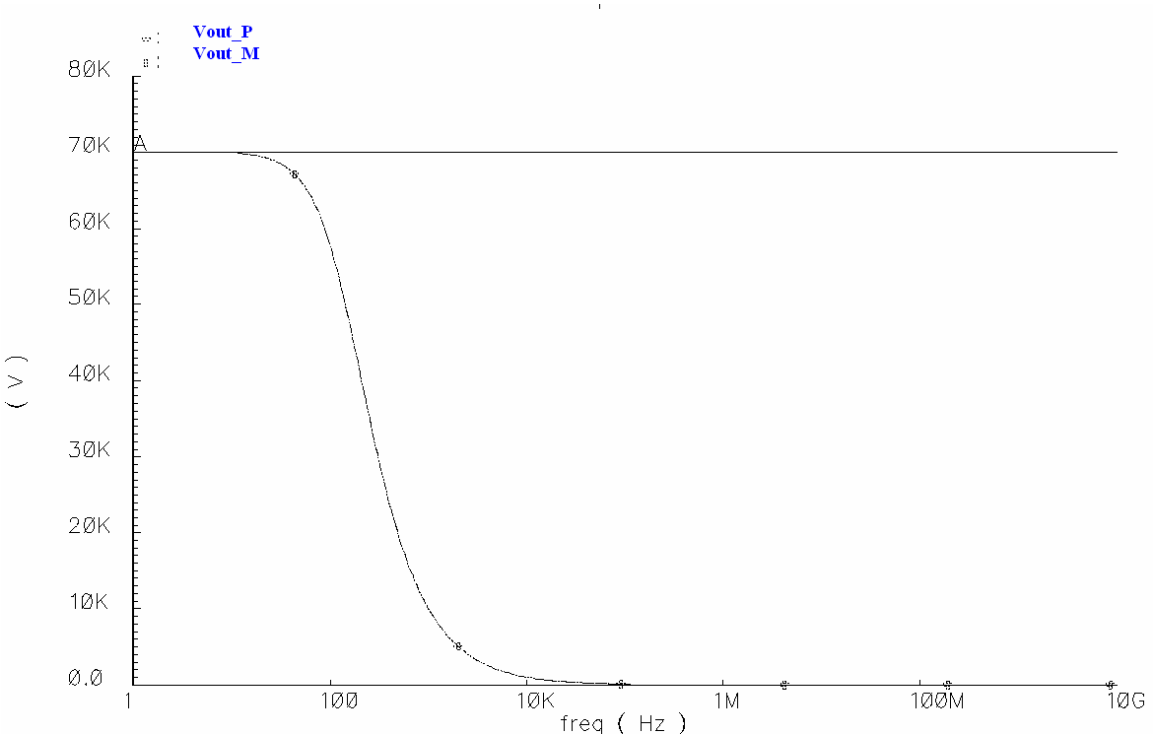


Figure 3-38: AC Analysis of FDFC op-amp (Layout)

AC analysis shows that the open loop gain was increased from 67k (96dB) to 70k (~97dB). Gain increased mainly because the transistors were adjusted to follow the NCSU 1.6 um deign rules, all the sizes of the transistors were tuned slightly higher when they were needed to be modified.

The transient response of the switched-capacitor integrator is shown in Figure 3-39

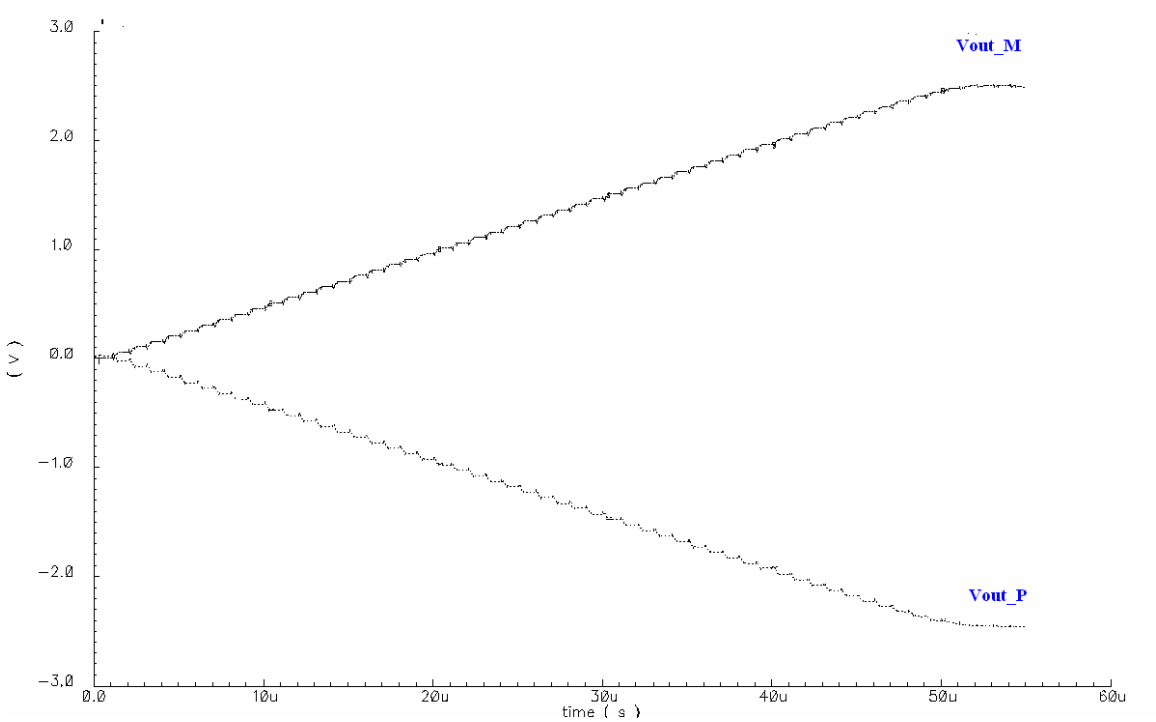


Figure 3-39: transient response of the switched-capacitor integrator (Layout)

The offset voltage was slightly changed when simulating with the layout design, but the offset voltage could be adjusted by adjusting the reference voltage of the CMFB reference. Therefore, the overall layout designs for all the components were successful.

4 CONCLUSION

The purpose of the analog bread board section was to walk through the design and implementation of an analog version of a second order Σ-Δ ADC in order to provide the proof of concept of the design for the electrophysiologic data acquisition integrated circuit. The requirements of the data acquisition circuit were to develop a bandpass ADC system that would reject motion artifacts and DC offsets associated with electrophysiologic data. The construction of a functional single ended input second order Σ-Δ ADC was accomplished. The second order Σ-Δ ADC introduced an op amp integrator in the feedback loop, represented as H2 in figure 1-1, which successfully eliminated any DC offset present in the input signal allowing for a maximum input range between 0 and 5 volts.

From the frequency analysis of the second order Σ-Δ ADC constructed it was shown that it was a fixed bandpass system, that is the corner frequencies were not selectable. It was also shown in the frequency analysis of the second order Σ-Δ ADC that the low frequency cutoff of the system was controlled by the time constant, τ_2, of the feedback op amp integrator, H2, and the high frequency cutoff was controlled by the time constant, τ_1, of the op amp integrator in the front end of the circuit, H1. For the analog breadboarded second order Σ-Δ ADC the time constants for the op amp integrators were determined by the resistor, at the input of the op amp, and capacitor, in the feedback loop of the op amp. When this system is finally implemented as a second order Σ-Δ ADC with a differential difference amplifier on the integrated circuit the time constants will be controlled by switch capacitors allowing for a programmable frequency response of the system. The second order Σ-Δ ADC frequency response in the results section showed that the system responded as predicted in the frequency analysis, so when this system is finally implemented the switch capacitors can be designed according to theory with the confidence that the system will respond accordingly.

Another feature of the second order Σ-Δ ADC was feedback resistor, k, from the Q output of the d-flip-flop. It was shown in the frequency analysis of the second order Σ-Δ ADC that this feedback resistor will control the amplification or attenuation of the input signal as desired. For the second order Σ-Δ ADC discussed in this application the feedback resistor was set to allow for no attenuation or amplification, but in future

implementations of the system in might be desirable to provide some amplification of the input signal.

Another important aspect of the analog breadboard part of this project was to establish the interfacing between the circuit and the PC along with implementing the FIR reconstruction filtering. The interfacing was accomplished through a National Instruments digital I/O board and connector block. The National Instrument digital I/O board chosen will allow for the increase of the sampling frequency of the Σ-Δ ADC in future applications if desirable. Labview was used in conjunction with the National Instrument digital I/O board to acquire a binary file of a set number of samples of the output of the Σ-Δ ADC. From the binary file acquired Matlab was then use to perform the FIR reconstruction filtering. The FIR filter designed was linear phase and had and order of 10000. From the FIR filter design and implementation it was observed that by setting the cutoff frequency 200 Hz above the frequency band of interest allowed for no attenuation of the highest frequency in the band and proper cutoff of high frequency noise.

Matlab was also used to perform certain evaluations of the Σ-Δ ADC systems. For testing purposes a function generator was used to produce a sine wave input to the Σ-Δ ADC systems. Since a sine wave input was used for testing Matlab was used to fit a sine wave to the digitally filtered output signal using the nonlinear least-squares method. The best fit sine wave was then used to determine the error of the Σ-Δ ADC system by taking the difference of the best fit sine wave from the digitally filtered sine wave. From the error data acquired the SNDR of the Σ-Δ ADC systems could then be calculated. The biggest draw back of acquiring accurate SNR measurements of the Σ-Δ ADC systems was the presence of harmonics of the input signal that appeared in the output signal. The presence of the harmonics only allowed for an SNDR measurement which was a measurement of signal to noise ratio along with the distortion from the harmonics. The DC evaluation of both Σ-Δ ADCs showed that the systems were linear systems which indicates that the harmonics of the present at the output were not a result of the systems. One possible source of the harmonics could be from the function generator used due to its limited resolution. Due to time constraints the source of the harmonics was not determined, but by placing the cutoff frequency of the FIR filter before the harmonics of

the input signal a gauge of the SNR could be determined. Performing a more qualitative evaluation of the noise floor in relation to the output tone in the FFT domain showed that the signal was about 100 dB above the noise floor. This result roughly indicates that there is 16 bits of resolution to the Σ-Δ ADC.

The analog bread board of the second order Σ-Δ ADC developed in this project set a solid foundation of analysis and proof of concept the electrophysiologic data acquisition system design that can be built off of in future work. From the evaluation of the second order Σ-Δ ADC it can be concluded that the feedback op amp integrator does track and eliminate any DC offset present in the input signal. The evaluation also demonstrated that the second order Σ-Δ ADC was a bandpass system and by setting the values of the time constants of H1 and H2 the corner frequencies can be controlled to match the various bandwidths of electrophysiologic signals to be acquired. Along with the development of the analog bread board version of the Σ-Δ ADC this project also developed the interface from the system to the PC. This project also developed the FIR reconstructing filtering on Matlab that can be developed upon further and finally incorporated on chip for future applications.

The original purpose of having integrated circuit design in this project was to scale down the analog bread board design into one single IC, which would perform the same results as mentioned.

The project started with simulated an existing op amp chosen from a reference book that could be suitable for the design. Although the performance of the FC op amp was not satisfied for the project application, it was a good foundation to implement a fully differential op amp. The fully differential op amp was designed to meet the gain requirement corresponded with the 16 bits resolution. The advantage of using fully differential op amp is to double the voltage swing of the signals, so the op amp would have greater ability to operate in a wider range. Common-mode feedback circuitry however also needed for FDFC op amp in order to balance the common-mode voltage, the designed CMFB functions correctly to maintain the common-mode. The Bias was separated from the op amp to increase the fabrication accuracy and lower the internal errors of the op amp. However, due to time constraint and other technical problems occurred while designing process, the IC was decided not to fabricate. However, the

major component, switched-capacitor integrator of Σ-Δ ADC was designed and layout in Cadence, which was also a good foundation for future work. The Switched Capacitor Integrator components built on the FDFC op-amp was an essential part for Σ-Δ ADC, which also is a discrete time integrator that is more popular in integrated realization as switched-capacitor integrator is less sensitive to sampling jitter and better distortion characteristics. (Martin p.540) Although the design was decided not to be fabricated, the design was worth for further implementation as the breadboard design had already proven that the Σ-Δ ADC for electrophysiologic data acquisition is feasible to implement.

5 FUTURE WORK

This project set forth a good foundation of development and analysis for the electrophysiologic data acquisition system but due to time constraints there are still areas that need to be addressed in future work. The next logical step to be taken on the analog bread board system would be the introduction of the differential difference amplifier in the front end. The amplifier would have a fixed gain, K, which would be determined by equation 5-1 according to figure 1-1.

$$V_1 = K(v_{id} - V_{TRACK}) \qquad \textit{eq) 5-1}$$

From equation 5-1 v_{id} would be the differential input voltage, V_{TRACK} would be the voltage that tracks the DC offset, and K would be a fixed gain determined by device geometry ratios. It would then need to be determined if it would be necessary to provide further amplification of the signal through the feedback resistor from the Q output of the d-flip-flop as previously discussed.

It would also be beneficial to evaluate the different RC values needed to determine the corner frequencies of the time constants for H1 and H2 for the frequency bands of the various electrophsiologic signals to be acquired, table 1-1. The values determined would then translate into multiple switch capacitor networks on the IC that would be able to be selectable for the desired frequency bandwidth of the system.

The issue of harmonics from the input tone present in the output would be another issue needed to be addressed in future work with the analog bread board system. A possible avenue worth investigating would be to look at the output of the signal generator with a spectrum analyzer to determine if the harmonics of the signal are present before entering the Σ-Δ ADC. If it is determined that the problem lies with the function generator then, for testing purposes, a lowpass filter could be used to for the output of before entering the Σ-Δ ADC. If the issue of the harmonics could be resolved then an accurate SNR evaluation could be preformed on the Σ-Δ ADC from the Matlab code developed in this project.

There could also be future work done on the Matlab FIR filtering developed in this project. For future applications the FIR filter designed in this project could be implemented on a real-time DSP chip or FPGA. The order and cutoff frequency of the FIR filter designed in this project would first have to be optimized for future applications.

One issue that might need to be looked into further is the difference of the passbands of the filtered and unfiltered data as mentioned previously. It did not appear to be a large issue for the work preformed in this project, but might prove to be beneficial to look into in future work.

Another issue that occurred with the PC evaluation was when the frequency ranges below 5 Hz were acquired in order to capture more then one period of the sine wave the number of samples need increased significantly. The problem that occurred was with using the nonlinear least-squares with data samples this large. The algorithm the nonlinear least-squares function uses could not handle data that large, so it could not be used to obtain an SNDR calculation or fit a sine wave to the digitally filtered sine wave. One possible solution to this problem would be to use the process of decimation to eliminate the abundant data. According to the sampling theorem the "sample rate only needs to be 2 times the input signal bandwidth in order to reliably reconstruct the input signal without distortion" (Jarman p.6). For an input signal of 1 Hz the Σ-Δ ADC is oversampling the data by 20 M, from the OVSR equation 2-1. By decimating the filtered data it could be reduce number of samples significantly which would allow the algorithm used by the linear least-squares to operate (Jarman p.6).

As for integrated circuit design, define the sizes of the transistors for the FDFC op-amp more precise is essential in order to minimize the offset voltage, so the IC would be more feasible to be fabricated even though the offset voltage can be eliminated by the reference voltage for the common-mode feedback loop. In the current status, only one set of time constant is simulated for switched capacitor integrator, further investigation on the time constant and different sets of capacitance ratio would be good to examine how the integrator would perform with different parameters. Another improvement that can be performed in the future is that for higher precision in fabrication process, the transistors should be separate into smaller transistors to increase the frequency responses. Therefore, less parasitic capacitance would be formed in transistors. Then the overall performance should be increased, and minimize the variations. In the current design, there are no dummy gates for the transistors in layout design. In real applications, dummy gates should be implemented along with the transistors, because during the fabrication process, there will be polysilicon variation at etches of the transistors and it would hurt the

precision severely especially high precision values are needed such as resistances and capacitance values. Also, only the differential pair in the FDFC op amp used common-centroid layout technique, this technique was used to minimize the gradient induced mismatches by reducing the centroids of the matched devices during fabrication process. This technique is essential for large differential pair. Lastly, the spaces between the transistors can be shortened; shorter distance would minimize the chances of errors and save more space. The Difference Differential Amplifier (DDA) was not designed in this project, in order to have the whole algorithm completely functioning; DDA should be implemented in the future.

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APENDIX A – MATLAB CODE

This is the host program used to call all of the functions.

```
//host
clear all
clc
clf(figure(1))
clf(figure(2))
clf(figure(3))
clf(figure(4))

data = file_read ('n3_500hz.bin'); %insert file name ex) 'a.bin'

fs = 1000000;   %smapling frequency
fo = 500;      %operating frequency
fc = 700;      %cutoff frequency
order = 10000;   %number of order for FIR
pts = 100000;     %number of points to plot for FIR filter
n = 2000;      %number of samples to plot

[b, fd, td] = my_fir(fs, fc, order, data);

FIR_Plot (fs, b, pts)

my_plots (fd, td, fs, n)

a = mean(fd);           %mean offset voltage of filtered data
X0 = [a 0.4 fo 0];      %vector used for bestfit

[d,bfit] = my_bestfit (X0, fd, fs);

fit_plot (bfit, fd, fs, n)

fit_info (d, bfit, fd);
```

This function reads in the binary file created when importing the data from Labview.

```
function [data] = file_read (file_name)

fid = fopen(file_name, 'r');
if fid < 0, error (['Can"t open file "' file_name '".']); end

data = fread(fid, 'int8');
fclose(fid);
return
```

This function performs the FIR filtering of the data and removes the start up transient.

```
function [b, fd, td] = my_fir(fs, fc, order, data)

% fs = sampling frequency
% fc = cutoff frequency
% order = # of taps+1

b = fir1(order,fc/(fs/2));

y = filter(b,1,data);
fd = y((order+1):end); %new array excluding start up transient from filtering
td = data(1+order/2:end-order/2); %truncates original data array by transient

return
```

This function performs most of the plotting.

```
function my_plots (fd, td, fs, n)

t = 1000*(0:n-1) / fs;

figure(1)
subplot(2,1,1);
plot(t,td(1:n))
ylabel('Magnitude');
xlabel('Time (msec)');
title('Original Data');

subplot(2,1,2);
plot(t,fd(1:n), 'r')
ylabel('Magnitude');
xlabel('Time (msec)');
title('Filtered Data');


figure(2)

LL = floor( ((length(td)-1)/2)+1 );
f = fs*[0:LL-1]/length(td);
FFTtd = abs(fft(td));
FFTfd = abs(fft(fd));

subplot(2,2,1:2);
loglog(f,FFTtd(1:LL))
hold on
loglog(f,FFTfd(1:LL),'--r')
ylabel('Magnitude');
```

```
xlabel('Log Frequency (Hz)');
title('FFT of Original Data and Filtered Data');
h = legend('Original Data', 'Filtered Data', 1);
axis([0 10^(5.7) 10^(-3) 10^(5.5)]);

subplot(2,2,3);loglog(f,FFTtd(1:LL))
ylabel('Magnitude');
xlabel('Log Frequency (Hz)');
title('FFT of Original Data');
axis([0 10^(5.7) 10^(-3) 10^(5.5)]);

subplot(2,2,4);
loglog(f,FFTfd(1:LL),'r')
hold on
ylabel('Magnitude');
xlabel('Log Frequency (Hz)');
title('FFT of Filtered Data');
axis([0 10^(5.7) 10^(-3) 10^(5.5)]);


return
```

This function performs the best fit plot along with the error plot.

```
function fit_plot (bfit, fd, fs, n)

t = 1000*(0:n-1) / fs;
l = length(fd);
t2 = 1000*(0:l-1) / fs;

figure (3)
subplot(2,1,1);plot(t, bfit(1:n))
hold on
plot(t, fd(1:n), 'r')
title('Non-linear Least Squares Best Fit Line');
ylabel('Magnitude');
xlabel('Time(msec)');
h = legend('Best Fit Line', 'Filtered Data', 1);
subplot(2,1,2);plot (t2,(bfit' - fd))%error plot
title('Error Plot (Best Fit - Filtered Data)');
xlabel('Time(msec)');
xlim([0 (1000*(l-1)/fs)]);

return
```

This function is used to create the best fit wave form to the filtered data.

```
function [d,bfit] = my_bestfit (X0, fd, fs)

t = (0:length(fd)-1) / fs;

d = lsqcurvefit(@myfun, X0, t', fd);
bfit = d(1) + d(2)*sin(2*pi*d(3)*t + d(4));

return
```

This function plots the lowpass FIR filter for both the magnitude and phase response.

```
function FIR_Plot (fs, b, pts)

a = fs; %sampling frequency
d = pts; %number of points to be graphed
figure(4)
freqz(b,1,d,a)
title('FIR Design');

return
```