Design of a Differential Opamp with CMFB

in 0.25µm process

ECE 523

CMOS Integrated Circuits - II

HW-7

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Submitted on 02/28/2011

1 Specification

Power Supply, Vdd = +2.5V

Load = 10pF

CMFB Phase Margin >45°

Output CM accuracy/error >+/- 0.1V

AD=AS=W*0.66µm & PD=PS=2*W+1.32µm

2 Design Procedure

1. Take the folded cascode opamp from HW4
2. Inorder to convert it to differential remove the diode connection from M9 and bias it with separate voltage source(which can be replaced later by the CMFB input) which will set the original current. Inorder to bring all the transistors to saturation try incrementing the W/L of either of the top/bottom pair current setting transistors. Adjust the ration such that output node voltage is clos to 1.25V.
3. Now design the CMFB circuit as a separate schematic. A four transistor topology has been chosen to do the averaging and not to affect the original differential circuit performance. The current mirror arrangment of opamp design is chosen here also to provide the necessary biasing.
4. CMFB output is given to the lower curretn setting transistor's (M9, M10) gate to complete the negative feedback loop.
5. Minor tweakings are to performed to the current seting transitors of CMFB block to bring everything to saturation.

2.1 Final Design

The final circuit schematic is shown above

Parameter	Value
C_L	10pF
I_{bias}	146µA
$W_{1,2}$(µm)	160.8
$W_{3,4}$(µm)	245
$W_{5,6}$,(µm)	115
$W_{7,8}$(µm)	41.4
$W_{9,10}$(µm)	29.7

$W_{11}(\mu m)$	125
$W_{12,14,}(\mu m)$	23.16
$W_{13}(\mu m)$	33
$W_{15}(\mu m)$	23.22
$W_{16,18}(\mu m)$	8.28
$W_{15}(\mu m)$	7
$W_{19,20}(\mu m)$	48
$W_{21,22,23,24}(\mu m)$	25
$W_{25,26}(\mu m)$	19.7
$L(\mu m)$	0.48

3 HSPICE Netlist

```
* # FILE NAME:
/NFS/FARM/U4/G/GEORGJUS/CADENCE/SIMULATION/FOLDED_CMFB_HW7/
* HSPICES/SCHEMATIC/NETLIST/FOLDED_CMFB_HW7.C.RAW
* NETLIST OUTPUT FOR HSPICES.
* GENERATED ON FEB 28 11:40:04 2011

* GLOBAL NET DEFINITIONS
.GLOBAL VDD!
* FILE NAME: ECE523_FOLDED_CMFB_HW7_SCHEMATIC.S.
* SUBCIRCUIT FOR CELL: FOLDED_CMFB_HW7.
* GENERATED FOR: HSPICES.
* GENERATED ON FEB 28 11:40:04 2011.



* Original subcircuit connection
XI3 NET3 NET5 NET4 SUB1
XI1 NET3 VIN_P VIN_N NET5 NET4 SUB2

Vp VIN_P 0 1.25
Vn VIN_N 0 1.25
.dc Vn 0 2.5 0.1
.plot DC V(NET5, NET4)
```

```
* To measure differential loop gain
*XI3 NET4 NET5 NET4 SUB1
*XI1 NET3 VIN_P VIN_N NET5 NET4 SUB2

*Vcmfb NET3 0 0.6884838
*Vcmout s1 0 1.25
*Cm1 s1 s2 1e-12
*Rm1 s2 s1 1e9
*Cm2 s2 VOUT1 1e-12
*Cm3 s1 s3 1e-12
*Rm2 s3 s1 1e9
*Cm4 s3 VOUT2 1e-12
*.ac dec 10 1 1000MEG
*.plot AC vdb(NET5, NET4)

* To measure CMFB loop gain - comment out for other things
*XI3 NET4 NET5 NET4 SUB1
*XI1 NET3 VIN_P VIN_N NET5 NET4 SUB2
*Vgain NET3 0 0.6884838 AC 1
*.ac dec 10 1 1000MEG



Vvdd VDD! 0 2.5

.param w19=48u w20=48u w21=21u w22=21u w23=21u w24=21u w25=19.7u w26=19.7u l=0.48u
w27=23.16u

* FILE NAME: ECE523_CMFB_HW7_BLOCK_SCHEMATIC.S.
* SUBCIRCUIT FOR CELL: CMFB_HW7_BLOCK.
* GENERATED FOR: HSPICES.
* GENERATED ON FEB 28 11:40:04 2011.

* TERMINAL MAPPING: VCMFB = VCMFB_OUT
*                   VOUT1 = VOUT1
*                   VOUT2 = VOUT2
.SUBCKT SUB1 VCMFB_OUT VOUT1 VOUT2
```

```
Vcm NET0109 0  1.25
IBIAS NET47 0  DC=121E-6  M=1.0

M19 NET0249 NET47 VDD! VDD!  CMOSP  w='w19' l='l' AD='0.66u*w19' AS='0.66u*w19'
PD='2*w19 + 1.32u' PS='2*w19 + 1.32u'
M20 NET0120 NET47 VDD! VDD!  CMOSP w='w20' l='l' AD='0.66u*w20' AS='0.66u*w20'
PD='2*w20 + 1.32u' PS='2*w20 + 1.32u'

*M21 VCMFB_OUT VOUT2 NET0249 NET0249  CMOSP w='w21' l='l' AD='0.66u*w21'
AS='0.66u*w21' PD='2*w21 + 1.32u' PS='2*w21 + 1.32u'
M21 NET0134 VOUT2 NET0249 NET0249  CMOSP w='w21' l='l' AD='0.66u*w21'
AS='0.66u*w21' PD='2*w21 + 1.32u' PS='2*w21 + 1.32u'

*M22 NET0134 NET0109 NET0249 NET0249  CMOSP w='w22' l='l' AD='0.66u*w22'
AS='0.66u*w22' PD='2*w22 + 1.32u' PS='2*w22 + 1.32u'
*M23 NET0134 NET0109 NET0120 NET0120  CMOSP w='w23' l='l' AD='0.66u*w23'
AS='0.66u*w23' PD='2*w23 + 1.32u' PS='2*w23 + 1.32u'

M22 VCMFB_OUT NET0109 NET0249 NET0249  CMOSP w='w22' l='l' AD='0.66u*w22'
AS='0.66u*w22' PD='2*w22 + 1.32u' PS='2*w22 + 1.32u'
M23 VCMFB_OUT NET0109 NET0120 NET0120  CMOSP w='w23' l='l' AD='0.66u*w23'
AS='0.66u*w23' PD='2*w23 + 1.32u' PS='2*w23 + 1.32u'

*M24 VCMFB_OUT VOUT1 NET0120 NET0120  CMOSP w='w24' l='l' AD='0.66u*w24'
AS='0.66u*w24' PD='2*w24 + 1.32u' PS='2*w24 + 1.32u'
*M25 VCMFB_OUT VCMFB_OUT 0 0  CMOSN  w='w25' l='l' AD='0.66u*w25' AS='0.66u*w25'
PD='2*w25 + 1.32u' PS='2*w25 + 1.32u'

M24 NET0134 VOUT1 NET0120 NET0120  CMOSP w='w24' l='l' AD='0.66u*w24'
AS='0.66u*w24' PD='2*w24 + 1.32u' PS='2*w24 + 1.32u'
M25 NET0134 NET0134 0 0  CMOSN  w='w25' l='l' AD='0.66u*w25' AS='0.66u*w25' PD='2*w25
+ 1.32u' PS='2*w25 + 1.32u'

*M26 NET0134 NET0134 0 0  CMOSN   w='w26' l='l' AD='0.66u*w26' AS='0.66u*w26'
PD='2*w26 + 1.32u' PS='2*w26 + 1.32u'
M26 VCMFB_OUT VCMFB_OUT 0 0  CMOSN   w='w26' l='l' AD='0.66u*w26' AS='0.66u*w26'
PD='2*w26 + 1.32u' PS='2*w26 + 1.32u'

M27 NET47 NET47 VDD! VDD!  CMOSP w='w27' l='l' AD='0.66u*w27' AS='0.66u*w27'
```

```
PD='2*w27 + 1.32u' PS='2*w27 + 1.32u'



* END OF SUBCIRCUIT DEFINITION.
.ENDS SUB1
* FILE NAME: ECE523_FOLDED_DIFF_BLOCK_HW7_SCHEMATIC.S.
* SUBCIRCUIT FOR CELL: FOLDED_DIFF_BLOCK_HW7.
* GENERATED FOR: HSPICES.
* GENERATED ON FEB 28 11:40:04 2011.

* TERMINAL MAPPING: VCMFB_IN = VCMFB_IN
*                   VIN1 = VIN1
*                   VIN2 = VIN2
*                   VOUT1 = VOUT1
*                   VOUT2 = VOUT2
.SUBCKT SUB2 VCMFB_IN VIN1 VIN2 VOUT1 VOUT2


.param w1=160.8u w2=160.8u w3=245u w4=245u,w5=115u w6=115u w7=41.4u w8=41.4u
w9=29.67u w10=29.67u w11=125u w12=23.16u w13=33u w14=23.16u w15=23.2u w16=8.28u
 +    w17=7u w18=8.28u l=480e-9


*V0 VIN1 0  1.25
*V1 VIN2 0  1.25
CL1 VOUT1 0  10E-12 M=1.0
CL2 VOUT2 0  10E-12 M=1.0
IBIAS NET47 0  DC=121E-6  M=1.0


M1 NET41 VIN1 NET44 NET44  CMOSN w='w1' l='l' AD='0.66u*w1' AS='0.66u*w1' PD='2*w1 +
1.32u' PS='2*w1 + 1.32u'
M2 NET37 VIN2 NET44 NET44  CMOSN w='w2' l='l' AD='0.66u*w2' AS='0.66u*w2' PD='2*w2 +
1.32u' PS='2*w2 + 1.32u'
M3 NET41 NET55 VDD! VDD!  CMOSP w='w3' l='l' AD='0.66u*w3' AS='0.66u*w3' PD='2*w3 +
1.32u' PS='2*w3 + 1.32u'
M4 NET37 NET55 VDD! VDD!  CMOSP w='w4' l='l' AD='0.66u*w4' AS='0.66u*w4' PD='2*w4 +
1.32u' PS='2*w4 + 1.32u'
M5 VOUT1 SOOCH1 NET41 NET41  CMOSP w='w5' l='l' AD='0.66u*w5' AS='0.66u*w5'
PD='2*w5 + 1.32u' PS='2*w5 + 1.32u'
M6 VOUT2 SOOCH1 NET37 NET37  CMOSP w='w6' l='l' AD='0.66u*w6' AS='0.66u*w6'
PD='2*w6 + 1.32u' PS='2*w6 + 1.32u'
```

```
M7 VOUT1 SOOCH2 NET21 NET21  CMOSN w='w7' l='l' AD='0.66u*w7' AS='0.66u*w7'
PD='2*w7 + 1.32u' PS='2*w7 + 1.32u'

M8 VOUT2 SOOCH2 NET17 NET17  CMOSN w='w8' l='l' AD='0.66u*w8' AS='0.66u*w8'
PD='2*w8 + 1.32u' PS='2*w8 + 1.32u'

M9 NET21 VCMFB_IN 0 0  CMOSN w='w9' l='l' AD='0.66u*w9' AS='0.66u*w9' PD='2*w9 +
1.32u' PS='2*w9 + 1.32u'

M10 NET17 VCMFB_IN 0 0  CMOSN w='w10' l='l' AD='0.66u*w10' AS='0.66u*w10' PD='2*w10
+ 1.32u' PS='2*w10 + 1.32u'

M11 NET44 NET9 0 0  CMOSN w='w11' l='l' AD='0.66u*w11' AS='0.66u*w11' PD='2*w11 +
1.32u' PS='2*w11 + 1.32u'

M12 NET47 NET47 SOOCH1 SOOCH1  CMOSP w='w12' l='l' AD='0.66u*w12' AS='0.66u*w12'
PD='2*w12 + 1.32u' PS='2*w12 + 1.32u'

M13 SOOCH1 NET47 NET55 NET55  CMOSP w='w13' l='3*l' AD='0.66u*w13' AS='0.66u*w13'
PD='2*w13 + 1.32u' PS='2*w13 + 1.32u'

M14 NET55 NET55 VDD! VDD!  CMOSP  w='w14' l='l' AD='0.66u*w14' AS='0.66u*w14'
PD='2*w14 + 1.32u' PS='2*w14 + 1.32u'

M15 NET7 NET55 VDD! VDD!  CMOSP w='w15' l='l' AD='0.66u*w15' AS='0.66u*w15'
PD='2*w15 + 1.32u' PS='2*w15 + 1.32u'

M16 NET7 NET7 SOOCH2 SOOCH2  CMOSN w='w16' l='l' AD='0.66u*w16' AS='0.66u*w16'
PD='2*w16 + 1.32u' PS='2*w16 + 1.32u'

M17 SOOCH2 NET7 NET9 NET9  CMOSN  w='w17' l='3*l' AD='0.66u*w17' AS='0.66u*w17'
PD='2*w17 + 1.32u' PS='2*w17 + 1.32u'

M18 NET9 NET9 0 0  CMOSN  w='w18' l='l' AD='0.66u*w18' AS='0.66u*w18' PD='2*w18 +
1.32u' PS='2*w18 + 1.32u'



* END OF SUBCIRCUIT DEFINITION.

.ENDS SUB2


*.lib "/nfs/guille/analog/c/cdsmgr/pdk/CDK1.4/local/models/hspice/public/publicModel/tsmc25dN"
NMOS

*.lib "/nfs/guille/analog/c/cdsmgr/pdk/CDK1.4/local/models/hspice/public/publicModel/tsmc25dP"
PMOS


* INCLUDE FILES


.include "/nfs/farm/u4/g/georgjus/ECE523/CMOSN.txt"

.include "/nfs/farm/u4/g/georgjus/ECE523/CMOSP.txt"
```

```
* END OF NETLIST
.TEMP    25.0000
.OP
.option post
*.save
*.OPTION  INGOLD=2 ARTIST=2 PSF=2
*+       PROBE=0
.END
```

4 Results

The following table compares the simulated results with the original specifications given.

Parameter	**Typical (T=27)**
C_L	10pF
Differential loop gain	64.7dB
Differential loop PM	70.1
Differential loop UGBW	140.3MHz
CMFB loop gain	47.2dB
CMFB loop PM	104
CMFB loop UGBW	32.67MHz
Total Current	3.06mA

Output CM error	34mV
Output Swing	2.4V
Total Power	7.57mW

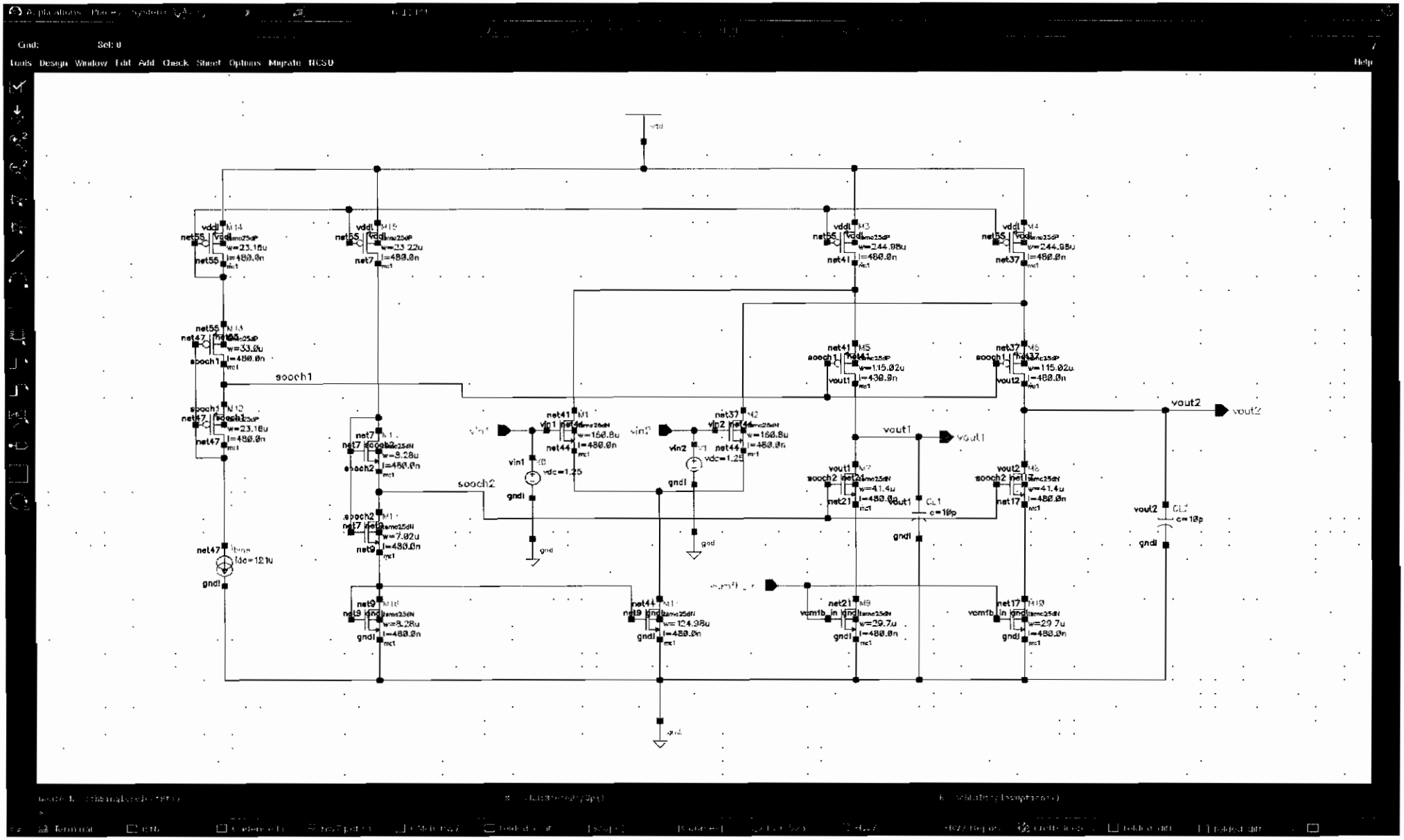
5 Conclusion

The circuit is has been designed and simulated. All design specifications were met.

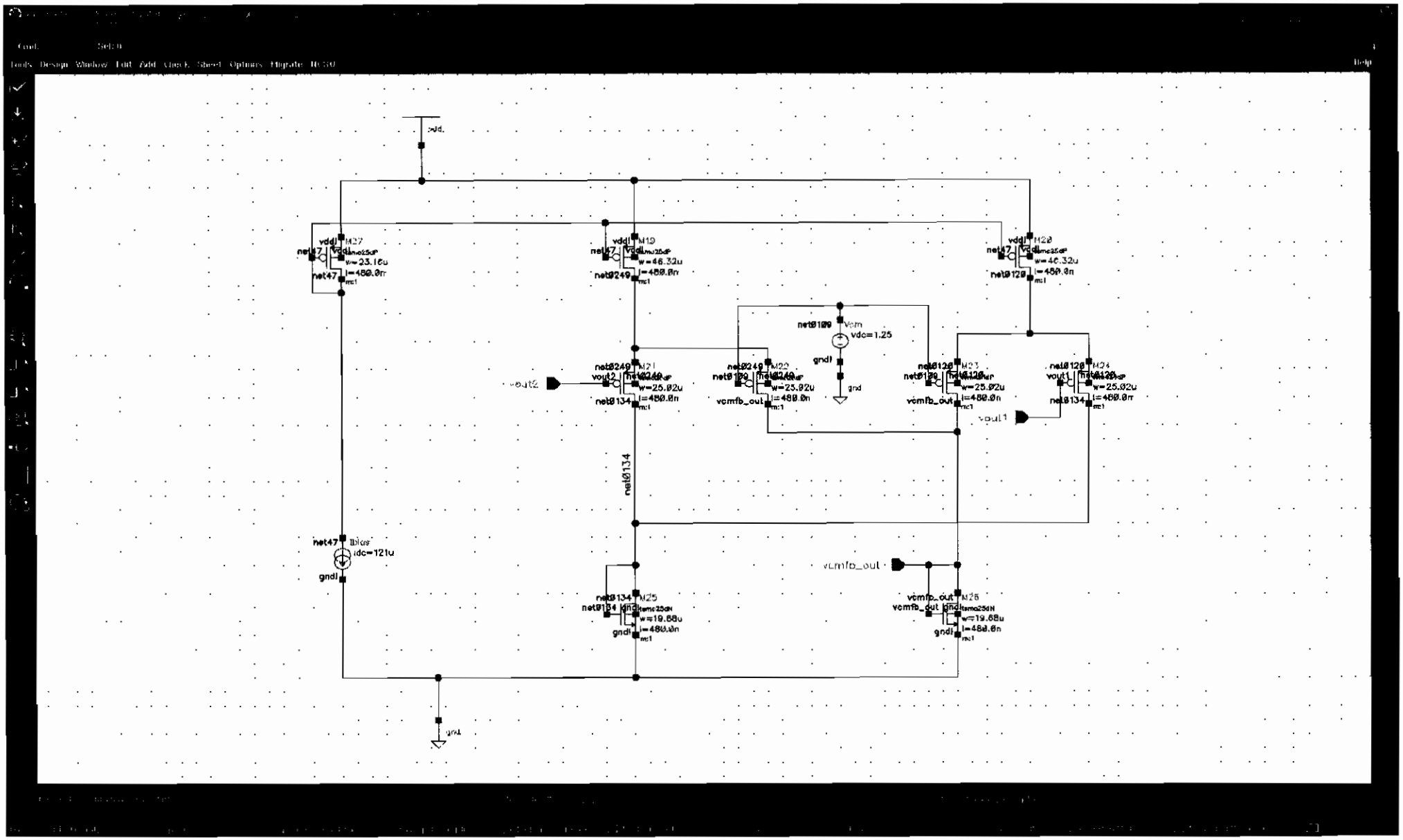
6 References

Analog Integrated circuits - Grey & Meyer

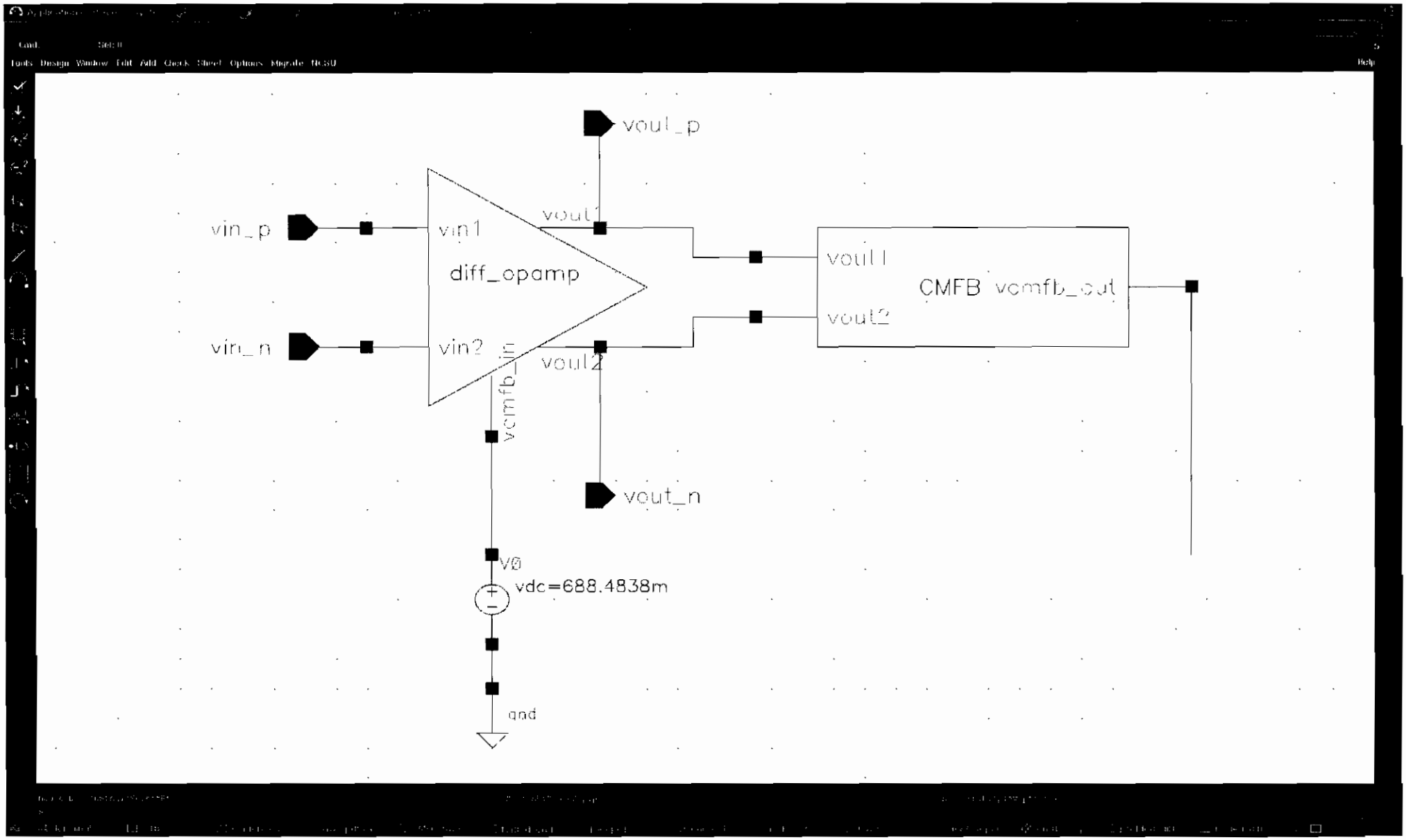
Differential Opamp circuit block



CMFB circuit block

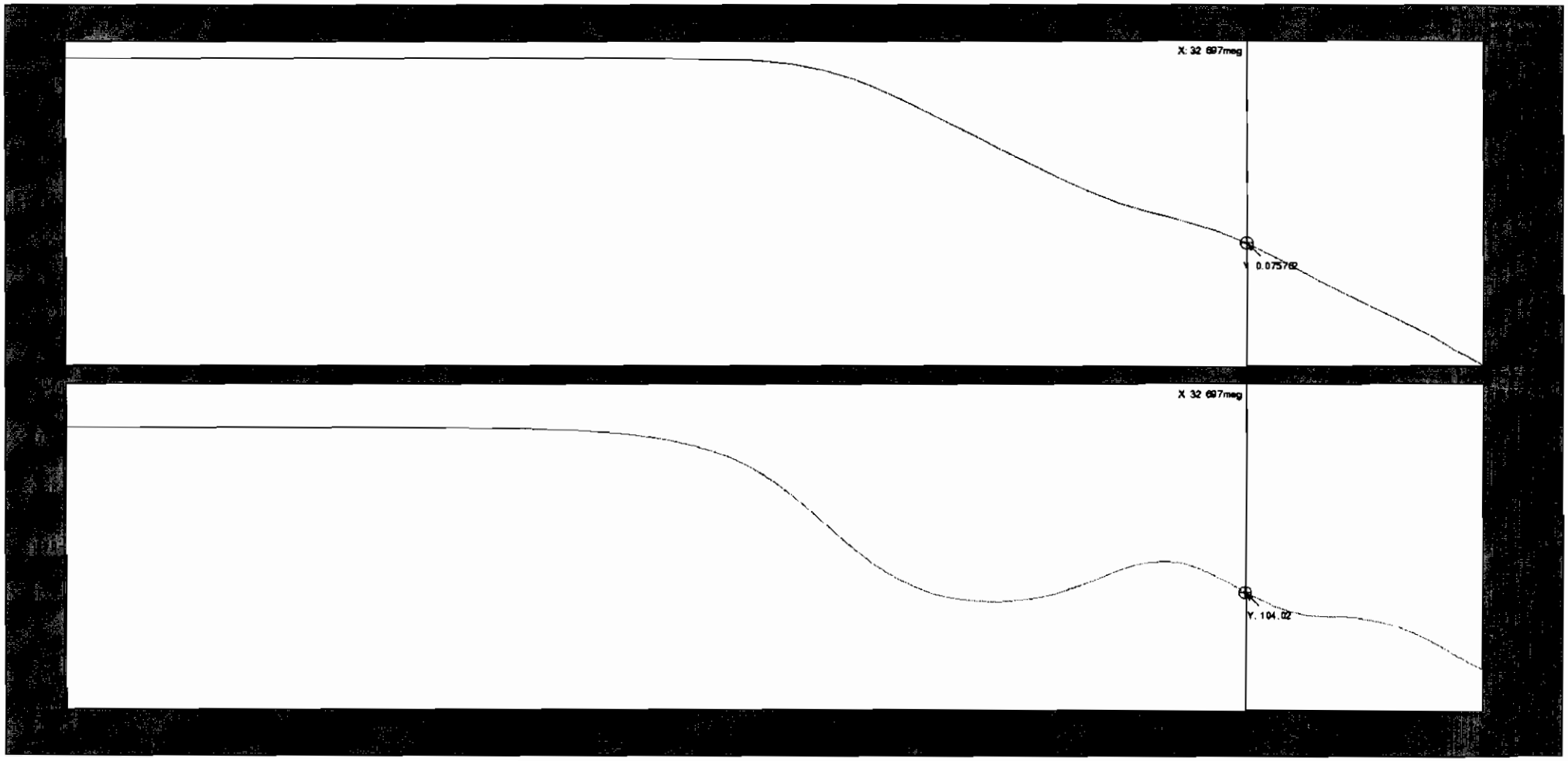


Final circuit



CMFB loop setup

Phase margin & unity gain bandwidth of CMFB loop



Differential loop setup

Differential loop measurements